Modified Increased-Level Model Predictive Control Methods With Reduced Computation Load for Modular Multilevel Converter

Xingxing Chen, *Student Member, IEEE*, Jinjun Liu, *Senior Member, IEEE*, Shuguang Song, *Student Member, IEEE*, Shaodi Ouyang, *Student Member, IEEE*, Hongda Wu, and Yue Yang

***Abstract*—It is considerable to reduce the computation load while keeping a good total harmonic distortion (THD) performance for the modular multilevel converter (MMC) with model predictive control (MPC). In this paper, the discrete-time mathematical model of the MMC is derived and the output voltage ripples of the cascaded submodules (SMs) are analyzed in detail. Accordingly, a modified increased-level MPC method A (IL-MPC-A) is proposed with $2N + 1$ ac-side output voltage levels. The computation load is significantly reduced without losing the harmonic circulating currents suppression and capacitor voltage ripples compensation capabilities. In this method, the cost function minimization step and capacitor voltage sorting algorithm are combined to determine the optimal control option. In addition, to avoid the selection of weighting factors and further reduce the computation load as the increasing of the SM number, another modified IL-MPC-B is proposed by directly calculating the optimal ac-side output voltage level and arm summation voltage according to the discrete-time mathematical model. As a result, the ac-side output current and circulating current controls are decoupled. Furthermore, the capacitor voltages are balanced with a proposed control scheme by adjusting the circulating current reference. The effectiveness of the proposed MPC methods is verified by simulation and experimental results.**

***Index Terms*—Capacitor voltage balancing, capacitor voltage ripples, computation load, model predictive control (MPC), modular multilevel converter (MMC).**

I. Introduction

In the past decade, the modular multilevel converter (MMC) has attracted extensive attention in both academia and industry. It exhibits several advantages, including expandable and redundant configuration, reduced switching frequency (RSF) and voltage stress of power switches, high quality of output voltage and current waveforms [1]–[4]. Owing to the features of this topology, the MMC is applicable to high-voltage (HV) and medium-voltage (MV) applications, such as a high-voltage direct-current (HVDC) system [5], [6], motor drives [7], a static synchronous compensator [8], and a battery energy storage system [9].

Manuscript received April 23, 2018; revised August 11, 2018 and October 6, 2018; accepted November 5, 2018. Date of publication November 21, 2018; date of current version May 22, 2019. This work was supported by the National Key Research & Development Plan of China under Grant 2018YFB0905800. Recommended for publication by Associate Editor M. A. Perez. *(Corresponding author: Xingxing Chen.)*

The authors are with the State Key Lab of Electrical Insulation and Power Equipment, School of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail:

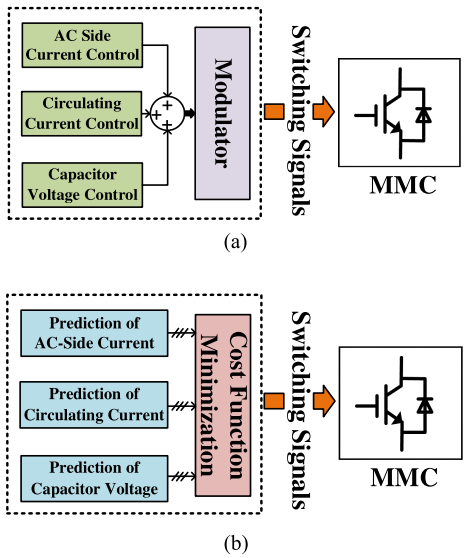

Fig. 1. Overall structure of two control systems for the MMC. (a) Cascaded control system. (b) MPC system.

The conventional cascaded control system of the MMC can be separated into three parts, i.e., ac-side output current control, circulating current control, and capacitor voltage control [10]–[15]. The first two objective controls can be realized by a proportional integral (PI) control strategy based on independent *dq* synchronous rotating frame [10] or a nonideal proportional resonant control strategy based on the *abc* or $\alpha\beta$ frame [11], [12]. Voltage control of all the floating capacitors can be characterized by a hierarchical control structure consisting of four layers [8], [13]–[15], i.e., overall capacitor voltage control, three phase balancing control, arm balancing control, and individual balancing control. The first three layers rely on a PI-based control method and the fourth layer can be implemented by sorting algorithm. The overall structure of the cascaded control system is shown in Fig. 1(a), where output of the three control parts is

added and sent to an extra modulator to generate the switching signals.

Compared with the cascaded control method, the model predictive control (MPC) is preferred for a multi-input multioutput system with consideration of the nonlinear characteristics of the target system, simple control structure, high dynamic performance, and handling multiple control targets [16]–[24]. Among MPC methods, the finite control set MPC (FS-MPC) is more attractive for power electronic converters [24]. Different kinds of MPC methods have been proposed for the MMC in [25]–[32]. Initially, a direct FS-MPC method is presented in [25] for an HV-applied MMC, considering all of the C_{2N}^{N} [N is the submodule (SM) number per arm, and C_{2N}^{N} represents the combination number by selecting N SMs from $2N$ SMs to be inserted] switching combinations when the inserted SM number is fixed to N in one phase-leg. However, it is impractical to implement this method with real-time control [26], due to the hundreds of number of SMs bringing with high computation load. The overall structure of the direct FS-MPC for the MMC is shown in Fig. 1(b) and that of the cascaded control system is shown in Fig. 1(a). Integrated with the voltage sorting balancing algorithm, an indirect FS-MPC is proposed in [26] with $N + 1$ control options, and further effort is made in [27] to avoid the selection of weighting factors by using two separate cost functions. Nevertheless, the control of the circulating current will not be effective in HV applications by only considering three control options and it also sacrifices the system dynamic performance [31]. Moreover, the capacitor voltage transient response is affected by using only one layer of the sorting balancing control. In order to reduce the influence of the common mode voltage, a three-phase based MPC method is presented in [28] and [29] with considering $(N + 1)^3$ switching combinations. The ac-side output voltage levels of the MMC by using the aforementioned FS-MPC methods are $N + 1$. To improve the total harmonic distortion (THD) performance of the MMC system, the inserted SM number in one phase-leg is no longer fixed to N and the ac-side output voltage levels are increased to $2N + 1$ in [30] with $(N + 1)^2$ control options. Also, to further reduce the number of the considered states, a voltage-level-based MPC method is proposed in [31]. However, the algorithm is not applicable to the MMC in MV applications with less SMs, since very few control options will be not effective to handle multiple control targets.

In this paper, the MPC methods proposed in the aforementioned references, which are able to generate $2N + 1$ ac-side output voltage levels, are classified as increased-levels MPC (IL-MPC) methods. Aiming at generating $2N + 1$ ac-side output voltage levels and reducing the computation load, a modified IL-MPC-A is presented in this paper first. The cost function is utilized to select the optimal control option to regulate the multiple control targets to their references. Also, the RSF voltage control algorithm proposed in [10] realizes the individual capacitor voltage balancing control. In order to suppress the harmonic circulating currents, the inserted SM number in one phase-leg is extended to $N \pm \varepsilon$ (ε is an integer and ≥ 1). In order to counteract the ac-side output voltage deviation and generate $2N + 1$ levels, the arm-inserted SM numbers are adjusted by adding

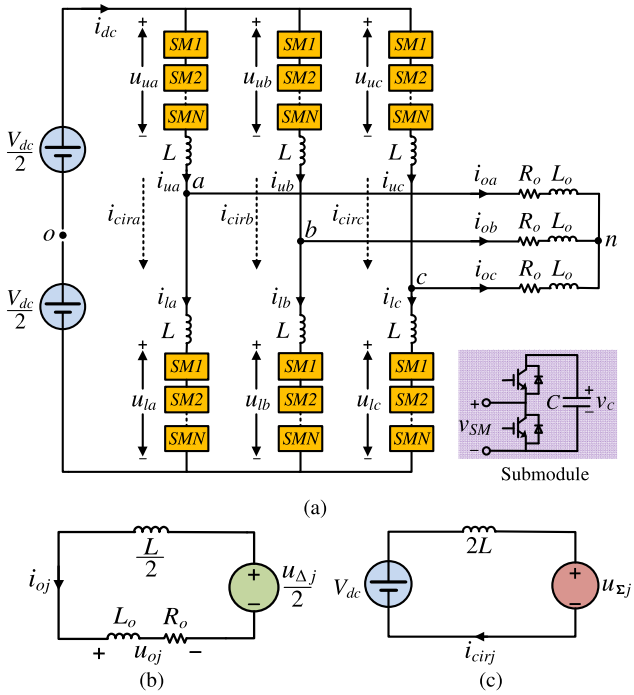

Fig. 2. Circuit configuration of the MMC with HBSM. (a) Three-phase circuit. (b) AC-side equivalent circuit. (c) Phase-leg equivalent circuit.

compensation values $\pm$ (1, 2, ..., ε). By directly calculating the optimal ac-side output voltage level and arm difference voltage according to the discrete-time mathematical model, another modified IL-MPC-B is proposed to avoid the selection of weighting factors and further reduce the computation load with the increase of the SM number. As a result, the ac-side output current and circulating current can be controlled by two separate control loops. The circulating current reference is adjusted by an extra control loop to balance the arm and overall capacitor voltages and improve the transient response. Simulation and experimental results are presented to demonstrate the effectiveness of the proposed methods under steady-state and dynamic-state conditions.

This paper is organized as follows. In Section II, the discrete-time mathematical model of the MMC is derived and the output voltage ripples of the cascaded SMs are analyzed. Then, the implementation of the proposed modified IL-MPC methods is presented in Section III. Simulation and experimental results are shown in Sections IV and V, respectively. Finally, Section VI concludes this paper.

II. System Descriptions of the MMC

A. Operation Principle and Mathematical Model

The three-phase circuit configuration of the MMC is shown in Fig. 2(a), which consists of three phase-legs, each being composed of an upper arm and a lower arm. Each arm is constructed with N cascaded half-bridge SMs (HBSMs) and an arm inductor L. C is the SM capacitance. There are two states of MMC SM under normal operating conditions, i.e., inserted and bypassed states. When the upper switch is turned ON and the lower switch

is turned OFF, the SM is inserted; on the contrary, the SM is bypassed. S_{xjy} is the SM switching function, which is given as

$$S_{xjy} = \begin{cases} 1 & \text{SM is inserted} \\ 0 & \text{SM is bypassed} \end{cases} \tag{1}$$

where $x = u$, l (arm symbol), $j = a$, b, c (phase symbol), and $y = 1, 2, 3, \ldots, N$ (SM index). $S_{\Delta j}$ and $S_{\Sigma j}$ are the difference and summation of the arm-inserted SM numbers, respectively, which are expressed as

$$S_{\Delta j} = \sum_{y=1}^{N} S_{ljy} - \sum_{y=1}^{N} S_{ujy} = n_{lj} - n_{uj} \tag{2}$$

$$S_{\Sigma j} = \sum_{y=1}^{N} S_{ljy} + \sum_{y=1}^{N} S_{ujy} = n_{lj} + n_{uj} \tag{3}$$

$$-S_{\Sigma j} \le S_{\Delta j} \le S_{\Sigma j} (|S_{\Delta j}| \le S_{\Sigma j}) \tag{4}$$

where n_{lj} and n_{uj} are the lower arm and upper arm inserted SM numbers, respectively.

The dc-side voltage is generated by a dc source $V_{\rm dc}$. u_{uj} and u_{lj} represent the summation voltages of the inserted SMs in the upper arm and lower arm, respectively. i_{uj} and i_{lj} represent the upper arm current and lower arm current, respectively. The ac side of the converter is connected to a series-connected resistor and inductor load ($R_{\rm o}$ and $L_{\rm o}$). u_{oj} is the load voltage. The ac-side output current i_{oj} and circulating current $i_{{\rm cir}j}$ are expressed as

$$i_{oj} = i_{uj} - i_{lj} \tag{5}$$

$$i_{{\rm cir}j} = \frac{i_{uj} + i_{lj}}{2} = \frac{i_{\rm dc}}{3} + i_{zj} \tag{6}$$

where $i_{\rm dc}$ is the dc component of the circulating current and i_{zj} represents the even-order harmonic components. Under balanced load condition, the main component of i_{zj} is a second-order negative sequence component and the reference of $i_{{\rm cir}j}$ is set to $i_{\rm dc}/3$ to suppress the harmonic circulating currents [10].

The dynamic behavior of the SM capacitor is described as

$$C\frac{dv_{cxjy}}{dt} = S_{xjy} i_{xj} \tag{7}$$

where v_{cxjy} is the SM capacitor voltage and its normal value is $V_{\rm dc}/N$ [1].

The generalized mathematical model of the MMC is given as follows [10]:

$$\frac{u_{\Delta j}}{2} = \left(\frac{L}{2} + L_o\right)\frac{di_{oj}}{dt} + R_o i_{oj} \tag{8}$$

$$\frac{u_{\Sigma j}}{2} = \frac{V_{\rm dc}}{2} - L\frac{di_{{\rm cir}j}}{dt} \tag{9}$$

where $u_{\Delta j}$ and $u_{\Sigma j}$ are the arm difference and summation voltages, respectively, which are given as

$$u_{\Delta j} = u_{lj} - u_{uj} \tag{10}$$

$$u_{\Sigma j} = u_{lj} + u_{uj}. \tag{11}$$

According to (8) and (9), the ac-side and phase-leg equivalent circuits of the MMC are shown in Fig. 2(b) and (c), respectively. The equivalent ac-side output voltage $u_{{\rm ac}j}$ is one half of $u_{\Delta j}$, as shown in Fig. 2(b). By using the forward Euler approximation method [24], the discrete-time mathematical model of the MMC can be deduced according to (1)–(11). The ac-side output current and circulating current are obtained as

$$i_{oj}(k+1) = \frac{T_s}{L + 2L_o} u_{\Delta j}(k) + \left(1 - \frac{2T_s R}{L + 2L_o}\right) i_{oj}(k) \tag{12}$$

$$i_{{\rm cir}j}(k+1) = \frac{T_s}{2L}[V_{\rm dc} - u_{\Sigma j}(k)] + i_{{\rm cir}j}(k). \tag{13}$$

The capacitor voltage is calculated as

$$v_{cxjy}(k+1) = v_{cxjy}(k) + \frac{T_s}{C} S_{xjy}(k) i_{xj}(k). \tag{14}$$

Therefore, the difference and summation of the arm capacitor voltages are given as

$$v_{\Delta j}(k+1) = \sum_{y=1}^{N} [v_{cljy}(k+1) - v_{cujy}(k+1)] \tag{15}$$

$$v_{\Sigma j}(k+1) = \sum_{y=1}^{N} [v_{cljy}(k+1) + v_{cujy}(k+1)]. \tag{16}$$

The references of $v_{\Delta j}$ and $v_{\Sigma j}$ are set to 0 and $2V_{\rm dc}$, respectively, to balance the arm and overall capacitor voltages in one phase-leg of the MMC [13]. Equations (10) and (11) can be rewritten as

$$u_{\Delta j}(k) = \sum_{y=1}^{N} [S_{ljy}(k) v_{cljy}(k) - S_{ujy}(k) v_{cujy}(k)] \tag{17}$$

$$u_{\Sigma j}(k) = \sum_{y=1}^{N} [S_{ljy}(k) v_{cljy}(k) + S_{ujy}(k) v_{cujy}(k)]. \tag{18}$$

In the above-mentioned discrete-time mathematical model, T_s is the sampling period. $i_{oj}(k)$, $i_{{\rm cir}j}(k)$, and $v_{cxjy}(k)$ are the measured values at step k. $i_{oj}(k+1)$, $i_{{\rm cir}j}(k+1)$, and $v_{cxjy}(k+1)$ are the predictive values at the next step.

B. Analysis of Cascaded SM Voltage Ripples

Attributing to the sorting balancing algorithm, the SM capacitor voltages in one arm are assumed to be equal to the same value. The disturbances will be introduced to the SM capacitor voltages due to the interactions of the arm currents and SM switches. At steady state, they are composed of dc, fundamental, and second-harmonic components [3]. If the capacitor voltage tolerance band (peak-to-peak value of the capacitor voltage ripple) is set to $2\delta\%$ of the normal SM capacitor voltage, the maximum and minimum capacitor voltages are written as

$$v_{c\,\max(\min)} = (1 \pm 0.01\delta) V_{\rm dc}/N. \tag{19}$$

The maximum and minimum values of $u_{\Sigma j}$ are obtained according to (3), (18), and (19), and are given as

$$u_{\Sigma j\_\max(\min)} = (1 \pm 0.01\delta) S_{\Sigma j} V_{\rm dc}/N. \tag{20}$$

In order to suppress the harmonic circulating currents, $u_{\Sigma j}$ should be set to $V_{\rm dc}$ [31]. Therefore, the maximum and minimum values of $S_{\Sigma j}$ are calculated as

$$S_{\Sigma j\_\max} = \text{ceil}\left(\frac{N}{1-0.01\delta}\right) \tag{21}$$

$$S_{\Sigma j\_\min} = \text{int}\left(\frac{N}{1+0.01\delta}\right) \tag{22}$$

function ceil(x) returns the nearest integer that is larger than x, for example, ceil(5.1) = 6 and ceil(5.6) = 6. Function int(x) returns the nearest integer that is smaller than x, for example, int(5.1) = 5 and int(5.6) = 5. The reason to use ceil(x) and int(x) to calculate $S_{\Sigma j\_\max}$ and $S_{\Sigma j\_\min}$, instead of using round(x) as [31] [function round(x) returns the nearest integer of x, for example, round(5.1) = 5 and round(5.6) = 6], is to guarantee the capability to suppress the harmonic circulating currents and generate $2N+1$ voltage levels. For example, if N is 9 and δ is 5, both $S_{\Sigma j\_\max}$ and $S_{\Sigma j\_\min}$ will equal to 9 by using round(x); therefore, the harmonic circulating currents cannot be effectively suppressed and $2N+1$ voltage levels cannot be generated since the inserted SM number is fixed to N. However, $S_{\Sigma j\_\max}$ and $S_{\Sigma j\_\min}$ will equal to 10 and 8, respectively, by using (21) and (22), which provides two additional states to suppress the harmonic circulating currents [32], and will be able to generate $2N+1$ voltage levels. In general, $S_{\Sigma j\_\max}$ should always larger than $N/(1-0.01\delta)$ and $S_{\Sigma j\_\min}$ should always smaller than $N/(1+0.01\delta)$.

For a certain value of $S_{\Delta j}$, if the capacitor voltage ripples are not considered, the ideal ac-side output voltage $u_{\text{ac}j\_\text{ideal}}$ can be obtained according to (2) and (17) (v_{cxjy} equals $V_{\rm dc}/N$), and is given as

$$u_{\text{ac}j\_\text{ideal}} = \frac{u_{\Delta j\_\text{ideal}}}{2} = \frac{S_{\Delta j}V_{\rm dc}}{2N} = \frac{\text{level}_j V_{\rm dc}}{N} \tag{23}$$

where level_j is the normalized ac-side output voltage level and is defined as

$$\text{level}_j = \frac{S_{\Delta j}}{2}. \tag{24}$$

However, if the capacitor voltage ripples are considered, the actual ac-side output voltage $u_{\text{ac}j\_\text{actual}}$ will be within the range of $[(1-0.01\delta)S_{\Delta j}V_{\rm dc}/\,2N,\ (1+0.01\delta)\,S_{\Delta j}V_{\rm dc}/2N]$ according to (19). The maximum and minimum deviation values between $u_{\text{ac}j\_\text{ideal}}$ and $u_{\text{ac}j\_\text{actual}}$ are obtained according to (4), and are given as

$$\tilde{u}_{\text{ac}j\,\max(\min)} = \pm\frac{0.01\delta S_{\Sigma j\_\max}V_{\rm dc}}{2N}. \tag{25}$$

In order to counteract the voltage deviation caused by the capacitor voltage ripples, and to obtain the ideal ac-side output voltage, level_j and $S_{\Delta j}$ in (23) should be adjusted ($\text{level}_j + \Delta\text{level}_j$ and $S_{\Delta j} + \Delta S_{\Delta j}$). According to (25), the maximum and minimum adjustment values are expressed as

$$\Delta\text{level}_{j\_\max(\min)} = \Delta S_{\Delta j\_\max(\min)}/2 = \pm 0.01\delta S_{\Sigma j\_\max}/2. \tag{26}$$

TABLE I
CONTROL OPTIONS OF THE MODIFIED IL-MPC-A

m	Inserted SMs	Upper arm	Lower arm	Level
1	N	n_{uj}	n_{lj}	$level_j$
2	N+1	n_{uj}+1	n_{lj}	$level_j$−1/2
3	N+1	n_{uj}	n_{lj} +1	$level_j$+1/2
4	N−1	n_{uj}−1	n_{lj}	$level_j$+1/2
5	N−1	n_{uj}	n_{lj} −1	$level_j$ −1/2
…	…	…	…	…
4ε−2	N+ε	n_{uj}+ε	n_{lj}	$level_j$−ε/2
4ε−1	N+ε	n_{uj}	n_{lj}+ε	$level_j$+ε/2
4ε	N−ε	n_{uj}−ε	n_{lj}	$level_j$+ε/2
1+4ε	N−ε	n_{uj}	n_{lj}−ε	$level_j$−ε/2

III. PROPOSED MODIFIED IL-MPC METHODS

A. Implementation of the Modified IL-MPC-A

The basic idea of the proposed modified IL-MPC-A is to utilize the cost function minimization step [29] to select the optimal control option to handle multiple control targets. The preselected control options are shown in Table I, where *m* is the control option number. The steps to obtain the control options in Table I are given as follows.

First step: To obtain the first control option in Table I under ideal condition, which means that the capacitor voltage ripples are not considered and the capacitor voltages are equal to their normal value $V_{\rm dc}/N$.

By replacing $i_{oj}(k+1)$ with its reference $i^*_{oj}(k+1)$ in (12), the optimal arm difference voltage is given as

$$u^*_{\Delta j}(k) = \frac{L+2L_o}{T_s}\left[i^*_{oj}(k+1) - \left(1-\frac{2RT_s}{L+2L_o}\right)i_{oj}(k)\right]. \tag{27}$$

The upper arm voltage reference is $[V_{\rm dc} - u^*_{\Delta j}(k)]/2$ [10] and the inserted SM number is N in one phase-leg for the first control option; therefore, the upper arm and lower arm inserted SM numbers are given as

$$n_{uj} = \text{round}\left[\frac{V_{\rm dc} - u^*_{\Delta j}(k)}{2V_{\rm dc}/N}\right] \tag{28}$$

$$n_{lj} = N - n_{uj}. \tag{29}$$

According to (2) and (24), level_j can be rewritten as

$$\text{level}_j = \frac{n_{lj} - n_{uj}}{2}. \tag{30}$$

Second step: To obtain the other control options in Table I. In order to suppress the harmonic circulating currents, the inserted SM number is no longer fixed to N in one phase-leg for the other control options. The maximum and minimum inserted SM numbers in one phase-leg are designed as $N+\varepsilon$ and $N-\varepsilon$, respectively. According to (21) and (22), ε should equal to the maximum value of $S_{\Sigma j\_\max} - N$ and $N - S_{\Sigma j\_\min}$. In order to guarantee the capability to counteract the maximum and minimum deviations of the ac-side output voltage, $\pm\varepsilon$ are

added to either n_{uj} or n_{lj} in (30), so that the normalized ac-side output voltage level in (30) is adjusted to level$_j \pm \varepsilon/2$. According to (26), ε should equal to ceil $(0.01\delta S_{\Sigma j\_\max})$. Considering both the harmonic circulating currents suppression and ac-side output voltage compensation, the designing principle of ε is given as

$$\varepsilon = \max[S_{\Sigma j\_\max} - N, N - S_{\Sigma j\_\min}, \text{ceil}(0.01\delta S_{\Sigma j\_\max})] \tag{31}$$

function max(x, y, z) returns the maximum value of x, y, and z. δ is set to 5 in this paper; therefore, ε can be calculated by using (31) for any value of the SM number N.

The other control options are obtained by adding $\pm$ (1, 2, ..., ε) to either n_{uj} or n_{lj}, as shown in Table I. Also, all of the $1 + 4\varepsilon$ control options ($m = 1, 2, 3, \ldots, 1 + 4\varepsilon$) will be considered to control the multiple targets in optimal, which means that in the cost function minimization step, the next step quantities prediction, and cost function calculation will be done for all of the $1 + 4\varepsilon$ control options. For the proposed method, $\varepsilon \geq 1$; therefore, at least five control options ($m = 1, 2, 3, 4, 5$) are given in Table I. The inserted SM numbers n_{uj} and n_{lj} are within the range of [0, N] and $n_{uj} + n_{lj} = N$ for the first control option; therefore, level$_j$ calculated in (30) will be among the $N + 1$ values of $(-N/2, -N/2 + 1, -N/2 + 2, \ldots, 0, \ldots, N/2 - 2, N/2 - 1, N/2)$. Additional ac-side output voltage levels level$_j \pm (0.5, 1, \ldots, 0.5\varepsilon)$ are generated by adding $\pm$ (1, 2,..., ε) to either n_{uj} or n_{lj} in (30). Therefore, the ac-side output voltage levels will be extended to $2N + 1$ values $(-N/2, -N/2 + 0.5, -N/2 + 1, -N/2 + 1.5, \ldots, 0, \ldots, N/2 - 1.5, N/2 - 1, N/2 - 0.5, N/2)$. It shows that $2N + 1$ output voltage levels will be generated by using the modified IL-MPC-A as long as $\varepsilon \geq 1$.

The implementation of the modified IL-MPC-A is illustrated in the following steps and the flowchart is shown in Fig. 3.

1) Measure the ac-side output current $i_{oj}(k)$, circulating current $i_{\text{cir}j}(k)$, and SM capacitor voltages $v_{cxjy}(k)$.
2) Calculate n_{uj}, n_{lj}, and level$_j$ according to (27)–(30) and refresh the control option table.
3) Sort the SM capacitor voltages in a descending order.
4) Do the cost function minimization to determine the optimal control option. J_2 is an assistant variable and set to a very large value before the recycling program. n_{ujm} and n_{ljm} are the inserted SM numbers of the m control option. n_{ujk} and n_{ljk} are the inserted SM numbers of the optimal control option. The maximum control option number $m_{\max} = 1 + 4\varepsilon$.

The next step electrical quantities $i_{oj}(k+1)$, $i_{\text{cir}j}(k+1)$, and $v_{cxjy}(k+1)$ are predicted by using (12), (13), and (14), respectively. The cost function is utilized to evaluate each control option, which is formulated as

$$\begin{aligned} J_1 = {} & \lambda_1 \left| i^*_{oj}(k+1) - i_{oj}(k+1) \right| \\ & + \lambda_2 \left| i^*_{cirj}(k+1) - i_{cirj}(k+1) \right| \\ & + \lambda_3 |v^*_{\Delta j}(k+1) - v_{\Delta j}(k+1)| \\ & + \lambda_4 |v^*_{\Sigma j}(k+1) - v_{\Sigma j}(k+1)| \end{aligned} \tag{32}$$

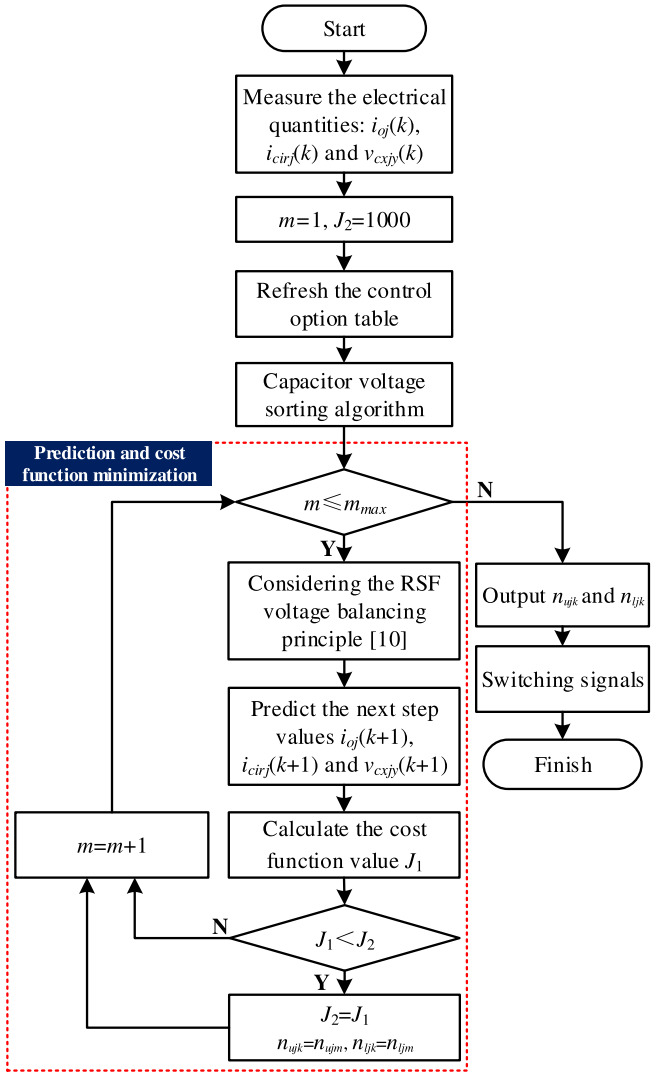

Fig. 3. Flowchart of the modified IL-MPC-A.

where λ_1, λ_2, λ_3, and λ_4 are the weighting factors. For every control options, the RSF voltage balancing principle [10] is considered, that is, no switching is applied to the already inserted (bypassed) SM during next switching cycle if extra SMs need to be inserted (bypassed). Therefore, the switching losses can be reduced. The optimal control option is selected through the cost function minimization step, which has the minimum cost function value.

The modified IL-MPC-A is compared with the MPC methods proposed in [25], [27], [29], and [30] regarding the ac-side output voltage levels and control option number. The comparison results are shown in Table II. As shown, the modified IL-MPC-A generates $2N + 1$ ac-side output voltage levels and significantly reduces the control option number.

B. Implementation of the Modified IL-MPC-B

In this part, a modified IL-MPC-B is proposed, and the comparisons of different MPC methods will be shown in the next part to clarify the advantages of the two proposed methods. The implementation of the modified IL-MPC-B is divided into three

TABLE II
COMPARISONS OF DIFFERENT MPC METHODS

MPC method	Output voltage levels	Control options				
		N=10	N=50	N=100	N=150	N=200
Direct-MPC [25]	N+1	$1.85e^{5}$	$1.01e^{29}$	$9.05e^{58}$	$9.38e^{88}$	$1.03e^{119}$
Indirect-MPC1 [27]	N+1	11	51	101	151	201
Three phase MPC [29]	N+1	1331	$1.32e^{5}$	$1.03e^{6}$	$3.44e^{6}$	$8.12e^{6}$
Indirect-MPC2 [30]	2N+1	121	2601	10201	22801	40401
Modified IL-MPC-A	2N+1	5	13	25	33	45

parts, i.e., ac-side output current control, circulating current control, and capacitor voltage control.

AC-side output current control: The optimal arm difference voltage $u^*_{\Delta j}(k)$ is calculated by using (27) to control the ac-side output current. In order to generate $2N+1$ output voltage levels, the lower arm inserted SM number cannot be calculated by using (29), because the inserted SM number in one phase-leg of the MMC is not fixed to N. Since the lower arm inserted SM number is unknown, the normalized ac-side output voltage level level_j cannot be calculated by using (30). Another way to calculate level_j is to first obtain the value of $S_{\Delta j}$, and then deduce level_j according to (24). Ideally, if the capacitor voltage v_{cxjy} equals its normal value V_dc/N, $S_{\Delta j}$ can be obtained according to (2) and (17), and is given as

$$S_{\Delta j} = \text{round}(Nu^*_{\Delta j}(k)/V_\text{dc}). \tag{33}$$

Then, the ideal normalized ac-side output voltage level level_j is deduced as

$$\text{level}_j = \frac{\text{round}(Nu^*_{\Delta j}(k)/V_\text{dc})}{2}. \tag{34}$$

n_{uj} and n_{lj} are within the range of [0, N]; therefore, $S_{\Delta j}$ calculated in (33) is among the values of $(-N, -N+1, -N+2, \ldots, 0, \ldots, N-2, N-1, N)$ according to (2). As a result, level_j will be among the values of $(-N/2, -N/2+0.5, -N/2+1, -N/2+1.5, \ldots, 0, \ldots, N/2-1.5, N/2-1, N/2-0.5, N/2)$. Therefore, $2N+1$ output voltage levels can also be generated by using the modified IL-MPC-B. In order to calculate the inserted SM numbers considering the capacitor voltage ripples, the upper arm inserted SM number in (28) is rewritten as

$$n_{uj1} = \text{round}\left[\frac{V_\text{dc} - u^*_{\Delta j}(k)}{2v_{\text{ave}j}}\right] \tag{35}$$

where $v_{\text{ave}j}$ is the average SM capacitor voltage in phase-leg j and is expressed as

$$v_{\text{ave}j} = \frac{v_{\Sigma j}(k)}{N}. \tag{36}$$

In order to produce the ideal normalized ac-side output voltage level, the lower arm inserted SM number is calculated by using (30), and is given as

$$n_{lj1} = 2\,\text{level}_j + n_{uj1}. \tag{37}$$

Arm and overall capacitor voltage controls in one phase-leg: In the conventional control system of the MMC based on the cascaded control method, it is very common to realize capacitor voltage controls by adjusting the circulating current reference [8], [34], [35]. The control block diagrams are shown in Fig. 4. $\Delta i_{\text{cir}j1}$ and $\Delta i_{\text{cir}j2}$ are the adjustment components of the circulating current reference used to control the arm and overall capacitor voltages, respectively. For the IL-MPC-B, the arm and overall capacitor voltage controls are also realized by adjusting the circulating current reference. However, $\Delta i_{\text{cir}j1}$ and $\Delta i_{\text{cir}j2}$ are no longer produced by PI controllers but will be calculated according to the discrete-time mathematical model of the MMC.

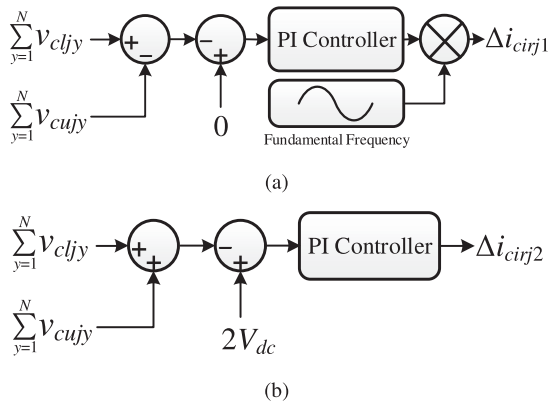

Fig. 4. Capacitor voltage controls in the conventional control system of the MMC. (a) Arm capacitor voltage control. (b) Overall capacitor voltage control.

The circulating current reference is $i_\text{dc}/3$ without considering the capacitor voltage controls, and it will be set to $i_\text{dc}/3 + \Delta i_{\text{cir}j1}$ and $i_\text{dc}/3 + \Delta i_{\text{cir}j2}$, respectively, to control the arm and overall capacitor voltages. By substituting (14) into (15) and (16) and replacing $v_{\Delta j}(k+1)$, $v_{\Sigma j}(k+1)$, $i_{oj}(k)$, and $i_{\text{cir}j}(k)$ by their references, (15) and (16) can be rewritten as

$$0 = v_{\Delta j}(k) + \frac{T_s}{C}S_{\Sigma j}(k)i^*_{oj}(k) + \frac{T_s}{C}S_{\Delta j}(k)\left(\frac{i_\text{dc}}{3} + \Delta i_{\text{cir}j1}\right) \tag{38}$$

$$2V_\text{dc} = v_{\Sigma j}(k) - \frac{T_s}{C}S_{\Delta j}(k)i^*_{oj}(k) + \frac{T_s}{C}S_{\Sigma j}(k)\left[\frac{i_\text{dc}}{3} + \Delta i_{\text{cir}j2}\right]. \tag{39}$$

Equations (38) and (39) are used to calculate the values of $\Delta i_{\text{cir}j1}$ and $\Delta i_{\text{cir}j2}$, respectively. It is reasonable to replace $S_{\Sigma j}(k)$ by N, since the change of the inserted SM number in

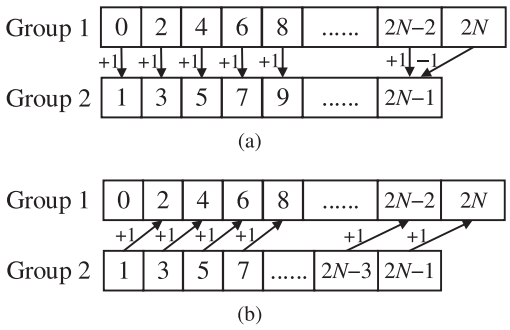

Fig. 5. Adjustment principle of $S_{\Sigma j}(k)$. (a) If $S_{\Delta j}(k)$ is an odd number. (b) If $S_{\Delta j}(k)$ is an even number.

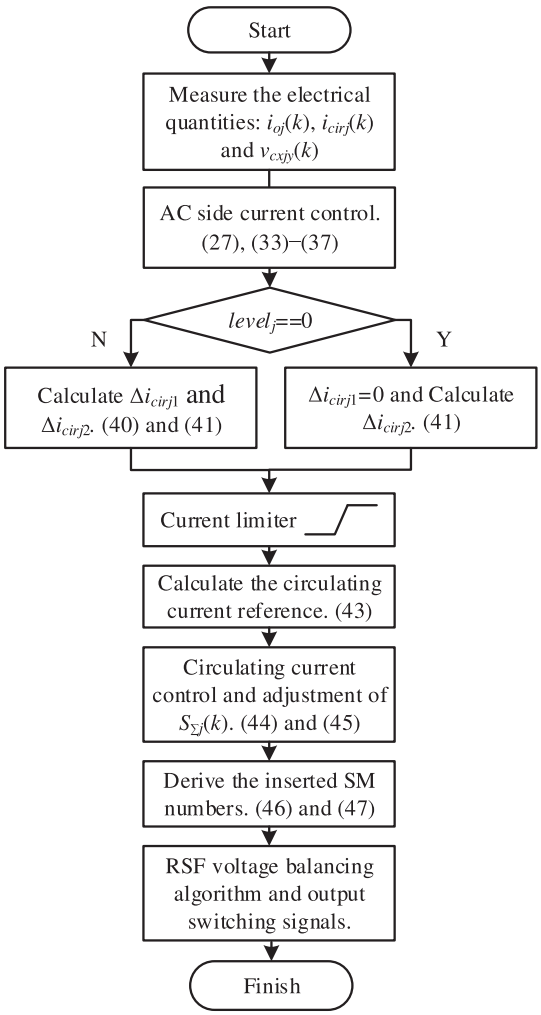

Fig. 6. Flowchart of the modified IL-MPC-B.

one phase-leg is relatively small compared with N. $S_{\Delta j}(k)$ is obtained from (33). Therefore, $\Delta i_{\mathrm{cir}j1}$ and $\Delta i_{\mathrm{cir}j2}$ can be calculated as

$$\Delta i_{\mathrm{cir}j1} = -\frac{C}{2T_s \mathrm{level}_j} v_{\Delta j}(k) + \frac{N i^*_{oj}(k)}{2\,\mathrm{level}_j} - \frac{i_{\mathrm{dc}}}{3} \tag{40}$$

$$\Delta i_{\mathrm{cir}j2} = -\frac{C}{T_s N} v_{\Sigma j}(k) + \frac{\mathrm{level}_j i^*_{oj}(k)}{N} + \frac{2CV_{\mathrm{dc}}}{T_s N} - \frac{i_{\mathrm{dc}}}{3}. \tag{41}$$

TABLE III
EXECUTION TIME COMPARISON OF THE MPC METHODS

SM number N		10	50	100	150	200
Indirect-MPC2 [30]	N_T	1.34e^5	2.83e^5	1.11e^6	2.47e^6	4.37e^6
	T_{ex}(us)	89.52	1880	7370	1.65e^4	2.91e^4
IL-MPC-A	N_T	1215	3519	6615	9279	1.24e^4
	T_{ex}(us)	8.1	23.46	44.1	61.86	82.5
IL-MPC-B	N_T	1030	1270	1570	1870	2170
	T_{ex}(us)	6.87	8.47	10.47	12.47	14.47

TABLE IV
PARAMETERS OF SIMULATION AND EXPERIMENTAL SYSTEMS

Parameters	Simulation	Experiment
DC-link voltage V_{dc}	10 kV	240 V
SM number per arm N	10	6
Normal value of capacitor voltage	1 kV	40 V
Fundamental frequency f	50 Hz	50 Hz
Submodule capacitance C	3.5 mF	2 mF
Arm inductance L	10 mH	3.5 mH
Load inductance L_o	5 mH	30 mH
Load resistance R_o	12 Ω	40 Ω
Control cycle T_s	100 μs	100 μs

Considering both the arm and overall capacitor voltage controls, the circulating current reference is expressed as

$$i^*_{\mathrm{cir}j}(k+1) = \frac{i_{\mathrm{dc}}}{3} + \Delta i_{\mathrm{cir}j1} + \Delta i_{\mathrm{cir}j2}. \tag{42}$$

It should be noticed that v_{cljy} and v_{cujy} contain harmonic components. 1/ level$_j$ is a csc(x) function in (40) at steady state and $\mathrm{level}_j i^*_{oj}(k)$ generates second-harmonic component in (41). Therefore, $\Delta i_{\mathrm{cir}j1}$ and $\Delta i_{\mathrm{cir}j2}$ can introduce harmonic components in the circulating current reference. In order to restrict the amplitude of circulating current ripple, a current limiter is applied and (42) is modified as

$$i^*_{\mathrm{cir}j}(k+1) = \frac{i_{\mathrm{dc}}}{3} + \text{Current limiter}\ (\Delta i_{\mathrm{cir}j1} + \Delta i_{\mathrm{cir}j2}). \tag{43}$$

There is a tradeoff between the amplitude of circulating current ripple and transient response of capacitor voltage control. The larger the absolute values of the current limits, the faster the capacitor voltage control.

Circulating current control: Replacing $i_{\mathrm{cir}j}(k+1)$ by its reference in (13), the optimal arm summation voltage $u_{\Sigma j}(k)$ is calculated as

$$u^*_{\Sigma j}(k) = V_{\mathrm{dc}} - \frac{2L}{T_s}\left[i^*_{\mathrm{cir}j}(k+1) - i_{\mathrm{cir}j}(k)\right]. \tag{44}$$

The summation of the inserted SM numbers $S_{\Sigma j}(k)$ can be calculated according to (3) and (18) ($v_{cxjy} = v_{\mathrm{ave}j}$), and is expressed as

$$S_{\Sigma j}(k) = \mathrm{int}\left[\frac{u^*_{\Sigma j}(k)}{v_{\mathrm{ave}j}}\right]. \tag{45}$$

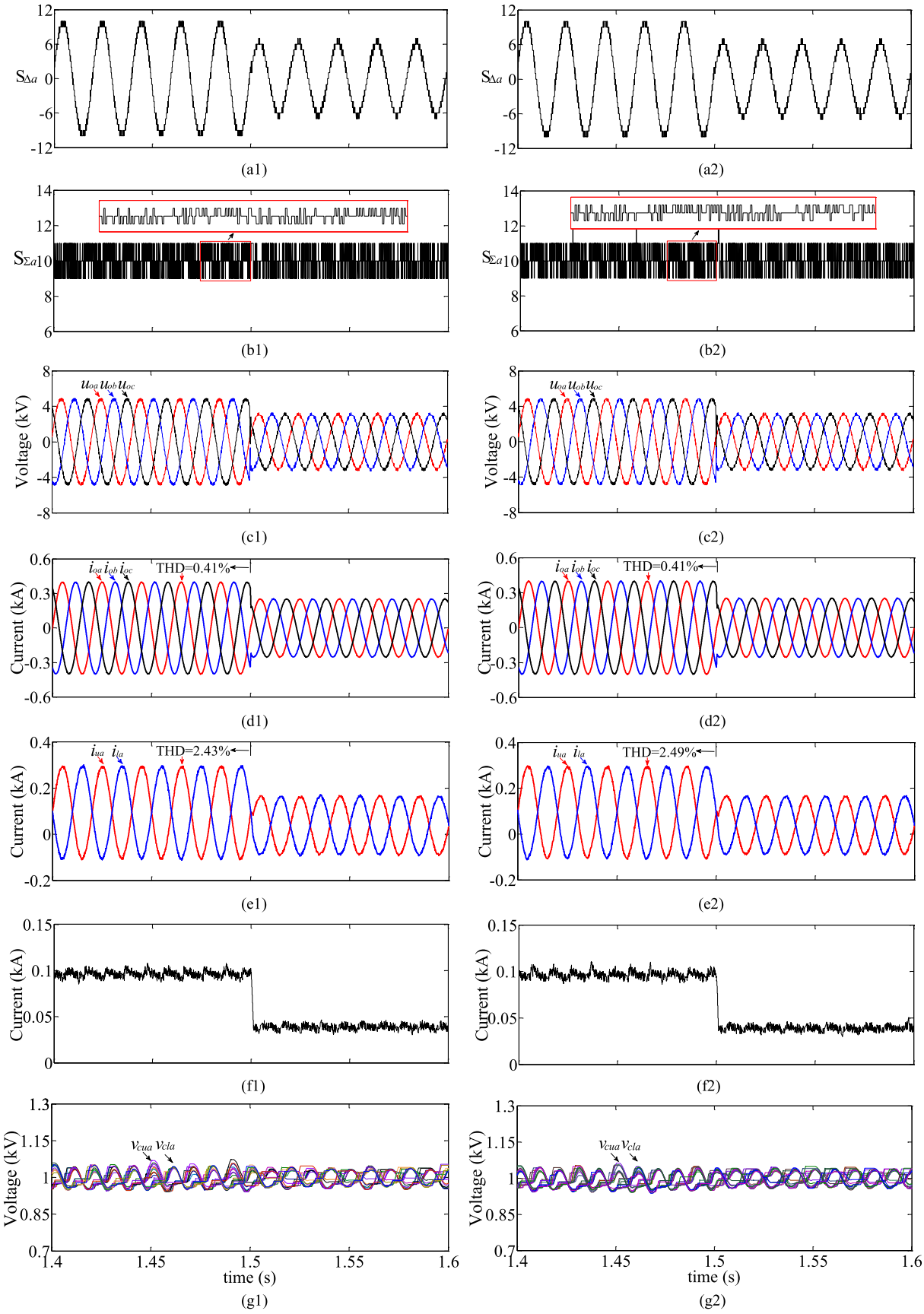

Fig. 7. Steady-state and dynamic-state performances of the MMC by using the modified IL-MPC-A with five and nine control options. (a) $S_{\Delta a}$. (b) $S_{\Sigma a}$. (c) Three-phase load voltages. (d) Three-phase ac-side output currents. (e) Phase a arm currents. (f) Phase a circulating current. (g) Phase a SM capacitor voltages.

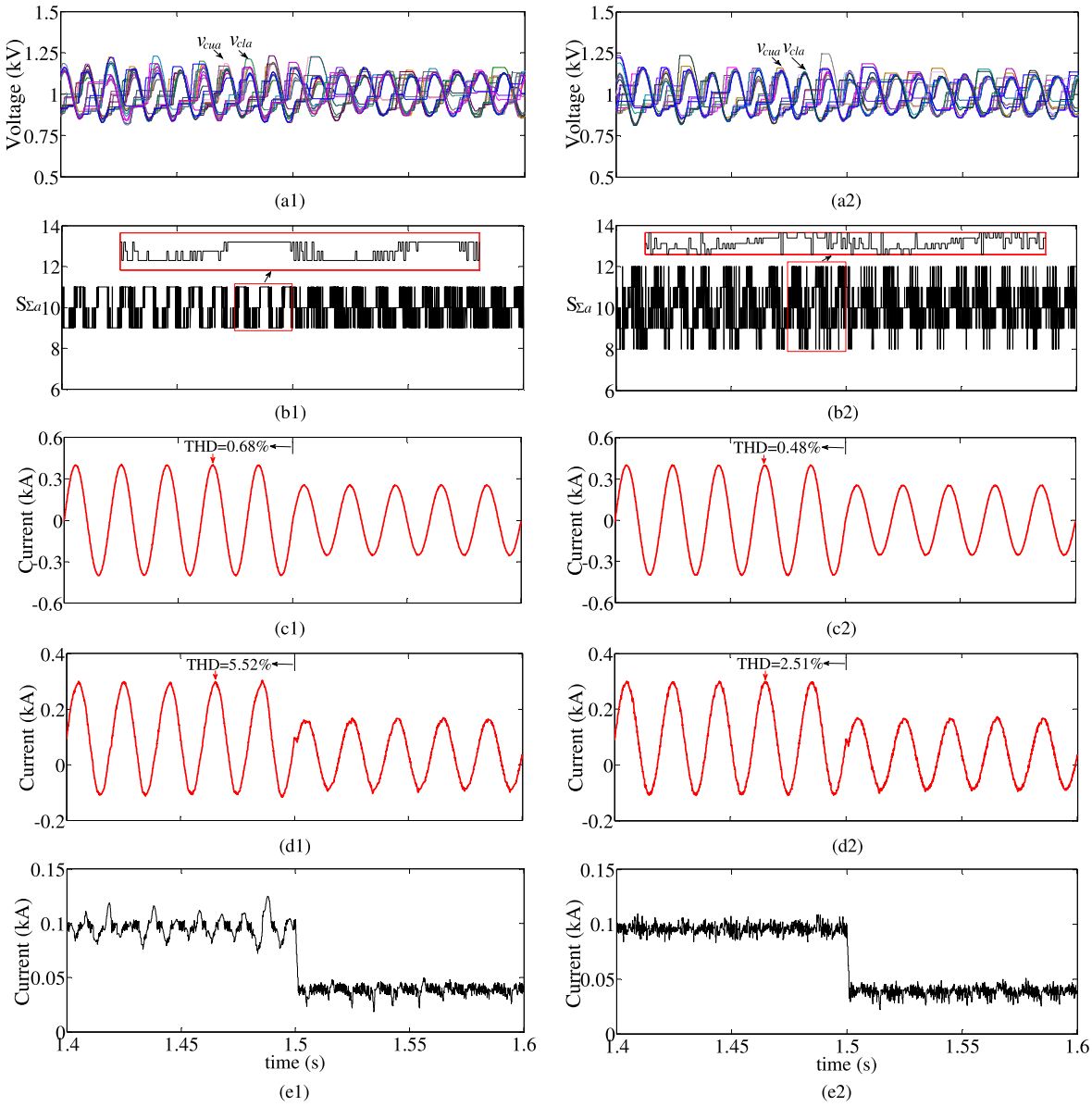

Fig. 8. Simulated waveforms of the MMC with increased capacitor voltages tolerance band. (a) Phase a SM capacitor voltages. (b) $S_{\Sigma a}$. (c) Phase a ac-side output current. (d) Phase a upper arm current. (e) Phase a circulating current.

In order to avoid affecting the ac-side current control while regulating the circulating current, $S_{\Sigma j}(k)$ calculated in (45) should be subject to $S_{\Delta j}(k)$ calculated in (33). $S_{\Delta j}(k)$ is unchanged if the same number of additional SMs is inserted or bypassed in the upper arm and lower arm according to (2). Therefore, if $S_{\Delta j}(k)$ is an odd (even) number, $S_{\Sigma j}(k)$ must be an odd (even) number. $S_{\Sigma j}(k)$ is adjusted according to different value of $S_{\Delta j}(k)$. As shown in Fig. 5(a) [see Fig. 5(b)], if $S_{\Delta j}(k)$ is an odd (even) number and $S_{\Sigma j}(k)$ calculated in (45) is among group 2 (group 1), the final value of $S_{\Sigma j}(k)$ equals the original value. If $S_{\Delta j}(k)$ is an odd (even) number and $S_{\Sigma j}(k)$ calculated in (45) is among group 1 (group 2), the final value of $S_{\Sigma j}(k)$ equals 1 added to the original value. If $S_{\Delta j}(k)$ is an odd number and $S_{\Sigma j}(k)$ is $2N$, the final value of $S_{\Sigma j}(k)$ equals $2N$- 1, as shown in Fig. 5(a).

The final upper arm and lower arm inserted SM numbers are given as

$$n_{uj2} = n_{uj1} + \frac{S_{\Sigma j}(k) - (n_{uj1} + n_{lj1})}{2} \tag{46}$$

$$n_{lj2} = n_{lj1} + \frac{S_{\Sigma j}(k) - (n_{uj1} + n_{lj1})}{2}. \tag{47}$$

After deriving the inserted SM numbers, the RSF capacitor voltage balancing algorithm is used to output the switching signals. The optimal peak-to-peak value of the harmonic circulating currents has a limited minimum value by using the proposed method [32]. The flowchart of the modified IL-MPC-B method is shown in Fig. 6.

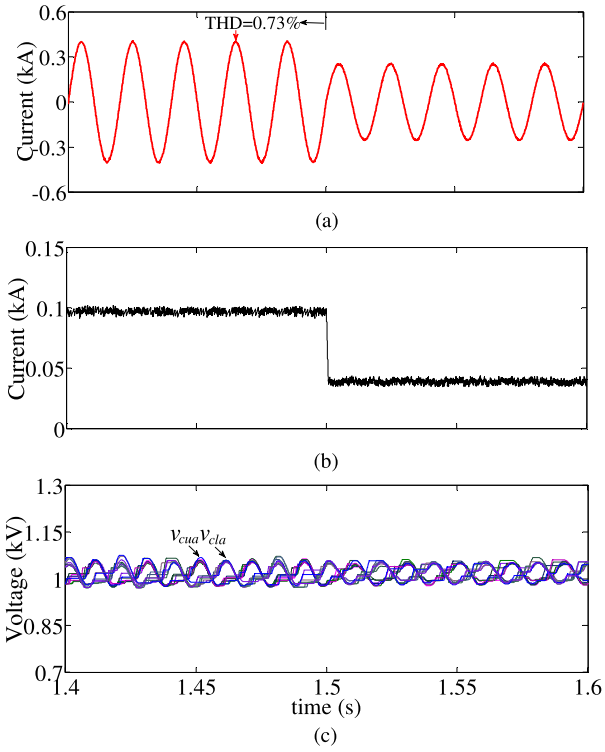

Fig. 9. Simulated waveforms of the MMC when the weighting factor λ_2 is changed. (a) Phase a ac-side output current. (b) Phase a circulating current. (c) Phase a SM capacitor voltages.

C. Comparison of Different MPC Methods

For the modified IL-MPC-A and other IL-MPC methods proposed in [30] and [31], the multiple targets control relies on the cost function minimization step. The next step electrical quantities $i_{oj}(k+1)$, $i_{\text{cir}j}(k+1)$, and $v_{cxjy}(k+1)$ and the cost function should be calculated for every control options. The optimal control option is selected by comparing every cost function values. As the control option number increases, the computation load also increases. Moreover, the weighting factors in the cost function are not easy to be determined [33].

In comparison, the modified IL-MPC-B can avoid the selection of weighting factors, and the multiple targets control is realized by calculating the control voltages [$u^*_{\Delta j}(k)$ and $u^*_{\Sigma j}(k)$] and currents ($\Delta i_{\text{cir}j1}$ and $\Delta i_{\text{cir}j2}$) according to the discrete-time mathematical model of the MMC.

The execution time of the Indirect-MPC2 [30], modified IL-MPC-A, and IL-MPC-B is evaluated using a digital signal processor TMS320f28335. The system clock is set to 150 MHz; therefore, one clock cycle takes 6.67 ns. The comparison results are shown in Table III. N_T is the total number of clock cycles and T_{ex} is the corresponding execution time. The number of clock cycles by using different MPC methods with different SM numbers can be evaluated using the TI Code Composer Studio (CCS) software. The execution time of the Indirect-MPC2 and modified IL-MPC-A is significantly affected by the SM number, because the control option number will be increased with increasing SM number, and the next step electrical quantities prediction and the cost function calculation should be repeated for every control options. The larger the control option number, the longer the execution time. If the execution time is too long, it will be difficult to realize real-time control for the MMC system. However, for the modified IL-MPC-B, only the average capacitor voltage calculation in (36) is affected by the SM number (more capacitor voltages should be added up with the increase in the SM number). The comparison results of the execution time indicate that both the modified IL-MPC-A and IL-MPC-B have low computation load compared to that of Indirect-MPC2. Also, the modified IL-MPC-B can further reduce the computation load with the increase in the SM number; thus, the control frequency can be increased to optimize the control performance.

IV. Simulation Results

A three-phase MMC system shown in Fig. 2 is constructed in PSCAD/EMTDC to demonstrate the proposed MPC methods, and the detailed system parameters are listed in Table IV.

The steady-state and dynamic-state performances of the MMC by using the modified IL-MPC-A are depicted in Fig. 7 ($x1$) ($x =$ a, b, c, d, e, f, g). The capacitor voltage tolerance band is designed as 10% ($\delta = 5$) of the normal SM capacitor voltage; therefore, 5 control options ($\varepsilon = 1$) are utilized with 10 SMs per arm to generate 21 voltage levels before 1.5 s, as shown in Fig. 7(a1). $S_{\Sigma j}$ changes among 9, 10, and 11 observed from Fig. 7(b1). The three phase load voltages are shown in Fig. 7(c1). The ac-side output current and arm currents of phase a are shown in Fig. 7(d1) and (e1), respectively. The corresponding THDs of i_{oa} and i_{ua} are 0.41% and 2.43%, respectively, before 1.5 s. During the whole time range, the harmonic components of the circulating current in Fig. 7(f1) are suppressed and the average SM capacitor voltages in Fig. 7(g1) are regulated to 1 kV. At 1.5 s, the active power is reduced by 60%. It is observed that the ac-side output current and circulating current are fast regulated to their new references. The average value of the upper arm and lower arm SM capacitor voltages are well balanced during the transient period.

ε is modified as 2; thus, nine control options will be utilized. The simulated waveforms are shown in Fig. 7 ($x2$). $S_{\Sigma a}$ changes among 9, 10, and 11 at most of the time as shown in Fig. 7(b2). The THDs of the ac-side output current i_{oa} and upper arm current i_{ua} have no improvement. Besides, the harmonic components of the circulating current have no further reduction. That means five control options are enough to control the target system with the designed SM number and capacitor voltage tolerance band.

Changing the SM capacitances from 3.5 to 1.5 mF, the peak-to-peak value of the capacitor voltage ripples increases to $\pm 20\%$ of the normal capacitor voltage value, as shown in Fig. 8(a1) and (a2). Therefore, ε should be designed as 2 according to (31). In Fig. 8 ($x1$) and ($x2$) ($x =$ a, b, c, d, e), ε is designed as 1 and 2, respectively. $S_{\Sigma a}$ changes among 9, 10, and 11, as shown in Fig. 8(b1), and changes among 8, 9, 10, 11, and 12, as shown in Fig. 8(b2). It is observed that the THD performances of i_{oa} and i_{ua} are improved in Fig. 8(c2) and (d2) compared with the

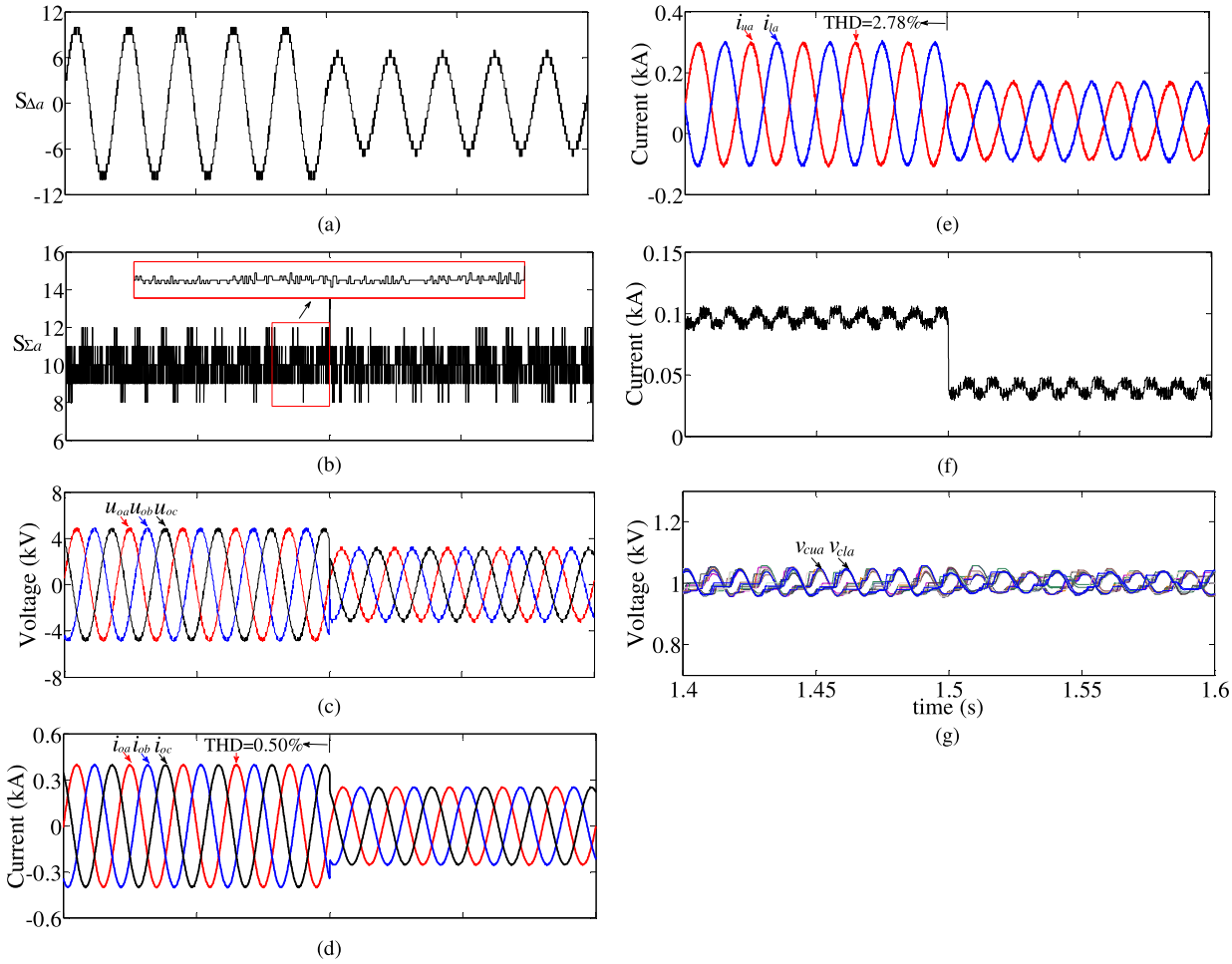

Fig. 10. Steady-state and dynamic-state performances of the MMC by using the modified IL-MPC-B. (a) $S_{\Delta a}$. (b) $S_{\Sigma a}$. (c) Three-phase load voltages. (d) Three-phase ac-side output currents. (e) Phase a arm currents. (f) Phase a circulating current. (g) Phase a SM capacitor voltages.

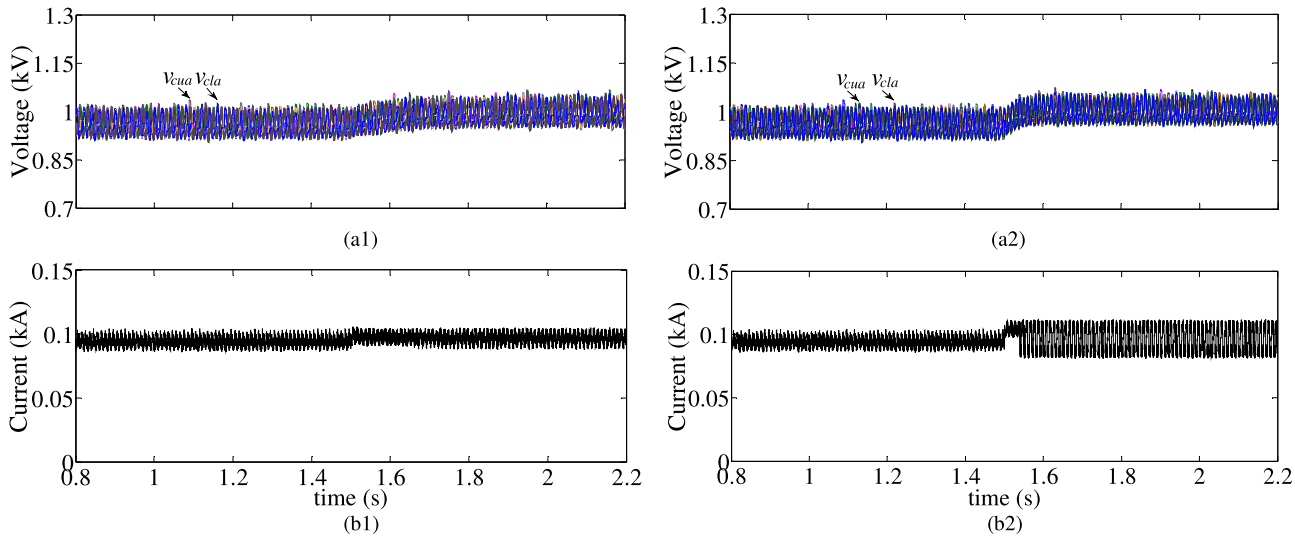

Fig. 11. Simulation verification of overall capacitor voltage control. (a) Capacitor voltages. (b) Circulating current.

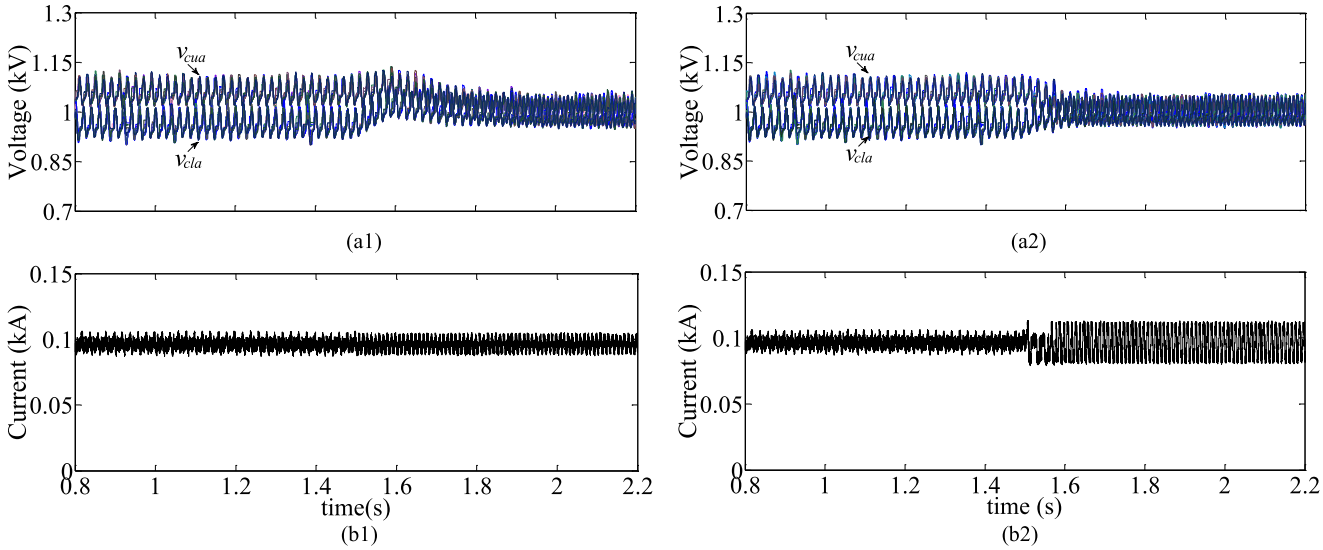

Fig. 12. Simulation verification of arm capacitor voltage control. (a) Capacitor voltages. (b) Circulating current.

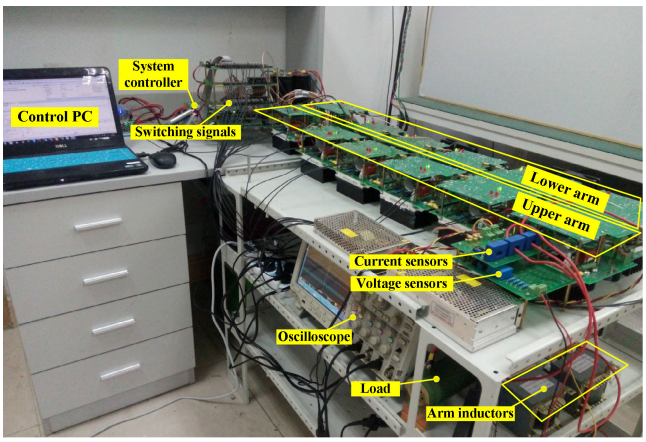

Fig. 13. Single-phase MMC prototype.

waveforms in Fig. 8(c1) and (d1). Moreover, the harmonic circulating currents are further reduced with more control options. The simulation results indicate that ε should be increased to introduce more control options with the increase in the capacitor voltage tolerance band and the total SM number.

The weighting factors are set to $\lambda_1 = 1$, $\lambda_2 = 0.5$, $\lambda_3 = 2\text{e}^{-5}$, and $\lambda_4 = 8\text{e}^{-5}$ in Fig. 7. If they are reset to $\lambda_1 = 1$, $\lambda_2 = 1$, $\lambda_3 = 2\text{e}^{-5}$, and $\lambda_4 = 8\text{e}^{-5}$, the simulation waveforms of the ac-side output current, circulating current, and capacitor voltages are shown in Fig. 9. It is observed that the harmonic circulating currents are further suppressed; however, the THD of the ac-side output current is increased and the average value of the capacitor voltage deviates from the normal value (1 kV). That means the selection of the weighting factors can affect the system performance and the improvement of one control objective can affect the performances of the other control objectives. The weighting factors should be well tuned to obtain a good system performance.

Fig. 10 shows the steady-state and dynamic-state performances of the MMC by using the modified IL-MPC-B with the same system parameters given in Table IV. Similarly, 21 ac-side output voltage levels are generated before 1.5 s, as shown in Fig. 10(a). $S_{\Sigma a}$ is calculated according to (45) followed by the adjustment step and no longer confined to 9, 10, and 11, as shown in Fig. 10(b). It should be noticed that the THD of the ac-side output current is 0.5% and increased slightly compared with the modified IL-MPC-A, since the average capacitor voltage $v_{\text{ave}j}$ is used to directly calculate the inserted SM numbers according to (35) and (45) for the modified IL-MPC-B, but several control options are utilized to optimize the ac-side output current control and inserted SM numbers selection for the modified IL-MPC-A. Even though the THD performance is improved a lot compared with $N + 1$ output voltage levels, the good dynamic performance is also verified by 60% reduction of the active power at 1.5 s. The current limits of $\Delta i_{\text{cir}j1}$ and $\Delta i_{\text{cir}j2}$ are designed as ± 5 A. The harmonic circulating currents are suppressed, and the average value of SM capacitor voltages are well balanced during the transient period, as shown in Fig. 10(f) and (g).

To verify the effectiveness of overall capacitor voltage control, the current limits of $\Delta i_{\text{cir}j1}$ are set to ± 5 A in Fig. 11 ($x1$) and ($x2$) ($x =$ a, b). $\Delta i_{\text{cir}j2}$ is set to 0 before 1.5 s. It is shown that the average value of the SM capacitor voltages deviates from the normal value. The overall capacitor voltage control is enabled at 1.5 s, and the current limits of $\Delta i_{\text{cir}j2}$ are set to ± 5 and ± 10 A in Fig. 11 ($x1$) and ($x2$), respectively. The average value of SM capacitor voltages recover to the normal value in a short time. The larger the absolute value of $\Delta i_{\text{cir}j2}$, the faster the transient response of overall capacitor voltage control and the larger the circulating current ripple.

Similarly, to verify the effectiveness of arm capacitor voltage control, the current limits of $\Delta i_{\text{cir}j2}$ are set to ± 5 A in Fig. 12 ($x1$) and ($x2$) ($x =$ a, b). $\Delta i_{\text{cir}j1}$ is set to 0 before 1.5 s. The upper

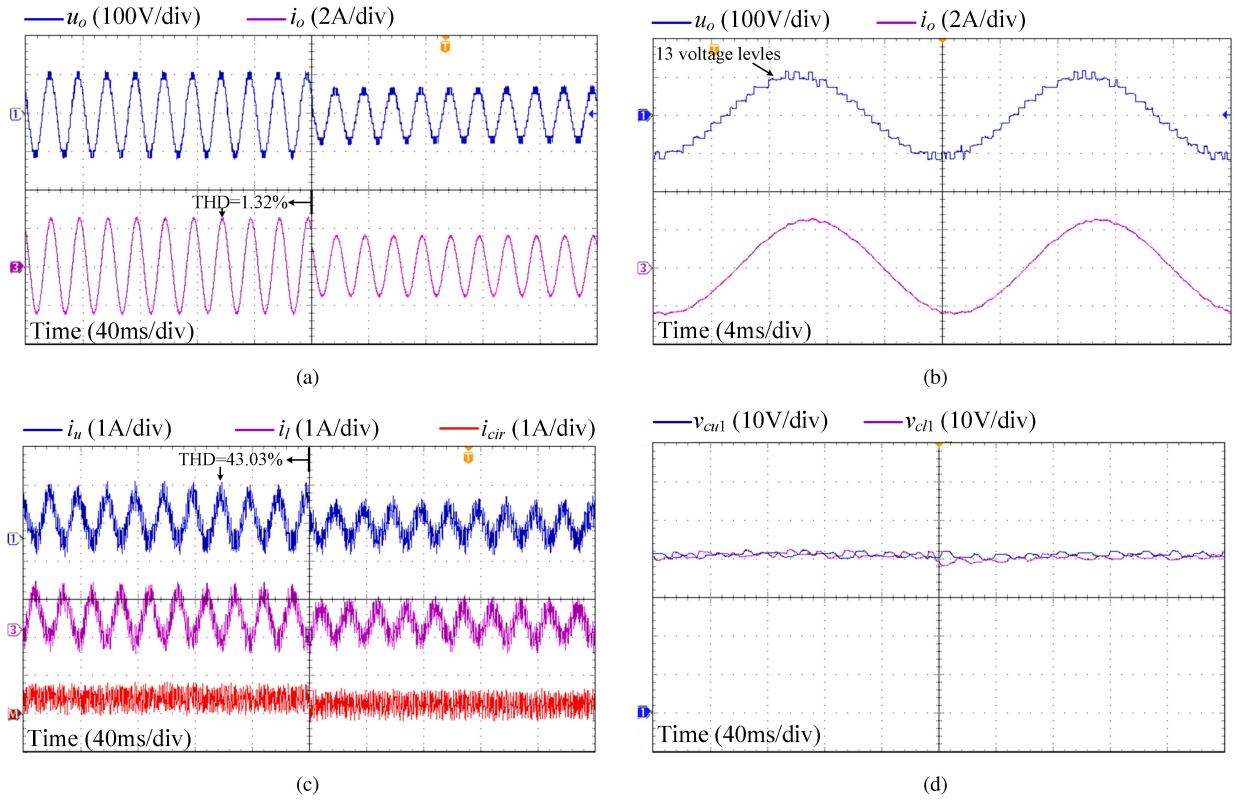

Fig. 14. Experimental verification of steady-state and dynamic-state performances with the modified IL-MPC-A. (a) Load voltage u_o and ac-side output current i_o. (b) Zoomed-in waveforms of u_o and i_o. (c) Upper arm current i_u, lower arm current i_l, and circulating current $i_{\rm cir}$. (d) Upper arm SM capacitor voltage v_{cu1} and lower arm SM capacitor voltage v_{cl1}.

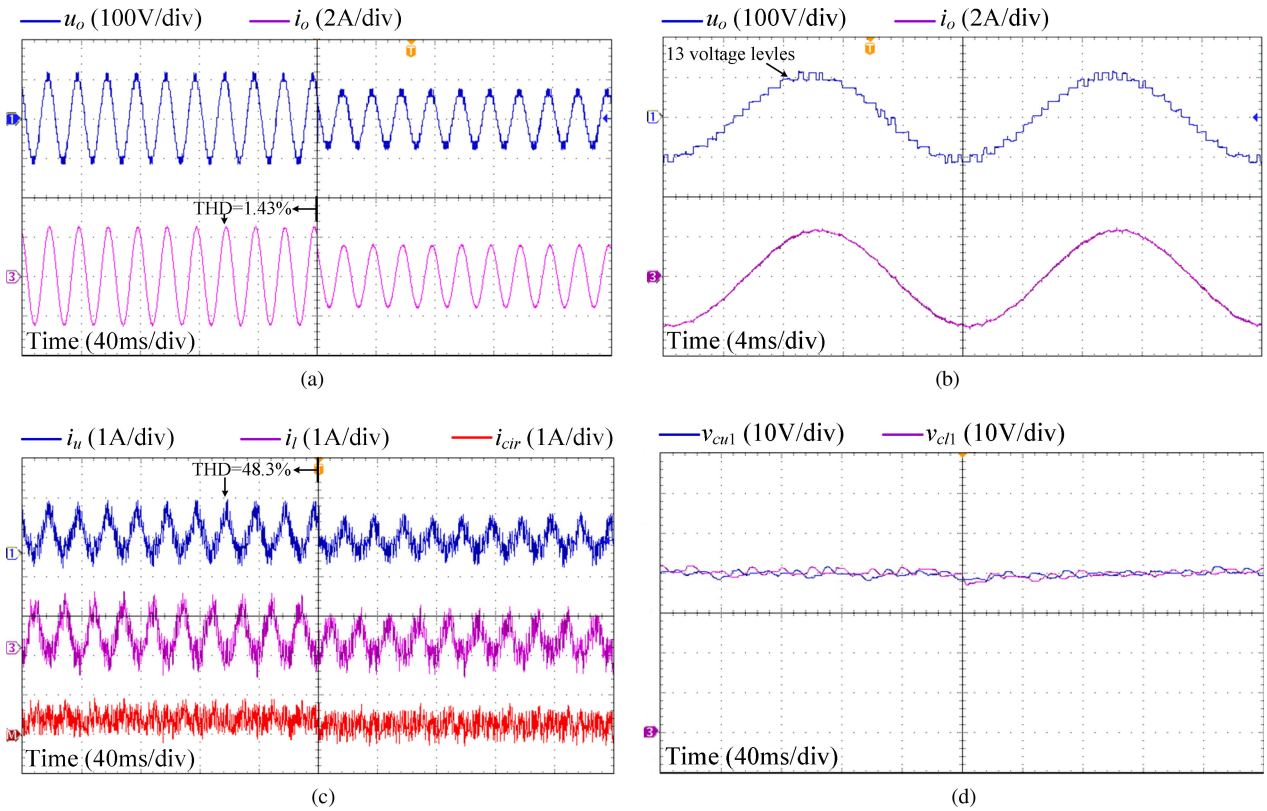

Fig. 15. Experimental verification of steady-state and dynamic-state performances with the modified IL-MPC-B. (a) Load voltage u_o and ac side output current i_o. (b) Zoomed-in waveforms of u_o and i_o. (c) Upper arm current i_u, lower arm current i_l, and circulating current $i_{\rm cir}$. (d) Upper arm SM capacitor voltage v_{cu1} and lower arm SM capacitor voltage v_{cl1}.

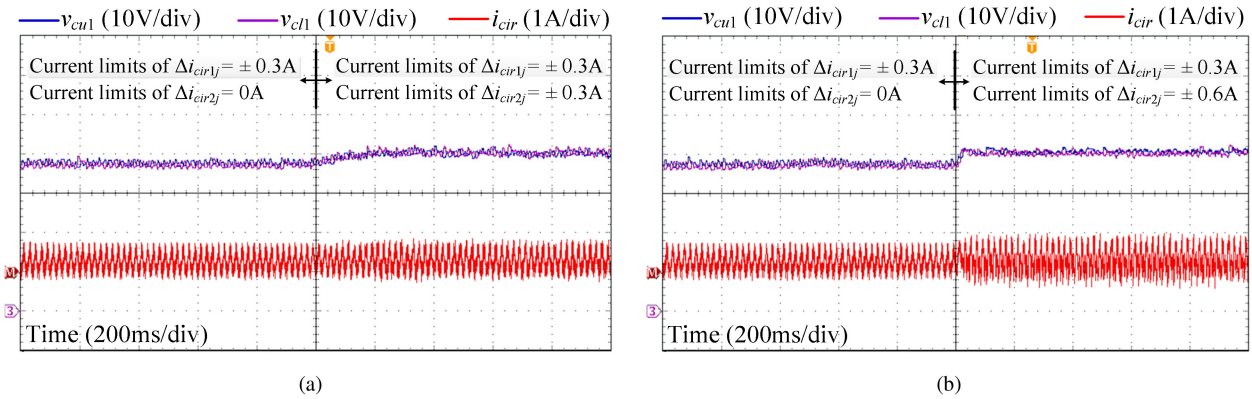

Fig. 16. Experimental verifications of overall capacitor voltage control. (a) $\Delta i_{\mathrm{cir}j2} = \pm 0.3$ A. (b) $\Delta i_{\mathrm{cir}j2} = \pm 0.6$ A.

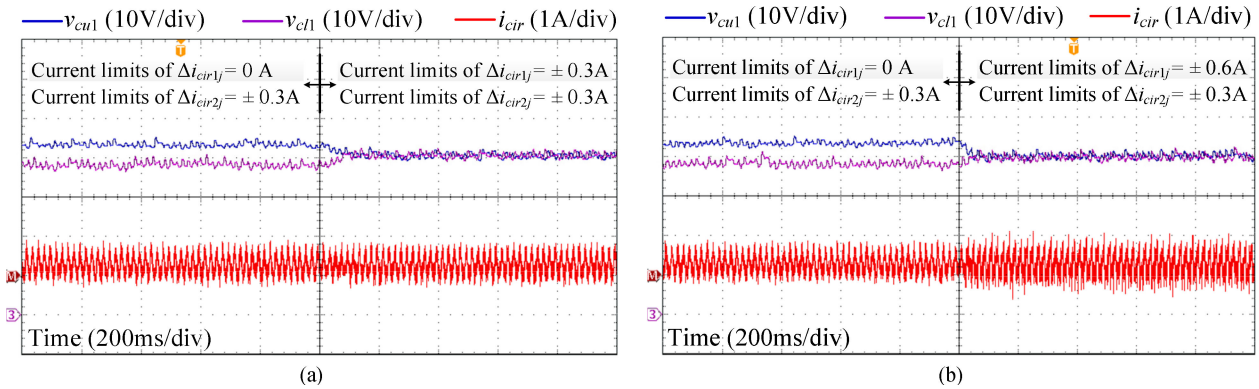

Fig. 17. Experimental verifications of arm capacitor voltage control. (a) $\Delta i_{\mathrm{cir}j1} = \pm 0.3$A. (b) $\Delta i_{\mathrm{cir}j1} = \pm 0.6$ A.

arm and lower arm capacitor voltages deviate from each other. The arm capacitor voltage control is enabled at 1.5 s and the current limits of $\Delta i_{\mathrm{cir}j1}$ are set to ±5 and ±10 A in Fig. 12 (*x*1) and (*x*2), respectively. The arm capacitor voltages are balanced in a short time. In comparison, the absolute values of the current limits in Fig. 12 (*x*1) are larger than those in Fig. 12 (*x*2); thus, the transient response of arm capacitor voltage control is faster in Fig. 12 (*x*2) with larger circulating current ripple.

V. Experimental Validation

A down-scaled single-phase MMC prototype, as shown in Fig. 13, is built to test the performance of the proposed MPC methods, and the system parameters are listed in Table IV. Six SMs are cascaded connected in each arm with a normal capacitor voltage value of 40 V.

The steady-state and dynamic-state performances of the MMC by using the modified IL-MPC-A are displayed in Fig. 14. Before the power decline at 200 ms, 13 load voltage levels are generated in Fig. 14(a) and the corresponding THD of the ac-side output current is 1.32%. The zoomed-in waveforms are shown in Fig. 14(b). The arm currents and circulating current are shown in Fig. 14(c). It shows that the harmonic circulating currents are suppressed and the THD of the upper arm current is 43.03%. The good dynamic performance is demonstrated by a 60% active power reduction. The circulating current and ac-side output current are fast regulated to their new references. The capacitor voltages are well balanced at steady state and during the transient period, as shown in Fig. 14(d).

Fig. 15 demonstrates the effectiveness of the modified IL-MPC-B. The experimental results show that the system performance of the MMC can maintain well by using the modified IL-MPC-B. In particular, the THD of the ac-side output current is 1.43% and increased slightly compared to that of the modified IL-MPC-A before the power decline, as shown in Fig. 15(a). The zoomed-in waveforms given in Fig. 15(b) show that 13 output voltage levels are generated. The current limits of $\Delta i_{\mathrm{cir}j1}$ and $\Delta i_{\mathrm{cir}j2}$ are set to ±0.3 A, so that the capacitor voltages can be well balanced while the circulating current ripple is limited, as shown in Fig. 15(c) and (d). The dynamic performance is similar to that in the experimental results by using the modified IL-MPC-A and is also verified by a 60% reduction of the active power.

The experimental verifications of overall capacitor voltage control are shown in Fig. 16(a) and (b). When the current limits of $\Delta i_{\mathrm{cir}j2}$ are set to 0, the average capacitor voltages are not balanced. When the current limits of $\Delta i_{\mathrm{cir}j2}$ are set to ±0.3 A in Fig. 15(a) and ±0.6 A in Fig. 16(b) at 1 s, the average capacitor voltages are balanced to the normal value. In comparison, the transient response is faster in Fig. 16(b), while the circulating

current ripple is also increased after the overall capacitor voltage control is enabled. The experimental verifications of arm capacitor voltage control are shown in Fig. 17(a) and (b). When the current limits of $\Delta i_{\mathrm{cir}j1}$ are set to 0, the upper arm and lower arm capacitor voltages deviate from each other. When the current limits of $\Delta i_{\mathrm{cir}j1}$ are set to ± 0.3 A in Fig. 17(a) and ± 0.6 A in Fig. 17(b) at 1 s, the arm capacitor voltages are balanced. The transient response is faster in Fig. 17(b) with larger circulating current ripple after the arm capacitor voltage control is enabled.

VI. Conclusion

In this paper, two modified IL-MPC methods are proposed to reduce the computation load of the control system while keeping a good THD performance for the MMC. First, a modified IL-MPC-A is presented by using the predesigned cost function to select the optimal control option. The inserted SM number in one phase-leg is extended to $N \pm \varepsilon$ to suppress the harmonic circulating currents. The arm-inserted SM numbers are adjusted by adding compensation values $\pm$ (1, 2,. . ., ε) to counteract the ac-side output voltage deviation and generate $2N + 1$ voltage levels. The individual capacitor voltage control is realized by the RSF voltage balancing algorithm. Second, another modified IL-MPC-B is presented with easier designing steps and to further reduce computation load with the increase in the SM number. The ac-side output current control has the highest priority and will not be affected by the circulating current control. The overall and arm capacitor voltages are balanced by using an additional control loop to adjust the circulating current reference. Finally, the performance and effectiveness of the proposed methods are verified by a three-phase simulated MMC system and a single-phase laboratory prototype.

References

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE PowerTech Conf.*, Bologna, Italy, Jun. 2003, vol. 3, pp. 272–277.

[2] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-Bus-applications," in *Proc. Int. Power Electron. Conf.*, Jun. 2010, pp. 502–507.

[3] L. Harnefors, A. Antonopoulos, S. Norrga, L. Ängquist, and H.-P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.

[4] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MCCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[5] X. Shi, Z. Wang, B. Liu, Y. Liu, L. M. Tolbert, and F. Wang, "Characteristic investigation and control of modular multilevel converter-based HVDC system under single-line-to-ground fault conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 408–421, Jan. 2015.

[6] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[7] Y. Okazaki *et al.*, "Experimental comparisons between modular multilevel DSCC inverters and TSBC converters for medium-voltage motor drives," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1805–1817, Mar. 2017.

[8] S. Du and J. Liu, "A study on DC voltage control for chopper-cell-based modular multilevel converters in D-STATCOM application," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2030–2038, Oct. 2013.

[9] T. Soong and P. W. Lehn, "Assessment of fault tolerance in modular-multilevel converters with integrated energy storage," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4085–4095, Jun. 2016.

[10] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[11] S. Li, X. Wang, Z. Yao, T. li, and Z. Peng, "Circulating current suppressing strategy for MMC-HVDC based on nonideal proportional resonant controllers under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 387–397, Apr. 2015.

[12] Y. Liang, J. Liu, T. Zhang, and Q. Yang, "Arm current control strategy for MMC-HVDC under unbalanced conditions," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 125–134, Feb. 2017.

[13] K. Sekiguchi, P. Khamphakdi, M. Hagiwara, and H. Akagi, "A grid-level high-power BTB (back-to-back) system using modular multilevel cascade converters without common DC-link capacitor," *IEEE Trans. Ind. Appl.*, vol. 50, no. 4, pp. 2648–2659, Jul. 2014.

[14] P. Khamphakdi, K. Sekiguchi, M. Hagiwara, and H. Akagi, "A transformerless back-to-back (BTB) system using modular multilevel cascaded converters for power distribution systems," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1866–1875, Apr. 2015.

[15] A. E. Leon and S. J. Amodeo, "Energy balancing improvement of modular multilevel converters under unbalanced grid conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6628–6637, Aug. 2017.

[16] J. Rodriguez, P. Cortes, R. Kennel, and M. P. Kazrnierkowski, "Model predictive control—A simple and powerful method to control power converters," in *Proc. 6th IEEE Int. Conf. Power Electron. Motion Control*, Wuhan, China, May 17–20, 2009, pp. 41–49.

[17] P. Cortes, J. Rodriguez, C. Silva, and A. Flores, "Delay compensation in model predictive current control of a three-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 1323–1325, Feb. 2012.

[18] D. E. Quevedo, R. P. Aguilera, M. A. Perez, P. Cortes, and R. Lizana, "Model predictive control of an AFE rectifier with dynamic references," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3128–3136, Jul. 2012.

[19] Y. Zhang, W. Xie, Z. Li, and Y. Zhang, "Model predictive direct power control of a PWM rectifier with duty cycle optimization," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5343–5351, Nov. 2013.

[20] T. Geyer and D. E. Quevedo, "Performance of multistep finite control set model predictive control for power electronics," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1633–1644, Mar. 2015.

[21] F. Ma, Z. He, Q. Xu, A. Luo, L. Zhou, and M. Li, "Multilevel power conditioner and its model predictive control for railway traction system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7275–7285, Nov. 2016.

[22] B. Riar, T. Geyer, and U. Madawala, "Model predictive direct current control of modular multilevel converters: Modeling, analysis, and experimental evaluation," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 431–439, Jan. 2015.

[23] J. Bocker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental comparison of model predictive control and cascaded control of the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 422–430, Jan. 2015.

[24] Z. Gong, P. Dai, X. Yuan, X. Wu, and G. Guo, "Design and experimental evaluation of fast model predictive control for modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 6, pp. 3845–3856, Jun. 2016.

[25] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1538–1547, Jul. 2012.

[26] P. Liu, Y. Wang, W. Cong, and W. Lei, "Grouping-sorting-optimized model predictive control for modular multilevel with reduced computational load," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1896–1907, Mar. 2016.

[27] J.-W. Moon, J.-S. Gwon, J.-W. Park, D.-W. Kang, and J.-M. Kim, "Model predictive control with a reduced number of considered states in a modular multilevel converter for HVDC system," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 608–617, Apr. 2015.

[28] A. Dekka, B. Wu, V. Yaramasu, and N. Zargari, "Model predictive control with common-mode voltage injection for modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1767–1778, Mar. 2017.

[29] A. Dekka, B. Wu, and N. Zargari, "Minimization of DC-bus current ripple in modular multilevel converter under unbalanced conditions," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4125–4131, Jun. 2017.

[30] M. Vatani, B. Bahrani, M. Saeedifard, and M. Hovd, "Indirect finite control set model predictive of modular multilevel converters" *IEEE Trans. Smart Grid.*, vol. 6, no. 3, pp. 1520–1529, May 2015.

[31] F. Zang, W. Li, and G. Joos, "A voltage-level-based model predictive control of modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5301–5312, Aug. 2016.

[32] X. Chen, J. Liu, S. Ouyang, S. Song and H. Wu, "A modified circulating current suppressing strategy for nearest level control based modular multilevel converter," in *Proc. IEEE Energy Convers. Congr Expo.*, 2017, pp. 1817–1822.
[33] P. Cortes *et al.*, "Guidelines for weighting factors design in model predictive control of power converters and drives," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2009, pp. 1–7.
[34] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.
[35] R. Lizana, M. A. Perez, S. Bernet, J. R. Espinoza, and J. Rodriguez, "Control of arm capacitor voltages in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1774–1784, Feb. 2016.

Xingxing Chen (S'16) received the B.S. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2015. He is currently working toward the Ph.D. degree at Xi'an Jiaotong University, Xi'an, China.

His research interests include multilevel converters, converter modeling, and control techniques.

Jinjun Liu (M'97–SM'10) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University (XJTU), Xi'an, China in 1992 and 1997, respectively.

He then joined the XJTU Electrical Engineering School as a faculty. From late 1999 until early 2002, he was with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, USA, as a Visiting Scholar. In late 2002, he was promoted to a Full Professor and then the Head of the Power Electronics and Renewable Energy Center, XJTU, which now comprises 16 faculty members and around 100 graduate students and carries one of the leading power electronics programs in China. He served as an Associate Dean of the Electrical Engineering School, XJTU from 2005 to early 2010, and the Dean for undergraduate education of XJTU from 2009 to early 2015. He is currently a Distinguished Professor of Power Electronics with XJTU, sponsored by the Chang Jiang Scholars Program of the Chinese Ministry of Education. He has coauthored three books (including one textbook), authored or coauthored more than 300 technical papers in peer-reviewed journals and conference proceedings, and holds 39 invention patents (China/US). His research interests include power quality control and utility applications of power electronics, microgrids for sustainable energy and distributed generation, and more/all electronic power systems.

Dr. Liu was the recipient of seven government awards at the national level or provincial/ministerial level for scientific research achievements or academic/teaching career achievements, the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, and the IEEE TRANSACTIONS ON POWER ELECTRONICS 2016 Prize Paper Award. He has served as the IEEE Power Electronics Society (PELS) Region 10 Liaison, has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2006, and has severed as the Vice President for membership of IEEE PELS from 2015. He is on Board of China Electrotechnical Society (CES) and was elected to a Vice President of the CES Power Electronics Society in 2013. He has been the Vice President for International Affairs, China Power Supply Society (CPSS) since 2013 and the founding Editor-in-Chief of CPSS Transactions on Power Electronics and Applications. He has been as the Vice Chair of the Chinese National Steering Committee for College Electric Power Engineering Programs since 2013.

Shuguang Song (S'16) received the B.S. degree from Xi'an Jiaotong University, Xi'an, China, in 2014, where he is currently working toward the Ph.D. degree, both in electrical engineering.

His research interests include multilevel converters in power quality, HVDC, and motor drive applications.

Shaodi Ouyang received the B.S. degree from the Huazhong University of Science and Technology, Wuhan, China, in 2011. He is currently working toward the Ph.D degree in electrical engineering at Xi'an Jiaotong University, Xi'an, China.

His research interests include multilevel converters, power electronic transformers, and dc/dc converters.

Hongda Wu received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2016. He is currently working toward the M.S. degree in electrical engineering at Xi'an Jiaotong University, Xi'an, China.

His research interests include modular multilevel converters and space vector modulation.

Yue Yang received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2017. He is currently working toward the M.S. degree in electrical engineering, Xi'an Jiaotong University.

His research interests include power electronic transformers and reliability of power electronic systems.