Interleaved High Step-Up Converter Integrating Coupled Inductor and Switched Capacitor for Distributed Generation Systems

Yifei Zheng, *Student Member, IEEE*, and Keyue Ma Smedley, *Fellow, IEEE*

***Abstract*—A new interleaved high step-up dc–dc converter is proposed for distributed generation systems. By integrating coupled-inductor and switched-capacitor techniques, the proposed converter achieves a very high step-up voltage gain without an extreme duty cycle or a high turns ratio. Also, a very low switch voltage stress can be achieved; thus, low-voltage-rating MOSFETs with a small ON-resistance can be used to lower the conduction loss. Moreover, thanks to the interleaved operation at the input side, the input current is shared and low current ripple is obtained. Furthermore, the zero-current-switching of the switches is realized, and the reverse recovery problem of the diodes is alleviated. In addition, the leakage energy can be recycled and an additional clamp circuit is not required. The operation principles and characteristics of the converter are discussed in detail. A prototype with 20-V input and 400-V output is developed to verify the theoretical analysis.**

***Index Terms*—Coupled inductor, high step-up converter, interleaved, switched capacitor (SC), voltage multiplier (VM).**

I. Introduction

DISTRIBUTED generation (DG) systems have attracted substantial attention in recent years. The integration of renewable energy into DG systems is becoming increasingly important. The renewable sources, such as photovoltaic arrays and fuel cells, generate a low output voltage, typically 20–40 V. Such a low-level voltage needs to be boosted to a high dc-bus voltage (380 or 400 V) for grid connection [1], [2]. Therefore, a high step-up dc–dc converter with a high efficiency is required in these systems.

The conventional boost converter is not suitable for high step-up applications due to the extreme duty-cycle operation, which results in high power losses. Various boosting techniques have been proposed to achieve high step-up conversion [3]. A switched capacitor (SC), also known as a voltage multiplier (VM) or a charge pump, is one approach to extend the voltage gain. Step-up converters combining the boost-type structure

Manuscript received June 21, 2018; revised September 4, 2018; accepted October 10, 2018. Date of publication October 28, 2018; date of current version May 22, 2019. This work was supported by the Research Scholarship of One-Cycle Control Inc. Recommended for publication by Associate Editor C. K. Tse. *(Corresponding author: Yifei Zheng.)*

The authors are with the Department of Electrical Engineering and Computer Science, University of California, Irvine, CA 92697 USA (e-mail:

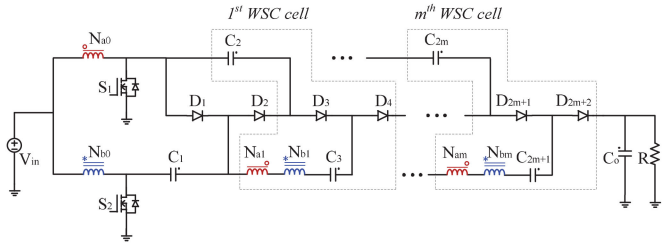

Fig. 1. Generalized structure of the proposed converter.

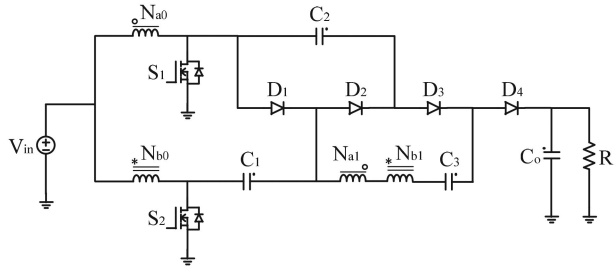

Fig. 2. Basic topology with one WSC cell.

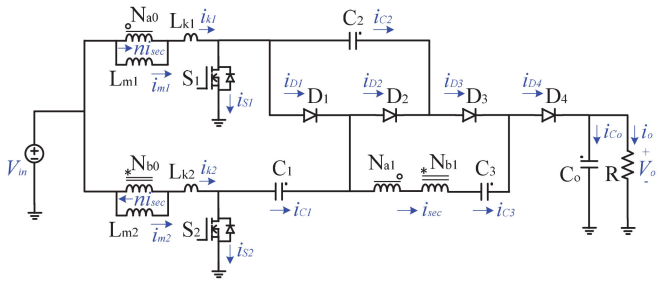

Fig. 3. Equivalent circuit.

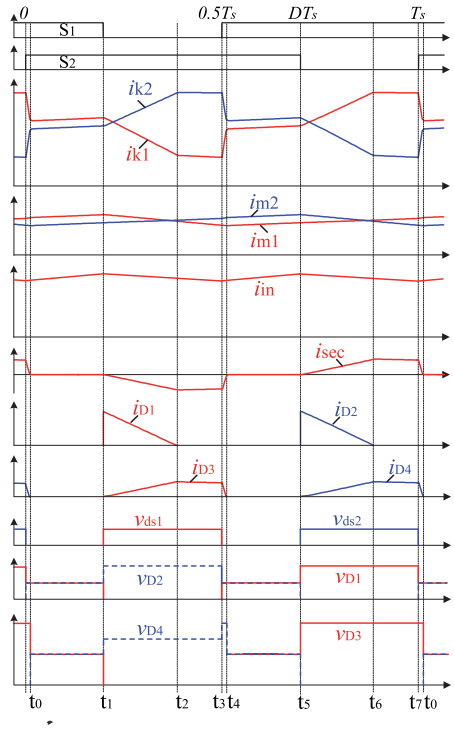

Fig. 4. Key waveforms.

with magnetic coupling and a VM module was proposed in [33]. Unfortunately, the currents through the two coupled inductors are not balanced. An interleaved high step-up converter with an active clamp circuit was proposed in [34]. The zero-voltage switching of the switches and the zero-current switching (ZCS) of the diodes are achieved, but additional active switches and gate drivers are required, leading to high costs. In [35]–[37], interleaved high step-up converters employing six windings were proposed. More flexible voltage gains are obtained at the price of increased circuit complexity.

Inspired by the aforementioned literature, this paper proposes a new interleaved high step-up converter integrating coupled-inductor and SC techniques. Interleaved operation is employed at the input side to reduce the input current ripple and increase the current level. Due to the SC and the series connection of the secondary windings, a very high step-up voltage gain can be achieved without an extreme duty cycle or a high turns ratio. Moreover, the proposed converter has a very low switch voltage stress; thus, low-voltage-rating MOSFETs with a small ON-resistance can be used to reduce the conduction loss. Furthermore, the ZCS turn-ON of the switches is realized, and the reverse recovery problem of the diodes is alleviated, which help reduce the switching losses. In addition, the leakage energy can be recycled, and an additional clamp circuit is not required.

The rest of this paper is organized as follows. The operation principles of the converter are described in Section II. Characteristics are analyzed in Section III. Topology variations are provided in Section IV. Design considerations are discussed in Section V. Experimental results are presented in Section VI. Conclusions are given in Section VII.

II. Proposed Converter and Operation Principles

The generalized structure of the proposed converter is shown in Fig. 1. It comprises an interleaved voltage-doubler boost converter and multiple winding-based SC (WSC) cells. Each WSC cell has two diodes, two capacitors, and two windings of the coupled inductors. Fig. 2 shows the basic topology with one WSC cell. It is composed of two coupled inductors, two switches, four diodes, three energy transfer capacitors, and one output capacitor. The primary windings of the coupled inductors are connected in parallel, and the secondary windings are connected in series. The turns ratios of the coupled inductors are the same. The coupling references are denoted by "o" and "$*$". Fig. 3 shows the equivalent circuit. Both coupled inductors are modeled as an ideal transformer with magnetizing inductance and leakage inductance. The two switches of the proposed converter are driven in an interleaved manner. The duty cycle D during the steady state is larger than 0.5. In this paper, the operation in continuous conduction mode (CCM) is discussed. The key waveforms are shown in Fig. 4. Eight modes are observed during one switching period. The corresponding circuits for each mode are shown in Fig. 5.

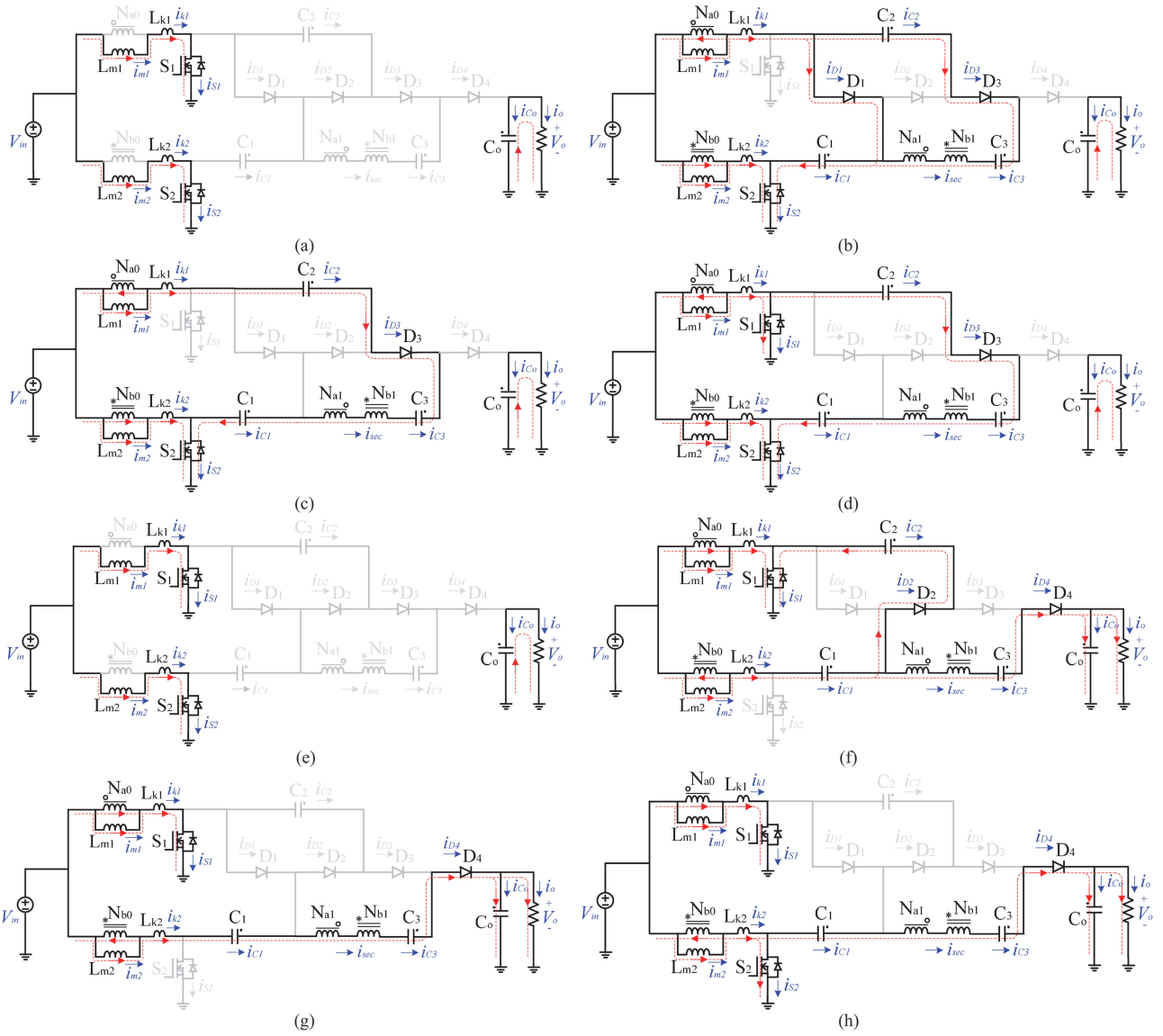

Fig. 5. Operation modes. (a) Mode 1 $[t_0$–$t_1]$. (b) Mode 2 $[t_1$–$t_2]$. (c) Mode 3 $[t_2$–$t_3]$. (d) Mode 4 $[t_3$–$t_4]$. (e) Mode 5 $[t_4$–$t_5]$. (f) Mode 6 $[t_5$–$t_6]$. (g) Mode 7 $[t_6$–$t_7]$. (h) Mode 8 $[t_7$–$t_0]$.

Mode 1 [t_0–t_1]: Both switches are ON, and all diodes are OFF, as shown in Fig. 5(a). The input source charges the magnetizing inductances and leakage inductances. As the leakage inductance is negligible compared with the magnetizing inductance, the following equations are obtained:

$$v_{m1} = V_{\text{in}} \tag{1}$$

$$v_{m2} = V_{\text{in}}. \tag{2}$$

Mode 2 [t_1–t_2]: At t_1, switch S_1 is turned-OFF, and thereby, diodes D_1 and D_3 conduct. The input source still charges L_{m2} and L_{k2}, while L_{m1} and L_{k1} begin to release energy, as shown in Fig. 5(b). The voltage stress is clamped by capacitor C_1. The leakage current i_{k1} charges capacitor C_1. Capacitor C_2 transfers energy to C_3 through diode D_3 and the secondary windings. The secondary current of the coupled inductors i_{sec} increases linearly in the opposite direction. The current through D_1 decreases linearly. The following equations are obtained:

$$v_{m1} = V_{\text{in}} - V_{C1} \tag{3}$$

$$v_{m2} = V_{\text{in}} \tag{4}$$

$$V_{C3} - V_{C2} - n\left(v_{m2} - v_{m1}\right) = 0 \tag{5}$$

$$i_{\text{sec}}\left(t\right) = -i_{D3}\left(t\right) = \frac{-nV_{C1} - V_{C2} + V_{C3}}{n^2\left(L_{k1} + L_{k2}\right)}\left(t - t_1\right) \tag{6}$$

$$i_{D1}\left(t\right) = i_{k1}\left(t\right) + i_{\text{sec}}\left(t\right) = i_{m1}\left(t\right) + \left(n+1\right) i_{\text{sec}}\left(t\right) \tag{7}$$

where $n = N_{a1}/N_{a0} = N_{b1}/N_{b0}$.

Solving (3)–(5), the following relationship can be derived:

$$V_{C3} - V_{C2} = nV_{C1}. \tag{8}$$

Mode 3 [t_2–t_3]: At t_2, the current through D_1 decreases to zero, and D_1 is naturally turned-OFF. Therefore, the reverse

recovery problem of D_1 is alleviated. The leakage current i_{k1} becomes equal to the secondary current $i_{\rm sec}$. It discharges C_2 and charges C_3 and C_1, as shown in Fig. 5(c). The equations are obtained as follows:

$$V_{\rm in} = v_{m1} + V_{C1} - V_{C2} + V_{C3} - n\left(v_{m2} - v_{m1}\right) \quad (9)$$

$$v_{m2} = V_{\rm in} \quad (10)$$

$$i_{k1}\left(t\right) = i_{m1}\left(t\right) + ni_{\rm sec}\left(t\right) = -i_{\rm sec}\left(t\right). \quad (11)$$

By manipulating (11), the secondary current $i_{\rm sec}$ can be expressed as follows:

$$i_{\rm sec}\left(t\right) = -i_{D3}\left(t\right) = -i_{k1}\left(t\right) = -\frac{1}{n+1}i_{m1}\left(t\right). \quad (12)$$

Then, i_{k2} can be written as follows:

$$i_{k2}\left(t\right) = i_{m2}\left(\rm t\right) - ni_{\rm sec}\left(t\right) = i_{m2}\left(t\right) + \frac{n}{n+1}i_{m1}\left(t\right). \quad (13)$$

Solving (8)–(10), v_{m1} in this mode can be derived as follows:

$$v_{m1} = V_{\rm in} - V_{C1}. \quad (14)$$

Mode 4 [t_3–t_4]: At t_3, switch S_1 is turned-ON, as shown in Fig. 5(d). As the leakage inductances limit the current changing rate, the ZCS of S_1 can be achieved. The current of D_3 decreases, and the falling rate is controlled by the leakage inductances, which alleviates the reverse recovery problem of D_3. The falling rate of D_3 is given by

$$\frac{di_{D3}\left(t\right)}{dt} = -\frac{V_{C3} + V_{C1} - V_{C2}}{n^2\left(L_{k1} + L_{k2}\right)}. \quad (15)$$

Mode 5 [t_4–t_5]: At t_4, the current of D_3 decreases to zero, and D_3 is turned-OFF, as shown in Fig. 5(e). This mode repeats mode 1.

Mode 6 [t_5–t_6]: At t_5, switch S_2 is turned-OFF, and thereby, diodes D_2 and D_4 conduct. The input source charges L_{m1} and L_{k1}, while L_{m2} and L_{k2} begin to release energy, as shown in Fig. 5(f). The voltage stress of S_2 is clamped by $V_{C2} - V_{C1}$. The leakage current i_{k2} discharges C_1. The secondary current of the coupled inductors $i_{\rm sec}$ increases linearly. It discharges C_3 and supplies the load current. The secondary windings and capacitor C_3 serve as voltage sources to extend the voltage gain. The current through D_2 decreases linearly and charges C_2. The following equations are obtained:

$$v_{m1} = V_{\rm in} \quad (16)$$

$$v_{m2} = V_{\rm in} + V_{C1} - V_{C2} \quad (17)$$

$$V_o - V_{C2} - V_{C3} + n\left(v_{m2} - v_{m1}\right) = 0 \quad (18)$$

$$i_{\rm sec}\left(t\right) = i_{D4}\left(t\right) = \frac{-V_o - nV_{C1} + \left(n+1\right)V_{C2} + V_{C3}}{n^2\left(L_{k1} + L_{k2}\right)}\left(t - t_5\right) \quad (19)$$

$$i_{D2}\left(t\right) = i_{k2}\left(t\right) - i_{\rm sec}\left(t\right) = i_{m2}\left(t\right) - \left(n+1\right)i_{\rm sec}\left(t\right). \quad (20)$$

Solving (16)–(18), the following relationship can be derived:

$$V_o = \left(n+1\right)V_{C2} - nV_{C1} + V_{C3}. \quad (21)$$

Mode 7 [t_6–t_7]: At t_6, the current through D_2 decreases to zero, and D_2 is naturally turned-OFF. Therefore, the reverse recovery problem of D_2 is alleviated. The leakage current i_{k2} becomes equal to the secondary current $i_{\rm sec}$. It discharges C_1 and C_3 and supplies the load current, as shown in Fig. 5(g). The equations are obtained as follows:

$$v_{m1} = V_{\rm in} \quad (22)$$

$$V_{\rm in} = v_{m2} - V_{C1} + n\left(v_{m2} - v_{m1}\right) - V_{C3} + V_o \quad (23)$$

$$i_{k2}\left(t\right) = i_{m2}\left(\rm t\right) - ni_{\rm sec}\left(t\right) = i_{\rm sec}\left(t\right). \quad (24)$$

By manipulating (24), the secondary current $i_{\rm sec}$ can be expressed as follows:

$$i_{\rm sec}\left(t\right) = -i_{D4}\left(t\right) = i_{k2}\left(t\right) = \frac{1}{n+1}i_{m2}\left(t\right). \quad (25)$$

Then, i_{k1} can be written as follows:

$$i_{k1}\left(t\right) = i_{m1}\left(t\right) + ni_{\rm sec}\left(t\right) = i_{m1}\left(t\right) + \frac{n}{n+1}i_{m2}\left(t\right). \quad (26)$$

Solving (21)–(23), v_{m2} in this mode can be derived as follows:

$$v_{m2} = V_{\rm in} + V_{C1} - V_{C2}. \quad (27)$$

Mode 8 [t_7–t_0]: At t_7, switch S_2 is turned-ON, as shown in Fig. 5(h). As the leakage inductances limit the current changing rate, the ZCS of S_2 can be achieved. The current of D_4 decreases, and the falling rate is controlled by the leakage inductances, which alleviates the reverse recovery problem of D_4. The falling rate of D_4 is given by

$$\frac{di_{D4}\left(t\right)}{dt} = -\frac{V_o - V_{C1} - V_{C3}}{n^2\left(L_{k1} + L_{k2}\right)}. \quad (28)$$

III. Performance Analysis

A. Voltage Gain

By applying the voltage-second balance principle to L_{m1} and L_{m2}, the following equations are obtained:

$$V_{\rm in}D + \left(V_{\rm in} - V_{C1}\right)\left(1 - D\right) = 0 \quad (29)$$

$$V_{\rm in}D + \left(V_{\rm in} + V_{C1} - V_{C2}\right)\left(1 - D\right) = 0. \quad (30)$$

Solving (29) and (30), the voltages V_{C1} and V_{C2} can be expressed as follows:

$$V_{C1} = \frac{V_{\rm in}}{1 - D} \quad (31)$$

$$V_{C2} = \frac{2V_{\rm in}}{1 - D}. \quad (32)$$

Substituting (31) and (32) in (8), V_{C3} can be derived as follows:

$$V_{C3} = \frac{\left(n+2\right)V_{\rm in}}{1 - D}. \quad (33)$$

Substituting (31)–(33) in (21), the voltage gain can be derived as follows:

$$M = \frac{V_o}{V_{\rm in}} = \frac{2n+4}{1 - D}. \quad (34)$$

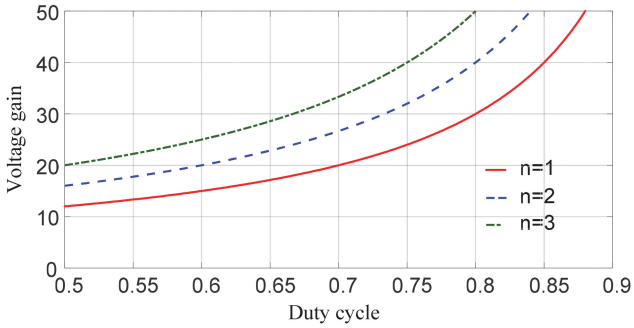

Fig. 6. Voltage gain versus duty cycle under different turns ratios.

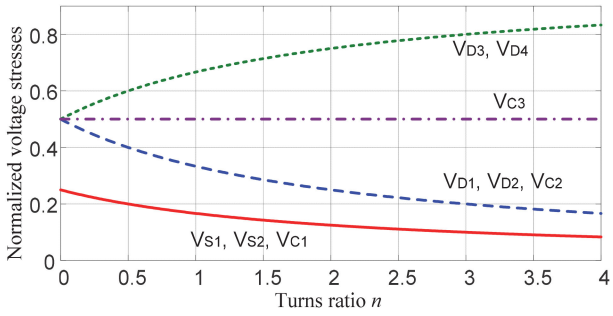

Fig. 7. Normalized voltage stresses.

Fig. 6 shows the curves of the voltage gain versus the duty cycle under different turns ratios. It can be seen that the proposed converter has a high step-up voltage gain without an extreme duty cycle or a high turns ratio.

B. Voltage Stress

The voltage stresses of the capacitors are given by

$$V_{C1}=\frac{V_o}{2n+4};\ V_{C2}=\frac{V_o}{n+2};\ V_{C3}=\frac{V_o}{2}. \tag{35}$$

The voltage stresses of the switches can be derived as follows:

$$V_{S1}=V_{S2}=\frac{V_{\text{in}}}{1-D}=\frac{1}{2n+4}V_o. \tag{36}$$

It can be seen that the switch voltage stress is only one-sixth of the output voltage, if the turns ratio is one. It becomes even lower when the turns ratio increases. Therefore, low-voltage-rating MOSFETs with a small ON-resistance are allowed to lower the conduction loss.

The voltage stresses of the diodes are determined by the capacitor voltages. They are given by

$$V_{D1}=V_{D2}=\frac{1}{n+2}V_o;\ V_{D3}=V_{D4}=\frac{n+1}{n+2}V_o. \tag{37}$$

The relationship between the voltage stresses of the components and the turns ratios of the coupled inductor is shown in Fig. 7. It can be seen that the switch voltage stress decreases as the voltage gain is extended by increasing the turns ratio. The voltage stresses on D_1 and D_2 also decrease as the turns ratio increases. The voltage stresses on D_3 and D_4 increase as the turns ratio increases, but they are always lower than the output voltage. The voltage stress on C_3 is always half of the output voltage. The voltage stresses on C_1 and C_2 decrease as the turns ratio increases.

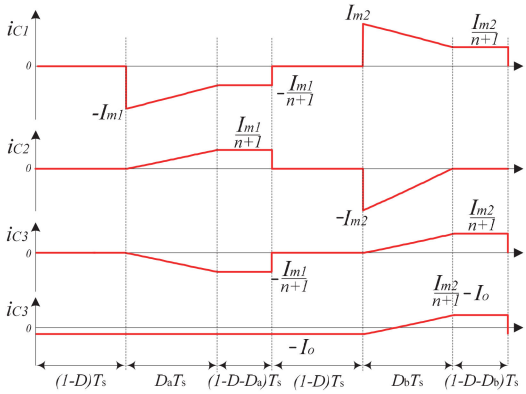

Fig. 8. Current waveforms of the capacitors.

C. Input Current Sharing

The average magnetizing currents are assumed as I_{m1} and I_{m2} by applying small-ripple approximation. Let t_2–$t_1=D_aT_s$ and t_6–$t_5=D_bT_s$. Ignoring modes 4 and 8, the current waveforms of the capacitors are as shown in Fig. 8. According to the charge balance of the capacitors, the following equations are obtained:

$$\frac{1}{2}\left(I_{m1}+\frac{I_{m1}}{n+1}\right)D_a+\frac{I_{m1}}{n+1}(1-\ D-D_a)$$
$$=\frac{1}{2}\left(I_{m2}+\frac{I_{m2}}{n+1}\right)D_b+\frac{I_{m2}}{n+1}(1-\ D-D_b) \tag{38}$$

$$\frac{1}{2}\cdot\frac{I_{m1}}{n+1}D_a+\frac{I_{m1}}{n+1}(1-D-D_a)=\frac{1}{2}I_{m2}D_b \tag{39}$$

$$\frac{1}{2}\cdot\frac{I_{m1}}{n+1}D_a+\frac{I_{m1}}{n+1}(1-D-D_a)$$
$$=\frac{1}{2}\cdot\frac{I_{m2}}{n+1}D_b+\frac{I_{m2}}{n+1}(1-D-D_b) \tag{40}$$

$$\left(\frac{1}{2}\cdot\frac{I_m}{n+1}-I_o\right)D_b+\left(\frac{I_m}{n+1}-I_o\right)(1-D-D_b)=I_oD. \tag{41}$$

Solving (38)–(41), the following relationships can be obtained:

$$I_{m1}=I_{m2}=I_m=\frac{n+2}{1-D}I_o \tag{42}$$

$$D_a=D_b=\frac{2}{n+2}(1-D). \tag{43}$$

It can be seen that the magnetizing currents of the two coupled inductors are balanced due to the charge balance of the capacitors.

The secondary windings of the coupled inductors are connected in series; thus, they share the same secondary current.

The average current flowing through L_{k1} can be evaluated as follows:

$$I_{Lk1} = \frac{1}{T_s}\left(\int_0^{(D-0.5)T_s} i_{m1}dt + \int_{(D-0.5)T_s}^{0.5T_s} (i_{m1} + ni_{\rm sec})\,dt + \int_{0.5T_s}^{DT_s} i_{m1}dt + \int_{DT_s}^{T_s} (i_{m1} + ni_{\rm sec})\,dt \right) = I_m. \tag{44}$$

The average current flowing through L_{k2} can be evaluated as follows:

$$I_{Lk2} = \frac{1}{T_s}\left(\int_0^{(D-0.5)T_s} i_{m2}dt + \int_{(D-0.5)T_s}^{0.5T_s} (i_{m2} - ni_{\rm sec})\,dt + \int_{0.5T_s}^{DT_s} i_{m2}dt + \int_{DT_s}^{T_s} (i_{m2} - ni_{\rm sec})\,dt \right) = I_m. \tag{45}$$

From (44) and (45), it can be seen that the primary currents of the coupled inductors are balanced.

D. Input Current Ripple

The input current of the proposed converter equals the sum of the primary currents of the coupled inductors. Since the coupled inductors share the same secondary current, the input current can be derived as follows:

$$i_{\rm in} = (i_{m1} + ni_{\rm sec}) + (i_{m2} - ni_{\rm sec}) = i_{m1} + i_{m2}. \tag{46}$$

From the operation principle, it can be seen that the magnetizing currents have an interleaved feature. The frequency of the input current ripple is twice the switching frequency. Therefore, the input current is continuous, and the ripple is significantly reduced.

The peak-to-peak ripple of the magnetizing current is given by

$$\Delta i_{Lm} = \frac{V_{\rm in} D}{L_m f_s}. \tag{47}$$

The peak-to-peak ripple of the input current is given by

$$\Delta i_{\rm in} = \frac{V_{\rm in}(2D-1)}{L_m f_s}. \tag{48}$$

The input current ripple normalized to the magnetizing current ripple is illustrated in Fig. 9. It can be seen that a smaller duty cycle results in a better ripple cancellation effect. Also, as seen from (47) and (48), smaller duty cycles lead to lower magnetizing current ripples and input current ripples. Thus, the size of the coupled inductor can be reduced, and the current stress of the input capacitor can be alleviated, which help improve the power density.

E. Voltage Gain Considering Parasitic Elements

Similar to the conventional boost converter, the voltage gain of the proposed converter would deviate from the ideal value if parasitic elements are considered, especially under extreme duty cycles. The equivalent circuit, including parasitic elements, is illustrated in Fig. 10. In order to simplify the calculation, it is assumed that the two switches have an identical ON-resistance $r_{\rm ON}$, the two coupled inductors have an identical primary resistance $r_{\rm pri}$ and an identical secondary resistance $r_{\rm sec}$, all capacitors have the same equivalent series resistance r_c, and all diodes have the same forward voltage drop V_d. Besides, the small-ripple approximation is used, and modes 4 and 8 are ignored in the calculation.

Fig. 9. Normalized input current ripple versus duty cycle.

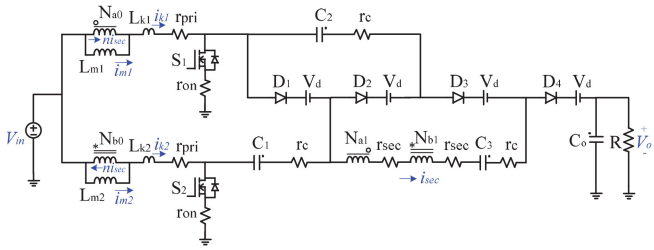

Fig. 10. Equivalent circuit including parasitic elements.

In modes 1 and 5, the equations with parasitic elements are derived as follows:

$$V_{\rm in} = v_{m1} + I_m\,(r_{\rm pri} + r_{\rm ON}) \tag{49}$$

$$V_{\rm in} = v_{m2} + I_m\,(r_{\rm pri} + r_{\rm ON}). \tag{50}$$

In mode 2, the equations with parasitic elements are derived as follows:

$$V_{\rm in} = v_{m1} + V_{C1} + (I_m + ni_{\rm sec})\,(r_{\rm pri} + r_c) + V_d + 2I_m r_{\rm ON} \tag{51}$$

$$V_{\rm in} = v_{m2} + (I_m - ni_{\rm sec})\,r_{\rm pri} + 2I_m r_{\rm ON} \tag{52}$$

$$V_{C3} - V_{C2} + n\,(v_{m1} - v_{m2}) - i_{\rm sec}\,(2r_{\rm sec} + 2r_c) = 0. \tag{53}$$

In mode 3, the equations with parasitic elements are derived as follows:

$$V_{\rm in} = v_{m1} + V_{C1} - V_{C2} + V_{C3} + n\,(v_{m1} - v_{m2}) - i_{\rm sec}\,(r_{\rm pri} + 3r_c + 2r_{\rm sec}) + V_d + 2I_m r_{\rm ON} \tag{54}$$

$$V_{\rm in} = v_{m2} + (I_m - ni_{\rm sec})\,r_{\rm pri} + 2I_m r_{\rm ON}. \tag{55}$$

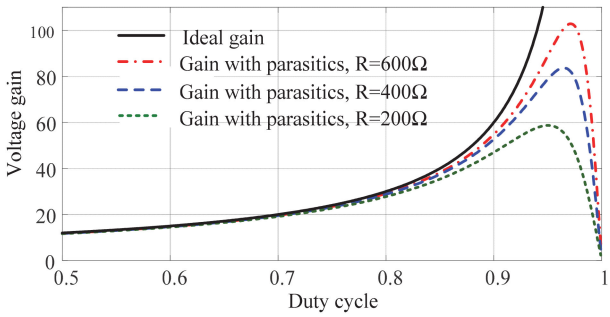

Fig. 11. Voltage gain with parasitic elements ($r_{\rm ON}=7.5$ mΩ, $r_{\rm pri}=20$ mΩ, $r_{\rm sec}=45$ mΩ, $r_c=8$ Ω, $V_d=0.75$ V, $n=1$, $V_{\rm in}=20$V).

In mode 6, the equations with parasitic elements are derived as follows:

$$V_{\rm in}=v_{m1}+(I_m+ni_{\rm sec})\,r_{\rm pri}+(2I_m-i_{\rm sec})\,r_{\rm ON} \tag{56}$$

$$V_{\rm in}=v_{m2}-V_{C1}+V_{C2}+(2I_m-i_{\rm sec})\,r_{\rm ON}+V_d+(I_m-ni_{\rm sec})\,(r_{\rm pri}+r_c)+(I_m-(n+1)i_{\rm sec})r_c \tag{57}$$

$$V_o-V_{C2}-V_{C3}+n\,(v_{m2}-v_{m1})-(\,I_m-(n+1)\,i_{\rm sec})\,r_c+i_{\rm sec}\,(2r_{\rm sec}+r_c)=0. \tag{58}$$

In mode 7, the equations with parasitic elements are derived as follows:

$$V_{\rm in}=v_{m1}+(I_m+ni_{\rm sec})\,(r_{\rm pri}+r_{\rm ON}) \tag{59}$$

$$V_{\rm in}=v_{m2}-V_{C1}+n\,(v_{m2}-v_{m1})-V_{C3}+V_o+i_{\rm sec}\,(r_{\rm pri}+2r_{\rm sec}+2r_c)+V_d. \tag{60}$$

By applying the voltage-second balance principle to L_{m1} and L_{m2}, the voltage gain considering parasitic elements can be solved as follows:

$$\frac{V_o}{V_{\rm in}}=\frac{\frac{2n+4}{1-D}-\frac{4V_d}{V_{\rm in}}}{1+\frac{n+2}{(n+1)^2(1-D)}\left(U\frac{r_{\rm ON}}{R}+V\frac{r_{\rm pri}}{R}+W\frac{r_{\rm sec}}{R}+Z\frac{r_c}{R}\right)} \tag{61}$$

where

$$U=7n^3+23n^2+28n+11+\frac{2(n+1)^2(n+2)(2D-1)}{1-D}$$

$$V=8n^3+18n^2+20n+8+\frac{2(n+1)^2(n+2)(2D-1)}{1-D}$$

$$W=4n+2$$

$$Z=1.5n^2+10n+6.$$

As discussed earlier, the ideal voltage gain of the proposed converter is independent of the load conditions. However, if the parasitic elements are considered, under given parasitic parameters, the voltage gain would decrease as the load increases, and the voltage gain would collapse under extreme duty cycles, as shown in Fig. 11.

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH SIMILAR CONVERTERS

Topologies	Proposed	Ref. [29]	Ref. [31]	Ref. [33]	Ref. [30]
Voltage gain	$\frac{2n+4}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+3}{1-D}$	$\frac{2n+2}{1-D}$
Voltage stress of switches	$\frac{1}{2n+4}$	$\frac{1}{2n+2}$	$\frac{1}{2n+2}$	$\frac{1}{2n+3}$	$\frac{1}{2n+2}$
Max. voltage stress of diodes	$\frac{n+1}{n+2}$	$\frac{n}{n+1}$	$\frac{n}{n+1}$	$\frac{2n+1}{2n+3}$	$\frac{n}{n+1}$
Switches	2	2	2	2	2
Diodes	4	4	4	4	6
Magnetic cores	2	2	2	2	2
Windings	4	4	4	4	4
Capacitors	4	4	4	4	5
Common ground?	Yes	Yes	No	Yes	Yes
Balanced current?	Yes	Yes	Yes	No	Yes

F. Comparison

The proposed converter is compared with other similar converters in the literature. All the converters have an input interleaved operation and can be used in high step-up applications. The voltage gain, normalized voltage stresses of the switches and diodes, the number of components, common ground connection, and current-sharing performance are given in Table I.

It can be seen from Table I that the proposed converter has the same component counts as the converters in [29], [31], and [33]. However, the proposed converter achieves a higher voltage gain and a lower switch voltage stress under the same duty cycle and turns ratio, as illustrated in Fig. 12. Also, the proposed converter has the features of common ground connection and balanced current-sharing. Compared with the converter presented in [30], the proposed converter has fewer components, but it achieves a higher voltage gain and a lower switch voltage stress. Overall, the proposed converter is more suitable for high step-up applications, and low-voltage-rating MOSFETs with a small ON-resistance are allowed to lower the conduction loss. It should be pointed out that the maximum diode voltage stress of the proposed converter is larger than that of the other converters, but it is still lower than the output voltage.

IV. TOPOLOGY VARIATIONS

In higher step-up applications, SC cells, shown in Fig. 13(a), can be added to the basic topology in order to further extend the voltage gain and reduce the switch voltage stress. If one SC cell is added, the new voltage gain can be expressed as follows:

$$\frac{V_o}{V_{\rm in}}=\frac{4n+6}{1-D}. \tag{62}$$

Another extension is to employ a coupled inductor with multiple windings. The WSC cell shown in Fig. 13(b) can be added.

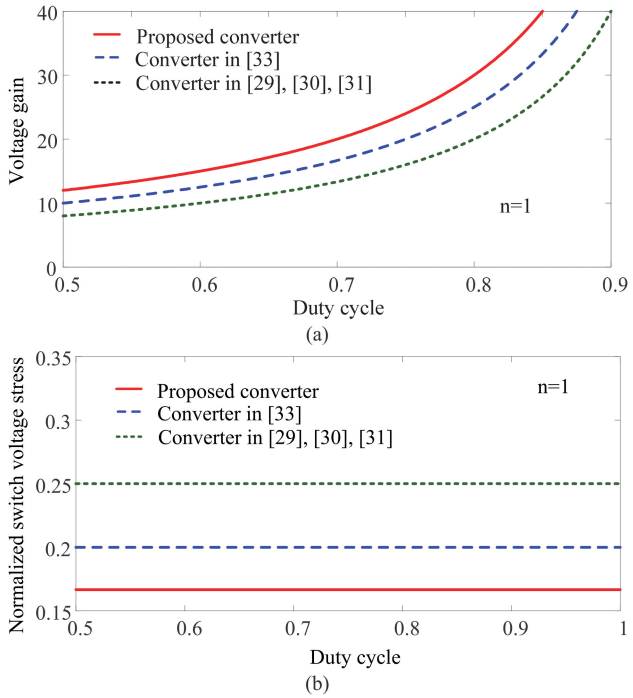

Fig. 12. Comparison when $n = 1$. (a) Voltage gain. (b) Normalized switch voltage stress.

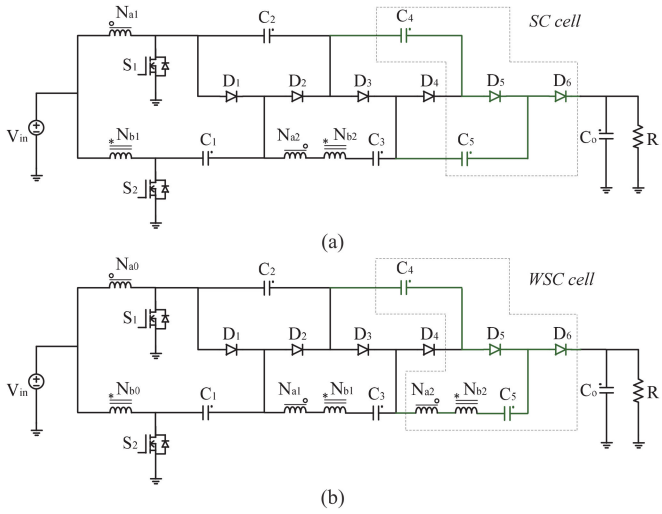

Fig. 13. Topology variations by adding (a) SC cells and (b) WSC cells.

The extra windings provide an extra degree of freedom; thus, a more flexible voltage gain can be achieved. If one WSC cell is added, the new voltage gain can be expressed as follows:

$$\frac{V_o}{V_{\text{in}}} = \frac{4n + 2n' + 6}{1 - D} \tag{63}$$

where $n = N_{a1}/N_{a0} = N_{b1}/N_{b0}$ and $n' = N_{a2}/N_{a0} = N_{b2}/N_{b0}$.

These variations achieve a higher voltage gain and a lower component voltage stress with a higher cost and an increased circuit complexity. They are more suitable for ultra-high step-up applications.

V. Design Considerations

A. Coupled-Inductor Design

From the aforementioned analysis, the duty cycle should be designed greater than 0.5. An extreme duty cycle must be avoided since the voltage gain could collapse. Once a proper duty cycle is selected, the turns ratio of the coupled inductors is determined by the required voltage gain. It is given by

$$n = \frac{V_o}{V_{\text{in}}} \cdot \frac{1 - D}{2} - 2. \tag{64}$$

The magnetizing inductances of the coupled inductors can be designed based on the magnetizing current ripple, which is also closely related to the input current ripple. The magnetizing inductance can be calculated as follows:

$$L_m = L_{m1} = L_{m2} = \frac{V_{\text{in}} D}{\Delta i_{Lm} f_s} = \frac{V_{\text{in}} (2D - 1)}{\Delta i_{\text{in}} f_s}. \tag{65}$$

In this paper, the converter is designed to be operated in the CCM. The minimum magnetizing inductance value for the CCM operation is given by

$$L_m > L_{m\_\text{crit}} = \frac{V_{\text{in}} D (1 - D)}{2 (n + 2) I_o f_s}. \tag{66}$$

The leakage inductances of the coupled inductors help alleviate the diode reverse recovery problem. Thus, the leakage inductances can be designed based on the current falling rate of the diodes, which are given by

$$L_k = L_{k1} = L_{k2} = \frac{(n + 1) V_o}{4n^2 (n + 2) \frac{di_{D3}}{dt}} = \frac{(n + 1) V_o}{4n^2 (n + 2) \frac{di_{D4}}{dt}}. \tag{67}$$

The peak currents of the coupled inductors are given by

$$I_{k1\_\text{pk}} = I_{k2\_\text{pk}} = \frac{(2n + 1)}{(n + 1)} I_m. \tag{68}$$

The rms currents of the primary windings are given by

$$I_{k1\_\text{rms}} = I_{k2\_\text{rms}} = \frac{n + 2}{1 - D} I_o \times \sqrt{\frac{2 (6n^3 + 14n^2 + 15n + 6) (1 - D)}{3 (n + 2) (n + 1)^2} + 2D - 1}. \tag{69}$$

The rms currents of the secondary windings are given by

$$I_{\text{sec\_rms}} = I_o \sqrt{\frac{2 (n + 2) (3n + 2)}{3 (n + 1)^2 (1 - D)}}. \tag{70}$$

B. Semiconductor Selection

The switches and diodes are chosen based on the voltage and current stresses. The voltage stresses of the switches and diodes can be calculated from (36) and (37). The rms current stresses

TABLE II
KEY PARAMETERS OF THE PROTOTYPE

Parameters	Value/Description
Input voltage	20 V
Output voltage	400 V
Output power	320 W
Switching frequency	50 kHz
Switches S_1-S_2	IPA075N15N3 (150 V)
Diodes D_1, D_2	STPS20200CT (200 V)
Diodes D_3, D_4	TST20H300CW (300 V)
Coupled inductors	Turns ratio = 1:1 Magnetizing inductance = 100 uH Leakage inductance = 3.5 uH
Capacitor C_1	22 uF Film capacitor
Capacitor C_2, C_3	8.2 uF Film capacitor
Capacitor C_o	2×56 uF electrolytic capacitor

of the switches are given by

$$I_{S1\_\mathrm{rms}} = \frac{n+2}{1-D} I_o \times \sqrt{2D - 1 - \frac{(1-D)\left(4n^3+12n^2+13n+4.67\right)}{(n+2)(n+1)^2}} \tag{71}$$

$$I_{S2\_\mathrm{rms}} = \frac{n+2}{1-D} I_o \sqrt{3-2D}. \tag{72}$$

The average currents flowing through the diodes are given by

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_o. \tag{73}$$

C. Capacitor Design

The capacitors are used to transfer energy from the input to the output. They are designed based on the voltage ripple $r\%$ and the output power P_o. The calculations of the capacitors are as follows:

$$C_1 = \frac{(2n+4)P_o}{r\% {V_o}^2 f_s} \tag{74}$$

$$C_2 = \frac{(n+2)P_o}{r\% {V_o}^2 f_s} \tag{75}$$

$$C_3 = \frac{2P_o}{r\% {V_o}^2 f_s}. \tag{76}$$

Generally, capacitors with a low equivalent series resistance (ESR) are preferred in order to reduce power losses. It is a favorable solution that film capacitors or multilayer chip-type ceramic capacitors are adopted. Moreover, multiple capacitors can be connected in parallel to reduce the ESR.

VI. EXPERIMENTAL RESULTS

A prototype with 20-V input and 400-V output was built in order to verify the performance of the proposed converter. The key parameters of the prototype are given in Table II. A picture of the prototype is shown in Fig. 14.

Fig. 15 shows the interleaved driving signals and the drain-to-source voltages of the switches. The duty cycles of the switches are around 0.7. The voltage stresses of the switches are clamped at around 68 V, which is much lower than the output voltage.

Fig. 16 shows that the input voltage is 20 V and the output voltage is 400 V. Therefore, a high voltage gain is achieved, even when the turns ratio is 1.

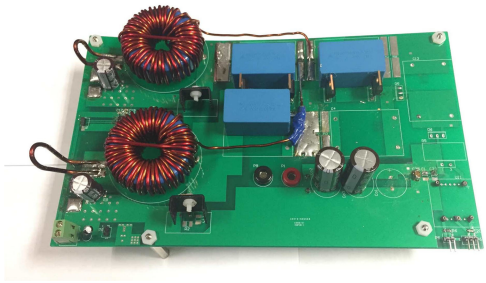

Fig. 14. Picture of the prototype.

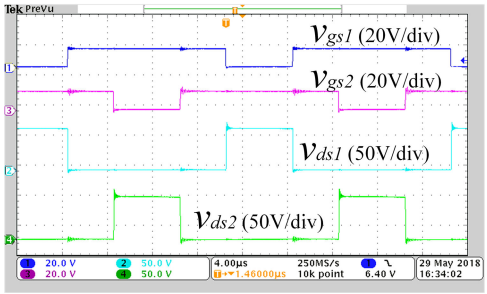

Fig. 15. Driving signals and drain-to-source voltages of the switches.

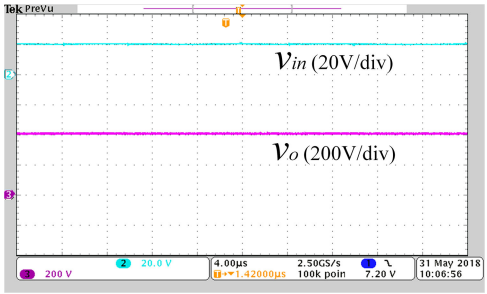

Fig. 16. Input and output voltages.

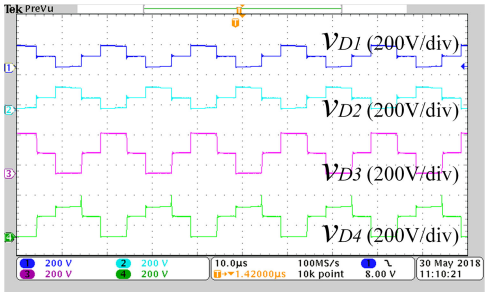

Fig. 17. Voltages across the diodes.

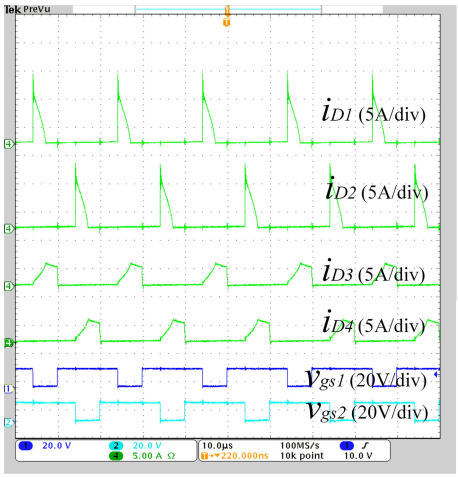

Fig. 18. Currents through the diodes.

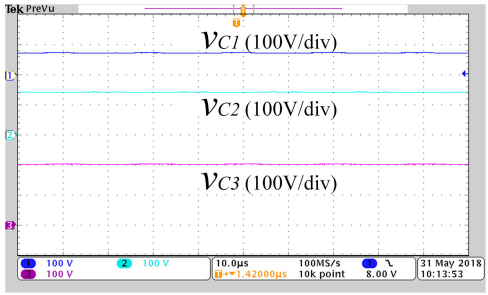

Fig. 19. Voltages across the capacitors.

Fig. 17 shows the voltages of the diodes. As can be seen, the blocking voltages of D_1 and D_2 are around 136 V and the blocking voltages of D_3 and D_4 are around 268 V, which match the calculations from (41). Fig. 18 shows the currents through the diodes. It can be seen that the reverse recovery problems of the diodes are alleviated due to the existence of the leakage inductances.

Fig. 19 shows the voltages across the capacitors. It can be seen that V_{C1}, V_{C2}, and V_{C3} are around 68, 136, and 200 V, respectively, which are consistent with the calculations from (37).

Fig. 20 shows the primary currents of the coupled inductors and the input current. It can be seen that balanced primary current sharing is achieved. The frequency of the input current ripple is twice the switching frequency, and the input current ripple is significantly reduced due to the interleaved operation.

Fig. 21(a) shows the voltage and current of S_1 at the turn-ON transition. Fig. 21(b) shows the voltage and current of S_2 at the turn-ON transition. As can be seen, both switches are turned-ON under the ZCS.

Fig. 22(a) shows the transient response due to load increase from 50% to 100%, and Fig. 22(b) shows the transient response due to load decrease from 100% to 50%.

The measured efficiency of the prototype is shown in Fig. 23. The peak efficiency is 94.9%. At full load, the efficiency is

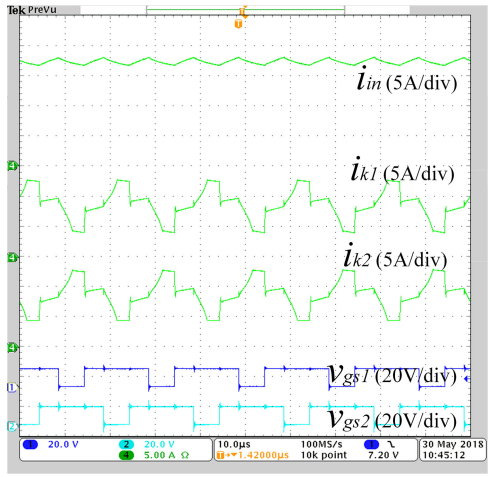

Fig. 20. Primary currents of the coupled inductors and the input current.

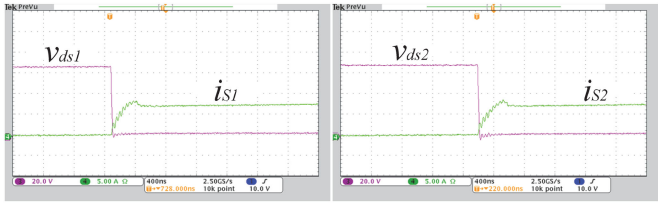

Fig. 21. ZCS turn-ON of the switches. (a) Voltage and current of S_1. (b) Voltage and current of S_2.

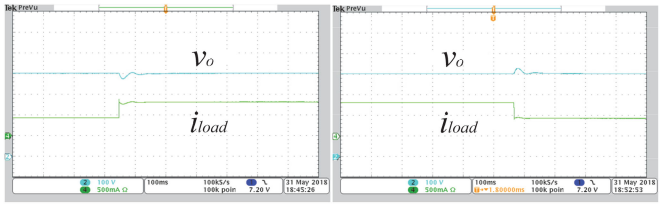

Fig. 22. Transient response. (a) Load increase. (b) Load decrease.

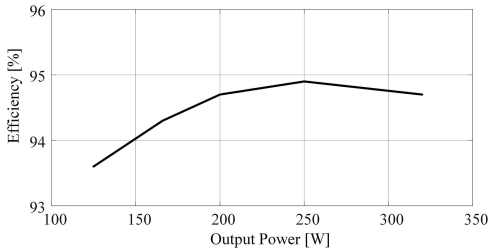

Fig. 23. Measured efficiency versus output power.

94.7%. The loss breakdown based on the prototype at full load is shown in Fig. 24. It can be seen that the dominant power losses are the coupled-inductor loss, the diode loss, and the switch loss. More coppers can be used in the coupled inductor to further improve the efficiency of the proposed converter.

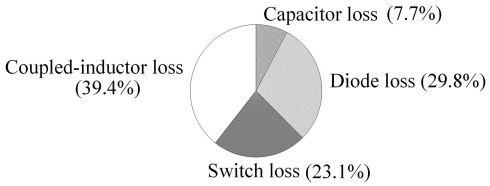

Fig. 24. Loss breakdown.

VII. Conclusion

An interleaved high step-up converter integrating coupled-inductor and SC techniques has been proposed in this paper. It is shown that a very high step-up voltage gain is achieved without an extreme duty cycle or a high turns ratio. Also, due to the low switch voltage stress, low-voltage-rating MOSFETs with a small ON-resistance are allowed to reduce the conduction loss. Furthermore, a low-ripple continuous input current is achieved, thanks to the interleaved operation at the input side. Moreover, the ZCS turn-ON of the switches is achieved, and the reverse recovery problem of the diodes is alleviated. In addition, the leakage energy is recycled. The operation principles and characteristics of the basic topology were analyzed in detail. A 20-V input and 400-V output prototype was built. Experimental results have verified the theoretical analysis.

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Yifei Zheng (S'16) received the B.S. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2009, and the M.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2012. He is currently working toward the Ph.D. degree in power electronics at the University of California, Irvine, Irvine, CA, USA.

From 2012 to 2015, he was an Electrical Engineer with Xi'an XJ Power Electronic Technology Corporation, Xi'an, China, involved with the development of high-power grid-connected inverters for photovoltaic and metro applications. His research interests include high step-up converters, high step-down converters, bidirectional converters, and their applications.

Keyue Ma Smedley (S'87–M'90–SM'97–F'08) received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 1982 and 1985, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 1987 and 1991, respectively.

She is currently a Professor with the Department of Electrical Engineering and Computer Science, University of California, Irvine, Irvine, CA, the Director of the UCI Power Electronics Laboratory, and a cofounder of One-Cycle Control Inc. Her technology has been integrated into commercial products spanning from audio amplifiers to V/var control, power grid dynamic voltage control, power quality control, renewable generation, energy storage systems, mobile power, microgrids, etc. Her soft switching and regenerative clamping circuits are widely used in industry. Her work has resulted in more than 180 technical publications, more than ten US/international patents, two start-up companies, and numerous commercial applications. Her research interests include high-efficiency dc–dc converters, high-fidelity class-D power amplifiers, four-quadrant three-phase and single-phase converters (covering PFC rectifiers, active power filters, inverters, var generation), switching capacitor converters, utility-scale fault current limiters, power grid modeling for high penetration renewables, solar power integration, power quality control, etc.

Dr. Smedley was the recipient of the UCI Innovation Award 2005. Her work with One-Cycle Control Inc., won the Department of the Army Achievement Award at the Pentagon in 2010.