High-Efficiency and High-Density Single-Phase Dual-Mode Cascaded Buck–Boost Multilevel Transformerless PV Inverter With GaN AC Switches

Qingyun Huang, *Member, IEEE*, Alex Q. Huang, *Fellow, IEEE*, Ruiyang Yu, Pengkun Liu, *Student Member, IEEE*, and Wensong Yu, *Member, IEEE*

***Abstract*—This paper introduces a high-efficiency and high-density single-phase dual-mode cascaded buck–boost multilevel transformerless photovoltaic (PV) inverter for residential application. This inverter topology combines a *regulated* cascaded H-bridge multilevel inverter stage with an *unregulated* GaN-based ac boost converter. The cascaded H-bridge inverter and the ac boost share a common inductor. Compared with the traditional cascaded H-bridge PV inverter, this topology significantly enlarges the input voltage range due to the additional ac boost. And, a flexible number of PV panels can be used. To control the multiple dc-link PV voltages and to reduce the switching loss of the ac boost, this paper further introduces a dual-mode operation. The two modes are buck mode and buck–boost mode. To maximize the utilizations of the dc-link voltages, this paper presents a minimized ac boost duty-cycle generation strategy with feedforward. Then, a dual-mode modulation based on the boost feedforward duty-cycle generation is introduced. This paper also uses an indirect current control for this inverter, since the ac boost is an unregulated stage. The ac boost stage is implemented with two interleaved phases and the ac switches based on the 650-V E-mode GaN FETs. Finally, an 8-port 2-kW prototype based on this topology is developed and demonstrated. Compared with the state-of-the-art microinverter-based 2-kW PV inverter system, the developed inverter prototype achieves 40% reduction of the total power loss, 25% improvement of the power density, 37.5% reduction of the power connectors, 50% reduction of the device count, and 87.5% reduction of the main magnetic count. Operating with natural convection cooling, this PV inverter achieves 98.0% efficiency at 60% of load and 97.8% efficiency at full load. The power density of the packaged PV inverter is 5.8 W/in^3.**

***Index Terms*—AC boost, buck–boost, cascaded H-bridge, dual mode, GaN, high density, high efficiency, photovoltaic (PV) system, sinusoidal pulsewidth modulation (SPWM), transformerless inverter.**

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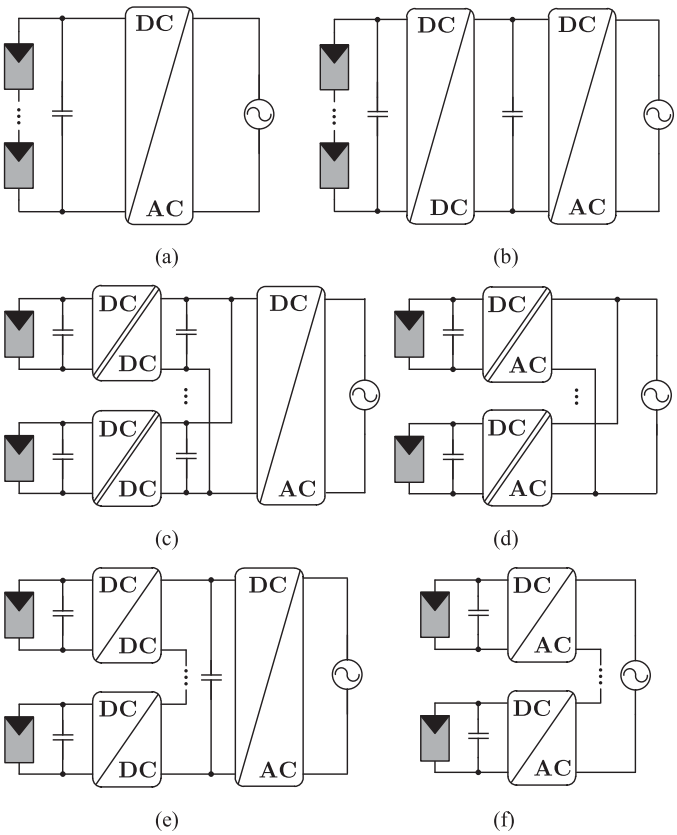

Fig. 1. Conventional single-phase PV inverter systems for residential application. (a) Single-stage transformerless string inverter. (b) Two-stage transformerless string inverter (a central non-isolated dc/dc converter connected to a central non-isolated dc/ac inverter). (c) Parallel-connected isolated dc/dc converters connected to a central non-isolated dc/ac inverter. (d) Parallel-connected isolated dc/ac inverters (microinverters). (e) Series-connected non-isolated dc/dc converters connected to a central non-isolated dc/ac inverter. (f) Series-connected non-isolated dc/ac inverters.

A parallel-type panel-based solution is reported in [32]–[36]. The circuit structure uses parallel isolated dc/dc converters followed by a non-isolated central dc/ac inverter, as shown in Fig. 1(c). To achieve high efficiency, a regulated boost converter cascaded with an unregulated resonant converter can be utilized for the isolated dc/dc converter, as shown in Fig. 2(a) [36]. Another parallel-type structure, as shown in Fig. 1(d), contains the parallel isolated dc/ac microinverters, which have proven success in the marketplace [3], [11], [31], [37]–[39]. A popular high-efficiency microinverter topology is the interleaved flyback with an unfolding bridge, as shown in Fig. 2(b) [38], [39]. The above two parallel-type solutions can realize the individual MPPT hence enhancing the energy harvesting capability under the partial shading conditions. Moreover, they provide the highest flexibility in terms of the number of PV panels. However, for the parallel-type solutions, each PV panel requires a high step-up isolated converter. Thus, the two parallel-type solutions, which require more high-voltage devices and more magnetic components, not only significantly increase the system cost, but also limit the system efficiency, compared with the transformerless string inverters. In addition, the parallel dc/dc solutions still have the high voltage dc arc fault issues.

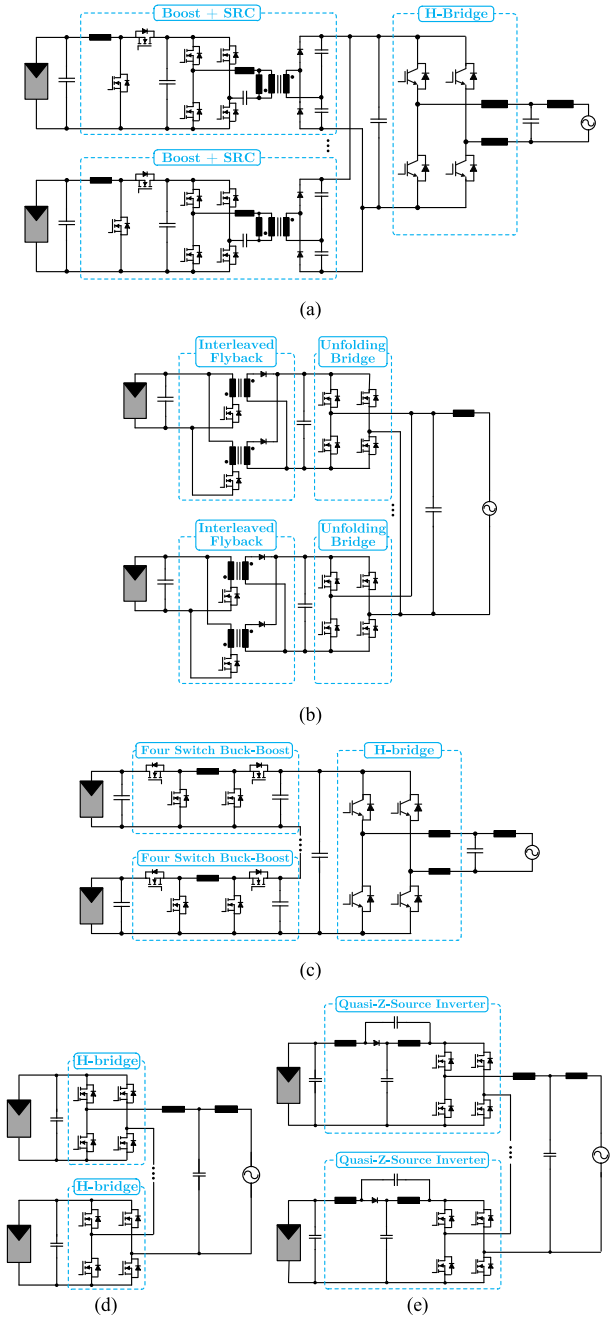

Fig. 2. Conventional panel-based single-phase PV inverter topologies. (a) Parallel boost converter followed by an unregulated resonant converter connected to a bipolar-modulated H-bridge inverter. (b) Parallel interleaved flyback followed by an unfolding bridge. (c) Series four-switch buck–boost converter connected to a bipolar-modulated H-bridge inverter. (d) Cascaded H-bridge inverter. (e) Cascaded quasi-Z-source H-bridge inverter.

The series-type panel-based solutions provide another way to boost the PV voltage to match the grid voltage. In a series-type structure, as shown in Fig. 1(e), each PV panel is connected to a non-isolated dc/dc converter, and these dc/dc converters are connected in a series. These dc/dc converters are also called the power optimizers [40]–[43]. Then, the series-connected dc/dc converters are connected to a non-isolated central dc/ac inverter. A typical topology for this series-type solution is shown in

Fig. 2(c). In this topology, the dc/dc converter is a four-switch buck–boost converter, which realizes the wide input and output voltage range and the high efficiency [40], [43]. This series-type solution can also realize the individual MPPT for each PV panel. Compared with the parallel-type solutions, the efficiency is improved, and the cost is reduced. However, due to the series connection of the dc/dc converters, there still exists a high-voltage dc link. Thus, the high voltage dc arc fault is still a major concern. Another series-type structure is shown in Fig. 1(f). In this structure, each PV panel is connected to a non-isolated dc/ac inverter; and these inverters are connected in series and then connected to the grid [46]–[48]. The cascaded H-bridge multilevel inverter is a well-known topology for this structure, as shown in Fig. 2(d) [46]–[48]. This topology not only realizes the individual MPPT, but also eliminates the high voltage dc arc faults due to the series connection of dc/ac inverters. Compared with the parallel-type solutions and the other series-type solutions, this topology achieves lower cost since there are no high-voltage devices and the H-bridges share a single output filter. This topology also achieves high efficiency due to the single-stage transformerless topology and the use of high-performance low-voltage Si power devices. Moreover, since the interleaving techniques significantly increase the equivalent frequency of the inductor, the switching frequency of each H-bridge can be dramatically reduced, and the efficiency is further improved. Thus, the cascaded H-bridge multilevel PV inverter is a great candidate for single-phase PV inverter residential application. However, since this topology is a step-down topology, there is a severe limitation on the minimum number of PV panels. It limits the flexibility for residential roof PV application. To address this drawback, a cascaded quasi-*Z*-source H-bridge inverter, as shown in Fig. 2(e), is reported [49]–[51]. The quasi-*Z*-source H-bridge inverter provides the voltage-boosting capability. The flexibility is improved. However, the power loss on the additional diodes and inductors reduces the system efficiency. Besides, the additional two main inductors for each PV panel significantly increase the size and the cost compared with the cascaded H-bridge inverter.

An active buck–boost single-phase centralized PV inverter topology, which is the H-bridge inverter followed by an ac boost converter, is discussed in [66] and [67]. The active buck–boost inverter topology discusses a promising topology concept, which is a dc/ac inverter followed by an ac/ac converter. The active buck–boost inverter topology [66], [67] adds the ac boost to the H-bridge to achieve the additional boost function, which enlarges the dc input voltage range. The flexibility of the PV panel numbers in the PV strings is also significantly increased. However, this active buck–boost PV inverter is still a centralized PV string inverter that cannot realize individual MPPT.

Based on the active buck–boost inverter topology and the cascaded H-bridge inverter topology, a panel-based single-phase PV inverter topology structure is introduced in this paper to address the shortcomings of the conventional single-phase PV inverters for residential applications. In this inverter structure, as shown in Fig. 3, each PV panel is connected to a non-isolated dc/ac inverter, and these inverters, which are connected in a series, are followed by a centralized non-isolated ac/ac converter.

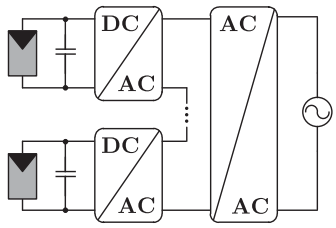

Fig. 3. Introduced inverter system: series-connected dc/ac inverters connected to a central ac/ac converter.

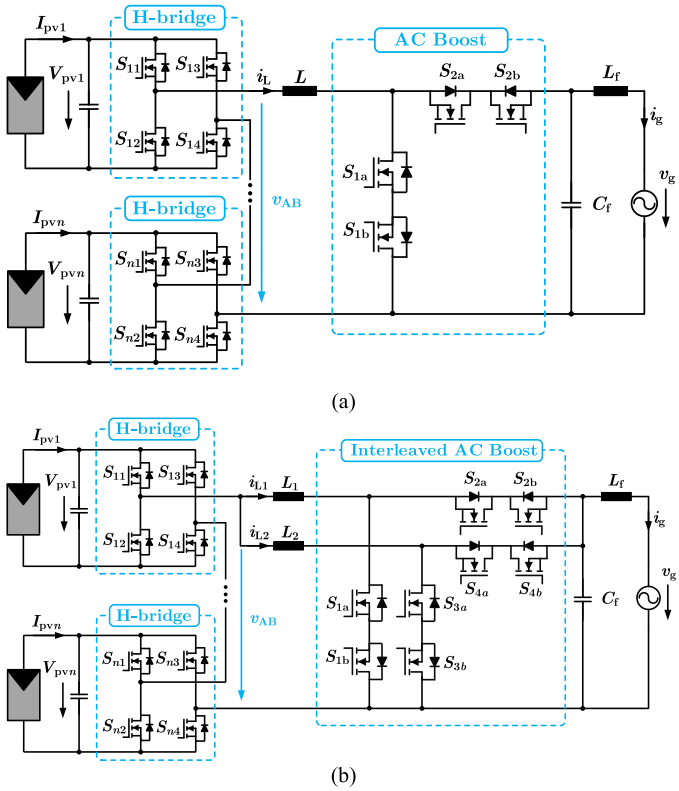

Fig. 4. Dual-mode cascaded multilevel buck–boost PV inverter topology. (a) Cascaded H-bridge inverter connected to a central ac/ac boost converter. (b) Cascaded H-bridge inverters connected to a central dual-phase interleaved ac/ac boost converter.

Based on this structure, the single-phase cascaded buck–boost multilevel transformerless PV inverter topology is presented in this paper. As shown in Fig. 4(a), the topology is a *regulated* cascaded H-bridge multilevel inverter followed by a *centralized unregulated* ac boost converter, which provides the voltage-boosting capability. Compared with the conventional cascaded H-bridge multilevel inverter, this PV inverter not only conserves all the advantages of the conventional cascaded H-bridge multilevel inverter, but also significantly increases the flexibility of the number of the PV panels due to the additional ac boost. In addition, compared with the cascaded quasi-*Z*-source H-bridge inverter, this inverter dramatically reduces the number and total size of the main inductors, since the cascaded H-bridge inverter and the ac boost converter share one common inductor. Compared with the active buck–boost inverter [66], [67], this PV inverter can realize individual MPPT due to the panel-based

structure. This single-phase transformerless PV inverter achieves all the following major benefits: the panel-based structure, the elimination of the high voltage dc arc fault, the high efficiency, the high power density, the low cost, and the high flexibility of the number of PV panels.

Traditionally, the active buck–boost inverter has two operation modes: buck mode and boost mode [66], [67]. However, the traditional dual-mode operation cannot be applied to the presented cascaded buck–boost multilevel inverter since the cascaded H-bridge must always switch to regulate the multiple dc-link voltages. Therefore, for the presented cascaded buck–boost multilevel inverter, this paper introduces a different dual-mode operation. The two operation modes are buck mode and buck–boost mode. In buck mode, the ac boost is bypassed, whereas the cascaded H-bridge switches and controls all the dc-link PV voltages. In buck–boost mode, the ac boost switches with feedforward duty cycles and without regulation, whereas the cascaded H-bridge still switches and controls all the dc-link PV voltages. Since the ac boost does not switch in buck mode, the switching loss of the ac boost is significantly reduced. Moreover, to maximize the utilizations of the dc-link voltages, this paper presents the minimized ac boost duty-cycle generation with feedforward. Based on the minimized ac boost feedforward duty cycle, this paper presents a dual-mode sinusoidal pulsewidth modulation (SPWM) to avoid the saturations of the H-bridge duty cycles, to achieve smooth mode transition, and to improve the system efficiency. In the traditional dual-mode modulation for the active buck–boost inverter [66], [67], the duty cycle of the H-bridge is saturated to 1 when the ac boost switches, and the ac boost duty cycle is generated by feedback controller. However, in our dual-mode SPWM, all the H-bridge duty cycles will not be saturated to 1, and the ac boost duty cycle is generated by feedforward. This paper also presents a system control strategy based on an indirect current control for the inverter since the ac boost is an unregulated stage.

The ac boost converter efficiency is improved by using GaN-based ac switches. Furthermore, two interleaved phases in the ac boost are introduced to significantly reduce the total inductor current ripple. A 2-kW 8-port PV inverter prototype, based on the presented topology, modulation, and control strategy, was developed and tested in this paper. Compared with the commercial 2-kW microinverter system [31], the developed 2-kW PV inverter prototype achieves 40% reduction of the total power loss, 25% improvement of the power density, 37.5% reduction of the power connectors, 50% reduction of the device count, and 87.5% reduction of the main magnetic count. Under natural convection cooling conditions, the developed PV inverter achieves 98.0% efficiency at 60% of full load and 97.8% efficiency at full load. Additionally, the power density of this PV inverter is 5.8 W/in^3 with the case, under natural convection cooling conditions.

This paper is organized as follows. The presented PV inverter topology and the implementation of the ac boost are described in Section II. The operation modes and equivalent circuits are described in Section III. The dual-mode SPWM and the implementations are presented in Section IV. The control strategy for this inverter is introduced in Section V. The hardware design of the 2-kW PV inverter prototype and the experimental verifications are presented in Section VI. Finally, Section VII concludes the paper.

II. Topology of Cascaded Buck–Boost Multilevel PV Inverter

The presented PV inverter topology is a regulated cascaded H-bridge multilevel inverter followed by a centralized unregulated ac boost converter, as shown in Fig. 4(a). In this topology, each PV panel is connected to an H-bridge inverter, and each dc-link voltage is regulated by the corresponding H-bridge. The centralized unregulated ac boost converter provides the voltage-boosting function for the inverter. This PV inverter topology significantly enlarges the input voltage range due to the additional ac boost. This topology is not a simple combination of the cascaded H-bridge and the ac boost. It is not easy to make this topology work appropriately when combing the two topologies. Since the cascaded H-bridge should be responsible for the control of all the individual PV panel voltages, the cascaded H-bridge must always be a regulated stage. This paper proposes to make the ac boost work as an unregulated stage, which can be regarded as a "transformer." Making the ac boost work without regulation significantly simplifies the control structure when combining the two stages.

With the interleaving modulation for the cascaded H-bridge, the output voltage $v_{\rm AB}$ of the cascaded H-bridge is still a multilevel waveform, and the inductor current ripple frequency is still much higher than the switching frequency of each H-bridge. Depending on the grid voltage $v_{\rm g}$ and the averaged output voltage $V_{\rm AB}$ of the cascaded H-bridge, there are two operation modes for this inverter: buck mode and buck–boost mode. To avoid the saturations of the H-bridge duty cycles, to achieve the smooth transition between the two modes, and to reduce the switching loss of the ac boost, a dual-mode SPWM is introduced. In buck mode, ac boost duty cycle is zero, and the ac boost is bypassed. Thus, in buck mode, there are no switching losses on the devices of the ac boost, and this inverter works just like the conventional cascaded H-bridge inverter. In buck–boost mode, both the cascaded H-bridge inverter and the ac boost switch at high frequency, and the ac boost operates with a non-zero feedforward duty cycle. In buck–boost mode, the unregulated ac boost works like a step-up transformer. The details of the dual-mode operation principles and the modulations will be explained in the following sections.

For the implementation of the ac boost converter, it requires 650-V ac switches. The 650-V Si super-junction MOSFETs cannot be utilized due to the severe reverse recoveries of their body diodes. The 650-V Si insulated-gate bipolar transistors (IGBTs) with fast anti-parallel diodes are also not suitable for achieving high frequency and high efficiency due to the high switching losses and high conduction losses. In this paper, the emerging 650-V GaN FETs, which achieve low switching losses and eliminate the reverse recovery issues [52]–[57], are utilized for the ac boost. The GaN-ac-switch-based ac boost converter delivers superior performance, including the low switching loss and low conduction loss. To further reduce the

conduction loss, more devices can be parallel. Alternatively, the dual-phase interleaving technique is utilized for the ac boost in this paper. The introduced PV inverter topology with dual-phase interleaved GaN ac boost is shown in Fig. 4(b). With the dual-phase interleaved GaN ac boost, both the conduction loss of the ac boost and the total current ripple of the inductor are reduced.

The ground leakage currents of this transformerless PV inverter are the same as those of the conventional cascaded H-bridge multilevel PV inverters since the grid neutral point of this inverter is also connected to the last H-bridge, as shown in Fig. 4. The additional ac boost does not change the analytical model for the ground leakage currents, compared with the conventional cascaded H-bridge PV inverters. The ground leakage current issues for the conventional cascaded H-bridge PV inverters have been studied and solved in [59]. In [59], it is pointed out that the leakage currents of the cascaded H-bridge PV inverters are determined by both the common mode outputs of the H-bridges and the differential mode outputs of the H-bridges. Thus, using the bipolar modulation for the H-bridge inverter or replacing the H-bridge inverters by the H5 inverters, the H6 inverters, the HERIC inverters, etc., cannot eliminate the ground leakage currents of the cascaded H-bridge inverters, although they are validated ways to eliminate the leakage currents of the single H-bridge PV inverters. However, in the introduced PV inverter and the conventional cascaded H-bridge inverter, each dc-link voltage is very low (about 30 V). With the interleaving modulations for the cascaded H-bridge, the multilevel voltage waveforms can be achieved. The high-frequency pulsating voltage of the introduced PV inverter and the conventional cascaded H-bridge inverter is only 30 V, which is less than one-tenth of the high-frequency pulsating voltage of the single H-bridge PV inverter with the 400-V dc link. Thus, the leakage currents of the introduced PV inverter and the conventional cascaded H-bridge inverter are significantly reduced compared with the single H-bridge PV inverters with the 400-V dc link. In [59], two high-frequency-filter-based suppression solutions have been reported and validated for solving the leakage current issues of the cascaded H-bridge PV inverters. The introduced PV inverter can also use the two high-frequency-filter-based suppression solutions described in [59]. Since the filter design is not what this paper focuses on, the detailed analysis and the filter design will not be discussed in this paper.

III. Operation Modes and Equivalent Circuits

The conventional dual-mode buck–boost inverters, such as the active buck–boost inverter [66], [67], are centralized inverters with single dc input source. Since the single dc voltage can be regulated by either the buck stage or the boost stage, these centralized dual-mode inverters can work in buck mode or boost mode. In buck mode, the boost is bypassed, and the buck controls the dc voltage. In boost mode, the buck is bypassed, and the boost controls the dc voltage. However, the presented cascaded buck–boost multilevel inverter has multiple independent dc input sources, and the ac boost is a centralized stage and shared by multiple H-bridges. Thus, the dc-link PV voltages must always be controlled by the cascaded H-bridge. In other words, to maintain the controllability for all the dc-link PV voltages, the cascaded H-bridge cannot be bypassed, and hence there is no boost mode for this inverter. This inverter can work in buck mode or buck–boost mode. In buck mode, the ac boost is bypassed, whereas the cascaded H-bridge switches and controls all the dc-link PV voltages. In buck–boost mode, the ac boost switches with feedforward duty cycles and without regulation, whereas the cascaded H-bridge still switches and controls all the dc-link PV voltages. This dual-mode operation can realize the control of the multiple dc-link PV voltages and reduce the switching loss of the ac boost.

The operation principles, analysis, and equivalent circuits are discussed in this section. To simplify the analysis, the inverter with a single ac boost [see Fig. 4(a)] is discussed in this section.

To achieve high utilization of the main inductor, unipolar SPWM is utilized for the cascaded H-bridge. Moreover, to minimize the switching loss of the cascaded H-bridge, only one half-bridge (S_{j1} and S_{j2}, $j = 1, \ldots, n$) of each H-bridge works with high frequency. The other half-bridge (S_{j3} and S_{j4}, $j = 1, \ldots, n$) of each H-bridge works with line frequency. For each H-bridge, the individual H-bridge modulation signal $v_{\mathrm{m}j}$ ($j = 1, \ldots, n$) is from –1 to 1 [46]–[48]. The averaged output voltage V_{AB} of the cascaded H-bridge is calculated as

$$V_{\mathrm{AB}} = \sum_{j=1}^{n} V_{\mathrm{pv}j} v_{\mathrm{m}j} \tag{1}$$

where $V_{\mathrm{pv}j}$ ($j = 1, \ldots, n$) is the output voltage of the jth PV panel. Based on the unipolar SPWM, the individual H-bridge duty cycle d_j is derived as

$$d_j = \begin{cases} v_{\mathrm{m}j} & v_g \geq 0 \\ v_{\mathrm{m}j} + 1 & v_g < 0 \end{cases} \quad j = 1, 2, \ldots, n \tag{2}$$

where d_j ($j = 1, \ldots, n$) is from 0 to 1, and v_{g} is the grid voltage.

A. Buck Mode

In buck mode, the cascaded H-bridge stage switches at high frequency. The ac boost converter is bypassed by keeping the high-side switches S_{2a} and S_{2b} ON, whereas the low-side switches, S_{1a} and S_{1b}, are always OFF. There is no switching loss on the ac boost. In buck mode, the following equation can be obtained:

$$\frac{v_g}{V_{\mathrm{AB}}} = 1. \tag{3}$$

The equivalent circuit of this inverter in buck mode is shown in Fig. 5(a). Since the ac boost is bypassed, the ac boost is equivalent to a transformer with a turns ratio of 1:1.

B. Buck–Boost Mode

In buck–boost mode, both the cascaded H-bridge and the ac boost operate at high switching frequencies. In this mode, the following equation can be obtained:

$$\frac{v_g}{V_{\mathrm{AB}}} = \frac{1}{1 - d_{\mathrm{Boost}}} \tag{4}$$

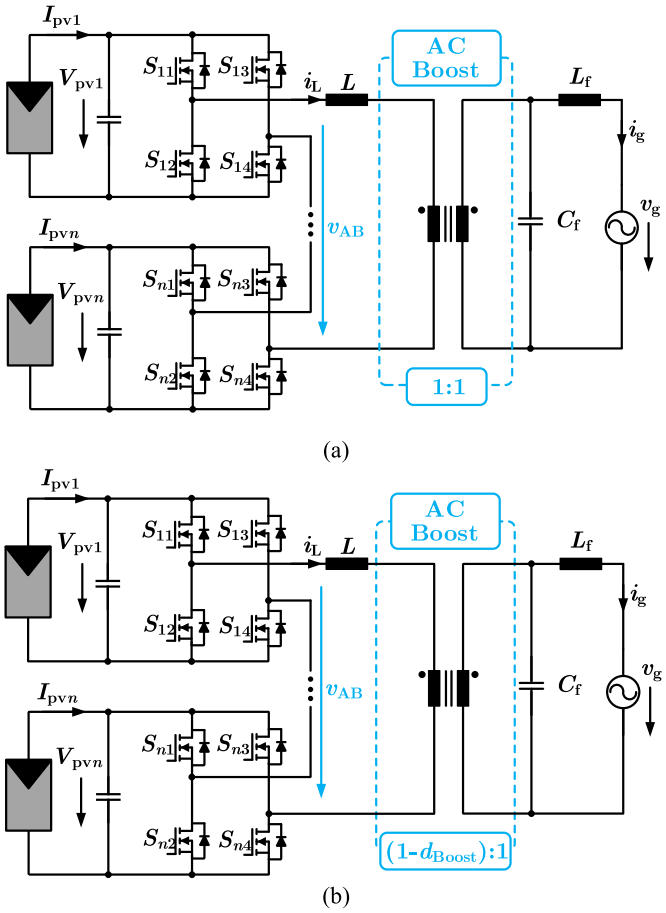

Fig. 5. Equivalent circuits. (a) Buck mode. (b) Buck–boost mode.

where d_{Boost} is the duty cycle of the ac boost. The ac boost duty cycle d_{Boost}, generated by a feedforward method, will be discussed in the next section. The equivalent circuit of this inverter in buck–boost mode is shown in Fig. 5(b). Since the ac boost switches at high frequency, the ac boost is equivalent to a step-up transformer with a turns ratio of $(1 - d_{\mathrm{Boost}})$:1.

IV. Dual-Mode SPWM With Minimized Boost Feedforward Duty Cycle

In [66] and [67], a dual-mode SPWM is discussed for the traditional active buck–boost inverter. In the traditional dual-mode modulation, the duty cycle of the H-bridge will be saturated to 1 during the boost mode. And, the transition point from the buck mode to the boost mode is the point when the buck duty cycle reaches 1. And the duty cycles for both the buck stage and the boost stage are determined by the feedback controller. However, for the presented dual-mode cascaded buck–boost multilevel inverter, there is no boost mode, and all the H-bridge duty cycles cannot be saturated to 1 since the multiple dc-link voltages must be always controlled by the cascaded H-bridge. The traditional dual-mode modulation for the active buck–boost inverter [66], [67] cannot be used for our cascaded buck–boost multilevel inverter. It is a big challenge to decide the optimized duty cycle of the ac boost, as well as to achieve the smooth transition between the buck mode and the buck–boost mode. To address this issue and to maximize the utilizations of the dc-link voltages, a minimized ac boost duty cycle generation with feedforward is introduced in this section. Based on the minimized ac boost feedforward duty cycle, this section describes a dual-mode modulation to avoid the saturations of the H-bridge duty cycles, to achieve smooth mode transition, and to improve the system efficiency. The detailed implementation of the dual-mode SPWM is also included in this section.

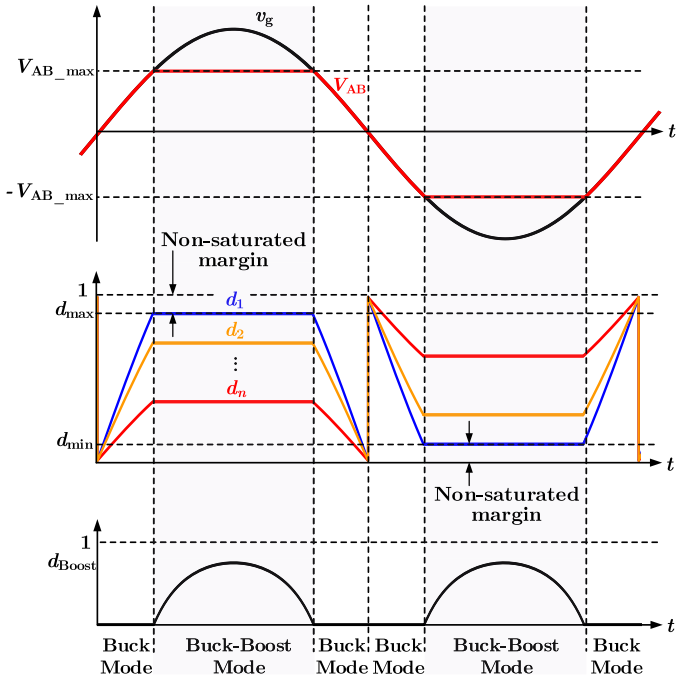

Fig. 6. Simplified operation principles.

A. Operation Principles of Dual-Mode SPWM for Cascaded Buck–Boost Multilevel Inverter

Each PV panel voltage must be controlled by its corresponding H-bridge. If the H-bridge duty cycle d_j ($j = 1, \ldots, n$) reaches 1, this duty cycle is saturated. To maintain the regulation capability of all the H-bridges, all the H-bridge duty cycles cannot reach 1. The larger ac boost duty cycle, which provides higher voltage-boosting gain, reduces the duty cycles of the cascaded H-bridge. Then, the utilizations of the dc-link voltages are reduced, and the total inverter efficiency is reduced too. Therefore, a dual-mode SPWM based on the minimized boost feedforward duty cycle is explained in this section. This modulation with the minimized boost duty cycle can maximize the utilizations of the dc-link voltages, avoid the saturations of the H-bridges' duty cycles, and achieve the smooth mode transition.

To provide a safe margin (e.g., 5%), the H-bridge duty cycles should be limited to $d_{\max}$ (e.g., 0.95) during the positive half-line cycle, and be limited to $d_{\min}$ (e.g., 0.05) during the negative half-line cycle. Thus, none of the H-bridge duty cycles will be saturated. The 5% margin is the non-saturated margin, as shown in Fig. 6.

The operation principles of the dual-mode SPWM are shown in Fig. 6. During the positive half-line cycle, when all the H-bridge duty cycles are lower than $d_{\max}$, the inverter works in buck mode. The duty cycle d_{Boost} of the ac boost is always zero, and the ac boost is bypassed. V_{AB} follows the grid voltage v_{g} during the buck mode. When any H-bridge duty cycle d_j ($j = 1, \ldots, n$) reaches $d_{\max}$, the averaged output voltage V_{AB} of the cascaded H-bridge reaches $V_{\text{AB\_max}}$, and the inverter enters the buck–boost mode. During the buck–boost mode of the positive half-line cycle, $V_{\text{AB\_max}}$ is the maximum averaged output voltage of the cascaded H-bridge, which prevents any H-bridge duty cycle from being higher than $d_{\max}$. Then, the ac boost provides the additional voltage-boosting ratio. During the buck–boost mode of the positive half-line cycle, the unregulated ac boost works with a minimized feedforward duty cycle d_{Boost}, which is calculated as

$$d_{\text{Boost}} = 1 - \frac{V_{\text{AB\_max}}}{v_g} \qquad v_g \geq V_{\text{AB\_max}}. \tag{5}$$

With this ac boost feedforward duty cycle d_{Boost}, during the buck–boost mode of the positive half-line cycle, all the H-bridge duty cycles are controlled to be constant, and V_{AB} is clamped to $V_{\text{AB\_max}}$, as shown in Fig. 6.

During the negative half-line cycle, when all the H-bridge duty cycles are higher than $d_{\min}$, the inverter works in buck mode. The duty cycle d_{Boost} of the ac boost is always zero, and the ac boost is bypassed. V_{AB} follows the grid voltage v_{g} during buck mode. When any H-bridge duty cycle ($j = 1, \ldots, n$) reaches $d_{\min}$, the averaged output voltage V_{AB} of the cascaded H-bridge reaches $-V_{\text{AB\_max}}$, and the inverter enters buck–boost mode. During the buck–boost mode of the negative half-line cycle, $-V_{\text{AB\_max}}$ is the minimum averaged output voltage of the cascaded H-bridge, which prevents any H-bridge duty cycle from being lower than $d_{\min}$. Then, the ac boost provides the additional voltage-boosting ratio. During the buck–boost mode of the negative half-line cycle, the unregulated ac boost works with a minimized feedforward duty cycle d_{Boost}, which is calculated as

$$d_{\text{Boost}} = 1 + \frac{V_{\text{AB\_max}}}{v_g} \qquad v_g \leq -V_{\text{AB\_max}}. \tag{6}$$

With this ac boost feedforward duty cycle d_{Boost}, during the buck–boost mode of the negative half-line cycle, all the H-bridge duty cycles are controlled to be constant, and V_{AB} is clamped to $-V_{\text{AB\_max}}$, as shown in Fig. 6.

B. AC Boost Feedforward Duty-Cycle Generation and Smooth Mode Transition

Based on the minimized ac boost feedforward duty cycles for the positive half-line cycle and the negative half-line cycle, the generation of the minimized ac boost feedforward duty cycle d_{Boost} can be unified and synthesized as

$$d_{\text{Boost}} = \begin{cases} 1 - \dfrac{V_{\text{AB\_max}}}{|v_g|} & |v_g| \geq V_{\text{AB\_max}} \\ 0 & |v_g| < V_{\text{AB\_max}}. \end{cases} \tag{7}$$

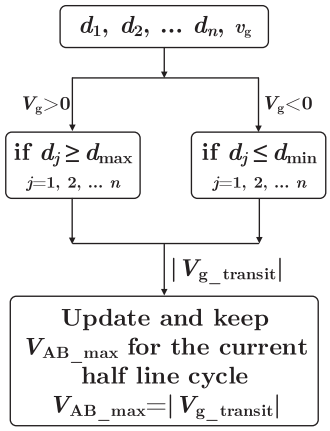

Fig. 7. Algorithm of $V_{\text{AB\_max}}$ generation.

For the traditional dual-mode active buck–boost inverter, the boost duty cycle is determined by the feedback controller since the H-bridge in the traditional active buck–boost inverter is bypassed when ac boost switches [66], [67]. However, in our cascaded buck–boost multilevel inverter, the ac boost duty cycle is calculated by feedforward, as shown in (7), since the cascaded H-bridge must always switch. Since the maximum averaged output voltage $V_{\text{AB\_max}}$ of the cascaded H-bridge varies with the variation of the operation conditions, determining the value of $V_{\text{AB\_max}}$ is another challenge. This paper presents an algorithm to update the value of $V_{\text{AB\_max}}$, as shown in Fig. 7. When any H-bridge duty-cycle d_j ($j = 1, \ldots, n$) reaches $d_{\max}$ during the positive half-line cycle or reaches $d_{\min}$ during the negative half-line cycle, the sensed grid voltage's absolute value $|V_{\text{g}}|$ at that instant is stored as the transition grid voltage $|V_{\text{g\_transit}}|$ for the current half-line cycle. Then, $V_{\text{AB\_max}}$ is updated and equal to the stored transition voltage $|V_{\text{g\_transit}}|$. $V_{\text{AB\_max}}$ is updated only once in each half-line cycle.

The waveform of d_{Boost} is depicted in Fig. 6. When d_{Boost} is zero, this inverter works in the buck mode. When d_{Boost} is between 0 and 1, this inverter works in buck–boost mode. Thus, the operation modes of the inverter are dependent on the ac boost feedforward duty cycle d_{Boost}. The smooth transition between the two modes is naturally realized by the ac boost feedforward duty cycle d_{Boost}.

C. Implementation of Modulation

The following explains the detailed implementation of the introduced dual-mode SPWM. The theoretical waveforms of the duty cycles and the gating signals are shown in Fig. 8. S_{j3} and S_{j4} ($j = 1, 2, \ldots, n$) are switched with line frequency. All S_{j1} ($j = 1, 2, \ldots, n$) are switched with high-frequency and interleaved gating signals. S_{j2} ($j = 1, 2, \ldots, n$) is the complementary gating signal to S_{j1} ($j = 1, 2, \ldots, n$). For the ac boost, during the positive half-line cycle, S_{1a} and S_{2a} are switched with complementary high-frequency gating signals; S_{1b} and S_{2b} are always ON. During the negative half-line cycle, S_{1b} and S_{2b} are switched with complementary high-frequency gating signals; S_{1a} and S_{2a} are always ON.

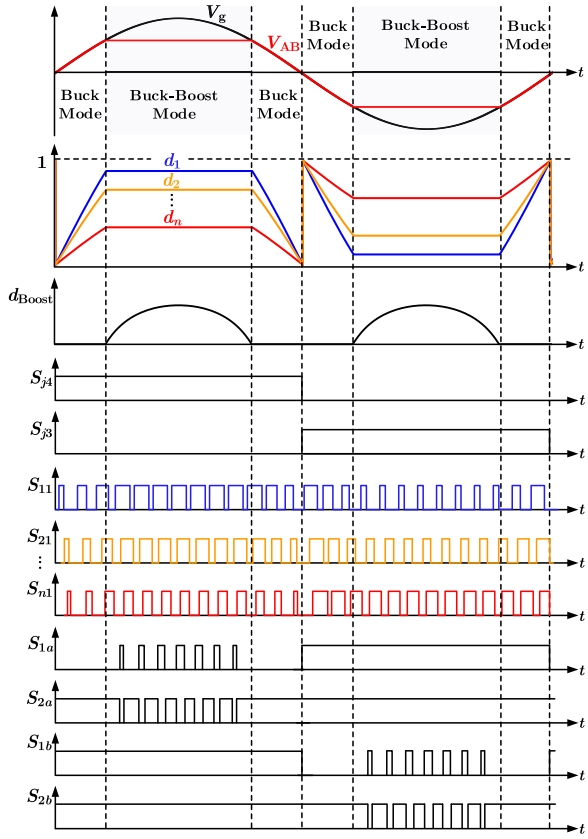

Fig. 8. Theoretical waveforms.

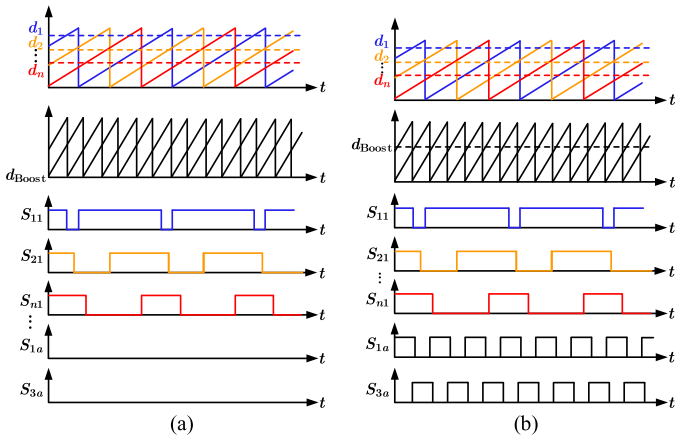

Fig. 9. Relationships of the duty cycles, carriers, and gating signals for the two modes in positive half-line cycle. (a) Buck mode. (b) Buck–boost mode.

The detailed relationships of the duty cycles, carriers, and gating signals for the two operation modes are shown in Fig. 9. For the cascaded H-bridges, n phase-shifted carriers are used to generate the interleaved gating signals. For the ac boost, two phase-shifted carriers are used to generate the interleaved gating signals. The frequency f_{Boost} of the ac boost carriers is much higher than the frequency f_{HB} of the H-bridge carriers to match the equivalent ripple frequency of the middle inductor.

The simplified implementation diagrams of the presented modulation schemes are shown in Fig. 10. A commonly used

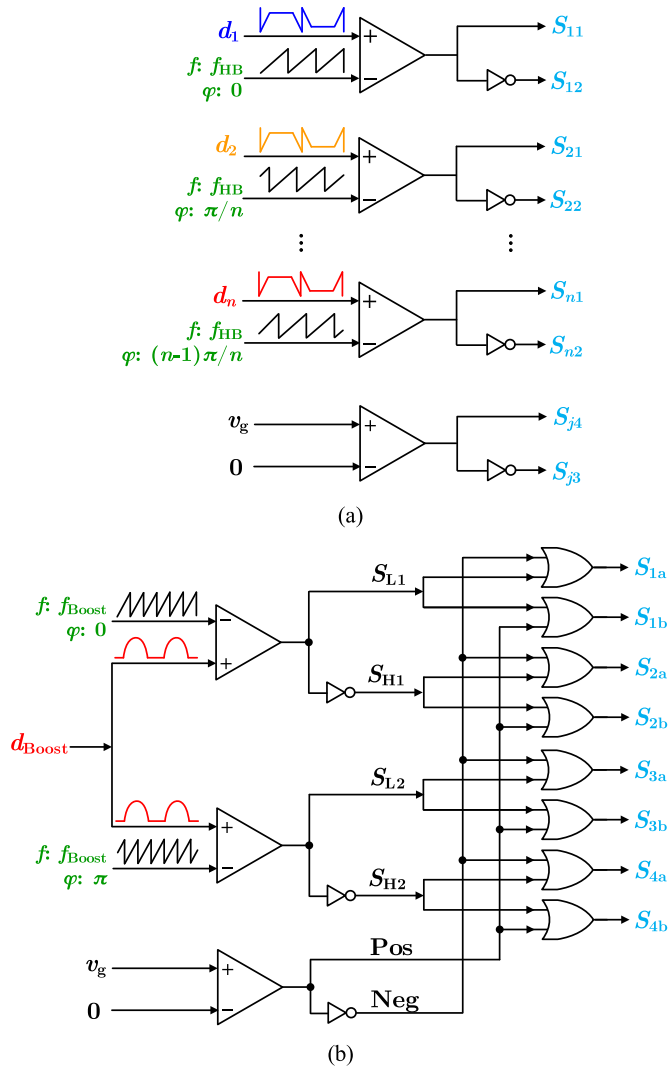

Fig. 10. Modulation scheme for the inverter. (a) Modulation for the cascaded H-bridge. (b) Modulation for the interleaved ac boost.

phase-shifted pulsewidth modulation (PWM) is used for the cascade H-bridge as shown in Fig. 10(a). The phase-shifted PWM combined with the grid voltage polarity signals generates the gating signals for the ac boost as shown in Fig. 10(b). The smooth mode transition is achieved by the presented ac boost feedforward duty cycle d_{Boost} and the presented modulation.

V. Control Strategy

The system control structure for this inverter is illustrated in Fig. 11. In this inverter, the cascaded H-bridge is the regulated stage. There are n individual voltage controllers to regulate the n PV voltages, respectively. The MPPT control of this PV inverter should be the same with the MPPT control of the conventional cascaded H-bridge PV inverter, and is well understood [46]–[48], [65]. For instance, for each H-bridge, there is an MPPT controller, and the MPPT controller can use some conventional MPPT algorithms, such as the conventional perturb and observe (P&O) MPPT algorithm. Each MPPT controller provides the voltage reference for the corresponding H-bridge.

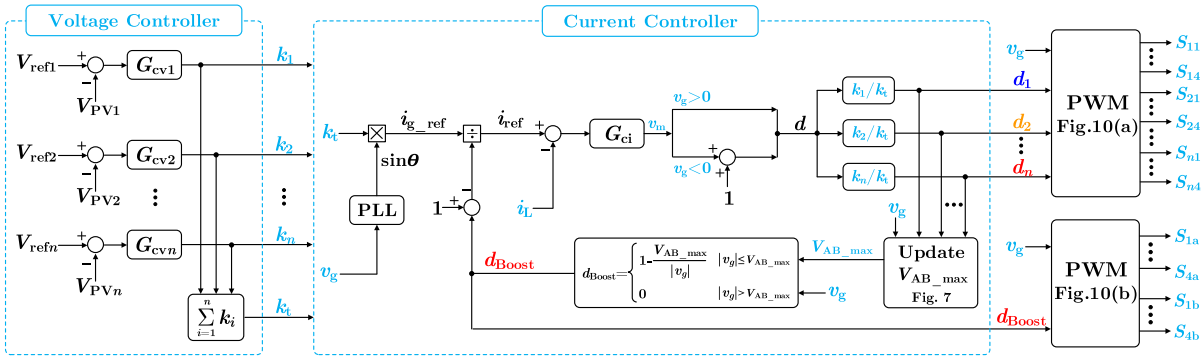

Fig. 11. Control strategy for the PV inverter.

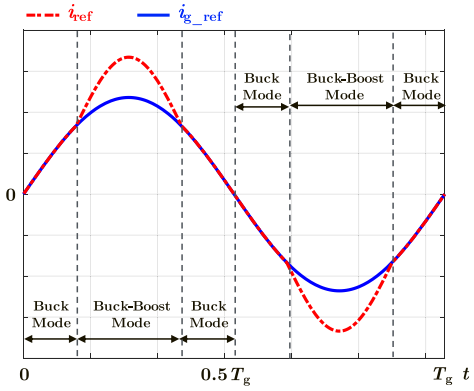

Fig. 12. Theoretical waveforms and relationship of the grid current reference i_{g_ref} and the middle inductor current reference i_{ref}.

Then, the individual dc voltage controller will regulate the corresponding dc-link voltage, as shown in Fig. 11. Since the MPPT control for the cascaded H-bridge PV inverter is well understood, there will be no details of the MPPT control in this paper. The output of each voltage controller is k_j ($j = 1, 2, \ldots, n$), and the sum of k_j is k_t [48]. The grid ac current reference i_{g_ref} is generated by multiplying k_t and the output signal $\sin\theta$ of the phase-locked loop (PLL).

Since the ac boost is an unregulated stage, this paper introduces an indirect current control that regulates the grid current i_g by controlling the middle inductor current i_L. The middle inductor current i_L is the input current of the ac boost. Thus, the middle inductor current reference i_{ref} is calculated based on the grid current reference i_{g_ref} and the ac boost feedforward duty cycle d_{Boost}, as shown in the following equation:

$$i_{ref} = \frac{i_{g\_ref}}{1 - d_{Boost}}. \tag{8}$$

The theoretical waveforms and the relationship of the grid current reference i_{g_ref} and the middle inductor current reference i_{ref} are shown in Fig. 12. The output of the current controller is the common modulation signal v_m, as shown in Fig. 11. The common modulation signal v_m is transformed to the common control signal d as

$$d = \begin{cases} v_m & v_g > 0 \\ v_m + 1 & v_g \le 0. \end{cases} \tag{9}$$

TABLE I
PARAMETERS OF THE 2-kW PV INVERTER PROTOTYPE

Symbol	Description	Value
v_g	Grid voltage	240VAC
f_g	Grid frequency	60 Hz
V_{PVj}	PV panel rated voltage (j=1, 2, ...n)	30 V
n	PV panel number	8
P_{out}	Rated output power	2 kW for 240VAC
f_H	H-bridge switching frequency	6 kHz
f_B	AC Boost switching frequency	24 kHz
L_1, L_2	Inductance	220 μH
C_j	DC link capacitance for each PV panel	13 mF

Then, based on [48], the individual H-bridge duty cycle d_j ($j = 1, 2, \ldots, n$) is generated by multiplying d and the proportional factor k_j/k_t as

$$d_j = d\frac{k_j}{k_t} \quad j = 1, 2, \ldots, n. \tag{10}$$

The gating signals for the cascaded H-bridge are generated by the individual duty cycles d_1–d_n and the phase-shifted PWM, as discussed and shown in Fig. 10(a). The maximum averaged output voltage V_{AB_max} of the cascaded H-bridge is updated, as shown in Fig. 7. With V_{AB_max} and v_g, the ac boost feedforward duty cycle d_{Boost} is generated by (7). And d_{Boost} is the input signal for the calculation of the middle inductor current reference i_{ref}, as shown in (8). With d_{Boost} and v_g, the gating signals for the interleaved ac boost are generated, as shown in Fig. 10(b).

VI. 8-PORT 2-kW PV INVERTER PROTOTYPE AND EXPERIMENTAL VERIFICATION

Based on this topology, which is the cascaded H-bridge followed by an interleaved GaN ac boost [see Fig. 4(b)], an 8-port 2-kW PV inverter prototype with natural convection cooling is designed and implemented. The system parameters are illustrated in Table I. The hardware implementations, including the devices, micro-controllers, sensors, etc., are described in

TABLE II
HARDWARE IMPLEMENTATION OF THE 2-kW PV INVERTER PROTOTYPE

Description	Implementation
60 V Si devices for H-bridges	BSC014N06NS, 60 V, 1.45 mΩ
Gate drivers for 60 V Si devices	ADUM7223
650 V GaN FETs for AC Boost	GS66508P, 50 mΩ
Gate drivers for GaN FETs	UCC27611
DC Link capacitors	UVZ1J332MRD, 63 V, 3.3 mF x 4
Micro-controller	TMS320F28377, TMS320F28335
Current sensors	ACS712
Voltage sensors	AMC1200

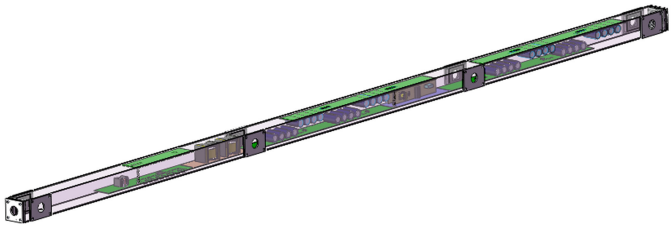

Fig. 13. 3-D drawing of the 2-kW prototype.

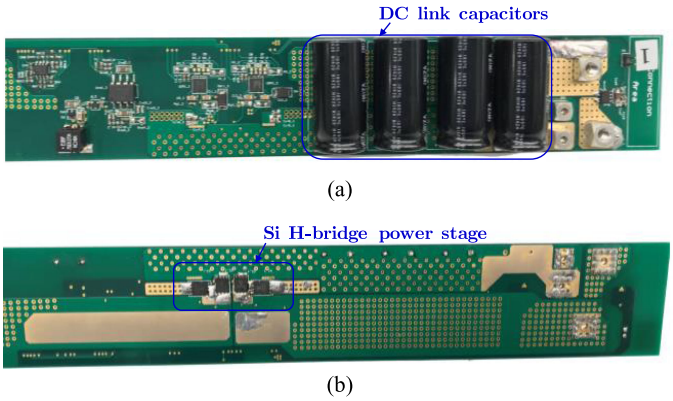

Fig. 14. Photograph of each single H-bridge. (a) Top view. (b) Bottom view.

Table II. The three-dimensional drawing of the inverter prototype is shown in Fig. 13. The size of the inverter with the case is 86 × 2 × 2 in^3. The power density is 5.8 W/in^3, which is 25% higher than the Enphase 2-kW microinverter system [31]. There are eight PV panels connected to this inverter. The photo of each single H-bridge is shown in Fig. 14. The size of each H-bridge is 9.3 × 1.7 × 0.79 in^3. The photo of the interleaved GaN ac boost is shown in Fig. 15. The size of the interleaved GaN ac boost is 9.5 × 1.7 × 1.4 in^3. The photo of the 2-kW prototype is shown in Fig. 16. This prototype uses the commercially available aluminum tube (85 × 2 × 2 in^3) as the enclosure. Using this standard aluminum tube significantly reduces the cost of the enclosure.

For the experimental verification, there are eight PV panels in total. Each dc link is connected to a PV panel and each dc link is regulated to 30 V, which is the rated dc voltage. The grid voltage v_g is 240 VAC/60 Hz. The peak grid voltage is

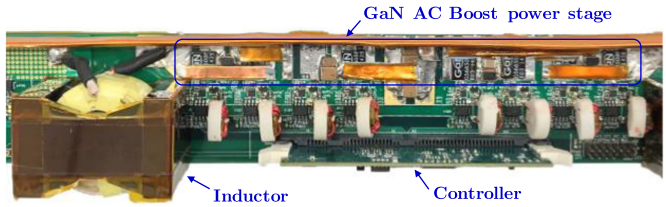

Fig. 15. Photograph of the interleaved GaN ac boost.

Fig. 16. Photograph of the 2-kW prototype.

340 V, which is much higher than the sum of all the dc-link voltages. However, the grid connection is easily realized by using the cascaded buck–boost multilevel inverter topology, the dual-mode modulation, and the control strategy.

The PWM signals for the first three H-bridges of the cascaded H-bridge are shown in Fig. 17. Fig. 17(a) shows the PWM signals during the transition time that is from the positive half-line cycle to the negative half-line cycle. Fig. 17(b) shows the PWM signals during the transition time that is from the negative half-line cycle to the positive half-line cycle. S_{11}–S_{81} are interleaved (only S_{11}–S_{31} are shown in Fig. 17 due to the limited oscilloscope channels). S_{14} operates with line frequency. During the positive half-line cycle, S_{14} is ON; during the negative half-line cycle, S_{14} is OFF.

Fig. 18 shows the ac boost feedforward duty-cycle signal d_{Boost} and the ac boost PWM gating signals. The ac boost duty-cycle signal d_{Boost} is tested via the integrated digital to analog channel of the TI micro-controller. When d_{Boost} is zero, the inverter operates in buck mode. When d_{Boost} is positive, the inverter operates in buck–boost mode. The mode transition is achieved smoothly by the ac boost feedforward duty cycle d_{Boost}.

The PWM gating signals for one phase of the interleaved ac boost are shown in Fig. 19. During the positive half-line cycle, S_{1a} and S_{2a} are complementary signals, whereas S_{1b} and S_{2b} are always ON. During the buck–boost mode of the positive half-line cycle, S_{1a} and S_{2a} are switched with high frequency. During the buck mode of the positive half-line cycle, S_{1a} is OFF, and S_{2a} is ON. During the negative half-line cycle, S_{1b} and S_{2b} are complementary signals, whereas S_{1a} and S_{2a} are always ON. During the buck–boost mode of the negative half-line cycle, S_{1b} and S_{2b} are switched with high frequency. During buck mode of the negative half-line cycle, S_{1b} is OFF, and S_{2b} is ON.

The key operating waveforms of this inverter, under rated voltages and full power conditions, are shown in Fig. 20. With the presented dual-mode modulation, during the buck mode,

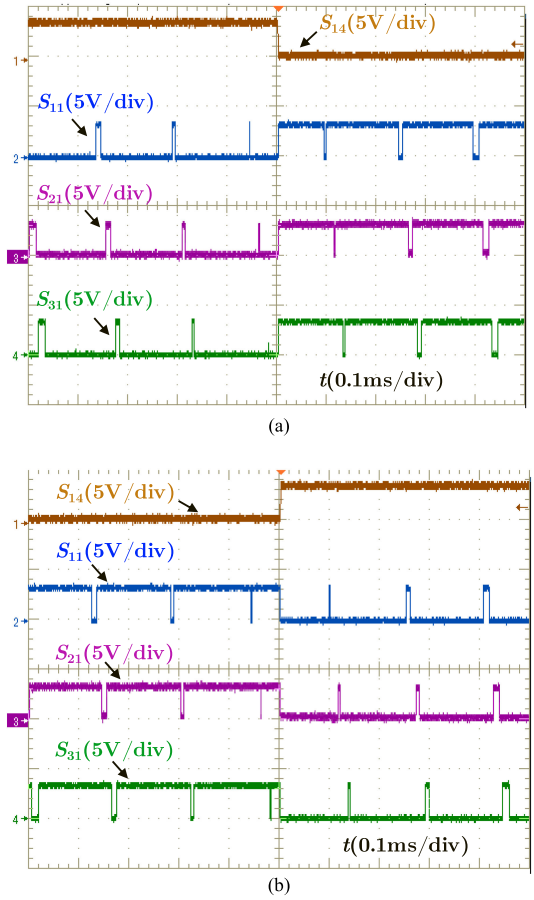

Fig. 17. PWM signals for the cascaded H-bridge. (a) Transition from the positive half-line cycle to the negative half-line cycle. (b) Transition from the negative half-line cycle to the positive half-line cycle.

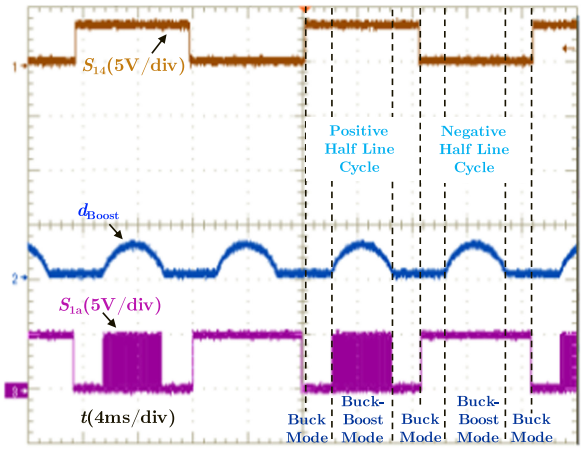

Fig. 18. AC boost PWM gating signals and ac boost duty-cycle signals.

the ac boost is bypassed, and the inverter works just like the cascaded H-bridge inverter. Thus, the output voltage v_{AB} of the cascaded H-bridge is a nine-level waveform during the buck mode. During the buck–boost mode, the ac boost switches with the feedforward duty cycle d_{Boost}. The sum of all the dc-link voltages is 240 V. The peak grid voltage is 340 V, which is much higher than the sum of all the dc-link voltages. However, the ac

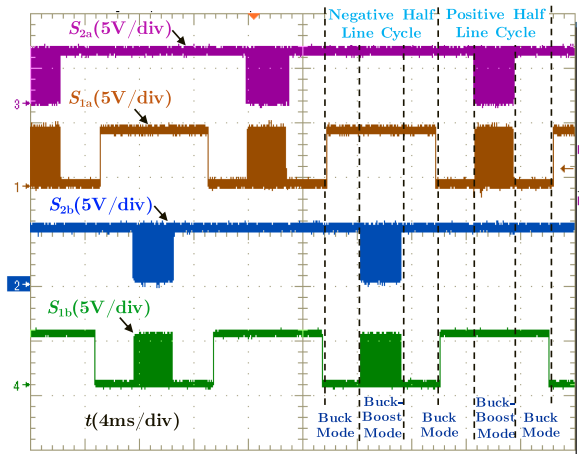

Fig. 19. AC boost PWM gating signals.

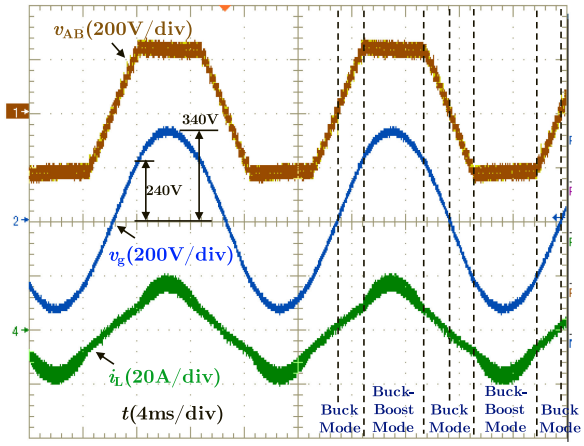

Fig. 20. Key operation waveforms under rated voltages and full power conditions.

boost stage boosts the voltage v_{AB} to the required grid voltage during the buck–boost mode, as shown in Fig. 20. The middle inductor current i_L is also shown in Fig. 20. Moreover, based on the presented modulation, the smooth transition between the two operation modes is realized, as shown in Fig. 20.

The thermal testing results under full power and natural cooling conditions have demonstrated outstanding thermal performance, as shown in Fig. 21. In Fig. 21(a), the maximum temperature rise for the GaN devices is 32 °C. As shown in Fig. 21(b), the maximum temperature rise for the 60-V Si devices is 15 °C. As shown in Fig. 21(c), the maximum temperature rise for inductors is 19 °C.

The efficiency curve is shown in Fig. 22. The full power efficiency is 97.8%. The peak efficiency is 98% under 60% of the full power condition. The efficiency performance of this inverter is superior to the commercial microinverter, which achieves 96.5% efficiency [31].

The loss comparison between the 2-kW state-of-the-art microinverter system [31] and the developed 2-kW inverter system under the full power condition is shown in Fig. 23. Since the presented non-isolated inverter topology [see Fig. 4(b)] only needs two main inductors, the loss on the main magnetic components

TABLE III
PERFORMANCE COMPARISON BETWEEN 2-kW MICROINVERTER SYSTEM AND 2-kW CASCADED BUCK–BOOST MULTILEVEL INVERTER SYSTEM

	2 kW Microinverter System	2 kW Cascaded Buck-Boost Multilevel Inverter System	Improvement
Efficiency	96.5%	97.8%	40% loss reduction
Power Density	4.6 W/inch^3	5.8 W/inch^3	25% improvement
Connectors	8 DC Connectors + 8 AC Connectors	8 DC Connectors + 2 AC Connectors	37.5% reduction
Semiconductors	150 V Si MOSFETs: 4x8 SiC Diodes: 2x8 650 V Si MOSFETs: 4x8	60 V Si MOSFETs: 4x8 650 V GaN FETs: 8	50% reduction
Main Magnetics	Transformers: 2x8	Inductors: 2	87.5% reduction

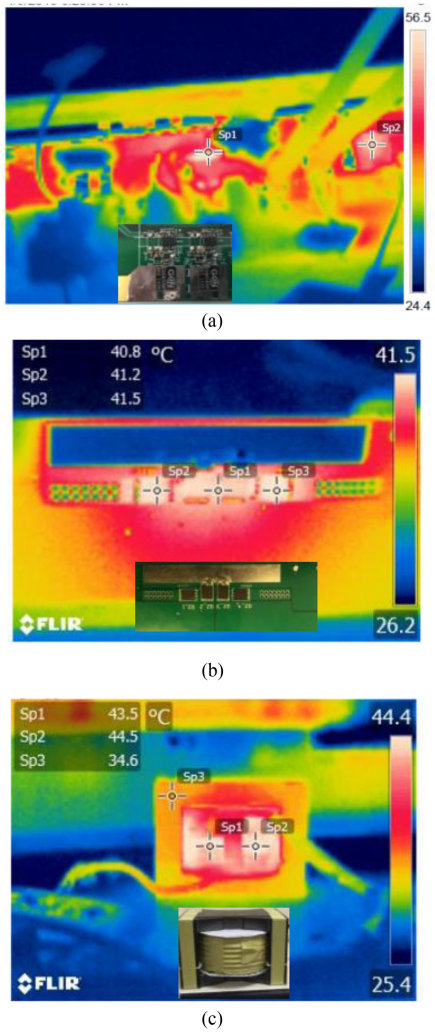

Fig. 21. Thermal testing results under rated voltages, full power, and natural cooling conditions. (a) Thermal image of GaN FETs. (b) Thermal image of 60-V Si MOSFETs. (c) Thermal image of the inductors.

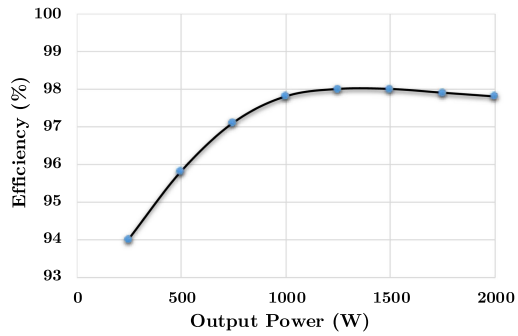

Fig. 22. Efficiency curve.

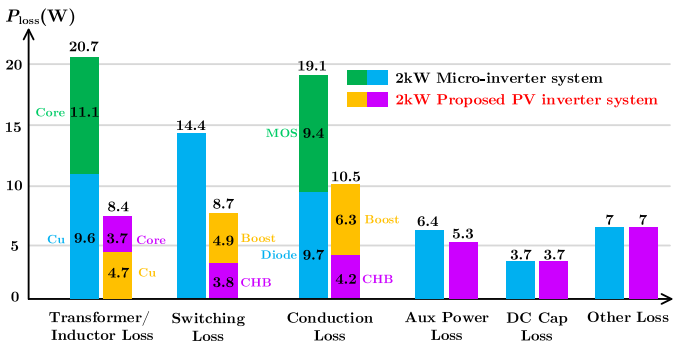

Fig. 23. Loss comparison between 2-kW microinverter system and 2-kW cascaded buck–boost multilevel inverter system under the full power condition.

is only 8.4 W, which has 60% reduction compared with the microinverter systems. The interleaving modulation for the cascaded H-bridge significantly reduces the switching frequency of the H-bridges. In this inverter, each H-bridge works at 6 kHz while still achieving 48 kHz current ripple frequency for the middle inductor. Thus, the switching loss for the cascaded H-bridge is extremely low. Additionally, the utilization of the emerging 650-V GaN FETs [58] achieves low switching loss for the ac boost. Compared with the microinverter system, 40% reduction of the total switching loss is realized by this inverter. With the utilization of 60-V Si MOSFETs (BSC014N06NS, 1.45 mΩ) and 650-V GaN FETs (GS66508P, 50 mΩ), the conduction loss of this inverter is only 10.5 W.

A detailed performance comparison between the state-of-the-art 2-kW microinverter system [31] and the 2-kW cascaded buck–boost multilevel inverter system is summarized in Table III. Compared with the 2-kW microinverter system, the developed inverter prototype achieves 40% total loss reduction, 25% power density improvement, 37.5% connector number reduction, 50% device count reduction, and 87.5% main magnetic component count reduction.

VII. Conclusion

This paper introduces a high-efficiency and high-density single-phase dual-mode cascaded buck–boost multilevel transformerless PV inverter for residential application. This inverter has a *regulated* cascaded H-bridge multilevel inverter followed by a *centralized unregulated* ac boost converter. Compared with the conventional cascaded H-bridge inverter, the additional ac boost enlarges the input voltage operation range. Compared with the conventional active buck–boost inverter, the cascaded buck–boost multilevel inverter has the individual MPPT capability. By combining the cascaded H-bridge and the ac boost, this PV inverter achieves all the following major features that are highly desirable for a residential PV inverter: the panel-based structure, the elimination of the high voltage dc arc fault, the high efficiency, the high power density, and the high flexibility of the number of PV panels. The traditional dual-mode active buck–boost inverter has buck mode and boost mode. For the presented cascaded buck–boost multilevel inverter, this paper introduces a different dual-mode operation, buck mode, and buck–boost mode since the cascaded H-bridge must always switch to control all the dc-link voltages whenever the ac boost switches or not. In the traditional dual-mode SPWM, the duty cycle of the H-bridge is saturated to 1 when the ac boost switches. However, for the presented cascaded buck–boost multilevel inverter, this paper introduces a different dual-mode modulation based on a minimized ac boost feedforward duty-cycle generation to avoid the saturations of the H-bridge duty cycles, to achieve smooth mode transition, and to improve the system efficiency. Making the ac boost work as an unregulated stage with feedforward control significantly simplifies the system control structure when combining the two stages. Moreover, this paper introduces an indirect current control which regulates the middle inductor current instead of directly controlling the grid current since the ac boost is an unregulated stage. This paper utilizes the emerging 650-V E-mode GaN FETs and two interleaved phases for the implementation of the ac boost to improve the system density and efficiency. An 8-port 2-kW PV inverter prototype is demonstrated and tested in this paper. The experimental waveforms verify the operation principles, the dual-mode modulation, and the control strategy for this inverter. Under natural convection cooling conditions, the developed PV inverter achieves 98.0% efficiency at 60% of full load and 97.8% efficiency at full load. The power density of this PV inverter is 5.8 W/in^3 with the case, under natural convection cooling conditions. Compared with the state-of-the-art microinverter-based 2-kW PV inverter system, the developed inverter prototype achieves 40% reduction of the total power loss, 25% improvement of the power density, 37.5% reduction of the power connectors, 50% reduction of the device count, and 87.5% reduction of the main magnetic count.

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