Efficiency Improvement of Grid Inverters With Hybrid Devices

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***Abstract*—In this paper, a hybrid switch with the combination of large-current silicon (Si) insulated gate bipolar transistor (IGBT) and small-current silicon carbide (SiC) metal-oxide semiconductor field-effect transistor (MOSFET) is utilized in a three-phase T-type three-level grid inverter. The hybrid switch can optimize the cost of the system while achieving high efficiency. The relationship between efficiency improvement and cost of the hybrid switch is investigated. Several switching patterns, which can decrease the loss of the small-current SiC MOSFET for the hybrid switch, are studied. Different switching patterns for the hybrid switch of the grid inverter are compared based on the inverter efficiency. Finally, a 20 kW three-phase T-type three-level grid inverter prototype with the hybrid switch of large-current Si IGBT and small-current SiC MOSFET (1:2.4 SiC/Si current ratio) is built to verify the main results.**

***Index Terms*—Grid inverter, high efficiency, hybrid switch, switching patterns.**

I. Introduction

In recent years, global solar installation has increased rapidly [1]. The efficiency improvement of photovoltaic (PV) inverters has attracted a lot of studies. In general, methods for efficiency improvement of the PV inverters can be classified into three categories: novel converter topologies, improved pulsewidth modulation (PWM) modulation methods, and using new devices.

With regards to novel converter topologies, HERIC [2], H5 [3], H6 [4], etc., have been proposed to increase the performance of a single-phase inverter. Either neutral-point-clamped (NPC) three-level inverters or T-type three-level inverters have been widely used for three-phase PV inverters [5].

Improved PWM modulation methods are used to reduce the dynamic loss of the inverter. PWM modulation methods such as discontinuous pulsewidth modulation (DPWM) [6]–[9], selective harmonic elimination pulsewidth modulation (SHEPWM) [10], and hybrid PWM [11], [12] can achieve high efficiency with given grid side power quality.

Since PV inverter's efficiency depends on power semiconductor device's performance, power semiconductor device man-

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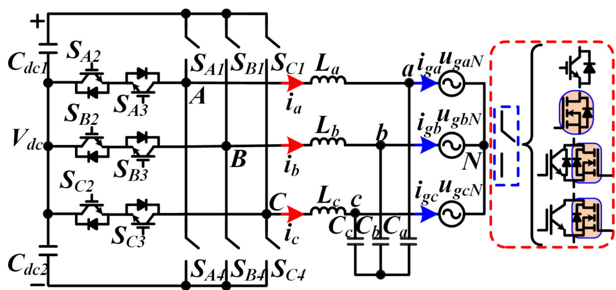


Fig. 1. Topology of the three-level inverter.

TABLE I
PARAMETERS OF THE INVERTER

Parameters	Symbol	Value
Switching frequency	f_s	18 kHz/50 kHz
Filter inductor	L	340 μH/156 μH
Filter capacitor	C	9.4 μF
DC link voltage	V_{dc}	600 V
Output line-to-line voltage (RMS)	U_o	380 V
Fundamental frequency	f_g	50 Hz
Rated three phase inverter power	P	20 kW
Modulation scheme	-	space vector modulation (SVM)

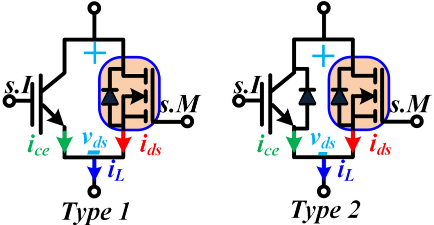


Fig. 2. Two types of hybrid switches.

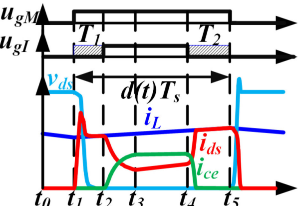


Fig. 3. Switching pattern PWM 1 and corresponding switching waveforms.

small-current SiC MOSFET of the hybrid switch, which can improve the system reliability, have seldom been reported in the literature. In addition, detailed comparisons of different switching patterns for the hybrid switch are not presented. Research works on the relationship between efficiency improvement and cost of the hybrid switch are not deeply investigated.

In this paper, the hybrid switch with the combination of large-current Si IGBT and small-current SiC MOSFET is utilized in a three-phase T-type three-level grid inverter. The hybrid switch can take the advantage of Si IGBT's good conduction characteristics and SiC MOSFET's good switching properties. Moreover, the hybrid switch can optimize the cost of the system while achieving high efficiency. The relationship between efficiency improvement and cost of the hybrid switch is derived in Section II. Several earlier switching patterns and switching patterns to reduce the loss of the small-current SiC MOSFET of the hybrid switch are studied in Section III. Also, different switching patterns for the hybrid switch of a grid inverter are compared in Section III. Finally, a 20 kW three-phase T-type three-level grid inverter prototype with the hybrid switch is built to verify the main results in Section IV. Section V concludes the paper.

II. Efficiency Improvement Versus Cost of the Hybrid Switch in a Three-Level Inverter

Hybrid switch with the combination of high-current Si IGBT and low-current SiC MOSFET is utilized in the three-phase T-type three-level grid inverter. The topology of the three-level inverter is described in Fig. 1. The horizontal switches S_{A2}, S_{A3}, S_{B2}, S_{B3}, S_{C2}, and S_{C3} are 650 V IGBTs. The antiparallel diodes of the horizontal IGBTs can be Si diodes or SiC diodes. The vertical switches S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_{C1}, and S_{C4} can be 1200 V Si IGBTs, 1200 V SiC MOSFETs, and 1200 V hybrid switches. All the analysis in the following chapter is based on the topology of the three-phase T-type three-level inverter. The parameters of the three-level inverter are listed in Table I.

As shown in Fig. 2, the hybrid switch has two typical types. Type 1 consists of SiC MOSFET and Si IGBT without an antiparallel diode in parallel. Type 2 consists of SiC MOSFET and Si IGBT with an antiparallel diode in parallel. The antiparallel diode of the Si IGBT can be SiC diode or Si diode. Detailed comparison of type 1 and type 2 is given in the subsequent content.

A. Analysis of a Common Switching Pattern

As shown in Fig. 3, PWM 1 is a frequently used switching pattern for the hybrid switch, which can realize the ZVS operation for the Si IGBT [35]. The switching waveforms in Fig. 3 are based on sinusoidal pulsewidth modulation (SPWM) when inductor current is large enough to make SiC MOSFET and Si IGBT distribute the total current together. The current will only go through the SiC MOSFET if inductor current is too small. And the waveforms of inductor current are multiple stages with SVM modulation employed. T_s is the switching period, $d(t)$ is the duty cycle in the switching cycle, u_{gM} is the gate signal of the SiC MOSFET, and u_{gI} is the gate signal of the Si IGBT. At t_1, the SiC MOSFET is turned ON first, while all the inductor current flows through the SiC MOSFET, which may lead to transient overcurrent and corresponding switching loss at very short time. At t_2, the Si IGBT is turned ON under the ZVS-ON condition for a low voltage drop over the Si IGBT. The turn-ON delay time T_1 should be large enough to allow complete conduction of the SiC MOSFET and small enough to ensure the safety of the SiC MOSFET under the transient condition. Another important issue for PWM 1 is the slow dynamics of the dynamic current commutation between SiC MOSFET and Si IGBT due to the parasitic inductance in the interconnection between SiC MOSFET and Si IGBT during the stage t_2–t_3. A switching pattern is introduced to reduce the impact of the above-mentioned problem when the Si IGBT conducts more current than the SiC MOSFET, which, however, increases the turn-ON loss [27]. At t_4, the Si IGBT is turned OFF under the ZVS-OFF condition for a low voltage drop over the Si IGBT and a large amount of stored charge in the Si

IGBT decreases as a result of the minority carrier recombination. Then, all the inductor current will flow through the SiC MOSFET. The turn-OFF delay time T_2 should be large enough to allow complete recovery of the carriers in the Si IGBT and short enough to ensure the safety of the SiC MOSFET under the transient condition. The selection of T_2 was a tradeoff between SiC MOSFET's conduction loss and Si IGBT's turn-OFF loss. At t_5, the SiC MOSFET is turned OFF under a hard switch condition. If the turn-OFF delay time T_2 is large enough, few stored charge is left at t_5. When the voltage drop over the Si IGBT increases with the turn-OFF of the SiC MOSFET, small current will flow through the Si IGBT to charge its parasitic capacitor, which realizes ZCS-OFF of the Si IGBT [26], [27], [39], [40]. In general, PWM 1 realizes the ZVS operation for the Si IGBT if the delay times T_1 and T_2 are large enough. However, all the inductor current flows through the SiC MOSFET during the delay times T_1 and T_2, which may cause SiC MOSFET overcurrent or overheat.

All the following analysis is based on PWM 1 (T_1 is equal to 0.2 μs and T_2 is equal to 1 μs). The following discussions are based on the assumption that the ZVS operation for the Si IGBT is realized.

B. Steady-State Current Sharing in the Hybrid Switch

As shown in Figs. 2 and 3, the conduction voltage drop of the SiC MOSFET is resistive and can be derived as follows:

$$v_{ds}(t) = R_{ds} \cdot i_{ds}(t) \tag{1}$$

where R_{dson} is the ON-state resistance of the SiC MOSFET, $i_{ds}(t)$ is the conduction current of the SiC MOSFET, and $v_{ds}(t)$ is the conduction voltage drop of the hybrid switch. The conduction voltage drop of the Si IGBT is a constant voltage plus a resistive drop, which can be expressed as follows:

$$v_{ds}(t) = v_{ce0} + R_{ce} \cdot i_{ce}(t) \tag{2}$$

where R_{ce} is the ON-state resistance of the Si IGBT, $i_{ce}(t)$ is the conduction current of the Si IGBT, and v_{ce0} is the ON-state zero-current voltage of the Si IGBT. The inductor current $i_L(t)$ can be calculated as follows:

$$i_L(t) = i_{ds}(t) + i_{ce}(t). \tag{3}$$

According to (1)–(3) and by assuming that the inductor current is constant during the switching cycle, steady-state current sharing of the hybrid switch can be described by the following equation:

$$\begin{cases} i_{ds}(t) = \dfrac{i_L(t) \cdot R_{ce} + v_{ce0}}{R_{dson} + R_{ce}} \\ i_{ce}(t) = \dfrac{i_L(t) \cdot R_{dson} - v_{ce0}}{R_{dson} + R_{ce}} \end{cases} \quad \text{if } i_L(t) \geq \frac{v_{ce0}}{R_{dson}} \tag{4}$$

$$\begin{cases} i_{ds}(t) = i_L(t) \\ i_{ce}(t) = 0 \end{cases} \quad \text{if } i_L(t) < \frac{v_{ce0}}{R_{dson}}. \tag{5}$$

With regards to current sensing, there are many current sensing technologies: integrated current shunts (coaxial shunts, resistive shunts, etc.), current transformers, Rogowski coils, Hall-effect current sensors, and so on [45]. Resistive shunts are applied in the double pulse test (DPT) in noncontinuous operation [46]–[48]. In this paper, the current of the hybrid switch is measured by current sensing resistors in parallel and Rogowski coils in continuous operation.

C. Loss Model in the Three-Level Inverter With the Hybrid Switch

It is assumed that f_s is the switching frequency and f_g is the line frequency. In a line cycle, the number of switching cycles $p = \text{round}(f_s/f_g)$. The turn-ON loss of the hybrid switch can be estimated by the following equation:

$$P_{\text{on}M} = 3f_g \sum_{k=0}^{p-1} \left[\frac{V_{dc}}{2V_{\text{base}}} E_{\text{on}}(k) \right] \tag{6}$$

where $E_{\text{on}}(k)$ is the turn-ON loss of the SiC MOSFET in the $(k+1)$ switching cycle, and V_{base} is the corresponding bus voltage when measuring the switching loss. The turn-OFF loss of the hybrid switch is obtained by the following equation:

$$P_{\text{off}\,M} = 3f_g \sum_{k=0}^{p-1} \left[\frac{V_{dc}}{2V_{\text{base}}} E_{\text{off}}(k) \right] \tag{7}$$

where $E_{\text{off}}(k)$ is the turn-OFF loss of the SiC MOSFET in the $(k+1)$ switching cycle.

When type1 is applied in the three-phase three-level grid-connected inverter with a nonunit power factor, the reverse recovery loss of the body diode of the SiC MOSFET in the hybrid switch can be calculated by the following equation:

$$P_{\text{recDM}} = 3f_g \sum_{k=0}^{p-1} \left[\frac{V_{dc}}{2V_{\text{base}}} E_{\text{recDM}}(k) \right] \tag{8}$$

where $E_{\text{recDM}}(k)$ is the reverse recovery energy of the body diode of the SiC MOSFET in the $(k+1)$ switching cycle.

When type 2 is applied in the three-phase three-level grid-connected inverter with a nonunit power factor, the reverse recovery loss of the antiparallel diode of the Si IGBT in the hybrid switch can be calculated by the following equation:

$$P_{\text{recDI}} = 3f_g \sum_{k=0}^{p-1} \left[\frac{V_{dc}}{2V_{\text{base}}} E_{\text{recDI}}(k) \right] \tag{9}$$

where $E_{\text{recDI}}(k)$ is the reverse recovery loss of the antiparallel diode of the Si IGBT in the hybrid switch in the $(k+1)$ switching cycle.

According to (4) and (5), the conduction loss of the SiC MOSFET in the hybrid switch in a line cycle $P_{\text{con}M}$ can be estimated by the following equation:

$$P_{\text{con}M} = 6f_g \sum_{k=0}^{q-1} R_{dson} \times \begin{pmatrix} i_{dsa}^2(k)T_{saM}(k) + i_{dsa\text{SR}}^2(k)T_{da}(k) \\ +i_{dsb}^2(k)T_{sbM}(k) + i_{dsb\text{SR}}^2(k)T_{db}(k) \\ +i_{dsc}^2(k)T_{scM}(k) + i_{dsc\text{SR}}^2(k)T_{dc}(k) \end{pmatrix} \tag{10}$$

where q is round $[f_s/(6f_g)]$; $i_{dsa}(k)$, $i_{dsb}(k)$, and $i_{dsc}(k)$ are the current of the SiC MOSFET in three phases in the $(k+1)$ switching cycle; $i_{dsa\mathrm{SR}}(k)$, $i_{dsb\mathrm{SR}}(k)$, and $i_{dsc\mathrm{SR}}(k)$ are the reverse current of the SiC MOSFET when the SiC MOSFET is operating in the synchronous rectification mode with a power factor not equal to 1 in three phases in the $(k+1)$ switching cycle; $T_{saM}(k)$, $T_{sbM}(k)$, and $T_{scM}(k)$ are the conduction time of the SiC MOSFET in three phases in the $(k+1)$ switching cycle; and $T_{da}(k)$, $T_{db}(k)$, and $T_{dc}(k)$ are the conduction time of the SiC MOSFET when the SiC MOSFET is operating in the synchronous rectification mode with the power factor not equal to 1 in the $(k+1)$ switching cycle. The conduction loss of the Si IGBT in the hybrid switch in a line cycle $P_{\mathrm{con}I}$ can be shown as follows:

$$P_{\mathrm{con}I} = 6f_g \sum_{k=0}^{q-1} \times \left(\begin{array}{l} v_{ce0}\left(|i_{cea}(k)| + |i_{ceb}(k)| + |i_{cec}(k)|\right) \\ +R_{ce}\left(\begin{array}{l} i_{cea}^2(k)T_{saI}(k) + i_{ceb}^2(k)T_{sbI}(k) \\ +i_{cec}^2(k)T_{scI}(k) \end{array} \right) \end{array} \right) \tag{11}$$

where $i_{cea}(k)$, $i_{ceb}(k)$, and $i_{cec}(k)$ are the current of the Si IGBT in three phases in the $(k+1)$ switching cycle, and $T_{saI}(k)$, $T_{sbI}(k)$, and $T_{scI}(k)$ are the conduction time of the Si IGBT in the $(k+1)$ switching cycle. When type 2 is applied in the three-phase three-level grid-connected inverter with the power factor not equal to 1 described in Fig. 1, the conduction loss of the antiparallel diode of the Si IGBT in the hybrid switch can be calculated by the following equation (in fact, the antiparallel diode of Si IGBT and SiC MOSFET operating in the synchronous rectification mode share the total current):

$$P_{\mathrm{conDI}} = 6f_g \sum_{k=0}^{q-1} \times \left(\begin{array}{l} v_{ce0d}\left(|i_{da}(k)| + |i_{db}(k)| + |i_{dc}(k)|\right) \\ +R_{ced}\left(\begin{array}{l} i_{da}^2(k)T_{da}(k) + i_{db}^2(k)T_{db}(k) \\ +i_{dc}^2(k)T_{dc}(k) \end{array} \right) \end{array} \right) \tag{12}$$

where $i_{da}(k)$, $i_{db}(k)$, and $i_{dc}(k)$ are the current of the antiparallel diode of the Si IGBT in three phases in the $(k+1)$ switching cycle, R_{ced} is the ON-state resistance of the antiparallel diode of the Si IGBT, and v_{ce0d} is the ON-state zero-current voltage of the antiparallel diode of the Si IGBT.

The turn-ON loss of the horizontal IGBT with the nonunit power factor is expressed as follows:

$$P_{\mathrm{onCI}} = 3f_g \sum_{k=0}^{p-1} \left[\frac{V_{dc}}{2V_{\mathrm{base}}} E_{\mathrm{onCI}}(k) \right] \tag{13}$$

where $E_{\mathrm{onCI}}(k)$ is the turn-ON loss of the horizontal IGBT in the $(k+1)$ switching cycle. The turn-OFF loss of the horizontal IGBT with the nonunit power factor is obtained by the following equation:

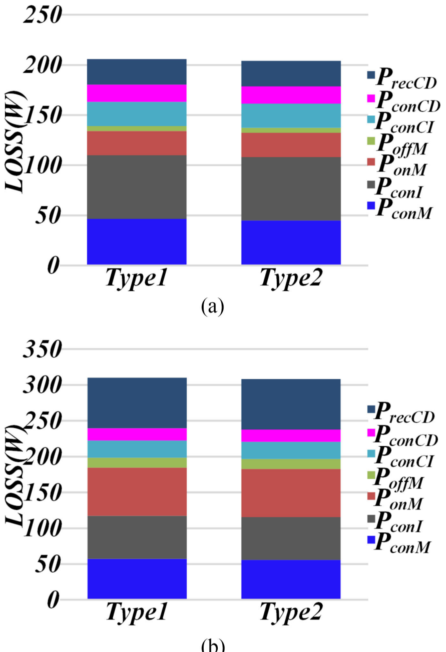


Fig. 4. Loss distributions of type 1 and type 2 @ 20 kW with power factor 1. (a) f_s = 18 kHz. (b) f_s = 50 kHz.

$$P_{\mathrm{offCI}} = 3f_g \sum_{k=0}^{p-1} \left[\frac{V_{dc}}{2V_{\mathrm{base}}} E_{\mathrm{offCI}}(k) \right] \tag{14}$$

where $E_{\mathrm{offCI}}(k)$ is the turn-OFF energy of the horizontal IGBT in the $(k+1)$ switching cycle.

The reverse recovery loss of the antiparallel diode of the horizontal IGBT with the nonunit power factor can be calculated by the following equation:

$$P_{\mathrm{recCD}} = 3f_g \sum_{k=0}^{p-1} \left[\frac{V_{dc}}{2V_{\mathrm{base}}} E_{\mathrm{recCD}}(k) \right] \tag{15}$$

where $E_{\mathrm{recCD}}(k)$ is the reverse recovery loss of the antiparallel diode of the horizontal IGBT in the $(k+1)$ switching cycle.

The conduction loss of the horizontal IGBT P_{conCI} and the conduction loss of the antiparallel diode of the horizontal IGBT P_{conCD} are not introduced here.

D. Comparison of Type 1 and Type 2 Hybrid Switches

Based on the parameters listed in Table I, the type 1 hybrid switch with IGBT IKW40N120T2 && SiC MOSFET C2M0080120D and the type 2 hybrid switch with IGBT IGW40T120 && SiC MOSFET C2M0080120D are selected. IGBT IKW50N65EH5 is chosen as the horizontal switch. Fig. 4 shows the loss distributions of type 1 and type 2 hybrid switches with two switching frequencies at rated output power 20 kW with the unit power factor. Fig. 4 shows that type 1 and type 2 have nearly the same loss at both 18 and 50 kHz switching frequency at the unit power factor.

However, the loss distributions of type 1 and type 2 hybrid switches are different with the nonunit power factor even with

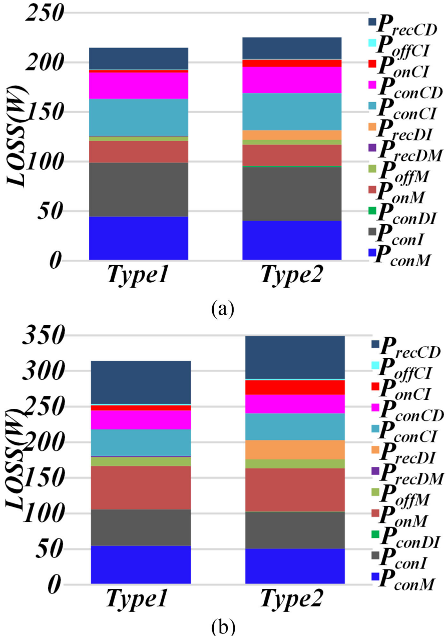


Fig. 5. Loss distributions of type 1 and type 2 @ 20 kW with power factor 0.8 lagging. (a) f_s = 18 kHz. (b) f_s = 50 kHz.

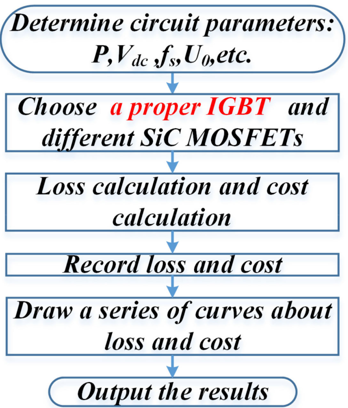


Fig. 6. Procedure for analyzing the loss and cost of the hybrid switch.

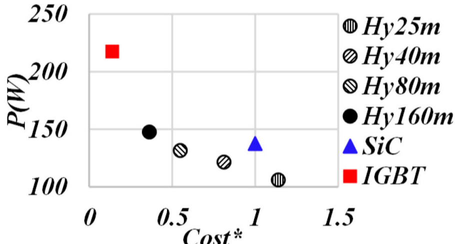


Fig. 7. Curves of Loss-Cost* when α equals 9.

the same switching frequency and output power. Fig. 5 shows the loss comparison of type 1 and type 2 hybrid switches with 20 kW with 0.8 power factor. It reveals that type 1 has less loss than type 2. Type 1 has smaller P_{recDM} and smaller P_{onCI} due to the good reverse recovery characteristics of the body diode of the SiC MOSFET, while type 2 has larger P_{recDI} and larger P_{onCI} due to the poor reverse recovery characteristics of the antiparallel diode of the Si IGBT. Therefore, type 2 is not suitable for high frequency for its large switching loss when the power factor is not equal to 1.

In general, the type 1 hybrid switch should be chosen. However, for the unit power factor case, the type 2 hybrid switch is still usable.

E. Relationship Between Efficiency Improvement and Cost of the Hybrid Switch in the Three-Level Inverter

The relationship between efficiency improvement and cost of the hybrid switch in the three-level inverter is required for reasonably selecting the device capacity of the hybrid switch so that the inverter can be optimized with respect to both efficiency and cost. An analysis of the relationship between efficiency improvement and cost of the hybrid switch according to the loss and the cost is described in this section. Due to the fact that the loss and cost of horizontal switches shown in Fig. 1 are fixed, only the loss and cost of vertical switches, which are implemented with hybrid switches (S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_{C1}, and S_{C4}). are considered in the following analysis.

It is assumed that the rated current of the Si IGBT is I_I, and the rated current of the SiC MOSFET is I_M. In order to calculate intuitively, the cost of the Si IGBT is described as "$1 * I_I$" and the cost of the SiC MOSFET is defined as "$\alpha * I_M$" where α represents that the cost of the SiC MOSFET at unit current is α times that of the Si IGBT, which is defined as the cost ratio of SiC MOSFET to IGBT. The cost of one driver board is defined as "β." Per-unit value of the cost of the hybrid switch Cost* can be expressed as follows:

$$\text{Cost}^* = \frac{\alpha I_M + I_I + 2\beta}{\alpha I_{M\text{ref}} + \beta} \tag{16}$$

where $I_{M\text{ref}}$ is the reference value of the rated current of the SiC MOSFET when only SiC MOSFET is used as a vertical switch. The total loss of hybrid switch P at the unit power factor can be calculated by the following equation:

$$P = P_{\text{on}M} + P_{\text{off}M} + P_{\text{con}M} + P_{\text{con}I}. \tag{17}$$

The following analysis is based on the parameters in Table I when the switching frequency is 18 kHz.

A procedure for analyzing the loss and cost of the hybrid switch is outlined in Fig. 6. First, the Si IGBT is selected with enough current rating for the 20 kW inverter. Then, the SiC MOSFET is selected with different ON-state resistances, which are supposed to be parallel with the selected IGBT. Finally, both loss and cost of different combinations of hybrid switches are calculated and recorded in a series of curves.

The curves of Loss-Cost* with different solutions of hybrid switches are shown in Figs. 7 and 8. Fig. 7 shows the cost versus efficiency with the assumption of the cost ratio of 9. Fig. 8 shows the cost versus efficiency with the assumption of the cost ratio of 5. The Si IGBT (IKQ50N120CT2) is selected. For SiC MOSFETs, C2M0160120D (160 mΩ), C2M0080120D (80 mΩ),

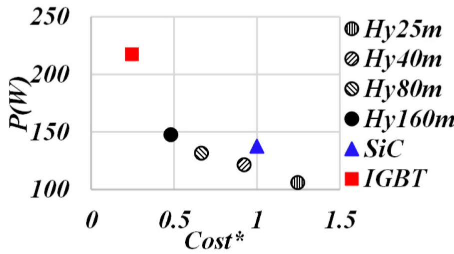


Fig. 8. Curves of Loss-Cost* when α equals 5.

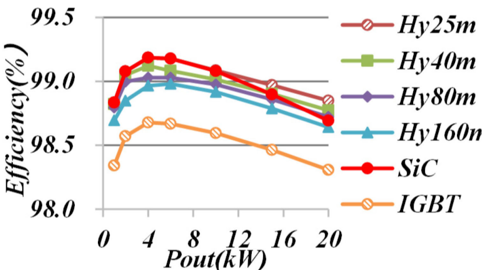


Fig. 9. Calculated efficiency @18 kHz.

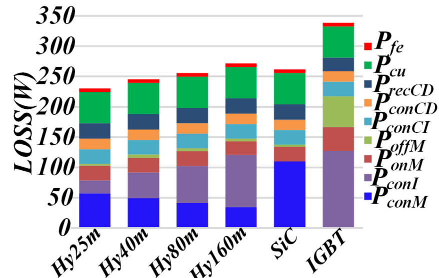


Fig. 10. Loss distributions at 20 kW @18 kHz.

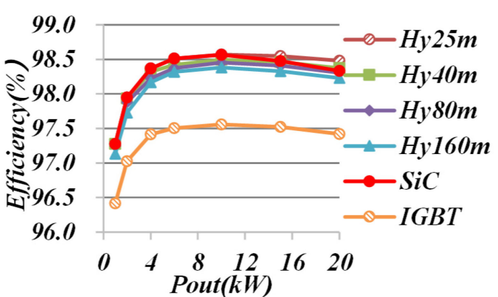


Fig. 11. Calculated efficiency @ 50 kHz.

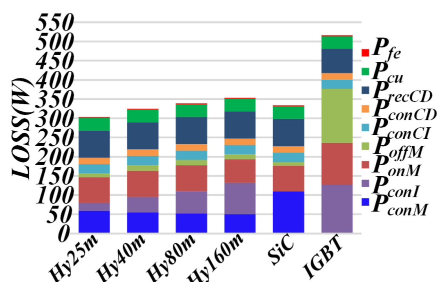


Fig. 12. Loss distributions at 20 kW @ 50 kHz.

C2M0040120D (40 mΩ), and C2M0025120D (25 mΩ) are used for analysis.

In both figures, the horizon axis presents the per-unit values of the cost of different solutions of hybrid switches and the vertical axis presents the loss of different solutions of hybrid switches at rated output power. The legends "*Hy25m,*" "*Hy40m,*" "*Hy80m,*" and "*Hy160m*" denote SiC MOSFETs used in hybrid switches: 25, 40, 80, and 160 mΩ, respectively, while the Si IGBT is fixed to be IKQ50N120CT2. The legends "*SiC*" and "*IGBT,*" respectively, show only SiC MOSFET (25 mΩ) and only IGBT (IKQ50N120CH3) of vertical switches.

Some results can be obtained taking Fig. 7 as an example. The large loss of only IGBT greatly limits the efficiency of the inverter although the cost is very low. Efficiency can be improved by using only SiC MOSFET, which, however, leads to a significant cost increase. The black points reflect the relationship between efficiency improvement or loss and cost of the hybrid switch. In general, efficiency improvement or loss and cost of the hybrid switch are a pair of contradictions. Optimization between efficiency and cost can be achieved by choosing the proper ratio of the hybrid switch. The comparison of Figs. 7 and 8 shows that the selection range of the hybrid switch gradually decreases with the decrease in cost ratio α.

F. Loss Distribution in the Three-Level Inverter

Fig. 9 shows the efficiency of different devices combinations with the switching frequency 18 kHz. Fig. 10 shows the loss distribution at rated output power 20 kW corresponding to Fig. 9. The legends "P_{fe}" and "P_{cu}," respectively, represent core loss of filter and copper loss of filter. The results in Figs. 9 and 10 show that the hybrid switch has a distinct advantage compared to only IGBT in efficiency. The efficiency of the hybrid switch is lower than only SiC MOSFET at light load, while the efficiency advantage of the hybrid switch is gradually obvious at heavy load when the cost of the hybrid switch is lower than only SiC MOSFET. Also, it can be concluded that the difference of the inverter loss when applying different hybrid switches is mainly the conduction loss of the hybrid switch.

Figs. 11 and 12 show the results, while the switching frequency is pushed up to 50 kHz. The comparison between 18 and 50 kHz shows that the hybrid switch is more advantageous compared to only IGBT at high switching frequency. The reverse recovery of the antiparallel diode in the horizontal switch is one of the biggest barriers for improving the efficiency and the switching frequency, which causes large loss both in the antiparallel diode and the vertical switch.

III. Different Switching Patterns for the Hybrid Switch in the Three-Level Inverter

Switching patterns for hybrid switches will affect the loss distribution and total efficiency of the inverter. In this section, different switching patterns for the hybrid switch in the three-level inverter are discussed. The parameters for calculation are listed in Table I at 18 kHz.

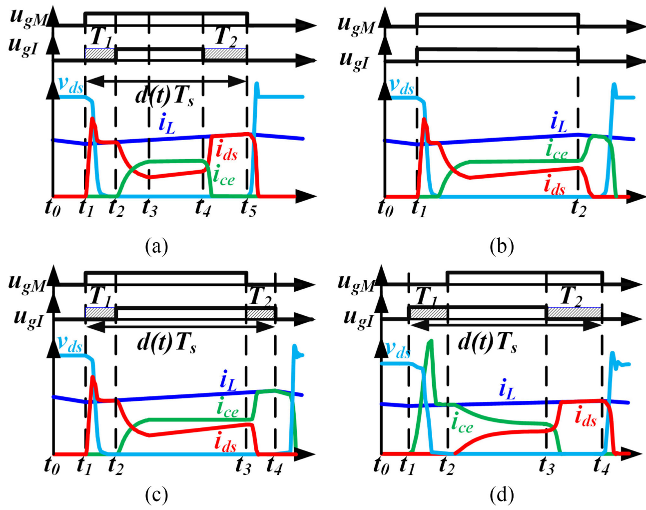


Fig. 13. Switching waveforms of (a) PWM 1, (b) PWM 2, (c) PWM 4, and (d) PWM 6.

A. Traditional Switching Patterns for the Hybrid Switch

Switching pattern PWM1 shown in Fig. 13(a) is discussed in Section II. Fig. 13(b) shows the switching pattern PWM 2, which is a special case of PWM 1 where the turn-ON delay time T_1 and the turn-OFF delay time T_2 are zero. At t_1, the driving signals of SiC MOSFET and Si IGBT are generated at the same time. But the SiC MOSFET is turned ON earlier than the IGBT due to its fast switching properties, which make the Si IGBT be under the ZVS-ON condition, and turn-ON loss is almost eliminated. At t_2, the SiC MOSFET is turned OFF earlier than the IGBT, which makes the SiC MOSFET be under the ZVS-OFF condition. PWM 2 realizes ZVS-ON for the Si IGBT and ZVS-OFF for the SiC MOSFET, which is more suitable for the ZVS-OFF topology. PWM 2 has larger switch-OFF loss, but the loss of the SiC MOSFET is smaller compared to PWM 1.

PWM 4 is shown in Fig. 13(c), where the SiC MOSFET is turned ON earlier than the IGBT by the turn-ON delay time T_1, and the SiC MOSFET is turned OFF also earlier than the IGBT by the turn-OFF delay time T_2. With enough turn-ON delay time T_1 and turn-OFF delay time T_2, PWM 4 can realize ZVS-ON for the Si IGBT and ZVS-OFF for the SiC MOSFET, which is more suitable for the ZVS-OFF topology. The characteristics of PWM 4 is the same to PWM 2.

PWM 6 is shown in Fig. 13(d), where the SiC MOSFET is turned ON later than the IGBT by the turn-ON delay time T_1, and the SiC MOSFET is turned OFF also later than the IGBT by the turn-OFF delay time T_2. With enough turn-ON delay time T_1 and turn-OFF delay time T_2, PWM 6 can realize ZVS-OFF for the Si IGBT and ZVS-ON for the SiC MOSFET, which is more suitable for the ZVS-ON topology. When the Si IGBT flows more current than the SiC MOSFET, PWM 6 can reduce the impact of the parasitic inductances and shows a faster dynamics of the current commutation than PWM 1 [27].

1) Analysis of the Conduction Loss of the Hybrid Switch With PWM 1: As shown in Fig. 13(a), to realize the ZVS condition for the IGBT, the following two equations needs to be satisfied:

$$T_1 \geq T_{\text{on}M} \tag{18}$$

$$T_2 \geq T_{\text{off}I} \tag{19}$$

where $T_{\text{on}M}$ is the turn-ON time of the SiC MOSFET, and $T_{\text{off}I}$ is the turn-OFF time of the Si IGBT. By combining (18) and (19), the following equation is obtained:

$$T_1 + T_2 \geq T_{\text{on}M} + T_{\text{off}I}. \tag{20}$$

If the sum of the two time delay is defined as T_d

$$T_1 + T_2 \triangleq T_d. \tag{21}$$

The total delay time T_d needs to satisfy the following equation:

$$T_d \geq T_{\text{on}M} + T_{\text{off}I}. \tag{22}$$

When T_d is greater than the duty cycle time of a switching cycle, only SiC MOSFET of the hybrid switch will work in this switching cycle as the gate signal u_{gI} is equal to zero. When T_d is greater than the maximum duty cycle time in a line cycle, only SiC MOSFET of the hybrid switch will work in the line cycle as the gate signal u_{gI} is equal to zero.

Once the Si IGBT can realize ZVS operation, the switching loss of the hybrid switch only depends on the selected SiC MOSFET and has nothing to do with T_d. However, the conduction loss of the hybrid switch is affected by T_d. The total conduction loss of all hybrid switches P_{con} in the inverter with T_d changing is shown in Fig. 14, and the conduction loss of all SiC MOSFETs in hybrid switches $P_{\text{con}M}$ in the inverter with T_d changing is presented in Fig. 15. It can be seen from the two figures that when T_d is larger than the maximum duty cycle time, only

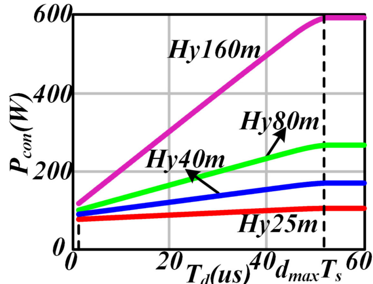


Fig. 14. Total conduction loss of hybrid switch versus T_d.

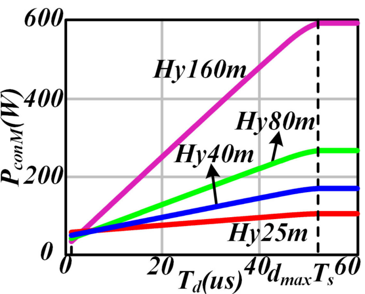


Fig. 15. Conduction loss of SiC MOSFET versus T_d.

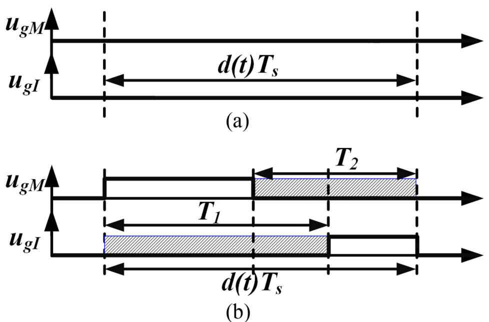


Fig. 16. Some possible abnormal work mode using PWM 4. (a) $T_1 > d(t)T_s$ and $T_2 > d(t)T_s$. (b) $T_1 < d(t)T_s$ and $T_2 < d(t)T_s$ and $(T_1 + T_2) > d(t)T_s$.

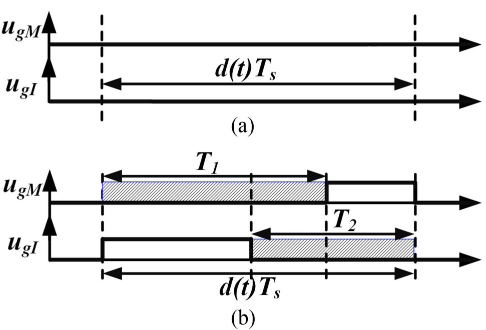


Fig. 17. Some possible abnormal work mode using PWM 6. (a) $T_1 > d(t)T_s$ and $T_2 > d(t)T_s$. (b) $T_1 < d(t)T_s$ and $T_2 < d(t)T_s$ and $(T_1 + T_2) > d(t)T_s$.

SiC MOSFET of the hybrid switch works in the circuit and the conduction loss reaches the saturation value. P_{con} increases with the increase of T_d, and $P_{\text{con}M}$ increases with the increase of T_d. Therefore, when the Si IGBT realizes ZVS operation, T_d can be chosen as small as necessary considering from the aspects of the inverter efficiency and the thermal problem of the SiC MOSFET. What is more, different ON-state resistances of SiC MOSFETs of hybrid switches mean different slopes. When T_d is fixed, P_{con} increase as the ON-state resistance of the SiC MOSFET increases, and mostly $P_{\text{con}M}$ increase as the ON-state resistance increases.

2) Analysis of Conduction Loss of the Hybrid Switch With PWM 4: As shown in Fig. 16, when both T_1 and T_2 are larger than $d(t)T_s$, the inverter cannot work normally as the gate signals u_{gM} and u_{gI} are equal to zero. When both T_1 and T_2 are smaller than $d(t)T_s$ and the sum of T_1 and T_2 is larger than $d(t)T_s$, similar situation will occur. Therefore, PWM 4 is more suitable for a dc–dc converter than dc–ac or ac–dc converter for the limited value of T_1 and T_2. There are other solutions, for example, changing PWM 4 to other PWM patterns under such cases. To make the Si IGBT be under the ZVS-ON condition, the following equation needs to be satisfied:

$$T_1 \geq T_{\text{on}M} \tag{23}$$

and to make the SiC MOSFET be under the ZVS-OFF condition, the following equation needs to be satisfied:

$$T_2 \geq T_{\text{off}\,M} \tag{24}$$

where $T_{\text{off}M}$ is the turn-OFF time of the SiC MOSFET.

P_{con} increases with the increase of T_1 and T_2. $P_{\text{con}M}$ increases with the increase of T_1 but decreases with the increase of T_2. T_1 can be chosen as small as necessary considering the inverter efficiency and the thermal problem of the SiC MOSFET. T_2 should be chosen based on the tradeoff of the inverter efficiency and thermal problem of the SiC MOSFET.

3) Analysis of the Conduction Loss of the Hybrid Switch With PWM 6: As shown in Fig. 17, similar to PWM 4, PWM 6 may work abnormally. The solution is changing PWM 6 to other PWM patterns. PWM 6 is more suitable for a dc–dc converter than dc–ac or ac–dc converter. To make the SiC MOSFET be under the ZVS-ON condition, the following equation needs to be satisfied:

$$T_1 \geq T_{\text{on}I} \tag{25}$$

where $T_{\text{on}I}$ is the turn-ON time of the Si IGBT, and to make the Si IGBT be under the ZVS-OFF condition, the following equation needs to be satisfied:

$$T_2 \geq T_{\text{off}\,I}. \tag{26}$$

P_{con} increases with the increase of T_1 and T_2. $P_{\text{con}M}$ decreases with the increase of T_1 but increases with the increase of T_2. When the Si IGBT realizes ZVS operation, T_2 can be chosen as small as necessary considering from the aspects of the inverter efficiency and the thermal problem of the SiC MOSFET. T_1 should be chosen based on the tradeoff of the inverter efficiency and thermal problem of the SiC MOSFET.

B. Switching Patterns Decreasing the Loss of the Small-current SiC MOSFET for the Hybrid Switch

Several switching patterns are studied in this chapter, which can decrease the loss of the small-current SiC MOSFET to reduce the risk of overheating and reliability degradation of the small-current SiC MOSFET.

PWM 3 in Fig. 18(a) is based on PWM 1. At t_3, the SiC MOSFET is turned OFF under the ZVS-OFF condition and the SiC MOSFET is turned ON under the ZVS-ON condition at t_4. This operation can reduce the conduction loss of the SiC MOSFET, which improves the reliability and longevity of the SiC MOSFET compared to PWM 1. In a sense, PWM 1 can be seen as a special case of PWM 3.

PWM 5 in Fig. 18(b) is based on PWM 4. At t_3, the SiC MOSFET is turned OFF under the ZVS-OFF condition and the SiC MOSFET is turned ON under the ZVS-ON condition at t_4. Similarly, PWM 5 can improve the reliability and longevity of the SiC MOSFET compared to PWM 4.

PWM 7 in Fig. 18(c) is based on PWM 6. At t_3, the SiC MOSFET is turned OFF under the ZVS-OFF condition and the SiC MOSFET is turned ON under the ZVS-ON condition at t_4. Similarly, PWM 7 can improve the reliability and longevity of the SiC MOSFET compared to PWM 6.

In conclusion, the operation of turn-OFF of the SiC MOSFET when the Si IGBT is ON can decrease the conduction loss of the

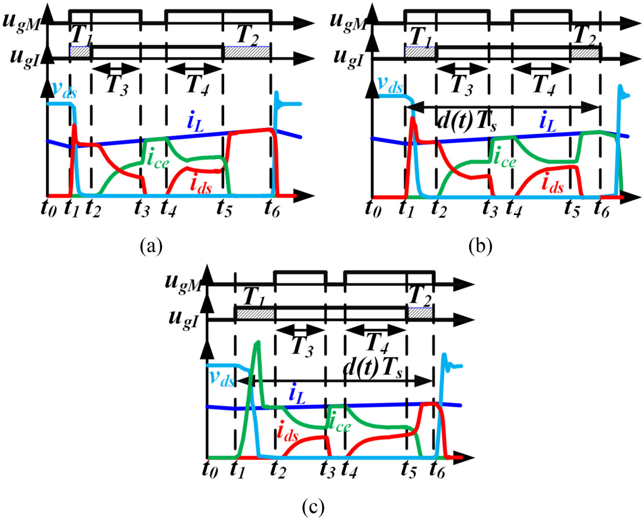


Fig. 18. Switching waveforms of (a) PWM 3, (b) PWM 5, and (c) PWM 7.

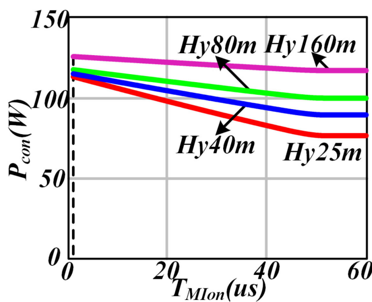


Fig. 19. Total conduction loss of hybrid switch versus T_{MIon}.

SiC MOSFET; however, this operation can increase the switching frequency of the SiC MOSFET, which slightly increases the switching loss.

1) Analysis of the Conduction Loss of the Hybrid Switch With PWM 3: As shown in Fig. 18(a), the time delay T_d is defined the same as (21), and the sharing conduction time T_{MIon} is defined as follows:

$$T_3 + T_4 \triangleq T_{\mathrm{MIon}}. \tag{27}$$

To make the Si IGBT be under the ZVS condition, delay time T_d needs to satisfy (22). PWM 1 can be considered as a special case of PWM 3 with the same T_d. PWM 3 will be changed to PWM 1 in the switching cycle when the sum of T_d and T_{MIon} is greater than the duty cycle time of this switching cycle and T_d is smaller than the duty cycle time of this switching cycle. Only SiC MOSFET of the hybrid switch will work in the switching cycle when T_d is greater than the duty cycle time of this switching cycle.

P_{con} with T_{MIon} changing is shown in Fig. 19, and $P_{\mathrm{con}M}$ with T_{MIon} changing is presented in Fig. 20 when T_d is 1.2 μs. It can be seen from the figures that PWM 3 becomes PWM 1 when T_{MIon} is large enough and the conduction loss reaches the saturation value, which is the value of PWM 1 with the same T_d. P_{con} decreases with the increase of T_{MIon}. However, $P_{\mathrm{con}M}$ increases with the increase of T_{MIon}. Therefore, T_{MIon} should be chosen based on the tradeoff of the inverter efficiency and thermal problem of the SiC MOSFET. Different ON-state resistances of SiC MOSFETs of hybrid switches mean different slopes. When T_d and T_{MIon} are fixed, P_{con} increase as the ON-state resistance of the SiC MOSFET increases, while the change of $P_{\mathrm{con}M}$ depends on the value of T_{MIon}.

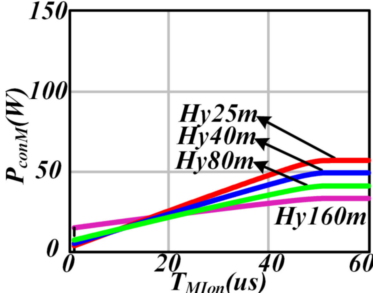


Fig. 20. Conduction loss of SiC MOSFET versus T_{MIon}.

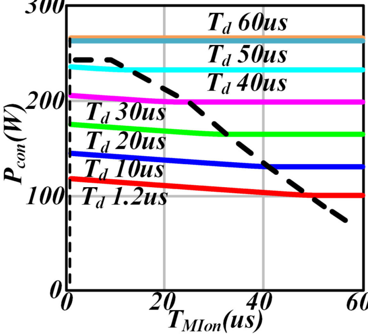


Fig. 21. Total conduction loss of hybrid switch versus T_d and T_{MIon}.

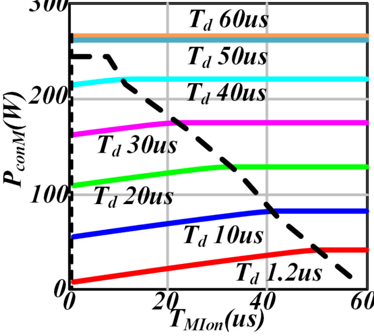


Fig. 22. Conduction loss of SiC MOSFET versus T_d and T_{MIon}.

P_{con} (Hy80m) with T_d and T_{MIon} changing is shown in Fig. 21, and $P_{\mathrm{con}M}$ (Hy80m) with T_d and T_{MIon} changing is presented in Fig. 22. The right side and upper side of the dotted line in the figures are the saturation region of PWM 3, which can be thought as the PWM 1 region with the same T_d. When T_{MIon} is fixed, both P_{con} and $P_{\mathrm{con}M}$ increase with the increase of T_d. The results in the figures conclude that when the Si IGBT realizes ZVS operation, T_d could be chosen as small as necessary considering from the aspects of the inverter efficiency and the thermal problem of the SiC MOSFET.

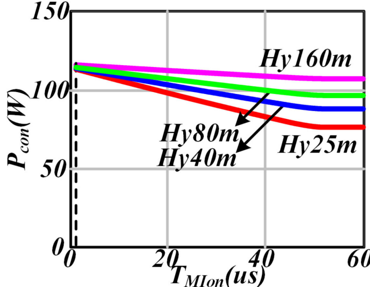


Fig. 23. Total conduction loss of hybrid switch versus T_{MIon}.

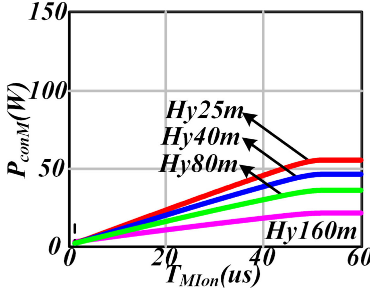


Fig. 24. Conduction loss of SiC MOSFET versus T_{MIon}.

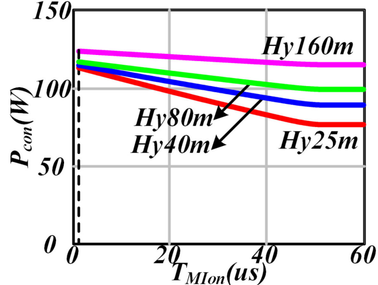


Fig. 25. Total conduction loss of hybrid switch versus T_{MIon}.

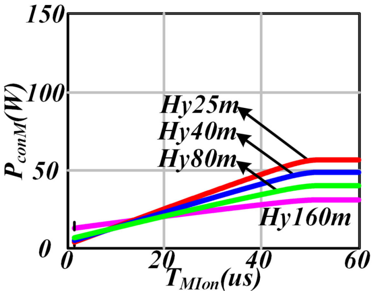


Fig. 26. Conduction loss of the SiC MOSFET versus T_{MIon}.

2) Analysis of the Conduction Loss of the Hybrid Switch With PWM 5: As shown in Fig. 18(b), T_1 and T_2 need to satisfy (23) and (24). PWM 4 can be considered as a special case of PWM 5 when time delays T_1 and T_2 of PWM 4 and PWM 5 are the same. PWM 5 will be changed to PWM 4 in the switching cycle when the sum of T_1, T_2, and T_{MIon} is greater than the duty cycle time of this switching cycle.

P_{con} with T_{MIon} changing is shown in Fig. 23, and $P_{\mathrm{con}M}$ with T_{MIon} changing is presented in Fig. 24 when T_1 is 0.2 μs and T_2 is 0.5 μs. It can be seen from the figures that PWM 5 becomes PWM 4 when T_{MIon} is large enough and the conduction loss reaches the saturation value, which is the value of PWM 4 with the same T_1 and T_2. When T_1 and T_2 are fixed, P_{con} decreases with the increase of T_{MIon}, while $P_{\mathrm{con}M}$ increases with the increase of T_{MIon}. Therefore, T_{MIon} should be chosen based on the tradeoff of the inverter efficiency and thermal problem of the SiC MOSFET. When T_1, T_2, and T_{MIon} are fixed, P_{con} increase as the ON-state resistance of the SiC MOSFET increases, while mostly $P_{\mathrm{con}M}$ decreases as the ON-state resistance increases.

3) Analysis of the Conduction Loss of the Hybrid Switch With PWM 7: PWM 7 can be considered as a special case of PWM 6 when T_1 and T_2 of PWM 6 and PWM 7 are the same. PWM 7 will be changed to PWM 6 in the switching cycle when the sum of T_1, T_2, and T_{MIon} is greater than the duty cycle time of this switching cycle.

P_{con} with T_{MIon} changing is shown in Fig. 25, and $P_{\mathrm{con}M}$ with T_{MIon} changing is presented in Fig. 26 when T_1 is 0.2 μs and T_2 is 1 μs. PWM 7 becomes PWM 6 when T_{MIon} is large enough and the conduction loss reaches the saturation value, which is the value of PWM 6 with the same T_1 and T_2 shown in the figures. When T_1 and T_2 is fixed, P_{con} decreases with the increase of T_{MIon}. However, $P_{\mathrm{con}M}$ increases with the increase of T_{MIon}. Therefore, T_{MIon} should be chosen based on the tradeoff of the inverter efficiency and thermal problem of the SiC MOSFET. When T_1, T_2, and T_{MIon} are fixed, P_{con} increase as the ON-state resistance of the SiC MOSFET increases, while the change of $P_{\mathrm{con}M}$ depends on the value of T_{MIon}.

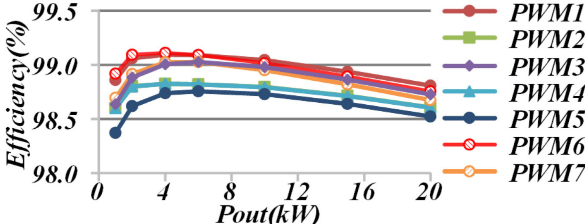


Fig. 27. Calculated efficiency of different switching patterns for the hybrid switch.

C. Comparison of Different Switching Patterns for the Hybrid Switch in the Three-Level Inverter

Fig. 27 shows the calculated efficiency of different switching patterns for the hybrid switch (Hy80m) assuming that the Si IGBT realizes ZVS-OFF operation when utilizing PWM 1, PWM 3, PWM 6, and PWM 7 (PWM 1 T_1: 0.2 μs T_2: 1 μs; PWM 2; PWM 3 T_1: 0.2 μs T_2: 1 μs T_{MIon}: 5 μs; PWM 4 T_1: 0.2 μs T_2: 0.5 μs; PWM 5 T_1: 0.2 μs T_2: 0.5 μs T_{MIon}: 5 μs; PWM 6 T_1: 0.2 μs T_2: 1 μs; PWM 7 T_1: 0.2 μs T_2: 1 μs T_{MIon}: 5 μs). Fig. 28 shows the loss distribution at rated output power 20 kW corresponding to Fig. 27. The legends "P_{on}" and "P_{off}," respectively, represent turn-ON loss and turn-OFF loss of the hybrid switch. The results in the figures show that PWM 1 and PWM 3 have the advantage over other switching patterns in heavy load, while PWM 6 and PWM 7 have the advantage over other switching patterns in light load. PWM 6 and PWM 7 have larger turn-ON loss but

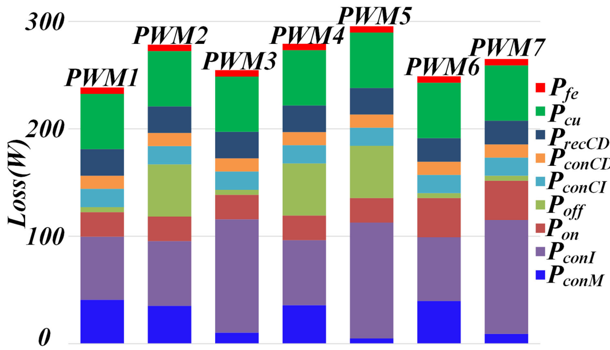


Fig. 28. Loss distributions at rated output power 20 kW.

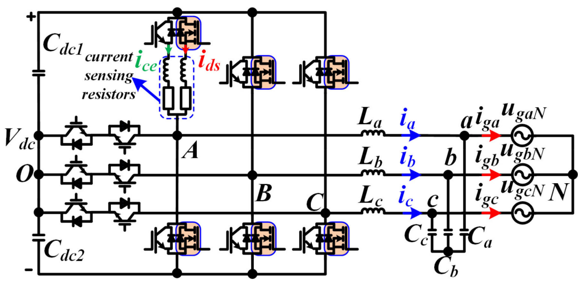


Fig. 29. Topology of the T-type three-level inverter for current sensing.

smaller diode recovery loss in heavy load, while PWM 6 and PWM 7 have smaller turn-ON loss and smaller diode recovery loss in light load (the reverse recovery of the antiparallel diode in the horizontal switch will both influence the diode recovery loss and turn-ON loss of the vertical switch) compared to PWM 1 and PWM 3 , respectively. PWM 2, PWM 4, and PWM 5 have larger turn-OFF loss for the high switching loss of the Si IGBT compared to PWM 1. The difference of PWM 1, PWM 2, PWM 4, and PWM 6 in the figures is the switching loss of the hybrid switch (the conduction loss of the hybrid switch in the figures is almost the same).

The discussions in the above-mentioned section show that utilizing PWM 1 has higher efficiency than using PWM 3 with the same T_d, but the conduction loss of the SiC MOSFET of utilizing PWM 1 is also higher than using PWM 3 with the same T_d. This provides a new idea for combining the switching patterns. Utilizing PWM 1 from light load to medium load can ensure light and medium load efficiency, while using PWM 3 at heavy load can ensure high efficiency with junction temperature of the SiC MOSFET reduced and system reliability improved. Also, PWM 1 and PWM 6 or PWM 3 and PWM 7 can be combined for high efficiency at full load. More deep research can be done in the future.

IV. Experimental Results

A. Current Sensing of the Hybrid Switch

A 20 kW T-type three-level three-phase grid-connected inverter prototype for current sensing is built, as shown in Fig. 29. The parameters of the inverter are listed in Table II. The hybrid switch is IKW40N120T2 in parallel with C2M0040120D, and the horizontal switch is IKW50N65EH5. PWM 1 is employed for the experiment. The current measurement comparison of Rogowski coils and resistive shunts (ten 50 mΩ 0805 resistors in parallel) in continuous operation is shown in Fig. 30. The steady current match well in two measurement ways, while Rogowski coils have better transient characteristics. However, Rogowski coils cannot measure the dc current. Fig. 31 shows the current sharing of the hybrid switch using resistive shunts. Fig. 32 describes the comparison of measured and theoretical current sharing of the hybrid switch with resistive shunts displaying the acceptable error.

TABLE II
PARAMETERS OF THE INVERTER

Parameters	Symbol	Value
Switching frequency	f_s	18 kHz
Filter inductor	L	670 μH@0A
Filter capacitor	C	9.4 μF
DC link voltage	V_{dc}	600 V
Output line-to-line voltage (RMS)	U_o	400 V
Fundamental frequency	f_g	50 Hz
Rated three phase inverter power	P	20 kW

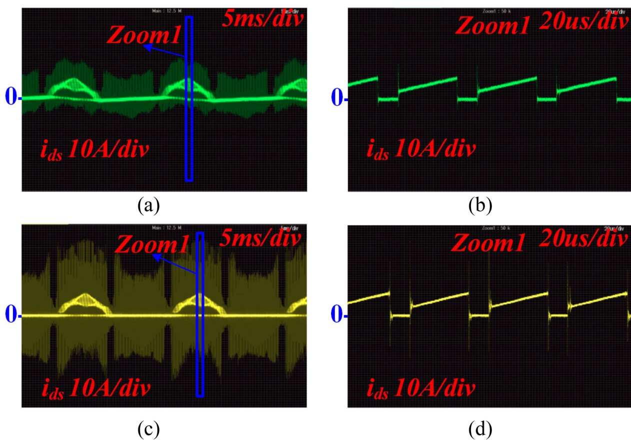


Fig. 30. Comparison of measured and theoretical current. (a) Rogowski coils. (b) Zoom1 of (a). (c) Ten 50 mΩ in parallel. (d) Zoom1 of (c).

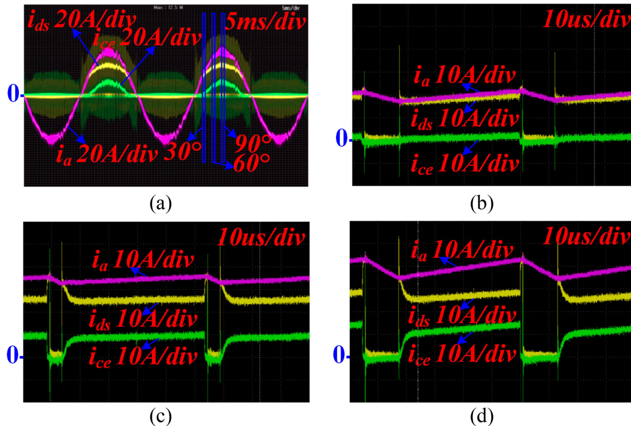


Fig. 31. Current sharing of hybrid switch @ 20 kW. (a) Current sharing @ 20 kW. (b) 30° of (a). (c) 60° of (a). (d) 90° of (a).

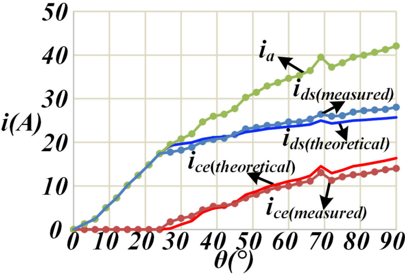


Fig. 32. Comparison of measured and theoretical current.

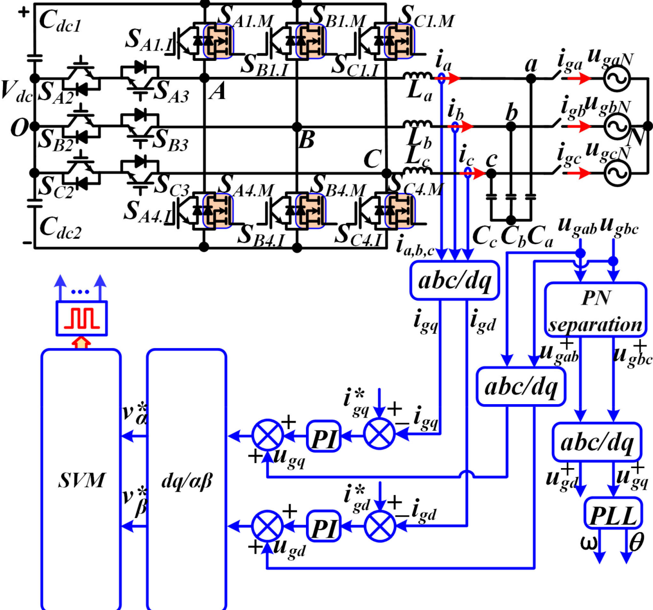


Fig. 33. Topology and control block diagram of the inverter.

B. Comparison of Different Switching Patterns for the Hybrid Switch

A 20 kW T-type three-level three-phase grid-connected inverter prototype is built, as shown in Fig. 33. The control block diagram of the inverter is also presented in Fig. 33. The vertical switch is the hybrid switch of IKW40N120T2 in parallel with C2M0080120D (1:2.4 SiC/Si current ratio HyS) and the horizontal switch is IKW50N65EH5. The cost of Hy80m is far less than the cost of only SiC MOSFET (C2M0025120D).

1) $f_s = 18$ kHz: The parameters of the inverter are listed in Table II. Fig. 34(a) and (b) reveals that the Si IGBT applying PWM 1 and PWM 3 is under the ZVS-ON condition. The Si IGBT of the hybrid switch still has the turn-OFF loss when T_2 equals 1 μs for large stored charge left in the Si IGBT. However, the Si IGBT of the hybrid switch has very small turn-OFF loss when T_2 equals 3 μs for few stored charge left in the Si IGBT. This phenomenon can be clearly shown between Fig. 35(a) and (b), and the experimental efficiency curve in Fig. 36 also shows this. The efficiency of PWM 1 is 0.1% higher than PWM 3 with the same T_d at rated power, which implies that the switching strategy utilizing PWM 1 from light load to medium load while

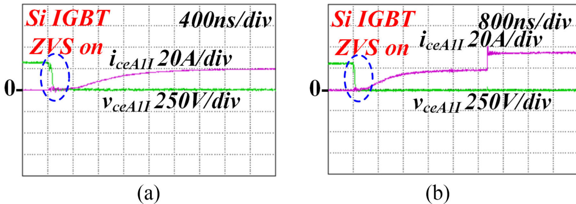


Fig. 34. Collector–emitter voltage and collector–emitter current of SA1.I. (a) PWM 1 with T_1 200 ns, T_2 1 μs. (b) PWM 3 with T_1 200 ns, T_2 1 μs, and T_{MIon} 5 μs.

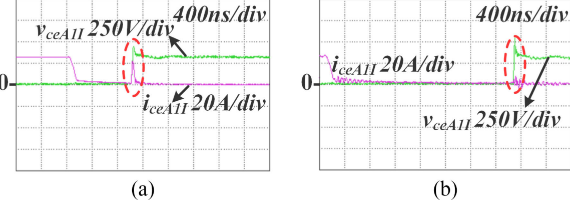


Fig. 35. Collector–emitter voltage and collector–emitter current of SA1.I. (a) PWM 1 with T_1 200 ns, T_2 1 μs. (b) PWM 1 with T_1 200 ns, T_2 3 μs.

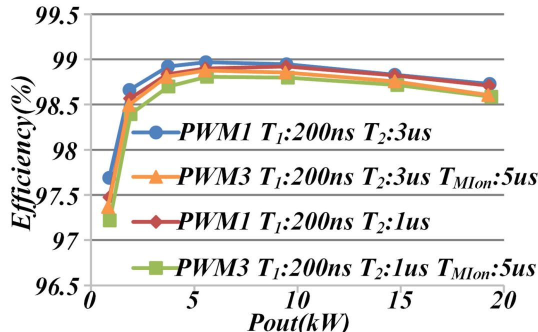


Fig. 36. Experimental efficiency of the inverter with PWM 1 and PWM 3.

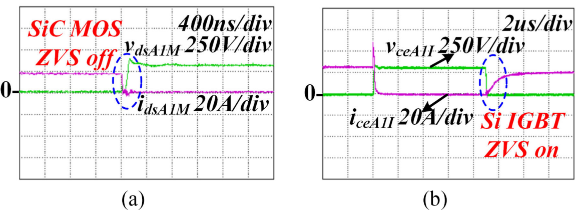


Fig. 37. Waveforms using PWM 2. (a) Drain–source voltage and drain–source current of SA1.M. (b) Collector–emitter voltage and collector–emitter current of SA1.I.

using PWM 3 at heavy load is feasible. In general, the selection of T_2 for PWM 1 and PWM 3 should be focused.

Waveforms using PWM 2, PWM 4, and PWM 5 are presented in Figs. 37, 38, and 39, and the results show that the SiC MOSFET is under the ZVS-OFF condition and the Si IGBT is under the ZVS-ON condition applying PWM 2, PWM 4, and PWM 5. The efficiency using PWM 2, PWM 4, and PWM 5 is relatively low due to the large turn-OFF loss shown in Fig. 40.

The efficiency of PWM 6 and PWM 7 shown in Fig. 41 is, respectively, higher than PWM 1 and PWM 3 with the same

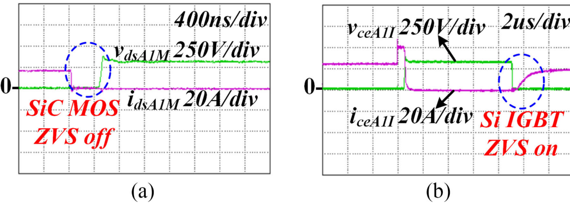


Fig. 38. Waveforms using PWM 4 with T_1 200 ns and T_2 500 ns. (a) Drain–source voltage and drain–source current of SA1.M. (b) Collector–emitter voltage and collector–emitter current of SA1.I.

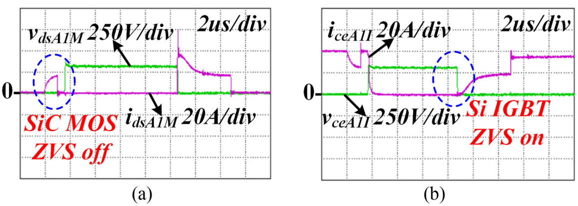


Fig. 39. Waveforms using PWM 5 with T_1 200 ns, T_2 500 ns, and T_{MIon} 5 μs. (a) Drain–source voltage and drain–source current of SA1.M. (b) Collector–emitter voltage and collector–emitter current of SA1.I.

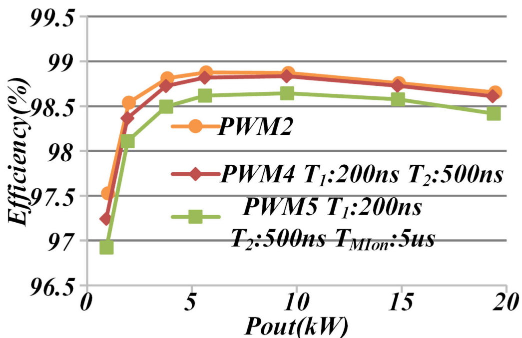


Fig. 40. Experimental efficiency of the inverter with PWM 2, PWM 4, and PWM 5.

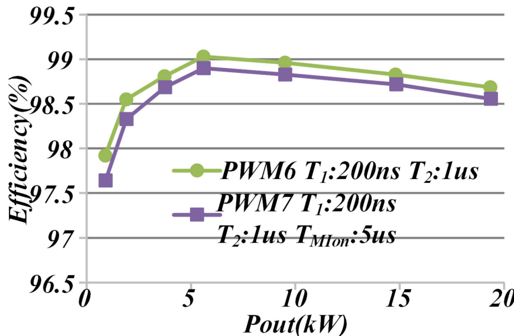


Fig. 41. Experimental efficiency of the inverter with PWM 6 and PWM 7.

delay time in light and half-load due to better diode reverse recovery, while the efficiency of PWM 6 and PWM 7 is lower than PWM 1 and PWM 3 with the same delay time in heavy load due to larger turn-ON loss. Fig. 42(a) and (b) shows that the SiC MOSFET applying PWM 6 and PWM 7 is under the ZVS-ON condition.

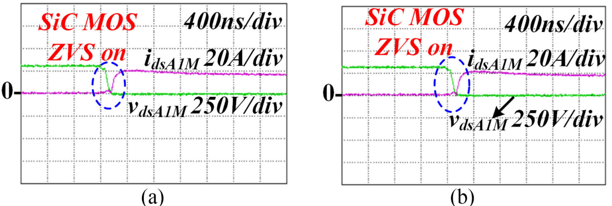


Fig. 42. Drain–source voltage and drain–source current of SA1.M. (a) PWM 6 with T_1 200 ns and T_2 1 μs. (b) PWM 7 with T_1 200 ns, T_2 1 μs, and T_{MIon} 5 μs.

TABLE III
PARAMETERS OF THE INVERTER

Parameters	Symbol	Value
Switching frequency	f_s	50 kHz
Filter inductor	L	235 μH@0A
Filter capacitor	C	9.4 μF
DC link voltage	V_{dc}	600 V
Output line-to-line voltage (RMS)	U_o	393 V
Fundamental frequency	f_g	50 Hz
Rated three phase inverter power	P	20 kW

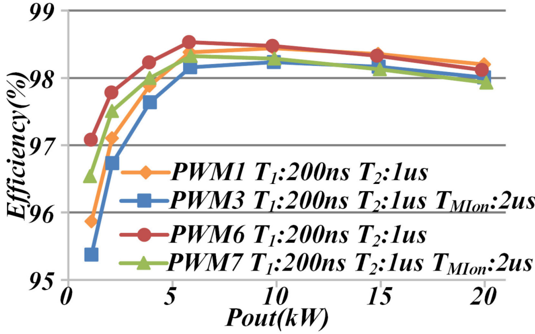


Fig. 43. Experimental efficiency of the inverter with PWM 1, PWM 3, PWM 6, and PWM 7 @ 50 kHz.

2) $f_s = 50$ kHz: The parameters of the inverter are listed in Table III. The value of the filter inductor decreases from 670 μH @ 18 kHz to 235 μH @ 50 kHz, which means smaller filter and higher power density. The efficiency with the hybrid switch at high switching frequency is comparable to that with the Si IGBT at low switching frequency. The efficiency of PWM 6 and PWM 7 shown in Fig. 43 is, respectively, higher than PWM 1 and PWM 3 with the same delay time in light and half-load due to better diode reverse recovery, while the efficiency of PWM 6 and PWM 7 is lower than PWM 1 and PWM 3 with the same delay time in heavy load due to larger turn-ON loss.

V. CONCLUSION

Hybrid switch with the combination of large-current Si IGBT and small-current SiC MOSFET (1:2.4 SiC/Si current ratio) is utilized in the three-phase T-type three-level grid inverter in this paper. Theoretical analysis and experiment results both show that utilizing the hybrid switch in the T-type three-level grid inverter can achieve high efficiency at a relatively low cost and improve the switching frequency, which means smaller filter

and higher power density at the same time. The inverter can be designed by compromising PV inverter's efficiency and its cost according to the derivate of the relationship between the hybrid switch's loss and its cost. Several switching patterns, which can decrease the loss of the small-current SiC MOSFET for the hybrid switch, are proved. After comparison of different switching patterns for the hybrid switch, it can be concluded that PWM 1 and PWM 3 are preferred for the efficiency advantage in heavy load, while PWM 6 and PWM 7 are better for the efficiency advantage in light and half-load.

References

[1] M. Schmela, "Global market outlook for solar power/2017–2021," Solar Power Europe, Brussels, Belgium, Jun. 13, 2017.

[2] H. Schmidt, S. Christoph, and J. Ketterer, "Current inverter for direct/alternating currents, has direct and alternating connections with an intermediate power store, a bridge circuit, rectifier diodes and a inductive choke," German Patent DE10 221 592 A1, Dec. 04, 2003.

[3] M. Victor, F. Greizer, S. Bremicker, and U. Huebler, "Verfahren zum Umwandeln einer elektrischen Gleichspannung einer Gleichspannungsquelle, insbesondere einer Photovoltaik-Gleichspannungsquelle in eine Wechselspannung," German Patent DE102004 030 912 B3, Jan. 19, 2006.

[4] W. Yu, J. S. J. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated ac-module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[5] T. Kerekes, M. Liserre, R. Teodorescu, C. Klumpner, and M. Sumner, "Evaluation of three-phase transformerless photovoltaic inverter topologies," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2202–2211, Sep. 2009.

[6] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063–1075, Nov./Dec. 1991.

[7] A. M. Trzynadlowski and S. Legowski, "Minimum-loss vector PWM strategy for three-phase inverters," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 26–34, Feb. 1994.

[8] D. Holmes and T. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, vol. 45. Hoboken, NJ, USA: Wiley, 2003, pp. 71–77.

[9] L. Dalessandro, S. D. Round, U. Drofenik, and J. W. Kolar, "Discontinuous space-vector modulation for three-level PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 530–542, Mar. 2008.

[10] J. Pontt, J. Rodriguez, and R. Huerta, "Mitigation of noneliminated harmonics of SHEPWM three-level multipulse three-phase active front end converters with low switching frequency for meeting standard IEEE-519-92," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1594–1600, Nov. 2004.

[11] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, May/Jun. 1997.

[12] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, Sep./Oct. 1998.

[13] Y. Hinata, M. Horio, Y. Ikeda, R. Yamada, and Y. Takahashi, "Full SiC power module with advanced structure and its solar inverter application," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, 2013, pp. 604–607.

[14] D. De, A. Castellazzi, A. Solomon, A. Trentin, M. Minami, and T. Hikihara, "An all SiC MOSFET high performance PV converter cell," in *Proc. 2013 15th Eur. Conf. Power Electron. Appl.*, Lille, 2013, pp. 1–10.

[15] S. Pisecki and J. Rąbkowski, "Experimental investigations on the grid-connected ac/dc converter based on three-phase SiC MOSFET module," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, 2015, pp. 1–10.

[16] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of SiC MOSFETs in a T-type inverter for grid-tie applications," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2808–2821, Apr. 2017.

[17] Y. Shi, L. Wang, R. Xie, Y. Shi, and H. Li, "A 60-kW 3-kW/kg five-level T-type SiC PV inverter with 99.2% peak efficiency," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9144–9154, Nov. 2017.

[18] W. Wondrak, R. Held, E. Niemann, and U. Schmid, "SiC devices for advanced power and high-temperature applications," *IEEE Trans. Ind. Electron.*, vol. 48, no. 2, pp. 307–308, Apr. 2001.

[19] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, Jun. 2002.

[20] D. Jiang, R. Burgos, F. Wang, and D. Boroyevich, "Temperature-dependent characteristics of SiC devices: Performance evaluation and loss calculation," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 1013–1024, Feb. 2012.

[21] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[22] Y. Jiang, G. Hua, E. Yang, and F. Lee, "Soft-switching of IGBTs with the help of MOSFETs in bridge-type converters," in *Proc. Power Electron. Spec. Conf.*, 1993, pp. 151–157.

[23] R. Watson, G. C. Hua, and F. C. Lee, "Characterization of an active clamp flyback topology for power factor correction applications," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 191–198, Jan. 1996.

[24] H. P. Yee and D. Liu, "An ASIC to control the paralleling of an IGBT with a MOSFET," in *Proc. Appl. Power Electron. Conf.*, Atlanta, GA, 1997, vol. 1, pp. 151–155.

[25] J. W. Kimball and P. L. Chapman, "Evaluating conduction loss of a parallel IGBT-MOSFET combination," in *Proc. Conf. Rec. 2004 IEEE Ind. Appl. Conf., 39th IAS Annu. Meeting*, 2004, vol. 2, pp. 1233–1237.

[26] K. F. Hoffmann and J. P. Karst, "High frequency power switch - improved performance by MOSFETs and IGBTs connected in parallel," in *Proc. Eur. Conf. Power Electron. Appl.*, Dresden, 2005, p. 11.

[27] G. Ortiz, C. Gammeter, J. W. Kolar, and O. Apeldoorn, "Mixed MOSFET-IGBT bridge for high-efficient medium-frequency dual-active-bridge converter in solid state transformers," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, Salt Lake City, UT, 2013, pp. 1–8.

[28] J.-S. Lai *et al.*, "A hybrid-switch-based soft-switching inverter for ultrahigh-efficiency traction motor drives," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1966–1973, May/Jun. 2014.

[29] J. Reichl, J. S. Lai, A. Hefner, J. M. Ortiz-Rodríguez, and T. Duong, "Design optimization of hybrid-switch soft-switching inverters using multiscale electrothermal simulation," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 503–514, Jan. 2017.

[30] M. Rahimo *et al.*, "Characterization of a silicon IGBT and silicon carbide MOSFET cross-switch hybrid," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4638–4642, Sep. 2015.

[31] U. R. Vemulapati, A. Mihaila, R. A. Minamisawa, F. Canales, M. Rahimo, and C. Papadopoulos, "Simulation and experimental results of 3.3 kV cross switch "Si-IGBT and SiC-MOSFET" hybrid," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, Prague, 2016, pp. 163–166.

[32] R. A. Minamisawa, U. Vemulapati, A. Mihaila, C. Papadopoulos, and M. Rahimo, "Current sharing behavior in Si IGBT and SiC MOSFET cross-switch hybrid," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1178–1180, Sep. 2016.

[33] W. Zhang, S. Anwar, D. J. Costinett, and F. Wang, "Investigation of cost-effective sic based hybrid switch and improved inductor design procedure for boost converter in electrical vehicles application," in *Proc. SAE 2015 World Congr. Exhib. Conf.*, 2015, pp. 1–9.

[34] A. Deshpande, Y. Chen, B. Narayanasamy, A. S. Sathyanarayanan, and F. Luo, "A three-level, T-type, power electronics building block using Si-SiC hybrid switch for high-speed drives," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, 2018, pp. 2609–2616.

[35] T. Zhao and J. He, "An optimal switching pattern for "SiC+Si" hybrid device based voltage source converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, 2015, pp. 1276–1281.

[36] J. He, R. Katebi, and N. Weise, "A current-dependent switching strategy for Si/SiC hybrid switch-based power converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8344–8352, Oct. 2017.

[37] Y. Wang, N. Zhu, C. Yan, and D. Xu, "Efficiency improvement of 2- and 3-level inverters for distributed photovoltaic application using hybrid devices," in *Proc. IEEE 2nd Int. Future Energy Electron. Conf.*, Taipei, 2015, pp. 1–7.

[38] Z. Li *et al.*, "Optimal control strategies for SiC MOSFET and Si IGBT based hybrid switch," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, 2018, pp. 1717–1721.

[39] A. Q. Huang, X. Song, and L. Zhang, "6.5 kV Si/SiC hybrid power module: An ideal next step?," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Chicago, IL, 2015, pp. 64–67.

[40] X. Song and A. Q. Huang, "6.5 kV FREEDM-Pair: Ideal high power switch capitalizing on Si and SiC," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, 2015, pp. 1–9.

[41] A. Deshpande and F. Luo, "Design of a silicon-WBG hybrid switch," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, Blacksburg, VA, 2015, pp. 296–299.

[42] A. Deshpande and F. Luo, "Comprehensive evaluation of a silicon-WBG hybrid switch," in *Proc. IEEE Energy Convers. Congr. Expo.*, Milwaukee, WI, 2016, pp. 1–8.

[43] A. Deshpande and F. Luo, "Practical design considerations for a Si IGBT + SiC MOSFET hybrid switch: Parasitic interconnect influences, cost and current ratio optimization," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2018.2827989.

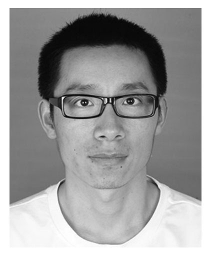
[44] J. Wang, Z. Li, X. Jiang, C. Zeng, and J. Shen, "Gate control optimization of Si/SiC hybrid switch for junction temperature balance and power loss reduction," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2018.2829624.

[45] C. Xiao, L. Zhao, T. Asada, W. G. Odendaal, and J. D. van Wyk, "An overview of integratable current sensor technologies," in *Proc. 38th IAS Annu. Meeting Conf. Rec. Ind. Appl. Conf.*, 2003, vol. 2, pp. 1251–1258.

[46] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich, and P. Mattavelli, "Evaluation of the switching characteristics of a gallium-nitride transistor," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, 2011, pp. 2681–2688.

[47] J. C. Hernandez, L. P. Petersen, M. A. E. Andersen, and N. H. Petersen, "Ultrafast switching superjunction MOSFETs for single phase PFC applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, 2014, pp. 143–149.

[48] J. A. Ferreira, W. A. Cronje, and W. A. Relihan, "Integration of high frequency current shunts in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 10, no. 1, pp. 32–37, Jan. 1995.



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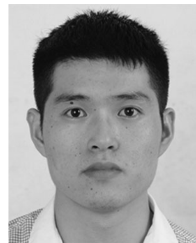

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