An Integrated Control and Protection Scheme to Inhibit Blackouts Caused by Cascading Fault in Large-Scale Hybrid AC/DC Power Grids

Sohrab Mirsaeidi, *Member, IEEE*, and Xinzhou Dong, *Fellow, IEEE*

***Abstract*—Cascading fault is one of the serious challenges in hybrid ac/dc power grids, which initiates from a dc or a severe inverter ac fault and leads to a blackout in the inverter ac side. However, owing to the fact that dc faults do not cause commutation failure, the existing commutation failure inhibition approaches are not effective in the prevention of cascading faults caused by dc fault. In order to resolve the challenge, this paper first develops a hybrid ac/dc relay (HADR) based on the positive-sequence component, which can detect and locate the fault events in hybrid ac/dc networks. Subsequently, an integrated control and protection scheme is presented using the developed HADR and a thyristor-controlled series compensator. The proposed scheme has the ability to prevent the blackouts caused by cascading fault using transmission capacity enhancement of the ac line and load-shedding in the inverter ac system. The salient feature of the proposed scheme is that it provides a very economical way to compensate for the loss of power caused by HVdc line outage. In addition, it does not require communications among the relays. The practical performance and feasibility of the proposed scheme is validated by laboratory testing, using the real-time Opal-RT hardware prototyping platform. The experimental results demonstrate that the proposed strategy can effectively inhibit the blackouts caused by cascading fault in hybrid ac/dc networks.**

***Index Terms*—Cascading fault, commutation failure, hybrid ac/dc power grids, integrated control and protection scheme.**

I. Introduction

HVDC transmission systems have increasingly been used in modern power transmission networks due to their numerous advantages such as providing higher power transmission capacity over long distances, and interconnecting asynchronous systems [1]–[4]. For example, in China, where generation and load centers are distributed unevenly, line-commutated converter based HVdc systems have been extensively applied for

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The strategies can be broadly classified into two categories: 1) by using modification of controllers and 2) by adding additional components or devices.

For the controller modification methods, it has been identified in the literature that commutation failure cannot be completely avoided if the fault is electrically close to the inverter [12], [13]. Hence, the objectives of these modifications are either to reduce the probability of commutation failure or to increase the recovery speed of dc system after commutation failure. In [14]–[18], voltage dependent current order limit method is proposed to protect the HVdc system by limiting the current order according to the ac voltage or dc voltage. Although this method has been widely adopted, dc current variation is not reflected in its performance and there is some room for improvement. Another approach is to advance the firing angle at inverter side immediately after the detection of ac voltage disturbance in order to give a larger commutation margin [11], [19]. However, the control system is not able to react if a serious fault occurs at the beginning or during the process of commutation. Moreover, the advancement of firing angle leads to increased reactive power consumption, which will further depress the inverter ac bus voltage, particularly in weak ac systems. Therefore, it is necessary to increase the extinction angle by a suitable amount.

Among the methods with addition of other components or devices, the most commonly used one is to add static VAR compensator (SVC) or static compensator (STATCOM) at the inverter ac side for dynamic reactive power support to regulate the ac voltage. However, the effectiveness of SVC in mitigating commutation failure is limited due to its relatively slow response time. The rapid control of STATCOM certainly gives some improvements, but it cannot be very useful under low impedance ground faults at the inverter ac bus [20]. Deployment of capacitor-commutated converter HVDC (CCC-HVDC) is another approach that reduces reactive power consumption using a series capacitor between the thyristor valves and the converter transformer [21]–[23]. Therefore, the commutation failure can be mitigated because the extinction angle margin is increased under normal operation. However, CCC-HVDC causes excessive voltage stress on thyristor valves [24], thus reducing the device lifetime.

Even though the above-mentioned strategies can effectively prevent the cascading faults caused by the inverter ac fault, they are not able to inhibit cascading faults resulting from dc fault since short-circuit on the dc line does not cause any commutation failure. Some feasible solutions for the prevention of blackouts caused by either dc fault or inverter ac fault are as follows.

1) Load-shedding of the inverter ac system corresponding to the HVdc line capacity before HVdc block. However, it still leads to a wide-scale power outage due to the large capacity of the HVdc line.
2) To increase the number of parallel ac lines to compensate for the loss of HVdc transmission power, but the installation of several backup ac lines requires significant investment.
3) To decrease the transmitted power by HVdc line so that the parallel ac line can compensate for the HVdc line outage without overload. Even though this strategy is not costly, deployment of an HVdc line with a power less than its nominal capacity is not economical.

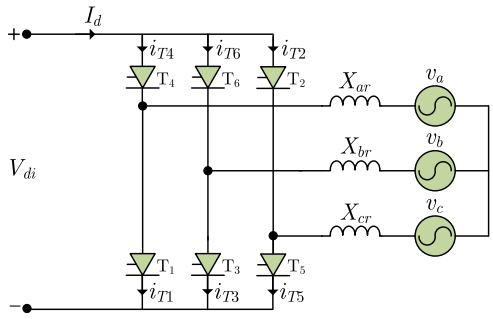

Fig. 1. Graetz bridge.

In this paper, an integrated control and protection strategy for hybrid ac/dc grids is proposed, which provides a very economical way to compensate for the loss of power caused by HVdc line outage without the need for wide-scale load-shedding, increasing the number of parallel ac lines, or reducing the transmitted power by the HVdc line.

The remainder of this paper is organized as follows. In Section II, concepts of commutation failure and cascading fault are described; in Section III, the structure of the proposed hybrid ac/dc relay (HADR) is discussed in detail; in Section IV, an integrated control and protection scheme is proposed to inhibit the blackouts caused by cascading fault; in Section V, the performance of the proposed scheme is tested under real-time conditions; finally, Section VI concludes this paper.

II. Commutation Failure and Cascading Fault

A. Commutation Failure

Fig. 1 depicts the basic structure of HVdc converter, which is known as Graetz bridge. This structure has been widely used in HVdc converters since it offers better utilization of the converter transformer and lower voltage across the non-conducting valve [19], [25]. As can be seen from the figure, it consists of six thyristor valves, $\mathrm{T}_1 \sim \mathrm{T}_6$, which are deployed for power transmission in two directions by applying different firing angles to the valves. The valves are turned ON and OFF in order, $X_{kr}(k = a, b, c)$ is the commutation reactance of each phase, and ω is the system frequency in radian. During the commutation process from valve T_1 to valve T_3, the voltage equation can be expressed as follows:

$$v_b - X_{br}\frac{\mathrm{d}i_{T3}}{\mathrm{d}\omega t} = v_a - X_{ar}\frac{\mathrm{d}i_{T1}}{\mathrm{d}\omega t} \tag{1}$$

where i_{T1} and i_{T3} are currents flowing through valves T_1 and T_3, respectively. Considering $i_{T1} = I_d - i_{T3}$ where I_d represents the transient dc current, (1) can be written as follows:

$$(X_{ar} + X_{br})\frac{\mathrm{d}i_{T3}}{\mathrm{d}\omega t} = v_b - v_a + X_{ar}\frac{\mathrm{d}I_d}{\mathrm{d}\omega t}. \tag{2}$$

Considering $X_{ar} = X_{br} = X_r$, and $\mathrm{d}I_d/\mathrm{d}\omega t = 0$, the process of commutation can be described by the following

equation:

$$\int_0^{I_d} 2X_r \mathrm{d}i_{T3} = \int_\alpha^{\pi-\gamma} (v_b - v_a)\,\mathrm{d}\omega t \tag{3}$$

where α and γ are the firing angle and extinction angle, respectively, and v_{ba} $(= v_b - v_a)$ is the commutating voltage. Therefore, (3) can be written as follows:

$$I_d = \frac{\sqrt{2}V_{\mathrm{LL}}}{2X_r}(\cos\alpha + \cos\gamma) \tag{4}$$

where V_{LL} is the rms line-to-line ac voltage. When a fault occurs at the ac side of the inverter, dc voltage decreases, which results in the increase of I_d. Since the overlap angle, μ, is directly proportional to the dc current, it also increases, which leads to the reduction of extinction angle. When γ drops below the thyristor turn-OFF time, leading to the unexpected turn-ON of a thyristor supposed to be off, a commutation failure occurs. It creates a short-circuit on the dc link, and if it repeats for several times or lasts for a long time, it results in the forced shutdown of the link [11].

B. Cascading Fault

Fault events in a hybrid ac/dc power grid, connecting the rectifier ac system to the inverter ac system through an HVdc link paralleled with an ac line, are of two types, ac and dc. Depending on the fault location, the ac faults can be divided into three categories, i.e., 1) inverter ac side; 2) rectifier ac side; and 3) parallel ac line. In such a hybrid grid, the transmitted power from the rectifier ac system to the inverter ac system is shared between the HVdc link and its paralleled ac line. However, the transmission capacity of the HVdc system is much higher than that of the ac line. Transmission of such a large amount of electric power by the HVdc link can only be accomplished under tightly controlled conditions. In a two-terminal HVdc system, each of rectifier and inverter stations has its own control system. Under steady-state conditions, rectifier and inverter control systems, respectively, operate in constant control (CC) and constant extinction angle (CEA) modes.

In response to a rectifier ac fault, the inverter control system switches to the CC mode and the rectifier is, therefore, forced to operate in the min-α mode. Hence, a rectifier ac fault does not pose a serious problem in the network operation.

Instead, an inverter ac fault causing a voltage depression of more than 10% at the inverter ac bus, leads to commutation failure. If the fault is not so severe or does not last for a long time, voltage dependent current order limiter (VDCOL) in the HVdc control system is triggered during the fault to safeguard the converter valves. Also, immediately after the fault is removed, VDCOL gradually increases the dc current according to its characteristic, which contributes to the recovery of the inverter station after the commutation failure. However, a severe inverter ac fault may result in repetitive commutation failures in the inverter station. In such a case, if the fault was not cleared in less than 500 ms [26], the HVdc link shuts down due to the forced blocking of the converter, and the large amount of power transmitted by HVdc line is transferred to its paralleled ac line with a lower transmission capacity. Thus, the ac line overload protection trips and a cascading fault occurs, which leads to the blackout of the inverter ac side.

In the case of a fault on the parallel ac line, its effect on the network behavior is highly dependent on the location of the fault. It means, if the fault happens close to the inverter station, it influences the network similar to the inverter ac fault, whereas if the fault occurs in the vicinity of the rectifier station, it has the same behavior with the rectifier ac fault. Nevertheless, in both cases, apart from the location of fault or response of the HVdc control system to the fault, the ac line protection must immediately trip to isolate the fault from the rest of the network. However, since the power flow of dc line is controlled, no overload occurs on the HVdc link and it continues its operation.

When a fault occurs on the HVdc link, the protection of dc line trips, but in this case, after disconnection of the HVdc link and fault clearance, the power flow is transferred to the parallel ac line, which causes its overload protection to take action. Consequently, a cascading fault occurs, which leads to the blackout of the inverter ac side.

With regard to the analyzed cases above, only faults at the inverter ac side or on the HVdc link lead to the cascading fault and blackout in the network. However, commutation failure does not occur in the dc fault case; hence, commutation failure inhibition approaches are not effective in the prevention of blackouts resulting from dc fault, and some alternative approaches should be devised.

III. Developed HADR

In order to detect and locate the fault events in a hybrid ac/dc power grid, this paper develops a relay based on the positive-sequence component, which hereinafter is referred to as HADR. The proposed HADR consists of two main parts, i.e., 1) fault incident detector and 2) fault locater, which are discussed in detail in the following sections.

A. Fault Incident Detector

When a fault occurs in a hybrid ac/dc system, different symmetrical components, i.e., positive-sequence, negative-sequence, and zero-sequence, may appear depending on the fault type. However, the positive-sequence component is the only one that appears in all types of faults [27]. Moreover, depending on the fault severity, the value of Thevenin's impedance at the location of relays decreases after the fault. Hence, in the developed HADR, the fault incident detector makes use of the comparison between pre-fault and post-fault values of Thevenin's equivalent positive-sequence impedance (TEPSI) as a criterion for the detection of various types of faults with different fault impedances. In order to determine the value of TEPSI seen by the HADR, the fault incident detector applies an online methodology using three consecutive voltage and current measurements of a phasor measurement unit (PMU) at different time instants.

Based on Thevenin's theorem, the positive-sequence voltage equation at each node of the network can be defined as follows:

$$V_1 = E_{t1} - Z_{t1} I_1. \tag{5}$$

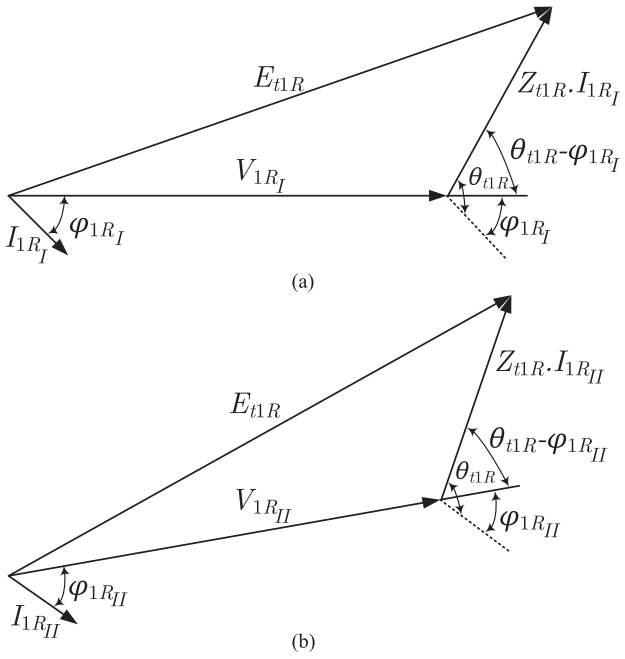

Fig. 2. Phasor diagrams for two PMU measurements at different time instants at the HADR location. (a) First measurement. (b) Second measurement.

Hence, the positive-sequence voltage equation at the HADR location becomes the following:

$$V_{1R} = E_{t1R} - Z_{t1R} I_{1R} \tag{6}$$

where E_{t1R} and Z_{t1R} represent Thevenin's equivalent positive-sequence voltage source and TEPSI seen from the HADR, respectively. The phasor diagrams of two (V_{1R}, I_{1R}) pairs measured at different time instants by the PMU are displayed in Fig. 2. Since E_{t1R} is the Thevenin's equivalent positive-sequence voltage source seen from the HADR, its magnitude for both measurements are identical. However, its angle in the second measurement is shifted by an angle equal to the phase drift due to the variations in the system frequency.

With reference to Fig. 2, the equation of E_{t1R} for the first measurement is expressed as follows:

$$E_{t1R}^2 = V_{1R_I}^2 + I_{1R_I}^2 Z_{t1R}^2 + 2V_{1R_I} I_{1R_I} \times Z_{t1R} \cos(\theta_{t1R} - \phi_{1R_I}). \tag{7}$$

By expanding $\cos(\theta_{t1R} - \phi_{1R_I}) = \cos\theta_{t1R}\cos\phi_{1R_I} + \sin\theta_{t1R}\sin\phi_{1R_I}$, and substituting $\cos\theta_{t1R} = \frac{R_{t1R}}{Z_{t1R}}$, $\sin\theta_{t1R} = \frac{X_{t1R}}{Z_{t1R}}$, $\cos\phi_{1R_I} = \frac{P_{1R_I}}{V_{1R_I} I_{1R_I}}$, and $\sin\phi_{1R_I} = \frac{Q_{1R_I}}{V_{1R_I} I_{1R_I}}$, (7) can be written as follows:

$$E_{t1R}^2 = V_{1R_I}^2 + I_{1R_I}^2 Z_{t1R}^2 + 2P_{1R_I} R_{t1R} + 2Q_{1R_I} X_{t1R} \tag{8}$$

where, R_{t1R}, X_{t1R}, P_{1R_I}, and Q_{1R_I} represent Thevenin's equivalent positive-sequence resistance and reactance, active power, and reactive power at the HADR location, respectively.

By following the same procedure, the equation of E_{t1R} for the second measurement can be expressed as follows:

$$E_{t1R}^2 = V_{1R_{II}}^2 + I_{1R_{II}}^2 Z_{t1R}^2 + 2P_{1R_{II}} R_{t1R} + 2Q_{1R_{II}} X_{t1R}. \tag{9}$$

By subtracting (9) from (8), we have the following:

$$V_{1R_I}^2 - V_{1R_{II}}^2 + (I_{1R_I}^2 - I_{1R_{II}}^2) Z_{t1R}^2 + 2(P_{1R_I} - P_{1R_{II}}) R_{t1R} + 2(Q_{1R_I} - Q_{1R_{II}}) X_{t1R}. \tag{10}$$

By substituting $Z_{t1R} = \sqrt{R_{t1R}^2 + X_{t1R}^2}$ and arranging (10), we have the following:

$$\left(R_{t1R} + \frac{P_{1R_I} - P_{1R_{II}}}{I_{1R_I}^2 - I_{1R_{II}}^2}\right)^2 + \left(X_{t1R} + \frac{Q_{1R_I} - Q_{1R_{II}}}{I_{1R_I}^2 - I_{1R_{II}}^2}\right)^2 = \frac{V_{1R_{II}}^2 - V_{1R_I}^2}{I_{1R_I}^2 - I_{1R_{II}}^2} + \left(\frac{P_{1R_I} - P_{1R_{II}}}{I_{1R_I}^2 - I_{1R_{II}}^2}\right)^2 + \left(\frac{Q_{1R_I} - Q_{1R_{II}}}{I_{1R_I}^2 - I_{1R_{II}}^2}\right)^2. \tag{11}$$

This is the equation of a circle with radius

$$r_{I,II} = \sqrt{\frac{V_{1R_{II}}^2 - V_{1R_I}^2}{I_{1R_I}^2 - I_{1R_{II}}^2} + \left(\frac{P_{1R_I} - P_{1R_{II}}}{I_{1R_I}^2 - I_{1R_{II}}^2}\right)^2 + \left(\frac{Q_{1R_I} - Q_{1R_{II}}}{I_{1R_I}^2 - I_{1R_{II}}^2}\right)^2}$$

centered at $O_{I,II} = \left(\frac{P_{1R_{II}} - P_{1R_I}}{I_{1R_I}^2 - I_{1R_{II}}^2}, \frac{Q_{1R_{II}} - Q_{1R_I}}{I_{1R_I}^2 - I_{1R_{II}}^2}\right)$ in the impedance plane, which specifies a locus for TEPSI seen from the HADR. However, (11), which is obtained by two (V_{1R}, I_{1R}) pairs measured at different time instants, cannot determine a certain value for Z_{t1R}. Hence, another measurement is required to be used with the first and second measurements to create two other circles for Z_{t1R}. The intersection of these three circles specifies a certain value for Z_{t1R}. By comparing the pre-fault and post-fault values of Z_{t1R} ($Z_{t1R,\text{pre}}$ and $Z_{t1R,\text{post}}$), the HADR can detect the fault incidence. However, since a fault in the network decreases $Z_{t1R,\text{post}}$ seen by all HADRs, deployment of an additional detector (fault locater) is necessary for location of the fault.

B. Fault Locater

In the developed HADR, the fault location is detected by the fault locater, which applies the superposition principle in the positive-sequence network. According to the superposition theorem, the positive-sequence network after a fault can be decomposed into "pre-fault" and "pure-fault" networks as illustrated in Fig. 3. In this figure, E_{U1} and E_{D1}, respectively, represent the upstream and downstream equivalent positive-sequence voltage sources; Z_{U1} and Z_{D1} denote the upstream and downstream equivalent positive-sequence impedances, respectively; Z_{L1} is the positive-sequence impedance of the transmission line; m and n denote distance parameters.

ΔV_{1R} and ΔI_{1R} in the pure-fault network in Fig. 3 are the incremental positive-sequence voltage and current signals seen at the HADR location, which are caused by the application of faults in the network. These incremental quantities are measured by subtracting the pre-fault signals ($V_{1R,\text{pre}}$ and $I_{1R,\text{pre}}$) at the HADR location from the corresponding post-fault signals ($V_{1R,\text{post}}$ and $I_{1R,\text{post}}$). Under normal conditions, the incremental signals are zero. When a fault occurs in the network, the incremental signals become non-zero and the direction of the fault can be recognized using phasor $\Delta Z_{1R} = \Delta V_{1R}/\Delta I_{1R}$. To be

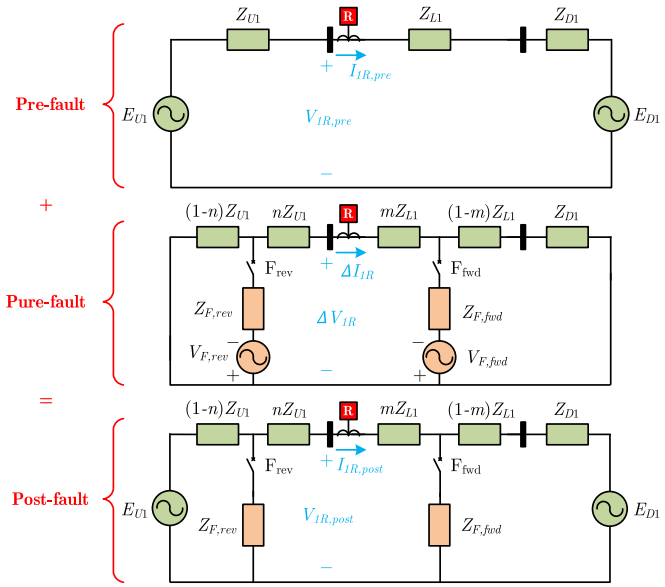

Fig. 3. Decomposition of the positive-sequence network after the fault into "pre-fault" and "pure-fault" networks.

more precise, in the case of forward fault $\mathrm{F_{fwd}}$, phasor ΔZ_{1R} is calculated using the voltage equation in the upstream loop of the HADR. Since the voltage source E_{U1} is short-circuited in the pure-fault network, $\Delta Z_{1R} = -Z_{U1}$, which lies in the third quadrant of the positive-sequence impedance plane, and the HADR will judge it as forward fault; whereas, during reverse fault $\mathrm{F_{rev}}$, $\Delta Z_{1R} = Z_{D1} + Z_{L1}$, which is calculated using the voltage equation in the downstream loop of the HADR. As a result, phasor ΔZ_{1R} lies in the first quadrant of the impedance plane and it will be judged as reverse fault.

IV. Proposed Integrated Control and Protection Scheme

Fig. 4 depicts the single-line diagram of a hybrid ac/dc network including a mono-polar 500-kV and 400-MW HVdc link paralleled with a 230-kV and 100-MW ac line, which hereinafter is referred to as "study network." The study network connects the ac system in the rectifier side to five identical ac systems in the inverter side, each of which receives a power of 100 MW. The HVdc link includes 12-pulse converters, ac filters, and shunt capacitors in both rectifier and inverter sides. The dc line and its parallel ac line are, respectively, modeled by the lumped T and Pi circuits, including both series impedances and shunt admittances. The parameters of the study network are listed in Table I.

As discussed in Section II-B, cascading fault is caused by a DC or a severe inverter AC fault which leads to the power flow transfer to the parallel AC line and results in a blackout in the inverter AC side. However, due to the fact that DC faults do not cause commutation failure, the existing commutation failure inhibition approaches are not effective in prevention of cascading faults caused by DC fault. In order to resolve the challenge, this paper proposes an integrated control and protection scheme using the developed HADR and a Flexible Alternating Current Transmission System (FACTS) device. The proposed scheme provides an economical way to prevent the blackout in the inverter AC side through transmission capacity enhancement of the AC line and load-shedding in the inverter AC system.

It should be noted that there are different types of FACTS devices including series, shunt, and combined series and shunt controllers, each of which is suitable for a specific application. Series controller impacts the driving voltage, and hence the current and power flow directly. Hence, if the purpose of deploying FACTS device is to control the power flow and damp oscillations, the series controller is several times more powerful than the shunt controller [28], [29]. However, the shunt controller behaves like a current source, which draws from or injects current into the line. Therefore, application of the shunt controller is a good way to control voltage at and around the point of connection through injection of reactive current (leading or lagging) alone, or a combination of active and reactive currents for a more effective voltage control and damping of voltage oscillations [28]. Even though the combined series and shunt controllers such as unified power flow controller have better performance, they are costlier than the series or shunt controllers, as identified in [30]. As a result, in this paper, thyristor controlled series compensator (TCSC) has been used for power flow control.

Fig. 5 shows the structure of a TCSC module. TCSC is a series controlled capacitive reactance, which can provide continuous control of power on the ac line over a wide range [31]. The behavior of the TCSC can be analyzed similar to that of a variable inductor connected in parallel with a fixed capacitor. The equivalent impedance Z_{eq} of this *LC* combination is expressed as follows:

$$Z_{\mathrm{eq}} = \left(j\frac{1}{\omega C}\right) \Big\| (j\omega L) = \frac{-j}{\omega C - \frac{1}{\omega L}}. \tag{12}$$

If $\omega C - \frac{1}{\omega L} > 0$, the reactance of the capacitor is less than that of the parallel-connected variable reactor, and hence the *LC* combination provides a variable-capacitive reactance, while if $\omega C - \frac{1}{\omega L} < 0$, it provides a variable-inductive reactance. There are three modes of the TCSC operation as follows.

1) By-passed thyristor mode: In this mode, the thyristors are made to fully conduct with a conduction angle of 180°. Gate pulses are applied as soon as the voltage across the thyristors reaches zero and becomes positive, resulting in a continuous sinusoidal of flow current through the thyristors valves. As a result, the TCSC module behaves like a parallel *LC* combination in this mode. However, the net current through the module is inductive, since the susceptance of the reactor is greater than that of the capacitor.
2) Blocked thyristor mode: In this mode, the firing pulses to the thyristor valves are blocked, and thus the TCSC module is reduced to a fixed-series capacitor, and the net TCSC reactance is capacitive.
3) Partially conducting thyristor or Vernier mode: This mode allows the TCSC to behave either as a continuously controllable capacitive reactance (referred to as capacitive-Vernier mode) or as a continuously controllable inductive

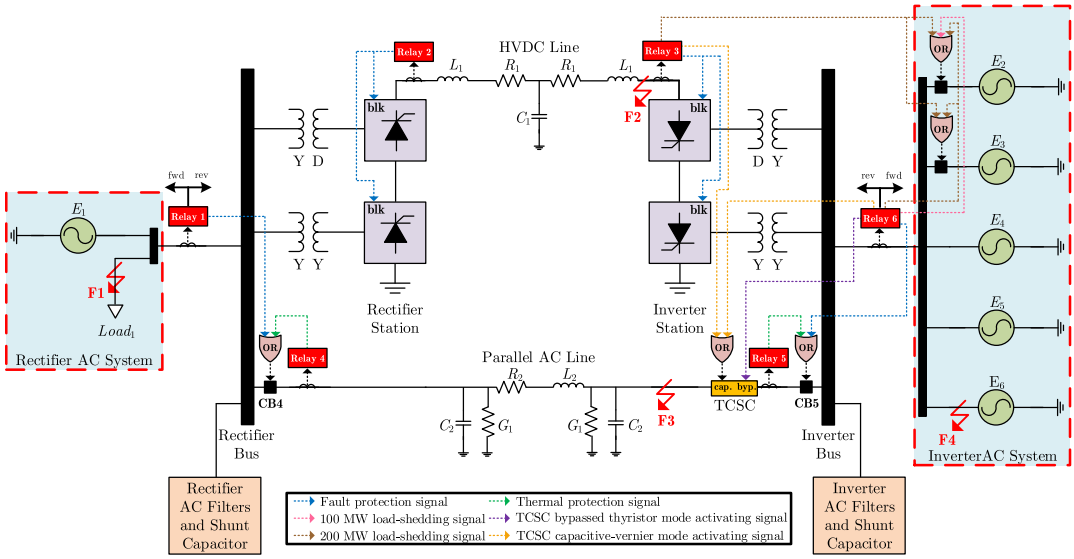

Fig. 4. Single-line diagram of the study network.

TABLE I
DETAILED PARAMETERS OF THE STUDY NETWORK

Network parameters	$Load_1$	100 MW + j30 Mvar
	R_1 and R_2	$R_1 = 2.5\ \Omega$, $R_2 = 43.31\ \Omega$
	L_1 and L_2	$L_1 = 0.5968$ H, $L_2 = 0.766$ H
	C_1 and C_2	$C_1 = 26\ \mu$F, $C_2 = 3\ \mu$F
	G_1	55.5 μS
Parameters of HVDC converters	Nominal firing angle in rectifier	15 deg
	Nominal extinction angle in inverter	15 deg
	Turn-off time of thyristor	30 μs
Parameters of TCSC	L	10 mH
	C	17.63 μF

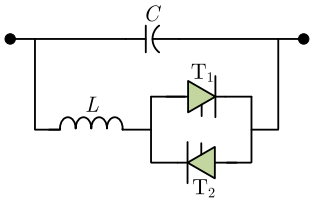

Fig. 5. Structure of a TCSC module.

reactance (referred to as inductive-Vernier mode), which is achieved by varying the thyristor-pair firing angle in an appropriate range.

In the proposed scheme, it is assumed that the TCSC module operates in the by-passed thyristor mode under normal conditions. Immediately after the occurrence of a primary dc or a severe inverter ac fault, it is transferred to the capacitive-Vernier mode to enable the parallel ac line to carry the power closer to its thermal rating. It should be noted that the parameters of the TCSC module are selected corresponding to the parameters of the parallel ac line so that the maximum of 75% percent series compensation is provided [32]. However, owing to the very large transmission capacity of the HVdc line in comparison with the ac line, the deployment of the TCSC module is not sufficient to compensate for the power loss resulting from the HVdc outage, and applying some load-shedding schemes in the inverter ac system would be necessary. It should be noted that the HVdc link in the study network shown in Fig. 4 is mono polar and it is paralleled with only one ac line so that the proposed scheme is validated under the worst conditions, in which the maximum contribution of the TCSC is required. However, in reality, for example in China, the majority of the HVdc links are bi-polar and are paralleled with at least two ac lines. Deployment of more compensated ac lines and the non-blocked HVdc pole not only reduces the contribution of the TCSC on each ac line, but also eliminates the need for load-shedding in the inverter ac system.

Protection of the study network is provided by Relays 1–6, as illustrated in Fig. 4. Since the failure of communication links in a network leaves the network unprotected, in the proposed scheme no communication link is considered among the relays. It is also assumed that the relays have the ability to detect the fault within half a cycle. Relays 2 and 3 are used to protect the dc line; Relays 1 and 6 are of the HADR type, which are able to recognize the occurrence and direction of fault; also, overload protection of the ac line is replaced by thermal Relays 4 and 5, which trip once the temperature of the ac line exceeded its thermal limit for a pre-specified period of time.

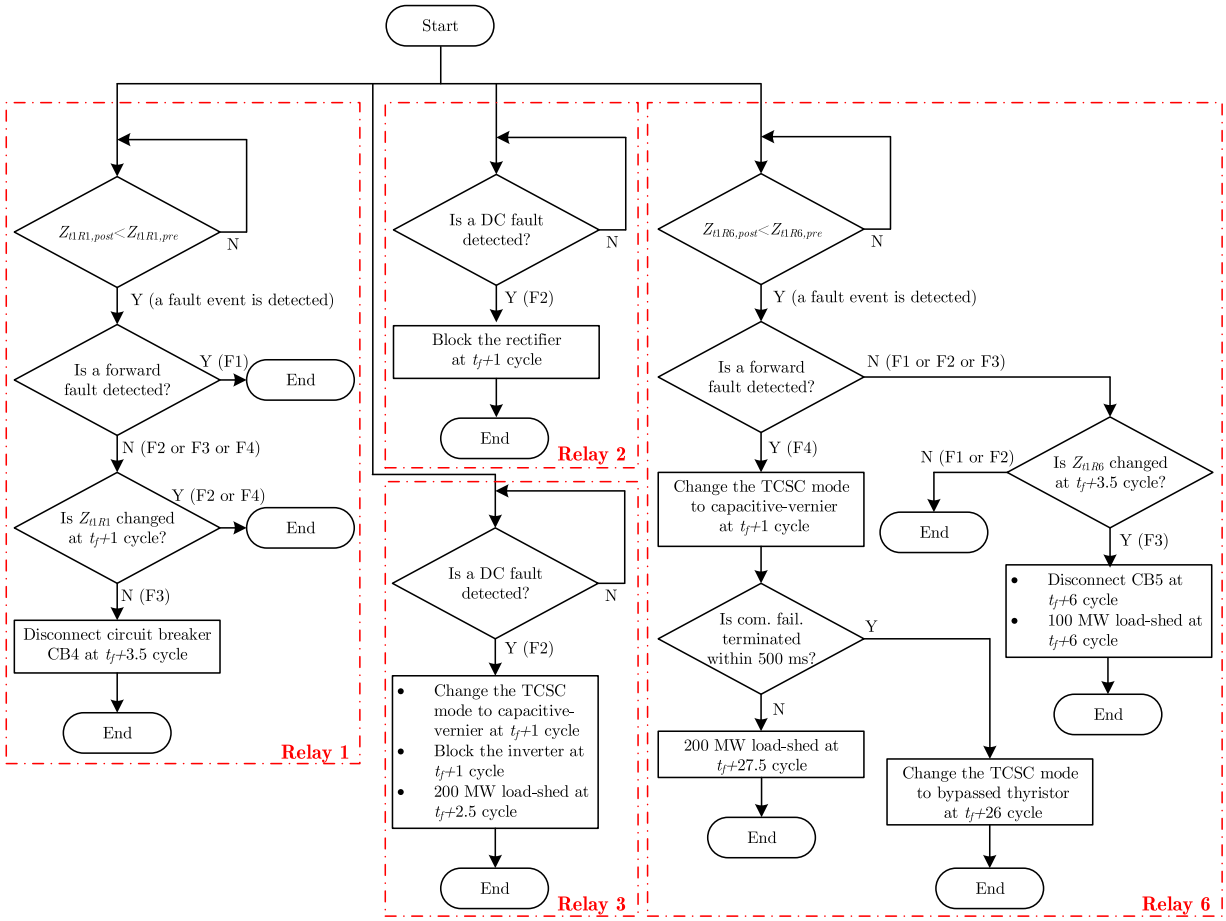

Fig. 6. Flowchart of the proposed integrated control and protection scheme for the study network shown in Fig. 4.

Fig. 6 demonstrates the flowchart of the proposed integrated control and protection scheme for the study network shown in Fig. 4. As can be seen from the figure, all the relays operate independently, since there is no communication link among them. However, in the proposed scheme, each relay can become aware of other relays' status by checking their performance. Since such a coordination among the relays may be time consuming, the proposed scheme is designed in such a way that faults are isolated from the rest of the network in less than the critical fault clearing time, which is typically six cycles [33].

With reference to Fig. 6, once a fault occurs in the study network, each of Relays 1, 2, 3, and 6 detects the fault occurrence and records its initiation time independently. In the case of a fault on the dc line (F2), since it will cause cascading fault, Relays 2 and 3, respectively, block the rectifier and inverter after one cycle (half-cycle for detection of fault and half-cycle for blocking the converters). Simultaneously, the TCSC is also switched to the capacitive-Vernier mode by Relay 3 (TCSC mode change from the by-passed thyristor to the capacitive-Vernier takes less than half-cycle [31]) to increase the transmission capacity of the ac line. However, with regard to the ac line thermal limit, the capacitive-Vernier mode of the TCSC can only compensate for the half of HVdc capacity. Hence, Relay 3 also issues a 200-MW load-shedding signal for the inverter ac system.

In Relays 1 and 6, which are of the HADR type, first the values of pre-fault and post-fault Z_{t1R} ($Z_{t1R,\text{pre}}$ and $Z_{t1R,\text{post}}$) are compared with each other by their fault incident detectors. If a fault incident was detected, then their fault locaters recognize the direction of the fault. If Relay 6 detected a forward fault, since an inverter ac fault may lead to cascading fault, it switches the TCSC from the by-passed thyristor mode to the capacitive-Vernier mode after one cycle (at $t_f + 1$ cycle). Since there is no communication link between Relays 1 with Relays 2, 3, and 6, Relay 1 makes decision based on the performance of these relays. Accordingly, if Relay 1 detected a reverse fault but did not recognize any change in the value of Z_{t1R1} at $t_f + 1$ cycle (resulting from the TCSC mode change at one cycle after the fault), then it makes sure that the fault has occurred on the parallel ac line, and thus issues a disconnection command to circuit breaker CB4. Considering two cycles for the operation of circuit breakers [34], the ac line is disconnected from its upstream side at $t_f + 3.5$ cycle. After that, Relay 6 also makes decision based on the performance of Relay 1. Therefore, if Relay 6 detects a reverse fault and also recognizes a change in the value of Z_{t1R6} at $t_f + 3.5$ cycle (resulting from disconnection of circuit breaker CB4), then it disconnects circuit breaker CB5 to isolate the faulted ac line from the rest of the network. However, since the power flow of the dc line is controlled, the power flow is not transferred to the dc line. Hence, Relay 6 also issues a 100-MW

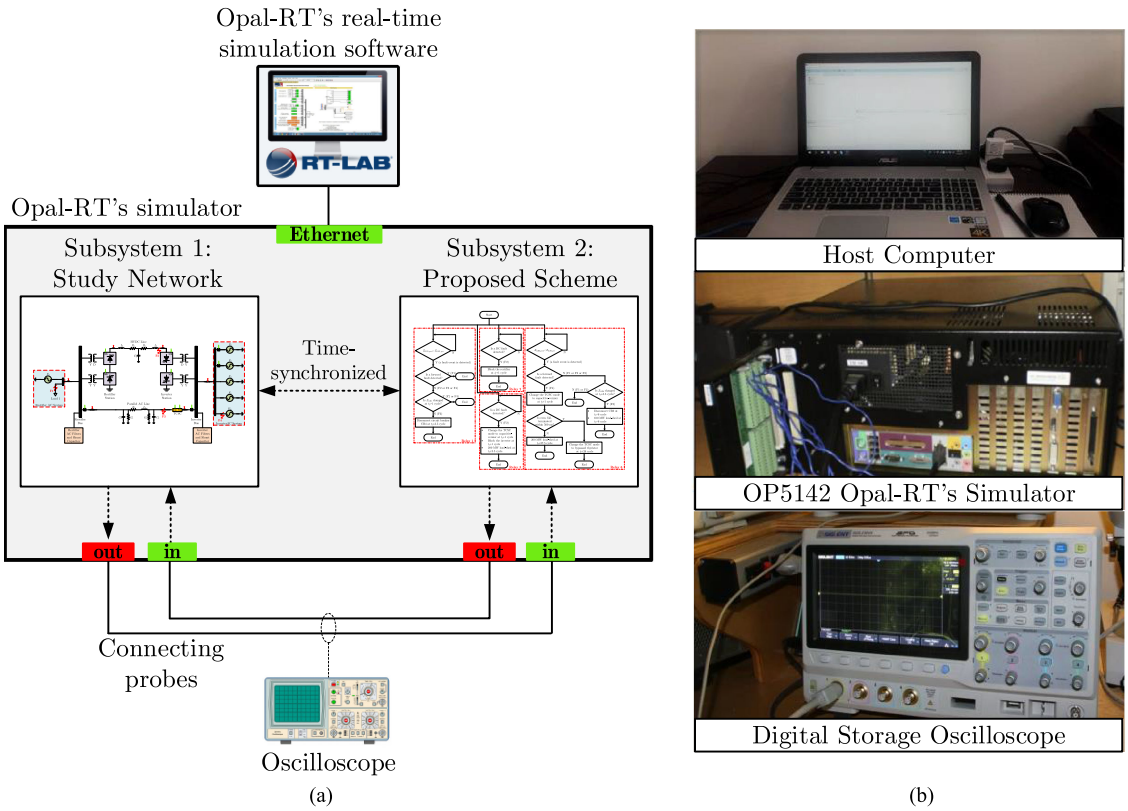

Fig. 7. (a) Experimental setup. (b) Experimental arrangement.

load-shedding signal for the inverter ac system. As mentioned above, once Relay 6 recognizes a forward fault, it changes the TCSC mode to the capacitive-Vernier mode to prepare it for the cascading fault caused by inverter ac fault. However, if the recognized forward fault by Relay 6 is not so severe or does not last more than 500 ms, then the HVdc converters are not blocked and no cascading fault occurs. Hence, the TCSC is switched back to the bypassed thyristor mode once the fault is cleared within 500 ms. Otherwise, the TCSC ensures that the occurred fault will lead to a cascading fault, and hence Relay 6 issues a 200-MW load-shedding signal for the inverter ac system at $t_f + 27.5$ cycle.

V. Experimental Validation

In order to validate the performance of the proposed integrated control and protection scheme under real-time conditions, a hardware prototype has been developed. With advances in the real-time simulation techniques, RT-Lab simulator developed by the Opal-RT technologies has emerged as one of the most promising tools for real-time performance analysis of the designed models. The RT-Lab is a real-time digital simulator, where simulations take place at a very high speed owing to the use of multiple numbers of processors. In other words, RT-Lab simulations mimic the real-time scenario in terms of execution speed, in contrast with other simulation tools such as MATLAB.

Fig. 7 shows the schematic diagram of the experimental test. As illustrated in the figure, the MATLAB/Simulink models are built in a host computer installed with Opal RT-Lab software. The computer is connected to Opal-RT simulator via Ethernet, and then the results are observed in a digital storage oscilloscope via connecting probes. As can be seen from Fig. 7(a), the entire real-time model consists of two separate subsystems, where Subsystem 1 represents the study network, and Subsystem 2 represents the proposed control and protection scheme. The input signals to the proposed scheme (Subsystem 2) are voltage and current phasors measured at the location of relays in the study network, which are generated by Subsystem 1; also, the output signals from Subsystem 2, which form the inputs of Subsystem 1 include converter blocking signals, circuit breaker disconnection signals, the TCSC change mode signals, and load-shed signals.

Figs. 8 and 9, respectively, present the obtained waveforms, and the performance of the HADRs 1 and 6 during the experimental test of the proposed scheme for four fault events at different locations of the study network. Also, Fig. 10 depicts the time diagrams corresponding to the obtained results shown in Fig. 8. In all cases, the fault is applied at $t = 1$ s. Faults F1, F3, and F4 are of symmetrical three-phase type, and Fault F2 is of line-to-ground type. $V_{1R,\text{post}}$ and $I_{1R,\text{post}}$ in Fig. 9, respectively, denote the post-fault positive-sequence voltage and current phasors measured by the HADRs in the study network. Also, ΔZ_{1R1} and ΔZ_{1R6} are the fault locater outputs of HADRs 1 and 6, respectively. In Fig. 8, V_{di}, I_{di}, and P_{di}, respectively, represent voltage, current, and power measured at the inverter dc side; V_{aci} is the rms voltage of inverter AC bus; P_{acline} and

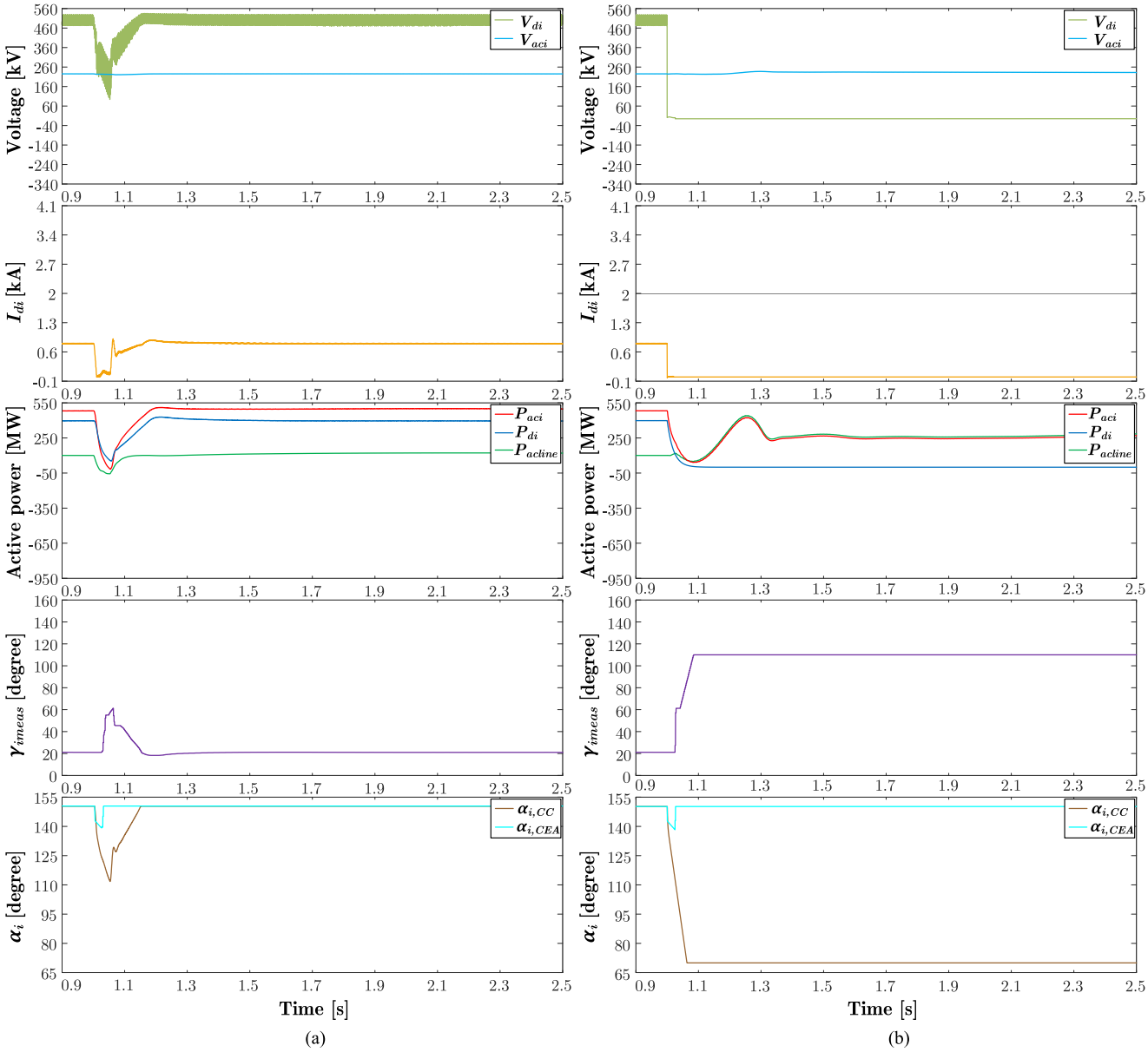

Fig. 8. *(Continued).*

P_{aci}, respectively, denote the active power flowing through the parallel ac line and the total active power leaving the inverter ac bus; γ_{imeas} is the measured extinction angle at the inverter station; also, $\alpha_{i,\text{CC}}$ and $\alpha_{i,\text{CEA}}$ are the output signals of the CC and CEA controllers in the inverter control system. The minimum value between these signals at each instant of time is considered as firing angle order for the thyristor valves.

As can be seen from Fig. 8, before the fault incident, the extinction angle has been controlled by the CEA controller in the HVdc control system. This controller is used to ensure that the extinction angle remains at its minimum permissible value to reduce the reactive power consumption of the inverter.

With reference to Fig. 8(a), a three-phase fault at point F1 does not cause a significant voltage drop at the inverter ac bus. However, the voltage reduction at the rectifier ac bus changes the operating point of the HVdc control system. The inverter control system switches to CC mode after 9.5 ms, which leads to the reduction of both $V_{\text{d}i}$ and $I_{\text{d}i}$. Such a reduction in $V_{\text{d}i}$ increases γ_{imeas}, and therefore no commutation failure occurs. At $t = 1.05$ s, the fault is cleared. Hence, both $V_{\text{d}i}$ and $I_{\text{d}i}$ increase and the inverter control system switches back to CEA mode at $t = 1.15$ s. As can be seen from Fig. 9(a), since F1 is located in the forward side of Relay 1 and in the reverse side of Relay 6, phasors ΔZ_{1R1} and ΔZ_{1R6}, respectively, lie in the third and first quadrants of the positive-sequence impedance plane; hence, Relays 1 and 6 do not take action according to Fig. 6.

When a dc fault occurs at point F2 [see Fig. 8(b)], only one converter, i.e., rectifier, is able to feed the fault, since the thyristors can only conduct in one direction, and $I_{\text{d}i}$ immediately becomes zero at the fault instant. Also, the inverter switches to

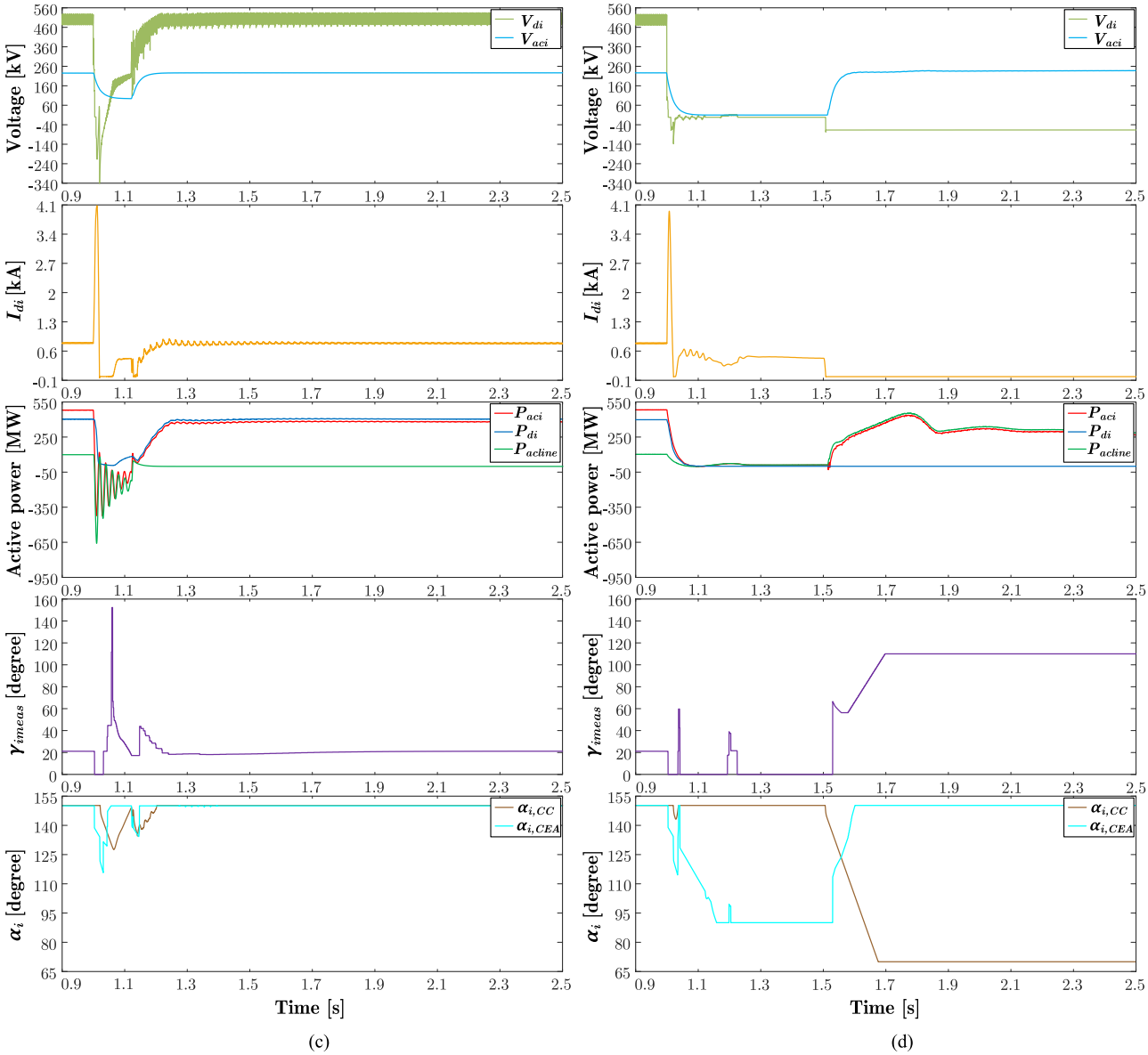

Fig. 8. Obtained waveforms during the experimental test of the proposed scheme for four fault events at different locations of the study network. (a) Case F1. (b) Case F2. (c) Case F3. (d) Case F4.

the CC mode after 1.7 ms, which leads to the increase of γ_{imeas}. However, regardless of the control action, Relays 2 and 3 immediately trip and isolate the dc line at $t = 1.02$ s. Simultaneously, Relay 3, which is located near the TCSC, sends a command signal to the TCSC to change its mode to the capacitive-Vernier mode. This leads to the increase of the transmission capacity by 200 MW, which can only compensate for half of the HVdc line with regard to its thermal limit. Hence, it also issues a 200-MW load-shedding signal for the inverter ac system. After power flow transfer to the ac line, Relays 4 and 5 protect the ac line and will trip once the temperature of the line exceeds its thermal limit for a pre-specified period of time. As can be seen from Fig. 9(b), both Relays 1 and 6 see the fault F1 at their reverse side, but they do not trip similar to the previous case.

In case of a three-phase fault at point F3 [see Fig. 8(c)], V_{aci} significantly reduces, since the fault is located in the vicinity of the inverter station. This sudden drop of V_{aci} results in reduction of V_{di} due to the principles of ac/dc conversion, which increases I_{di} to maintain the active power P_{di} at the rated power of inverter station according to $P_{\text{di}} = V_{\text{di}} I_{\text{di}}$. Since the overlap angle μ is directly proportional to the direct current, it also increases and reduces the extinction angle γ_{imeas}, leading to commutation failure after 3.5 ms. In this fault case, similar to the previous case, both Relays 1 and 6 detect the fault at their reverse side, as shown in Fig. 9(c). However, since the TCSC mode has not been changed at $t = 1.02$ s, Relay 1 issues a disconnection command to circuit breaker CB4, and the ac line is disconnected from its upstream side at $t = 1.07$ s. Accordingly, Relay 6 senses a change in the value of Z_{t1R6} at $t = 1.07$ s and sends a disconnection command to circuit breaker CB5 to isolate the faulted ac line from the rest of the network. It also issues a 100-MW load-shedding signal for the inverter ac system due to the outage of ac line.

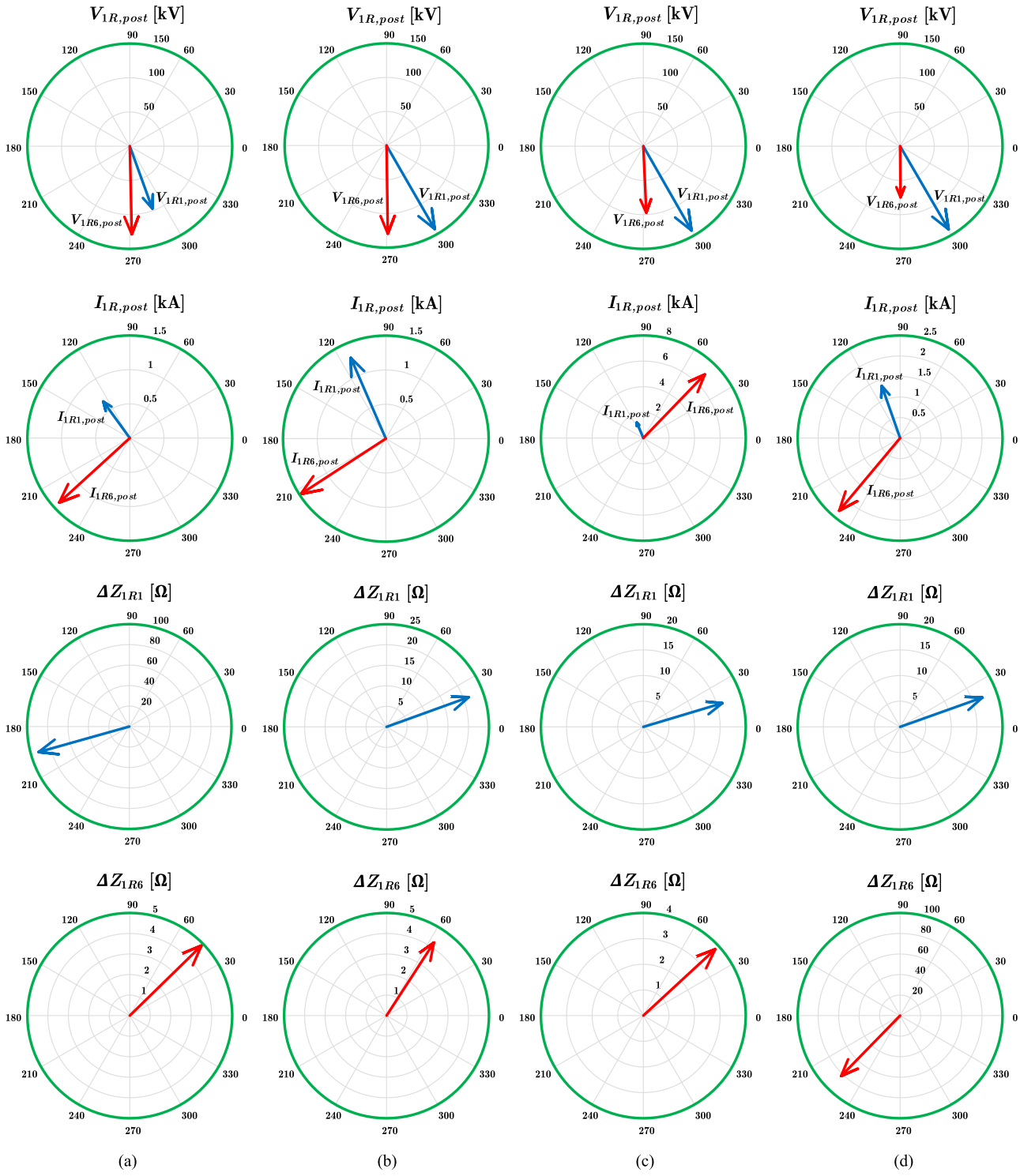

Fig. 9. Performance of HADRs 1 and 6 during the experimental test of the proposed scheme for four fault events at different locations of the study network. (a) Case F1. (b) Case F2. (c) Case F3. (d) Case F4.

Similar to case F3, where a three-phase fault occurs at point F4 [see Fig. 8(d)], commutation failure happens after 3.5 ms. Hence, Relay 6, which recognizes a forward fault, changes the TCSC mode to the capacitive-Vernier within one cycle after the fault. However, it continuously checks the commutation failure status for 500 ms to change the TCSC mode to the by-passed thyristor once the fault was cleared within this period of time. However, since the fault is not removed within this time period, the HVdc converters are automatically blocked at $t = 1.5$ s and the power flow is transferred to the parallel ac line. Accordingly,

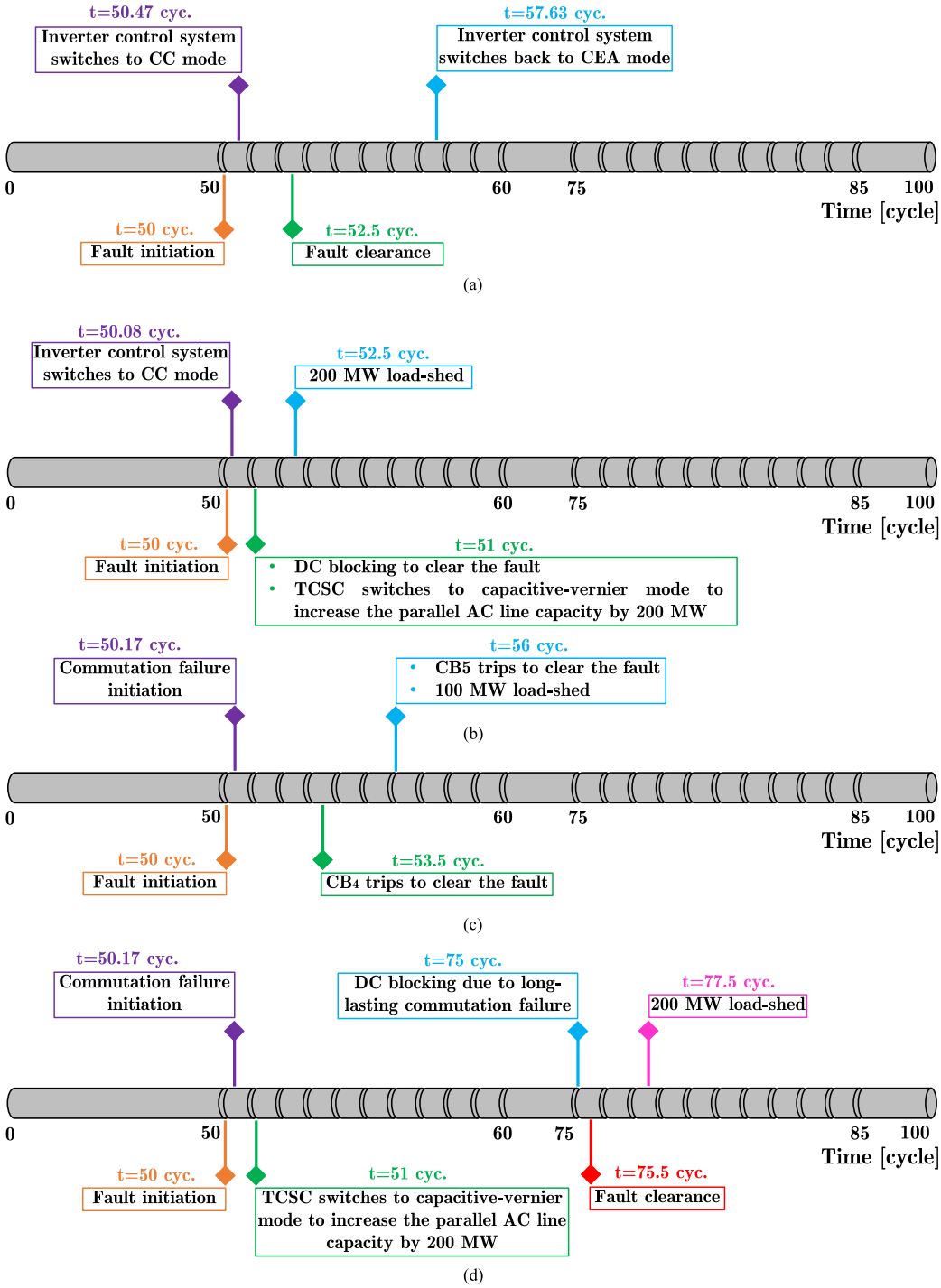

Fig. 10. Time diagrams corresponding to the obtained results shown in Fig. 8. (a) Case F1. (b) Case F2. (c) Case F3. (d) Case F4.

Relay 6 also issues a 200-MW load-shedding signal to alleviate the overload of the parallel ac line.

VI. Conclusion

In this paper, first, the mechanism of commutation failure was described, and then, cascading fault that initiates from a dc or a severe inverter dc fault, leading to a blackout in the inverter ac side was discussed. Since no commutation failure occurs during the process of a cascading fault caused by the dc fault, the available commutation failure inhibition methods are only effective in the prevention of blackouts caused by the inverter ac fault. To address this challenge, an integrated control and protection scheme along with an HADR was proposed, which has the ability to prevent the blackouts caused by cascading fault without the need for communication infrastructure. The

effectiveness of the proposed scheme under real-time conditions was verified using Opal-RT hardware prototyping platform. The obtained results indicated that the proposed approach is able to prevent the blackouts caused by either dc or inverter ac fault in hybrid ac/dc grids.

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