A Simple Approach to Enhance the Effectiveness of Passive Currents Balancing in an Interleaved Multiphase Bidirectional DC–DC Converter

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***Abstract*—This paper studies the high power density bidirectional dc–dc converter with interleaving, soft-switching, and near critical conduction mode (near-CRM) operation. Systematic design and control methods are proposed to enhance the effectiveness of passive currents balancing between multiple interleaved phases without using individual phase current feedbacks. This paper first analyzes the zero voltage turn-ON operation, including the turn-OFF energy diversion by the added snubber capacitor and the turn-OFF resonance models. Second, the intrinsic inverse co-relation between the phase current deviation and the resulting effective duty cycles variation is quantitatively formulated and modeled as a closed-loop mechanism that balances the currents passively. Then, the design constraints of the system parameters including the snubber capacitance, dead time, and valley currents of the near-CRM mode are formulated to guarantee the effectiveness of counteracting the current unbalance. Finally, a variable switching frequency control is proposed to actively control the valley current and maintain the current balancing effectiveness throughout the operating range. An IGBT-based 20-kW three-phase interleaved prototype with the maximum efficiency of 99.1% is constructed to verify the proposed design and control methods.**

***Index Terms*—Interleaved dc–dc converter, multiphase current balance, near critical conduction mode (near-CRM), zero-voltage switching (ZVS).**

NOMENCLATURE

$V_{\rm dc}$	High dc-link voltage.
V_o	Low dc-link voltage.
$D_{\rm control}$	Control duty cycle of DSP output signal.
$D_{\rm actual}$	Effective duty cycle of the half-bridge output.
$T_{\rm deadtime}$	IGBT control dead time.
T_s	Switching period.
$f_{\rm sw}$	Switching frequency.
$i_L(t)$	Inductor current at the time t.
$I_{\rm avg}$	Inductor average current.
I_{p-}	Desired negative valley current value.

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tends to deviate the multiple phase currents from the equal split conditions [12]–[14]. Therefore, multiple current sensors and closed-loop current regulators are used per-phase as in [15]–[19] to achieve the active balancing of the multiphase currents. Chae *et al*. [18] realize the high precious current sharing by adding input voltage ripple difference information to overcome the difference between the per-phase inductor current feedbacks. Bae *et al*. [19] propose a digital resistive current control to share the multiphase currents by converting the effective input characteristic of the converters seen by the source to a resistive load sink. To reduce the system hardware complexity and the cost, a few current balancing methods without per-phase current sensors are proposed. In [20]–[22], a single dc-link current sensor is used to reconstruct the multiphase inductor currents to actively balance the individual phase current. However, the high-frequency oscillating current due to the dc-link parasitics at the voltage transitional edges makes the accurate current sampling and reconstruction infeasible for certain operating ranges. Abu Qahouq *et al*. [14] use the duty cycle compensation to minimize the multiphase asymmetry and the resulting current unbalance. However, the current balancing effectiveness is still limited by the difference of the equivalent resistance and voltage per phase.

Besides the aforementioned actively controlled current balance methods, the multiphase currents passive balancing mechanisms (or self-balance as called in some literature) have also been investigated. In [2] and [13], the discontinuous inductor current (DCM) effectively reset the inductor current to zero in each switching cycle. Hence, the current unbalance is just proportional to the tiny duty cycle deviation, which would otherwise induce tremendous current unbalance between the multiphase inductors under the continuous current mode. Despite its popularity, the DCM usually suffers from the significant parasitic oscillations around the current zero crossing points. GarcÍa *et al*. [23] discuss the observation of an intrinsic mechanism of current self-balance in the interleaved multiphase dc–dc converter under natural ZVS. Later, for the converters under ZVS mode (such as a full-bridge DAB), Costinett *et al*. [24] analyze and formulate the inherent mechanism that automatically compensates for the inductor-applied volt–second mismatch due to asymmetries in circuits or modulation waveforms. Even though the work in [24] does not specifically deal with the current balancing in between the interleaved phases, Kim *et al*. [20] and GarcÍa *et al*. [23] demonstrate that the incremental duty cycle of a phase leg due to current deviation tends to correct the current unbalance. However, in practice and in the laboratory validation, it is seen that the multiphase currents are not necessarily well balanced passively under different system parameters and operating points. To enhance the effectiveness in counteracting the current unbalance in an interleaved bidirectional dc–dc converter, this paper proposes the systematic and quantitative methods to design the system parameters and to control the converter with variable switching frequencies.

Section II analyzes the ZVS process and the resonance model during the turn-OFF. It is also proposed that the snubber capacitor is added to each switch to enhance the effectiveness of the current balancing. With near-CRM mode, the inductive current reverses direction in each switching cycle. Then, the combined parasitic and snubber capacitors of the upper and lower switches

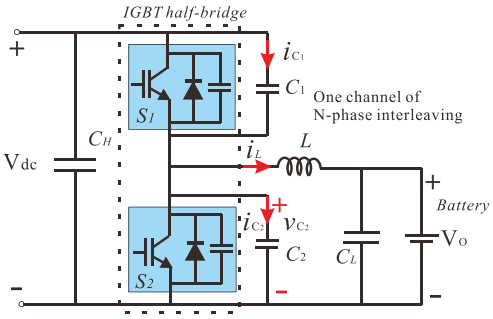


Fig. 1. One channel of the multiphase interleaved bidirectional dc–dc converter with the proposed additional snubber capacitors.

can be charged and discharged by the inductive current alternately, making the ZVS mode sustainable. During the turn-OFF, the inductive current diversion from the switch by the snubber capacitor is experimentally analyzed and the resonance model is established. In Section III, the resonant turn-OFF transition times and the resulting duty cycle variation are first formulated as the function of the current with the coefficients, such as the external snubber capacitance, valley current, and dead time. Then, the inverse co-relation between the incremental current and the duty cycle variation are explained in detail. It is exemplified that the differences in currents between the interleaved phases tend to converge into a negligible level as the resulting variation of the effective duty cycle changes the current in the opposite way. Then, the effectiveness of current self-balance is quantified and modeled as a closed-loop feedback system where the snubber capacitance and valley/peak currents can be properly selected to adjust the loop gains. Accordingly, Section IV introduces the design constraints and procedure to properly select the values for the external snubber capacitance, valley/peak currents, and dead time in order to enhance the effectiveness of the current balance. Moreover, a variable switching frequency control is proposed to actively control the valley current to maintain the effectiveness of the current balance throughout the operating range. An IGBT-based 20-kW three-phase interleaved dc–dc prototype is constructed to verify the proposed design and control methods to maintain the balanced currents. The prototype is designed for the modular interface between the individual battery pack with the dc bus or the dc microgrid. Experimental results are presented and discussed in Section V. As for the interleaved dc–dc converter running the soft-switching and near-CRM mode, this IGBT-based prototype also demonstrates the high power density and efficiency (maximum efficiency at 99.1%). Finally, Section VI concludes this paper.

II. ZVS Process and the Resonance Model During the Turn-Off

As in Fig. 1, when each phase of an interleaved bidirectional dc–dc converter operates in the near-CRM mode, the ZVS turn-ON is achieved with the inductor current swapping polarities within each switching cycle. Also as in Fig. 1, it is proposed that the lossless snubber capacitor (C_1 and C_2) is added in parallel with each switch (and its parasitic output capacitance) to enhance the effectiveness of the passive current balance

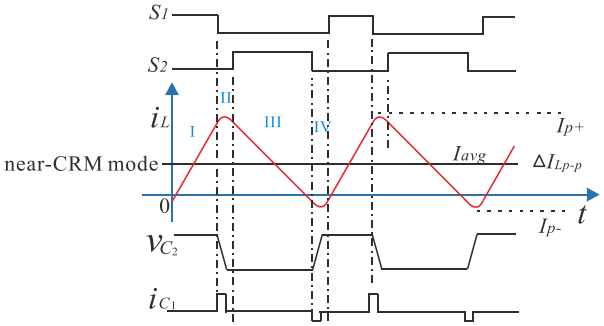


Fig. 2. Waveforms of the soft switching under the near-CRM mode (gate signals, inductor current, voltage across the S_2 and C_1 current).

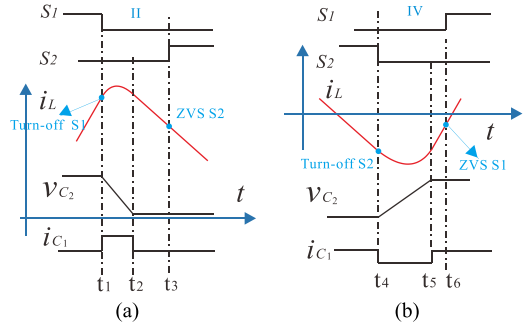


Fig. 3. Zoom in onto the dead times in Fig. 2. (a) Phase II with the peak current. (b) Phase IV with the valley current.

between multiple phases. Therefore, during the turn-OFF, C_1, C_2 (with the IGBT switch parasitic capacitances) and L constitute a resonance network, and the C_1 and C_2 partially divert the inductive current otherwise entering the switch (through the parasitic capacitance).

A. Near-CRM Mode

The near-CRM mode is illustrated in Fig. 2. With the snubber capacitors C_1 and C_2 together with the switch parasitic capacitances being charged and discharged, the transitional rates of the voltages across the switches could be adjusted by proper capacitance selection. With the resonant transition, the inductor current ripples present the round-shaped current peaks and valleys. The resonance model is to be established in Section II-B to derive the effectiveness in counteracting the current deviation. Also note in Fig. 2 that the valley current is kept much smaller than the peak even when the average current is low. This is to maintain the effectiveness of current balancing with the method proposed later in this paper.

As shown in Fig. 2, the near-CRM mode has four distinctive phases in a switching cycle. In phase I, S_1 is ON and S_2 is OFF, the inductor current ramps up from the negative value to its positive peak. The phase II is the dead time. When S_1 is first turned OFF, and S_2 is then turned ON with ZVS. In phase III, $*S_1$ is OFF and S_2 is ON, the inductor current ramps down from its positive peak to the negative value. The phase IV is the dead time again, during which S_2 is first turned OFF, and S_1 is then turned ON with ZVS.

Fig. 3 zooms in onto the phases II and IV, where t_1 and t_4 are the starting points of the turn-OFF events of S_1 and S_2, and the t_2 and t_5 are their ending points. The t_3 and t_6 are the starting points of the turn-ON events of S_2 and S_1.

The previous analysis is based on the positive average output current. However, it is noted that the previous near-CRM operation analysis are totally interchangeable with the cases of the negative average output current, by simply replacing the small negative valley current with the small positive peak current.

B. Current Diversion and the Resonance Model During the Turn-OFF

During the turn-OFF of a switch with the inductive current, the current will not be picked up by the diode of the complementary switch, until the switch voltage rise up to the dc link, making the diode forward biased. By adding snubber capacitors, the inductor current otherwise flowing through the switch during the turn-OFF is partially diverted by the C_1 and C_2, and the resulting *dV/dt* across the switch is slowed down by the proper selection of the lossless snubber capacitance. As in the experimental results in Fig. 4, the larger lossless snubber capacitances absorb the more turn-OFF energy from the IGBT (its parasitic capacitance). This result also verifies the test results in [1] and [25]–[28], where the snubber capacitors are added for the turn-OFF loss reduction. Even though the purpose of adding snubber capacitors in this paper is for enhancing the passive current balance effectiveness, the test results in Fig. 4 does prove that adding larger snubber capacitors does not introduce extra turn-OFF losses with the resulting longer turn-OFF time.

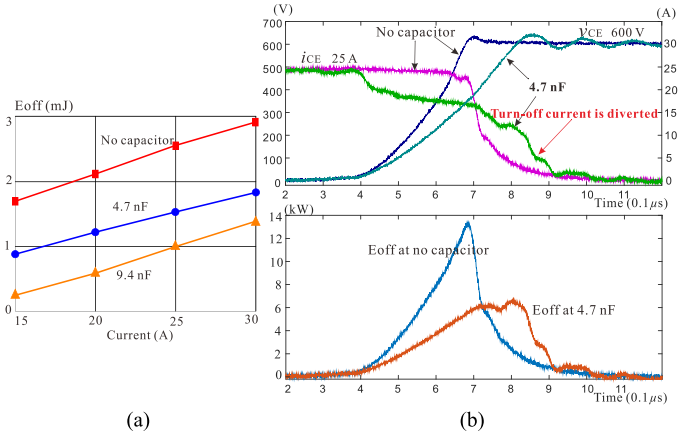


Fig. 4. Laboratory test results of the turn-OFF with snubber capacitors. (a) Turn-OFF energy of the switch with different snubber capacitors. (b) Turn-OFF current and energy diversion. (Test condition: inductor 430 μH, $V_{\rm dc} = 600$ V, 1200-V MiniSKiiP IGBT).

Fig. 5(a) illustrates the current conduction paths during S_1 turn-OFF [at t_1 in Fig. 3(a)]. Under the positive peak current, the C_1 and C_2 (with its switch parasitic capacitances) are charged toward the input dc voltage and discharged to zero, respectively. This resonance transition is formulated by

$$\begin{cases} i_L = -2C\frac{dv_{C_2}}{dt} \\ v_{C_2} - V_o = L\frac{di_L}{dt} \end{cases} \tag{1}$$

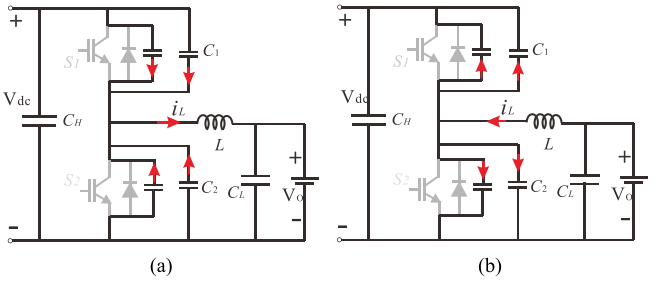


Fig. 5. Turn-OFF in the near-CRM mode with snubber capacitors. (a) S_1 turn-OFF at the positive peak current. (b) S_2 turn-OFF at the negative valley current.

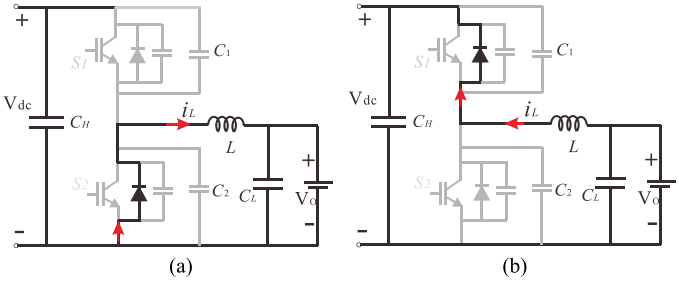


Fig. 6. ZVS turn-ON in the near-CRM mode. (a) S_2 turns ON at the positive peak current. (b) S_1 turns ON around the negative valley current.

where the positive direction of the inductor current and the capacitors voltages are marked in Fig. 1, and the C is the combination of C_1 and C_2 together with its switch parasitic capacitances, approximately, $C = C_1 = C_2$.

At the t_1 in Fig. 3(a), the LC resonance starts and continues until the t_2 when the C_2 voltage is discharged to zero. The initial conditions at the t_1 is that $v_{C_2}(0) = v_{C_2}(t_1) = V_{\rm dc}$, $i_L(0) = i_L(t_1)$. Depending on (1) and initial conditions in between the t_1 and t_2, the LC resonance can be solved as

$$v_{C_2}(t) = (V_{\rm dc} - V_o)\cos(\omega_n t) - Z_n i_L(t_1)\sin(\omega_n t) + V_o \tag{2}$$

$$i_L(t) = \frac{(V_{\rm in} - V_o)}{Z_n}\sin(\omega_n t) + i_L(t_1)\cos(\omega_n t) \tag{3}$$

where ω_n is the resonance frequency $(\omega_n = \frac{1}{\sqrt{2LC}})$ and Z_n is the intrinsic impedance $(Z_n = \sqrt{\frac{L}{2C}})$.

Near-CRM mode is needed for the soft switching. When S_2 turns OFF, the C_1 (with switch parasitics) previously charged up to the input dc-link voltage during S_1 turn-OFF will need to transfer its stored energy to C_2 (with switch parasitics) via the negative inductor current. Fig. 5(b) illustrates the current conduction paths during S_2 turn-OFF (at t_4 moment). Herein, C_1 (with switch parasitics) initially at the input dc voltage is discharged and C_2 (with switch parasitics) is charged toward the input dc voltage. The charge and discharge rates here are obviously much slower than those during the S_1 turn-OFF, since the negative valley current is much smaller than the peak current (positive). At the t_4 in Fig. 3(b), the S_2 turns OFF and the S_1 remains OFF, the LC resonance starts and continues until t_5. The initial condition at the starting point of the resonance is $v_{C_2}(0) = v_{C_2}(t_4) = 0$, $i_L(0) = i_L(t_4)$. From the t_4 to t_5 as in Fig. 3(b), the LC resonance can be solved as

$$v_{C_2}(t) = -V_o\cos(\omega_n t) - Z_n i_L(t_4)\sin(\omega_n t) + V_o \tag{4}$$

$$i_L(t) = \frac{-V_o}{Z_n}\sin(\omega_n t) + i_L(t_4)\cos(\omega_n t). \tag{5}$$

C. ZVS in Turn-ON

As illustrated in Fig. 6, under the near-CRM mode shown in Fig. 3, the S_1 and S_2 ZVS turn-ON is achieved at the t_3 and t_6. The inductive current at the t_3 and t_6 are positive and negative, respectively, so that the inductive current has already been picked up by the anti-parallel diode before turning ON the switch.

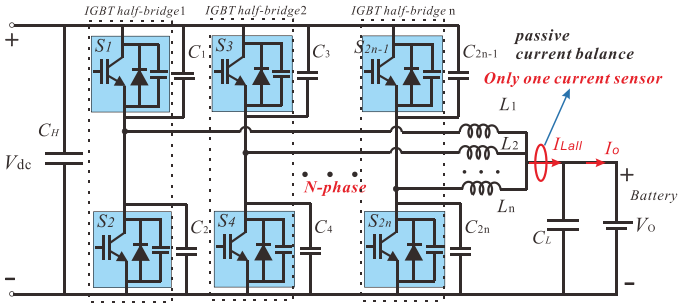


Fig. 7. Interleaved multiphase bidirectional dc–dc converter with additional snubber capacitors, which only one current sensor is used. The passive current balancing and variable switching frequency control are implemented on this topology.

III. Analysis of Passively Balanced Current

The half-bridge running the near-CRM mode not only reduces the inductor size, it also makes the soft-switching sustainable. To reduce the massive current ripples, multiple phase legs are interleaved in order to reduce the output current ripples and the capacitor size. The multiphase interleaved bidirectional dc–dc converter with the added snubber capacitors, as shown in Fig. 7, is used to illustrate the mechanism of the passive current balancing between the multiple phases under the near-CRM mode.

A. Resonant Transition Times During the Dead Time

The resonance times during the turn-OFF are further derived from (2)–(5). Around the peak current, the resonance time from the t_1 to t_2 during the S_1 turn-OFF is

$$\Delta t_{21} = \frac{1}{\omega_n}\arcsin\frac{V_o}{\sqrt{(V_{\rm dc} - V_o)^2 + Z_n^2 i_L^2(t_1)}} + \frac{1}{\omega_n}\arcsin\frac{(V_{\rm dc} - V_o)}{\sqrt{(V_{\rm dc} - V_o)^2 + Z_n^2 i_L^2(t_1)}}. \tag{6}$$

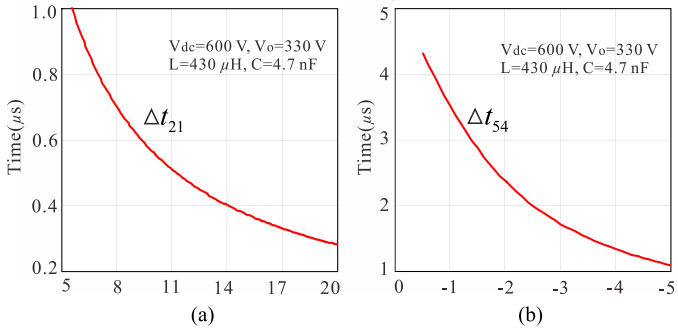


Fig. 8. Resonance times exemplified. (a) At the peak current. (b) At the valley current.

Similarly, around the valley current, the resonance time from t_4 to t_5 during the S_2 turn-OFF event is

$$\Delta t_{54} = \frac{1}{\omega_n} \arcsin \frac{V_{\rm dc} - V_o}{\sqrt{V_o^2 + Z_n^2 i_L^2\,(t_4)}} + \frac{1}{\omega_n} \arcsin \frac{V_o}{\sqrt{V_o^2 + Z_n^2 i_L^2\,(t_4)}}. \tag{7}$$

The resonance times are determined by the *LC* parameters, initial current and input/output dc voltages. It is observed from (6) and (7) that for the given input and output voltages, as the initial current increases, the resonance time decreases and the rising and falling ramps of the output voltage get steeper. Quantitative computation of actual transition times using (6) and (7) are exemplified in Fig. 8. It is obvious that the valley current corresponds to much longer transition times than the peak current.

B. Effective Duty Cycle and Its Current Unbalance Counteracting Effectiveness

During the dead time, the effective voltage output of the half bridge is different than the controller command. As shown in Fig. 3, when S_1 turns OFF with the positive current, the half-bridge voltage falls to zero in a near linear ramp from the input dc voltage and remains at zero for the rest of the dead time. When S_2 turns OFF with the negative current, the half-bridge output voltage ramps up to the input dc voltage and remains there for the rest of the dead time. Therefore, the effective duty cycle of the half bridge is altered as

$$D_{\rm actual} = D_{\rm control} + \frac{1}{T_s}\left(\frac{\Delta t_{21}}{2} + \frac{\Delta t_{54}}{2} + \Delta t_{65}\right) \tag{8}$$

where $\frac{\Delta t_{54}}{2} + \Delta t_{65} = T_{\rm deadtime} - \frac{\Delta t_{54}}{2}$. By substituting (6) and (7) into (8), the effective duty cycle is rewritten as

$$D_{\rm actual} = D_{\rm control} + \frac{T_{\rm deadtime}}{T_s} - \frac{1}{2T_s\omega_n}\left[\arcsin\frac{V_{\rm dc}-V_o}{\sqrt{V_o^2+Z_n^2 i_L^2\,(t_4)}} + \arcsin\frac{V_o}{\sqrt{V_o^2+Z_n^2 i_L^2\,(t_4)}} - \arcsin\frac{V_o}{\sqrt{(V_{\rm dc}-V_o)^2+Z_n^2 i_L^2\,(t_1)}} - \arcsin\frac{(V_{\rm dc}-V_o)}{\sqrt{(V_{\rm dc}-V_o)^2+Z_n^2 i_L^2\,(t_1)}}\right] \tag{9}$$

where $i_L\,(t_4)$ is the valley current and $i_L\,(t_1)$ is the peak current, and the inductor average current is $\frac{i_{\rm peak}-i_{\rm valley}}{2}$.

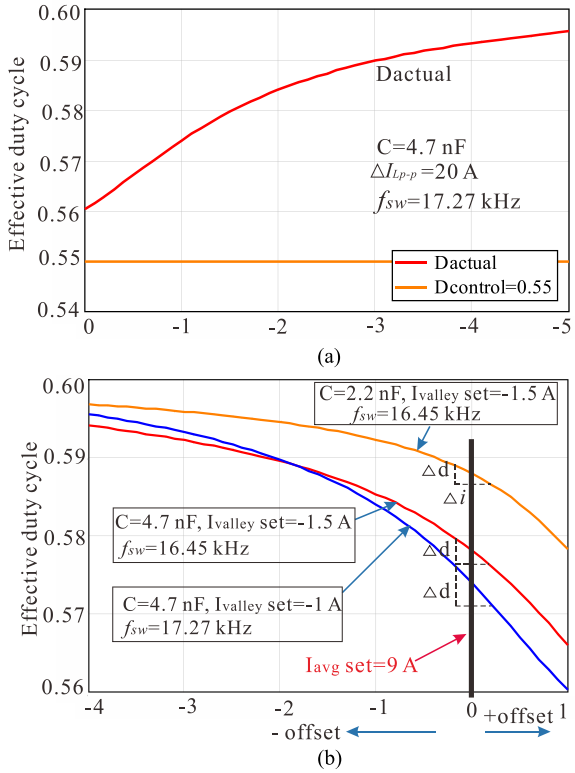


Fig. 9. (a) Effective duty cycle varying with the average current (and the valley current). (b) Droop characteristics of the effective duty cycle around a given average inductor current with different snubber capacitance and valley currents. ($V_{\rm dc} = 600$ V, $V_o = 330$ V, $L = 430$ μH, dead time $= 3$ μs).

According to (9), inverse co-relation exists between the average current deviation and the effective duty cycle variation of each phase leg. The average current deviation (with the given peak to peak value) shifts the valley current accordingly, and alter the duty cycle. It is also seen that the effective duty cycle of each phase is also affected by the two other coefficients including dead time and snubber capacitance.

As shown in the non-linear curve in Fig. 9(a), when the peak-to-peak current is fixed, the operating point with the larger average current (hence the smaller negative valley current) will have more effectiveness in counteracting the current deviation due to the larger duty cycle gradient. Fig. 9(b) shows the comparison of the duty cycle variation over the current deviation around the same average current of 9 A with different valley currents and snubber capacitances. To get the same average current of 9 A, the two curves with –1.5 and –1 A valley currents obviously need to use two different switching frequencies. When the average current deviates from 9 A (the valley current shifts accordingly with the fixed peak-to-peak current), the curve with the initial -1 A valley current has larger duty cycle gradient. The curve with the 2.2-nF snubber capacitance has a larger duty cycle absolute value, but its duty cycle gradient around 9-A average current point is smaller than the curve of the 4.7 nF.

Therefore, the duty cycle gradient indicates the effectiveness of the counteracting effects against the current unbalance, and it is defined as in (10). Fig. 10 plots the gradients showing that the currents unbalance compensation is more effective

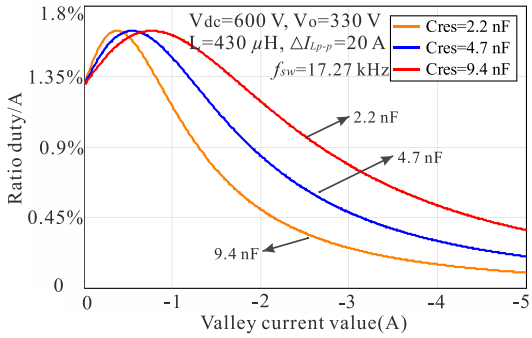


Fig. 10. Effectiveness of the passive current balancing with different snubber capacitances and valley currents.

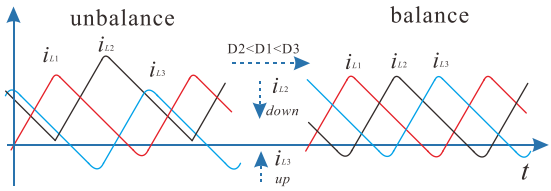


Fig. 11. Passively balanced multiphase current for an interleaved bidirectional dc–dc converter.

with more snubber capacitance and less valley current. Note that Fig. 10 plots are computed with the fixed peak-to-peak current, so that the different valley currents on the x-axis means different average currents. Actually, as the valley current has much larger impacts on the duty cycle than the peak current, it would make no difference to the plots, if the average current is fixed and the valley current change is achieved by dynamically varying the switching frequency (hence the peak-to-peak current)

$$K_{\mathrm{DI}} = \frac{dD_{\mathrm{actual}}}{di_{L\mathrm{valley}}}. \tag{10}$$

C. Passively Balanced Multiphase Currents

As the variation of the duty cycle tends to change the current in the opposite way, the differences in currents between the interleaved phases tend to converge into a negligible level. The process is exemplified in the Fig. 11. The inductor current of the first phase is normal. The current of the second phase is initially shifted upward to the extent that it no longer has the negative valley current. The current of the third phase has an initial negative offset.

According to (8), the effective duty cycles of three half bridges are

$$D_{1\mathrm{actual}} = D + \frac{T_{\mathrm{deadtime}}}{T_s} + \frac{1}{2T_s}\left[\Delta t_{21}\left(i_{L1\mathrm{peak}}\right) - \Delta t_{54}\left(i_{L1\mathrm{valley}}\right)\right] \tag{11}$$

$$D_{2\mathrm{actual}} = D + \frac{1}{2T_s}\Delta t_{21}\left(i_{L2\mathrm{peak}}\right) \tag{12}$$

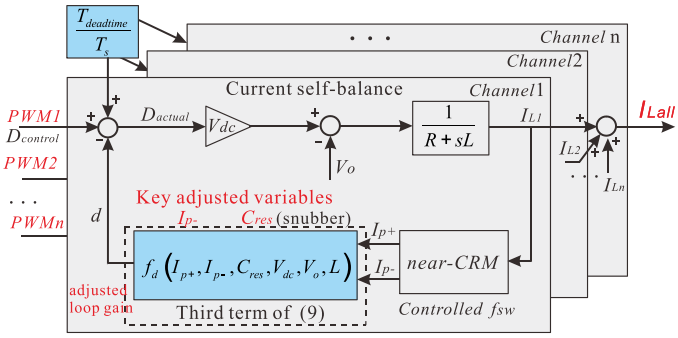


Fig. 12. Intrinsic closed-loop mechanism for passively balanced current (current self-balance).

$$D_{3\mathrm{actual}} = D + \frac{T_{\mathrm{deadtime}}}{T_s} + \frac{1}{2T_s}\left[\Delta t_{21}\left(i_{L3\mathrm{peak}}\right) - \Delta t_{54}\left(i_{L3\mathrm{valley}}\right)\right]. \tag{13}$$

The relation between the three effective duty cycles are: $D_{2\mathrm{actual}} < D_{1\mathrm{actual}} < D_{3\mathrm{actual}}$ while the average currents satisfy $I_{L2} > I_{L1} > I_{L3}$. Obviously, the lower current increases the duty cycle, and then the higher duty cycle tends to increase the output current. These counteracting mechanisms decrease the second inductor current, and increases the third inductor current. Finally, the currents between three phases are balanced passively, without the need for the individual phase current feedbacks.

D. Intrinsic Closed-Loop Mechanism for Passively Balanced Current

The inverse co-relation between the current deviation and the duty ratio variation can be instructively formulated and modeled as a closed-loop system, as shown in Fig. 12. As the inductors' internal resistances are low, the slight difference in the output duty cycles due to the asymmetry of the interleaved phases would have introduced significant current unbalances. Fortunately, the adjustment of the snubber capacitance and the valley current (or the peak current in the boost mode) effectively increase the loop gain and enhance the effectiveness of minimizing the current unbalance. Moreover, the dead time also affects the effectiveness of counteracting the currents unbalance as shown in Fig. 12. In Section IV, these three parameters are to be properly designed based on the proposed design constraints and procedure, and the needed valley current is maintained by the proposed variable switching frequency control.

IV. Design and Control Methods for Passive Current Balance

A. Parameters Design Constraints

To passively balance the currents of the multiple phases and guarantee the soft switching, the design constraints are proposed.

First, the converter must operate in the near-CRM mode where the inductor current has both positive and negative values in each

switching cycle. So, the inductive current at the t_1 and t_4 must be positive and negative, respectively.

Second, the *LC* resonance must be completed before the snubber capacitors get fully charged or discharged, namely the transition times as in (6) and (7) have to be solvable if

$$\begin{cases} \frac{V_o}{\sqrt{(V_{\rm dc}-V_o)^2+Z_n^2 i_L^2(t_1)}} < 1 \\ \frac{V_{\rm dc}-V_o}{\sqrt{V_o^2+Z_n^2 i_L^2(t_4)}} < 1. \end{cases} \tag{14}$$

By substituting the Z_n as in (3) into (14), the relationships between *L*, *C*, and initial resonance currents are formulated as

$$\begin{cases} Li_L^2(t_1) > 2CV_{\rm dc}(2V_o - V_{\rm dc}) \\ Li_L^2(t_4) > 2CV_{\rm dc}(V_{\rm dc} - 2V_o). \end{cases} \tag{15}$$

To maintain soft switching, (15) has to be valid, i.e., the inductor should carry and transfer enough energy to the snubber capacitors. The *LC* parameters, input and output voltages, and the initial resonance currents at the t_1 and t_4 are to be plug into (15) to verify its validity.

Third, another constraint is the dead time. It consists of the resonance transition time and the hold time when the inductive current flows through the antiparallel diode. The dead time constraints can be expressed as

$$\begin{aligned} \max\{\Delta t_{21}, \Delta t_{54}\} &< T_{\rm deadtime} \\ &< \min\{\Delta t_{21} + \Delta t_{{\rm rev}S2}, \Delta t_{54} + \Delta t_{{\rm rev}S1}\} \end{aligned} \tag{16}$$

where $\Delta t_{{\rm rev}S1}$ is the maximum possible conduction time of the S_1 antiparallel diode, which is derived from (5) and (7) as

$$\Delta t_{{\rm rev}S1} = \frac{L_1}{V_{\rm in} - V_o}\left[\frac{V_o}{Z_n}\sin(\omega_n \Delta t_{54}) - i_L(t_4)\cos(\omega_n \Delta t_{54})\right] \tag{17}$$

and $\Delta t_{{\rm rev}S2}$ is the maximum possible conduction time of the S_2 antiparallel diode, which is derived from (3) and (6) as

$$\Delta t_{{\rm rev}S2} = \frac{L_1}{V_o}\left[\frac{V_{\rm in} - V_o}{Z_n}\sin(\omega_n \Delta t_{21}) + i_L(t_1)\cos(\omega_n \Delta t_{21})\right] \tag{18}$$

According to (16), the dead time should be between the resonance time and what takes for the diode current to go to zero. The valid dead time ranges required to achieve the soft-switching and balanced currents are plotted in Fig. 13.

The ranges shift up and down as the snubber capacitances increase or decrease. The minimum dead time decreases and the maximum dead time increases, as the valley current increases.

B. Parameters Design Procedure Exemplified

First, Figs. 10 and 13 are plotted under the given operating conditions. Then, the system parameters of the snubber capacitance, valley current value, and dead time can be looked up from the figures, and they also have to simultaneously satisfy several constraints as defined in the previous section.

By looking up Fig. 10, it is obvious that a small valley current has better unbalance compensation; also large valley current introduces higher ripples and more conduction and inductor losses. However, too small a valley current risks entering positive direction and might violate (15), so that the soft-switching is not sustainable. As discussed subsequently, the switching frequency is dynamically adjusted to regulate the small valley current (negative), so that the design margin is needed for the inductor tolerance varying during the operation. Considering the inductor tolerance, the desired valley current absolute value can be defined as

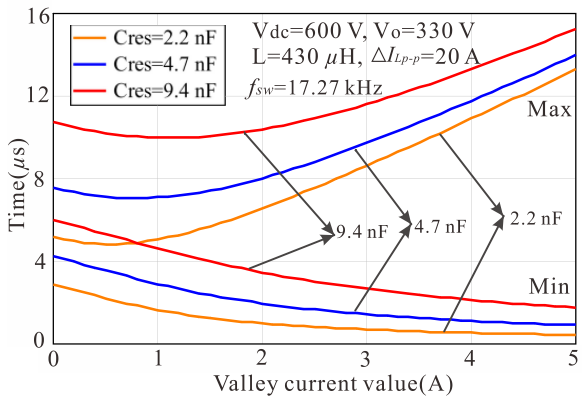


Fig. 13. Dead time ranges with the different snubber capacitances and valley currents, according to (16).

$$|I_{p-}| \geq 0.5\varepsilon_{\rm tol} \cdot \Delta I_{Lp-p}. \tag{19}$$

The maximum dc average current corresponds to the lowest switching frequency and the highest ripple peak-to-peak value. Here is a worst case example with the maximum per-phase peak-to-peak current (ΔI_{Lp-p}) of 23 A and a worst case of +8% inductance deviation ($\varepsilon_{\rm tol} = 8\%$) in the sendust core inductor. In this worst case, the peak-to-peak current value would be reduced with the highest deviation of 1.84 A (= 23 A × 8%), and the absolute value of the valley current would be reduced by 0.92 A (= 0.5 × 8% × 23 A) according to (19).

As long as we set the valley current absolute value ($|I_{p-}|$) slightly larger than 0.92 A, the small valley current value can be maintained as negative by the variable switching frequency control using the nominal inductance value. Therefore, 1.5 A is selected as a good practical number. It is then concluded that the general selection rule of the valley current value is to proportionally scale from the maximum dc average value (roughly half of the maximum peak-to-peak current) with a percentage larger than the inductor tolerance.

Once the negative valley current is selected, the snubber capacitance become the only coefficient of the plots in Figs. 10 and 13. Moreover, off-the-shelf snubber capacitors come with discrete capacitances, such as 2.2 and 4.7 nF, which further narrows down the snubber capacitance selection. From Figs. 10 and 13, the rating of the snubber capacitance can be looked up illustratively. The snubber capacitance selection and its effectiveness of the unbalance compensation, as plotted in Fig. 10, have to be verified with trial and error in practical design, depending on the actual system non-linearity and asymmetry in the multiphase currents test results. For example, the design goal is set as to fight against 1% duty cycle asymmetry with certain

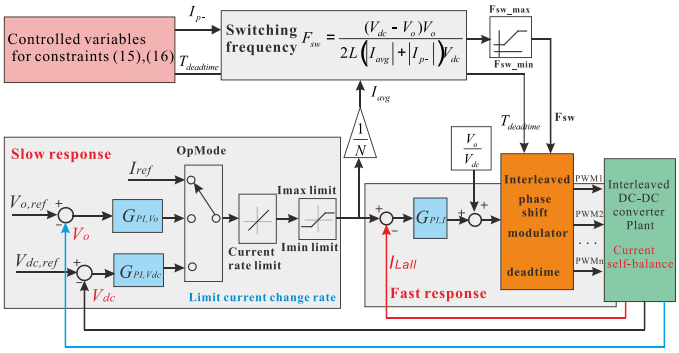


Fig. 14. Proposed variable switching frequency control to passively balance currents by maintaining the proper valley current.

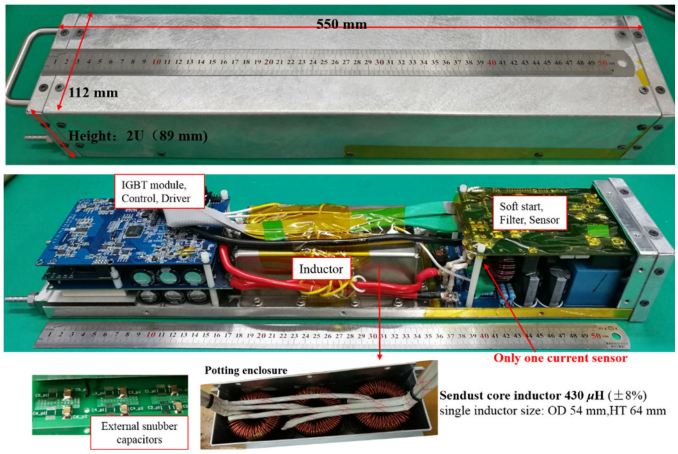


Fig. 15. Laboratory prototype of a three-phase interleaved bidirectional dc–dc converter with additional ceramic snubber capacitors.

acceptable current unbalance. Then, as shown in Fig. 10 and the laboratory test results in Fig. 20, the 2.2-nF snubber results in obvious current unbalance, whereas 4.7 and 9.4 nF appear satisfactory.

However, deciding how much current unbalance is acceptable against how much duty cycle asymmetry is more of a subjective judgment and engineering decision to make. This paper simply provides the design procedure and equations as the quantitative and illustrative tools to assist this engineering decision.

Meanwhile, the dead time range is another consideration when selecting between 4.7 and 9.4 nF. As shown in Fig. 13, the snubber capacitance of 4.7 nF is preferable as it requires a smaller range of the dead time than 9.4 nF. Then, considering the fact that the negative valley current will shift with the inductance tolerance in prior discussion, a medium value of dead time such as 4 μs should be selected within its range from 2.2 to 7.5 μs (when valley current is 1.5 A).

Once the valley current 1.5 A, the capacitance of 4.7 nF and the dead time of 4 μs are determined, constraint (15) is to be further validated.

C. Proposed Control Method

To maintain the same counteracting effectiveness against the current unbalance, the valley current has to be fixed even with a varying average output current. Therefore, the current peak-to-peak value needs to change with the output average by dynamically adjusting the switching frequency according to the input and output dc voltages and the average inductor current as

$$f_{\rm sw} = \frac{(V_{\rm dc} - V_o)V_o}{2L\left(|I_{\rm avg}| + |I_{p-}|\right)V_{\rm dc}} \tag{20}$$

where $I_{\rm avg}$ is the average inductor current and I_{p-} is the desired negative valley current (such as –1.5 A) for the positive average output current in buck mode or the positive peak current (such as +1.5 A) for the negative average output current in boost mode.

Fig. 14 is the proposed variable switching frequency control together with the rest of the system control, i.e., the current loop that uses one overall feedback of the output current from all the interleaved phases. It is worth noting that the dynamic adjustment of switching frequencies implies the loss of the dynamic performance. Fortunately, the non-isolated dc–dc converter, as shown in Fig. 7, is usually for energy storage (battery charging) applications with relatively slow and ramped current commands. Meanwhile, if the switching frequencies adjustment is open loop, the extra margin is added to the valley current command as previously discussed. Even in the worst case when the valley current is not accurately maintained due to open-loop imperfections, the system will still be stable, although it would lose the current self-balance or soft-switching advantage and more EMI would be observed, as verified by the laboratory test. As the multiphase currents are passively balanced, it is also viable to use the one overall output current feedback to maintain the desired negative valley current value of each phase.

V. Experimental Results

To verify the theoretical analysis, a three-phase interleaved bidirectional dc–dc converter prototype is constructed, as shown in Fig. 15, and the converter parameters are listed in Table I. It is for the application of the modular interface between the individual battery pack and the dc-bus (or dc microgrid). As the rightmost one-third of the prototype volume are mostly auxiliary parts that are application related, the active portion is only 3.8 L (112 mm × 89 mm × 380 mm), which demonstrated high power density.

Please note that the snubber capacitance selection is after the inductance and the other system parameter design has already been done. The inductance is designed according to the voltage and current requirements of the target product (input dc voltage is 720–750 V, output dc voltage is 520–650 V, and average output current is 0–±30 A). The inductor of each interleaved phases, the switching frequency range, and all the parameters are optimized for high power density system design. According to the inductor parameters design results, it is custom-made in-house.

With the total average output current of 30 A, each phase has 10-A average value, the IGBT switching frequency upper limit is set at 25 kHz, and the lower limit is set at 6 kHz. The lower limit is set, so that the dc capacitor will not be over-sized. Under

TABLE I
PARAMETERS OF THE EXPERIMENTAL THREE-PHASE INTERLEAVED BIDIRECTIONAL DC–DC CONVERTER

Description/Symbol	Value
Input voltage, V_{dc}	720–750 V for mode 1 520–650 V for mode 2
Output voltage, V_o	520–650 V for mode 1 200–450 V for mode 2
Output current, I_o	0 – ±30 A
Maximum power	20 kW
Main inductor (at average current 10 A), L_1–L_3	430 μH
Resonant capacitor C_{res}, C_1–C_6	4.7 nF
High DC-link capacitor, C_H	360 μF
Low DC-link capacitor, C_L	150 μF
Switching frequency, f_{sw}	6–25 kHz
Valley current for the buck mode, I_{p-}	-1.5 A
IGBT module part number	SKiiP 39AC12T4V1
Gate drive IC	2ED020I12-F2
DSP control IC	TMS320F28335

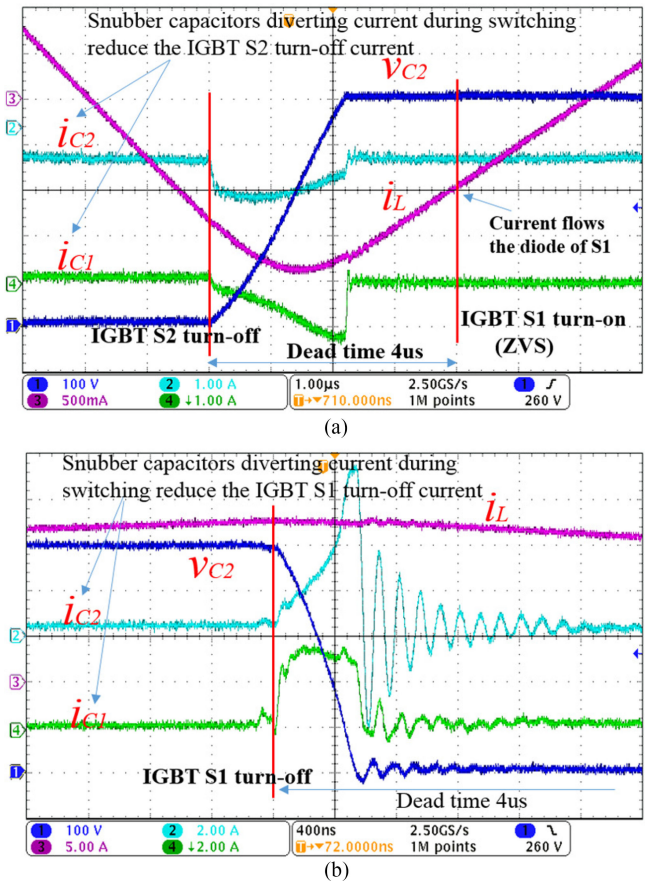


Fig. 16. Key transition waveforms of the resonant turn-OFF and the subsequent ZVS turn-ON. (a) Valley current. (b) Peak current.

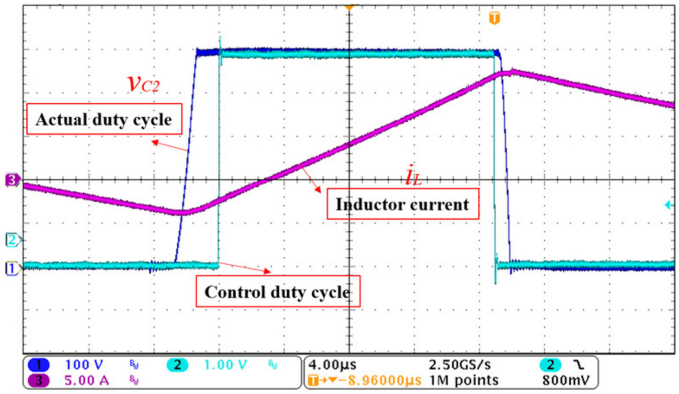


Fig. 17. Effective and the original duty cycle command (with external 4.7-nF snubber capacitors) working in the near-CRM mode.

the near-CRM mode, the current ripples of the three interleaved phases are slightly larger than 200% of the average dc current per phase. The output current after interleaving will have the reduced ripple amplitudes and the three times the switching frequency. Then, the 6-kHz lower limit is selected according to the ratings and size requirements of the absorbing dc capacitors.

Given the lowest switching frequency of 6 kHz, the needed inductance is computed as follows:

$$L = \frac{(V_{\rm dc} - V_o)V_o}{f_{\rm sw}\Delta I_{Lp-p}V_{\rm dc}} \tag{21}$$

where $\min\{\frac{(V_{\rm dc}-V_o)V_o}{V_{\rm dc}}\} = \frac{(720-650)\times 650}{720} = 63.2$, so that

$$L_{\max} = \frac{1}{f_{\rm sw\_min}\Delta I_{Lp-p}} \cdot \min\left\{\frac{(V_{\rm dc}-V_o)V_o}{V_{\rm dc}}\right\} = \frac{63.2}{6000\times 23} = 458\ \mu\text{H}.$$

Cost effective sendust core materials are used to fabricate the required inductor. The resulting inductor has 496 μH at 0 A and 430 μH at 10-A average current. Note that if the actual inductance is slightly lower than $L_{\max}$, the actual lowest switching frequency will be slightly higher than 6 kHz.

Even though the application in this paper prefers the IGBT, the proposed "effective enhancement" and analysis in this paper are also applicable to the MOSFET-based converters. In [4], the ZVS and resonance transition for MOSFETs with parasitic non-linear capacitance has been studied with a single-channel dc–dc converter, and the additional duty cycle compensation mechanism still exist. Although it would take extra numerical efforts to handle the larger non-linear capacitance in the MOSFETs in parameters design.

A. Basic Waveforms

The test conditions are: $V_{\rm dc} = 600$ V, $V_o = 330$ V, $I_{p-} = -1.5$ A, $I_{p+} = 18$ A (per phase), dead time = 4 μs. The IGBT S_2 turn OFF and S_1 ZVS turn ON events around the inductor valley current are shown in Fig. 16(a). The resonant valley current waveform validates Fig. 3(b). When S_2 turns OFF, the inductive

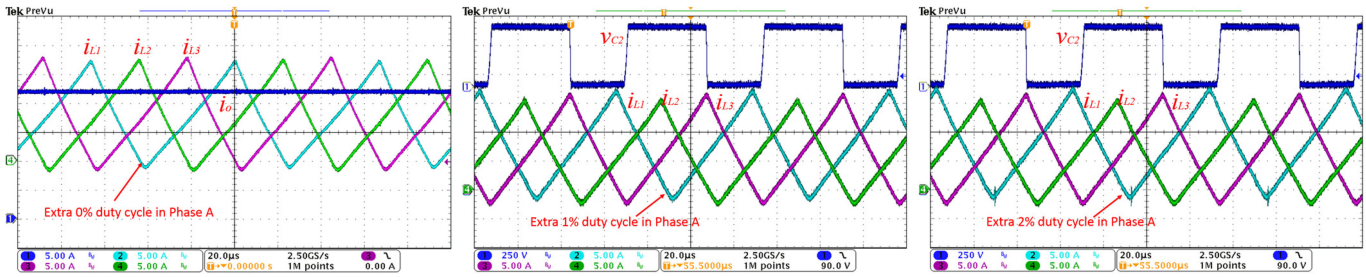
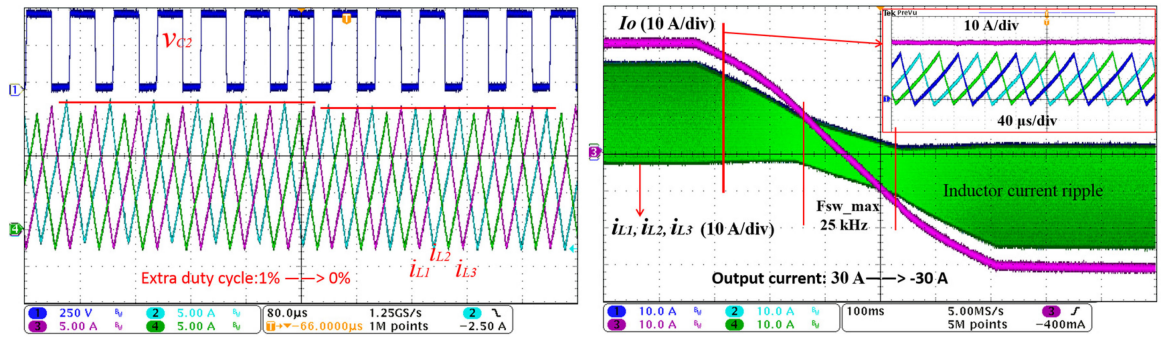


Fig. 18. Three interleaved inductor currents with an extra 0%, 1%, and 2% duty cycle deviation in phase A (channel 2).



(a) (b)

Fig. 19. Dynamic transitions. (a) Inductor currents with 1% to 0% of duty deviation in phase A (channel 2). (b) Combined output current sweeping from 30 to –30 A.

current flowing through IGBT S_2 is diverted by capacitors C_1 and C_2 as in the traces 2 and 4. The switch *dv/dt* is slowed down by the snubber capacitors.

The S_1 turn-OFF around the inductor peak current is shown in Fig. 16(b). The waveforms validate Fig. 3(a). When S_1 turns OFF, the inductive current flowing through IGBT S_1 is diverted by capacitors C_1 and C_2. The oscillations in the snubber capacitors' currents are due to the IGBT parasitic capacitance varying with the voltage, as well as the parasitic inductance and resistance in the snubber capacitors. From Fig. 16(b), it is calculated that the parasitic inductance is about 0.44 μH. It is also obvious that the turn-OFF resonant transition time (2.2 μs) at the valley current is much longer than that (550 ns) at the peak current, so that valley current has the dominant effects in the current self-balance.

Fig. 17 validates that the additional output voltage duty cycle is introduced into the original control duty cycle.

B. Deviation Correction

The waveforms of the three interleaved inductor currents are shown in the traces 2–4 in Fig. 18, the total average output current is 22 A. The external 4.7-nF snubber capacitor and −1.5-A valley current are used here. The peak and valley currents of the three interleaved phase legs are well balanced even with the duty cycle deviation introduced into the phase A.

C. Dynamic Transition

Fig. 19(a) shows the transition from the duty cycle deviation 1% to none. Fig. 19(b) shows that the fixed valley current is maintained by the variable switching frequency control method defined by Fig. 14, with the combined output current dynamically sweeping from +30 to –30 A. As the dc–dc converter is for the energy storage (battery pack charging) applications, the ramp rate limiter in Fig. 14 as used in the current command makes the variable switching frequency control function without transient disturbance. It is observed from the well-aligned envelopes of the peak and valleys that the effectiveness of the current balance is well maintained.

The proposed variable switching frequency control remains the same for both the positive and negative power flow. The only difference is that the small "negative valley current" being regulated actually becomes the small "positive peak current" under the negative power flow. This makes no difference to its effectiveness of passive current balancing. It is also instructive to note that the dynamic transition of the power flow direction means the dynamic switching frequency changing with the varying output current, as labeled in Fig. 19(b).

D. Snubber Capacitances Impacts

The effectiveness of counteracting the current unbalance by choosing difference snubber capacitances is demonstrated in Fig. 20 where the current unbalance is decreased as the snubber capacitances increase.

E. Dead Time Out of Bounds

As shown in Fig. 21(a), when the snubber capacitance is too small, 5-μs dead time is excessive; as a result, the IGBT is not

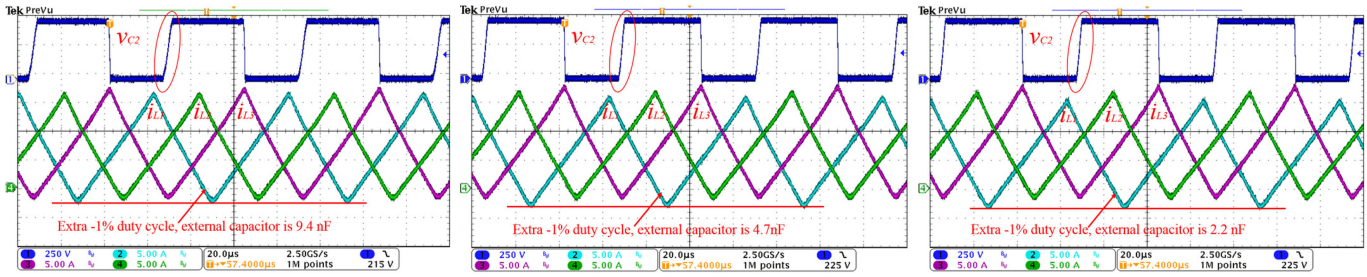
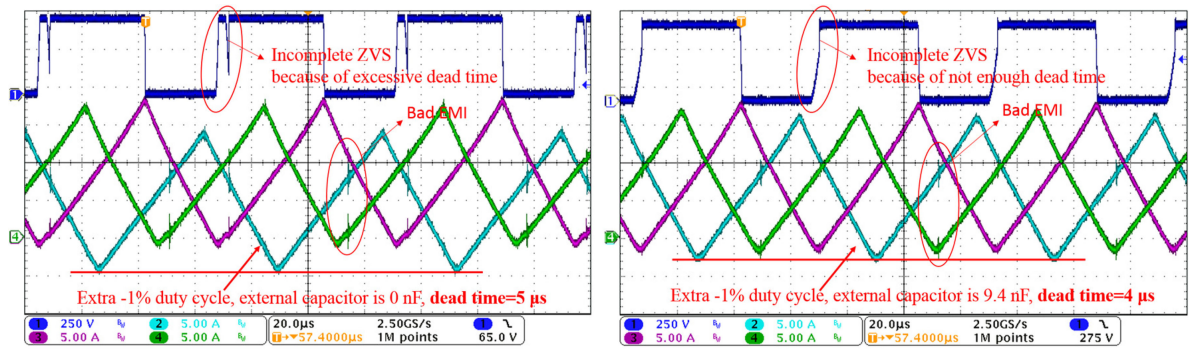
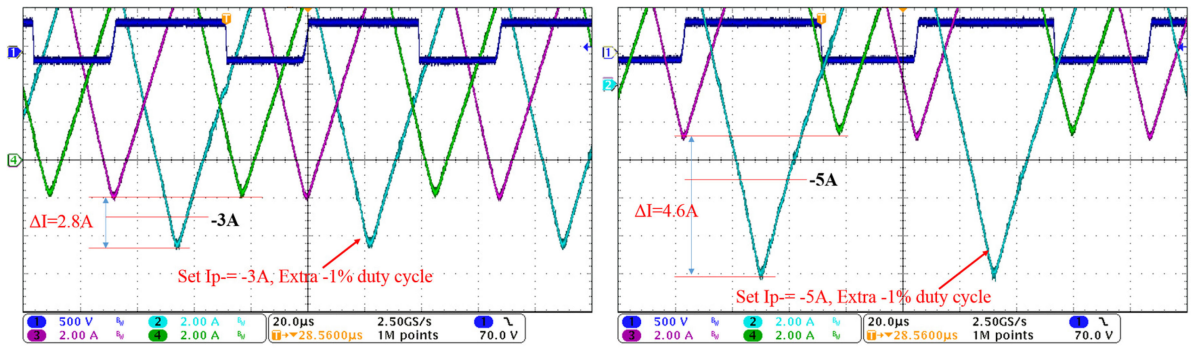


Fig. 20. Inductor currents with an extra –1% duty cycle in phase A (channel 2), with snubber capacitor being 9.4 nF, 4.7 nF, and 2.2 nF (dead time = 5 μs).



(a) (b)

Fig. 21. Extra –1% duty cycle in phase A (channel 2). (a) Snubber capacitor 0 nF, dead time = 5 μs. (b) Snubber capacitor 9.4 nF, dead time = 4 μs.



(a) (b)

Fig. 22. Extra –1% duty cycle in phase A (channel 2) with external capacitor 4.7 nF, dead time = 5 μs. (a) $I_{p--} = -3$ A. (b) $I_p = -5$ A.

switched ON at an appropriate time. In Fig. 21(b), the snubber capacitance is too large, so that 4-μs dead time is not enough to finish ZVS transition. In either cases, the soft switching is not realized and EMI spikes are obvious at the transitional edges. Meanwhile, according to the analysis in this paper, the capability of passive current balancing is also lost, so that the currents are unbalanced under the intentionally applied 1% duty ratio difference in one phase.

F. Valley Currents Impacts

The effectiveness of counteracting the current unbalance by choosing different valley currents is demonstrated in Fig. 22. Obviously, the current unbalance is dramatically increased with a larger valley current when the output current and snubber capacitance are the same. Combinations of the different injected duty cycle deviations and the different valley currents are tested and the results are tabulated in Table II. It is obvious that the low valley current is highly effective in balancing the multiphase currents.

TABLE II
LABORATORY DATA OF THE CURRENT UNBALANCE WITH DIFFERENT DUTY CYCLE DEVIATION AND DIFFERENT VALLEY CURRENTS

Valley current	ΔI (A) +1%	ΔI (A) +0.5%	ΔI (A) -0.5%	ΔI (A) -1%
-2 A	0.4	0.2	0.4	1.2
-3 A	1.9	0.8	1.4	2.8
-4 A	2.8	1.9	2.4	4.2
-5 A	4.0	2.6	3.4	4.6

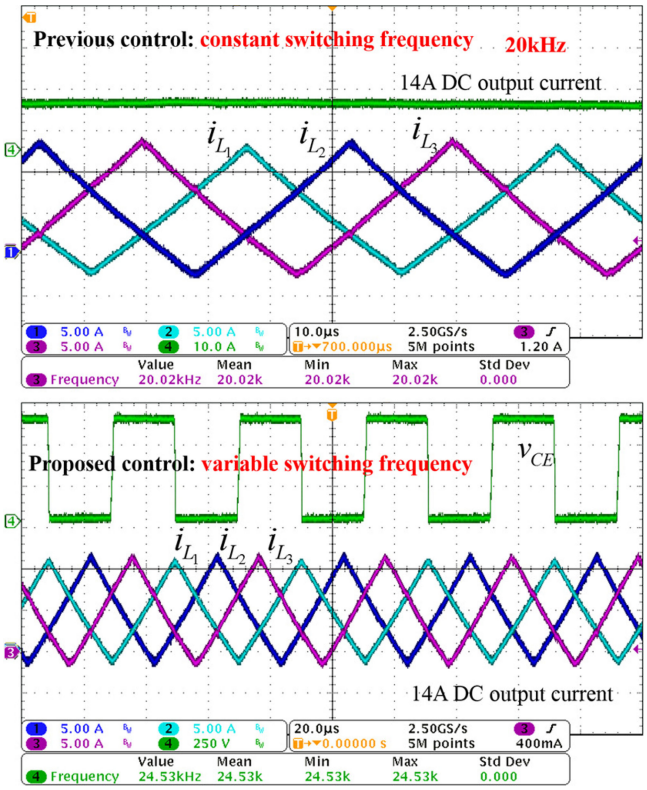


Fig. 23. Comparisons in low output current between our control method and previous constant switching frequency control.

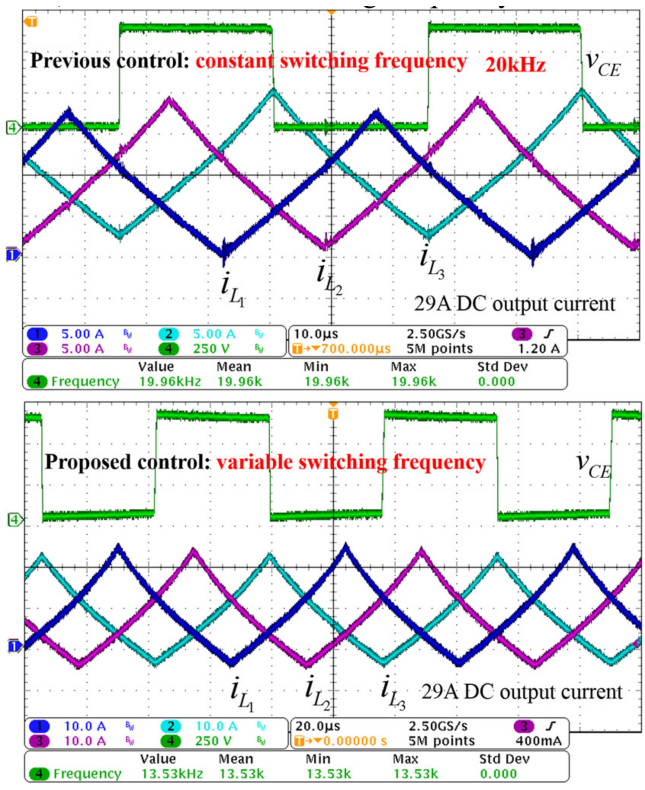


Fig. 24. Comparisons in high output current between our control method and previous constant switching frequency control.

Note that there will always be certain amount of currents unbalance. As illustrated in Fig. 12, the passive current balancing is equivalent to a feedback system with "proportional gains," so that the unbalance cannot be completely eliminated. The proposed "effectiveness enhancement" such as the valley current regulation are equivalent to increasing this "proportional gain" and make the current unbalance smaller, given certain amount of the system asymmetry in multiphase duty ratios.

Also note that Fig. 20 shows much smaller current unbalance with the same 4.7-nF snubber capacitance by comparison. This is because the valley current in Fig. 20 is only –1. A, which is more effective than Fig. 22(a) with –3-A valley current.

G. Comparison With the Constant Switching Frequency Control

The variable switching frequency control well regulates the required small valley current of the opposite polarity, so that the effectiveness of passive current balancing is maintained. By comparison, the constant switching frequency control would not have this advantage. We added the laboratory tests to compare them.

The following comparison as shown in Figs. 23 and 24 are performed under the same input and output conditions ($V_{\rm dc}$ = 600 V, $V_{\rm o}$ = 300 V). The constant switching frequency is set at 20 kHz and the proposed variable switching frequency control has its frequency vary from 6 to 25 kHz depending on the load current.

As shown in Fig. 23, when the load current is 14 A, the constant switching frequency control will have similar negative valley current, so that its multiphase currents are as balanced as in the variable frequency control results.

But as shown in Fig. 24, when the total output current is increased to 29 A, the constant switching frequency control has its average current shifted up and the valley current values are no longer negative. Therefore, the multiphase currents become apparently unbalanced even when no additional duty cycle difference is injected. Meanwhile, the EMI spikes appear at the ripple valley, indicating that the ZVS mode is lost and hard-switching occurs. By comparison, the proposed variable switching frequency control well regulate the constant small valley currents, so that the passive current balancing is maintained.

In some other operating point ($V_{\rm dc}$ = 520 V, V_o = 400 V) as shown in Fig. 25, this unbalance is particularly obvious, since the inductor currents enters the CCM mode (ripple ratio $<$ 200%) at the constant switching frequency of 20 kHz.

H. Converter Efficiency

The constructed three-phase interleaved bidirectional dc–dc converter prototype as shown in Fig. 15 verifies the controllable effectiveness of passive multiphase currents balancing without per-phase current feedbacks. Moreover, it also confirms the efficiency improvement with the ZVS soft-switching under the

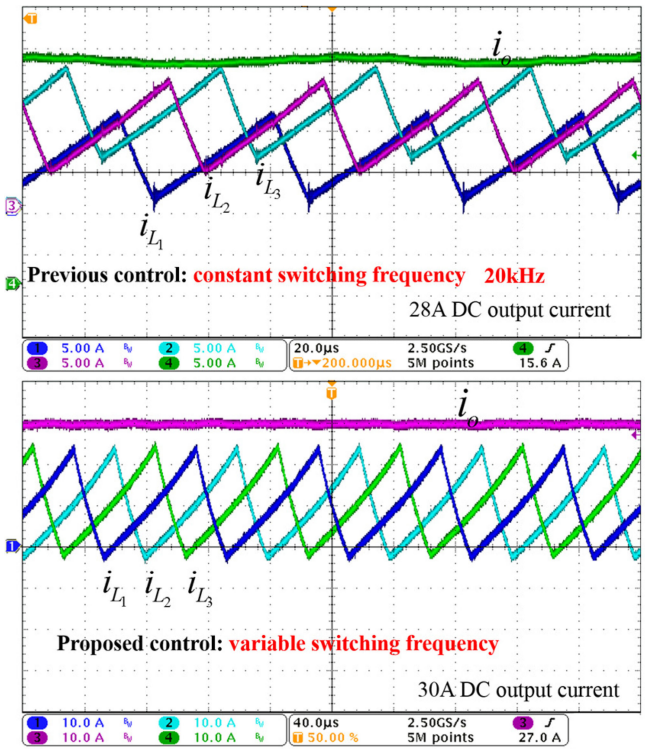


Fig. 25. Comparisons in current balance between our control method and previous constant switching frequency control ($V_{\rm dc} = 520$ V, $V_{\rm o} = 400$ V).

TABLE III
LOSS CALCULATION RESULTS AT THE MAXIMUM POWER OF 20 KW ($V_{\rm dc} = 730$ V, $V_o = 640$ V, $I_o = -30$ A)

Items	Loss (W)
Inductor windings	17.7
Auxiliary wiring including relay, wire and terminal	12.2
Inductor core losses	58.7
Conduction losses of the power module	28.8
Turn-off loss of the power module	33.2
Others: Core dc bias and proximity losses, resonance loss	No accurate calculation
Total	**150.6**

near-CRM mode. The converter efficiency (not including 12-V auxiliary power supply) is 99.1% at the maximum power of 20 kW, which is also verified with the computational losses results in Table III. It is also obvious from the loss break down that the inductor core losses are significant, and the switching losses (turn-OFF losses only) are lower by comparison. This has two reasons. First, interleaving makes each phase to switch at relatively low frequency. Second, with the near-CRM mode and the variable switching frequencies control, the highest output current has the lowest switching frequency (6.92 kHz), which results in lower IGBT switching losses.

The efficiency curves of two working modes are shown in Fig. 26. Note that Fig. 26(a) is plotted with two vertical axes. One is the efficiency (power loss) and the other is the switching

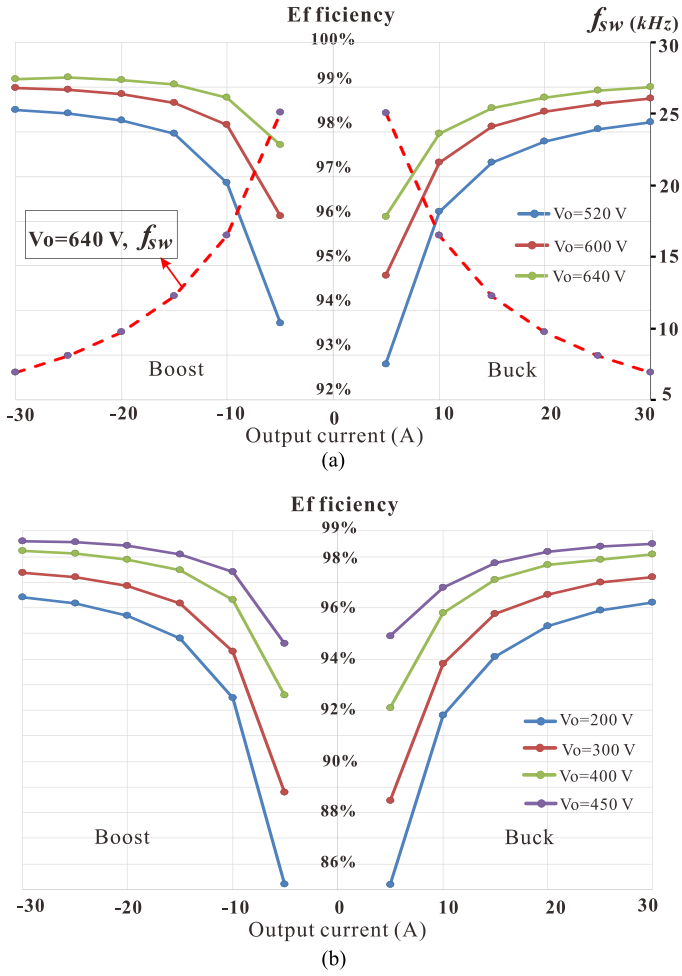


Fig. 26. Efficiency of the three-phase interleaved bidirectional dc–dc converter prototype. (a) Mode 1: battery charging from 730-V dc bus (battery voltage 520–640 V). (b) Mode 2: battery charging from 600-V dc bus (battery voltage 200–450 V).

frequency. For each output current and the efficiency number (power loss), the corresponding switching frequency value can be easily looked up from the plot. The small volume of the prototype, as shown in Fig. 15, implies that the high efficiency is not achieved at the cost of the power density, and the interleaved topology does reduce the overall inductor volume significantly.

VI. CONCLUSION

Despite the previous discoveries in the passive mechanism of balancing the currents of the interleaved multiphases, it is seen in practice and in the laboratory validation that the multiphase currents are not necessarily well balanced passively under different system parameters and operating points. To address this issue, this paper proposed the design constraints and control methods to enhance the current balancing capabilities in the interleaved bi-directional dc–dc converter with the soft-switching and near-CRM mode. Based on the ZVS and the resonance transition analysis, the inverse co-relation between the current deviation and the duty cycle variation of each phase leg is formulated and modeled as the closed-loop current balancing mechanism. Then, more importantly, this paper contributes in the parameters design constraints for the proposed additional snubber capaci-

tors, valley currents of the current ripples, and the dead time. The parameter design practices are equivalent to adjusting the feedback loop gains of the closed-loop mechanism. Moreover, to maintain the desired valley current, a variable switching frequency control method is proposed. As a result, the effectiveness of counteracting the current unbalance can be well maintained and quantitatively enhanced. Thorough experiments have been performed to validate the proposed design and control methods. Even though the study and the laboratory validation is based on the three-phase interleaved system, the proposed methodologies are readily applicable to the converter with any number of the interleaved phases. Therefore, this type of converter is a promising candidate for the bi-directional dc–dc conversion to achieve high power density and efficiency at the reduced sensors cost.

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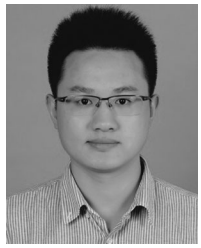

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