A Plug-Play Active Resonant Soft Switching for Current-Auto-Balance Interleaved High Step-Up DC/DC Converter

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***Abstract*—In high gain voltage conversion applications, the low-side switches usually suffer large current stress, resulting in dominate switching loss. In this paper, a general soft-switching method based on an advanced interleaved high-step-up converter, which features excellent performance but works in hard-switching, is presented to combat this issue by using a plug-play resonant circuit. Under this soft-switching method, the main switches reach zero-voltage switching (ZVS) turn-ON and ZVS turn-OFF, and the soft-switching condition is derived. Meanwhile, the added auxiliary switches could be turned OFF under ZVS condition and turned ON under zero-current switching condition as well. More importantly, due to its location out of the energy transferring path, the auxiliary circuit will never lead gain lost to the converter and maintain its other existing merits, such as current auto-balancing and diode inverse-recovery well. A 1-kW prototype is built and tested to verify the significant efficiency improvement and merits maintenance for the proposed converter considering active resonant soft switching.**

***Index Terms*—Coupled inductor, current auto-balance, high step up, soft switching.**

I. Introduction

With increasing energy shortage and environmental issues, renewable energy, such as photovoltaic cells and fuel cells, generation technology has gained extensive attention. However, the low output voltage of photovoltaic cells and fuel cell hardly qualifies them in grid connected. Therefore, high step-up dc/dc converters are usually employed as the front-end converters to step up low voltage to high dc-bus voltage [1]–[3]. Much work about how to achieve high gain with high efficiency at medium and small power applications has been reported [4]–[20].

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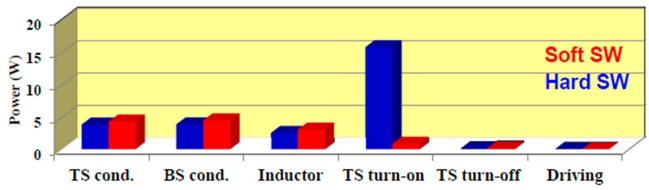

Fig. 1. Loss breakdown in dc–dc converter [26]. Note: "SW" stands for switching. "TS cond." represents the conduction loss of switches. "TS turn-ON" stands for turn-ON loss of switches. "TS turn-OFF" stands for turn-OFF loss of switches. "BS cond." stands for total conduction in connection and capacitor etc. "Driving" stands for driving loss of switches and "Inductor" stands for the total inductor loss.

gain has been obtained for those converters, the current auto-balancing between two interleaved branches is not achieved well, which leads to a high burden for one branch and a large input current ripple at asymmetry condition [23], [24].

To improve this issue, an advanced converter is presented in [25], which is the first to reach complete current auto-balancing in reported literatures due to its special cross coupling and interleaved structure. However, the converter works in hard switching in essence because the parasitic capacitor is too small to support ZVS turn-OFF for the main switch and the energy stored in the parasitic capacitance makes ZCS turn-ON reluctant. There are rapid voltage rising rate for voltage across the main switch at turn-OFF process and pulse current riding through the main switch at its turn-ON process, resulting in some capacitive turn-ON loss. Generally speaking, the turn-ON loss dominates in conversion loss if the converter is operated under hard switching, as shown in Fig. 1. Hence, soft switching for turn-ON becomes a pressing issue.

These can be grouped into two operation approaches to realize soft switching for high step-up converters with coupled-inductor technology [27]–[31]. One method is quasi-resonant operation where the leakage inductance and parasitic capacitance are employed as resonant *LC* tank [28], [29]. However, there is current with large peak value flowing back to the input source, hindering efficiency improvement. Another method obtains the reverse current in primary side of coupled inductor through reflection current of secondary side. Although there is still flow-back current, the current peak has been reduced significantly. Unfortunately, the strict control sequence makes it impractical.

This paper presents an active resonant soft-switching method to overcome the above-mentioned issue for an advanced high step-up interleaved converter. The proposed converter reaches high voltage gain at medium power rating, meanwhile, the input current ripple and the voltage stress of main switches are both small. The active switches can achieve both ZVS turn-ON and ZVS turn-OFF, the reverse-recovery loss of output diode is cut down. Due to the cross coupling of the coupled inductor, the converter has ability to automatically balance two branch currents, even in the case that the duty cycle of switches or coupled inductors is asymmetric. The descriptions of topology and its operation principle are provided in Section II. The performance analysis is discussed in Section III. Then, in Section IV, a general soft-switching method is derived to extend its application

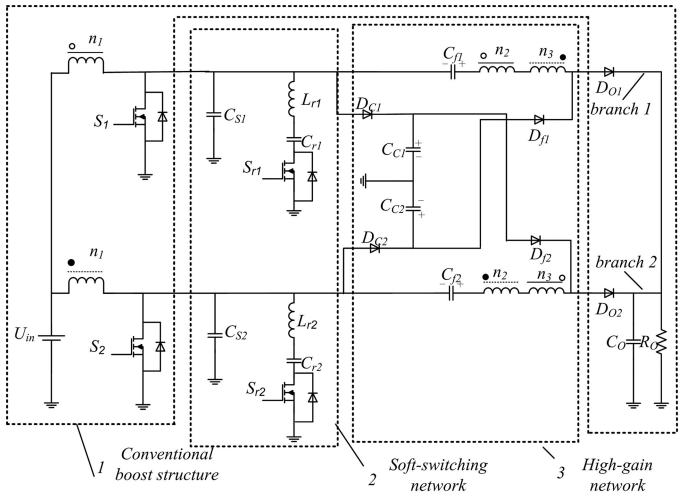

Fig. 2. Proposed converter.

in high step-up converters. In Section V, a prototype is built and tested to validate the theory in Sections II and III. Finally, Section VI concludes this paper.

II. Operation Principle

The proposed converter is shown in Fig. 2 where a conventional interleaved boost converter is located in the dashed block 1, an auxiliary circuit used to realize soft switching is located in the dashed block 2, a coupled inductor and a voltage multiplier are located in the block 3. There are two coupled inductors each with three windings in the proposed converter. The coupling references are marked by "○" and "•." The primary windings of two coupled inductors with n_1 turns are employed as the filter inductors. The secondary windings of two coupled inductors with n_2 turns are used to multiply voltage. The third windings of two coupled inductors with n_3 turns embedded into other branch are used to automatically balance the current and multiply voltage. The clamped-diodes D_{C1}, D_{C2} and clamped-capacitors C_{C1}, C_{C2} are used to recover the energy of leakage inductance and reduce the voltage spike of main switch. The feedforward diodes D_{f1}, D_{f2} and switched-capacitors C_{f1}, C_{f2} are used to improve voltage gain. The two auxiliary circuits are composed of absorption capacitors C_{S1}, C_{S2}, resonant inductors L_{r1}, L_{r2}, resonant capacitors C_{r1}, C_{r2}, and auxiliary switches S_{r1}, S_{r2}, respectively. Two branches are coupled together though the coupled inductors and switched capacitors.

The equivalent circuit of the proposed converter based on the coupled inductor analysis is shown in Fig. 3(a) where two coupled inductors are represented by their equivalent transformer models. The equivalent transformer models include ideal transformers, magnetizing inductances L_{m1}, L_{m2}, and leakage inductances L_{k1}, L_{k2} referred to the primary, respectively. L_{1P} and L_{2P} are the primary windings of ideal transformers, whereas L_{1S1}, L_{1S2}, L_{2S1}, and L_{2S2} are the secondary windings of ideal transformers. To simplify analysis, the turns ratio of two coupled inductors are set as $N = n_2/n_1 = n_3/n_1$.

Considering soft-switching analysis, the equivalent circuit in Fig. 3(a) could be simplified further as Fig. 3(b).

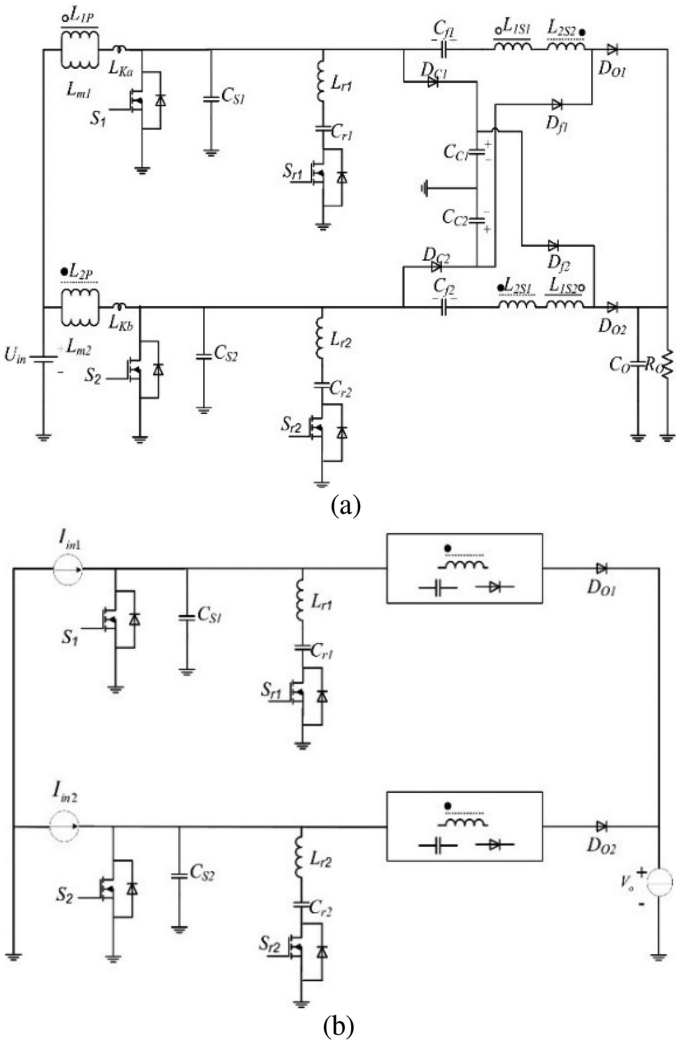

Fig. 3. Equivalent circuit of the proposed converter. (a) Coupled inductor based. (b) Soft switching based.

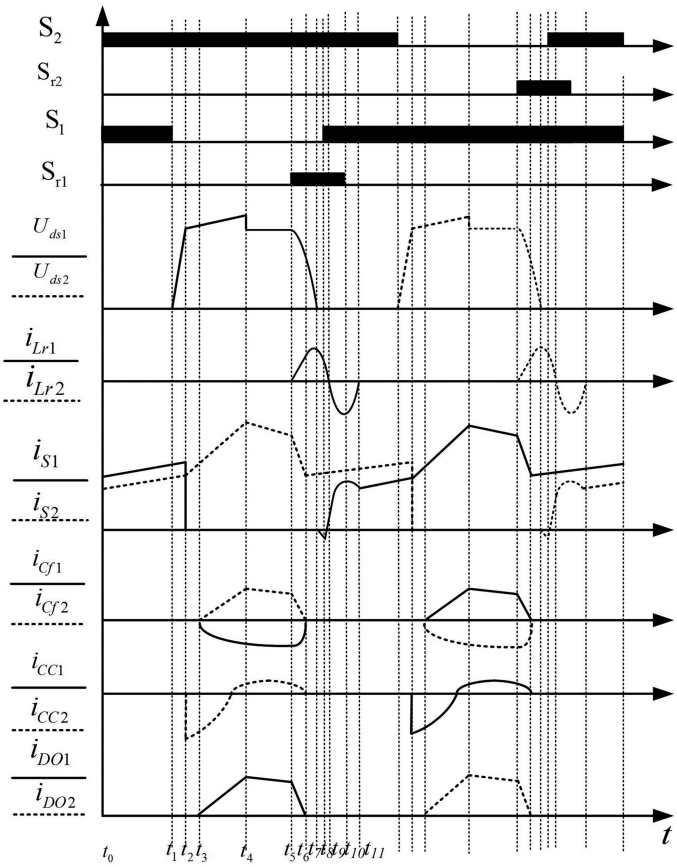

Fig. 4. Key waveforms of the proposed converter.

Under steady state, the proposed converter has 22 operation modes during whole switching period. Due to the symmetry of the topology, only 11 modes in half period are analyzed in this paper. The key waveforms are shown in Fig. 4. The operation modes are described in details as follows.

1) *Mode 1 [t_0–t_1]:* In the mode, main switches S_1 and S_2 are turned ON, and diodes D_{O1}, D_{O2}, D_{C1}, D_{C2}, D_{f1}, and D_{f2} are reverse-biased, as shown in Fig. 5(a). Magnetizing inductance L_{m1}, L_{m2} and leakage inductance L_{Ka}, L_{Kb} are charged linearly. The current rising rate of the leakage inductance is given by

$$\frac{di_{LKa}}{dt} = \frac{U_{\text{in}}}{L_{Ka} + L_{m1}} \tag{1}$$

$$\frac{di_{LKb}}{dt} = \frac{U_{\text{in}}}{L_{Kb} + L_{m2}}. \tag{2}$$

2) *Mode 2 [t_1–t_2]:* As shown in Fig. 5(b), the mode starts at t_1, when main switch S_1 is turned OFF. Absorption capacitors C_{S1} is charged by magnetizing inductance L_{m1} and leakage inductance L_{Ka}. The drain-to-source voltage of main switch U_{S1_ds} increases linearly, whereas the reverse voltage across diode D_{C1} decreases. Thus, main switch S_1 can achieve ZVS turn-OFF. This mode ends until the reverse voltage across diode D_{C1} decreases down to zero. U_{ds1} is given by

$$u_{S1\_ds}(t) = \frac{i_{Lm1}(t - t_1)}{C_{S1}}. \tag{3}$$

3) *Mode 3 [t_2–t_3]:* As shown in Fig. 5(c), the mode starts at t_2, when clamp diode D_{C1} starts to conduct. Clamped capacitor C_{C1} is charged by the current of magnetizing inductance L_{m1} and leakage inductance L_{Ka}. The drain-to-source voltage of main switch U_{S1_ds} is clamped by capacitor C_{C1}

$$u_{S1\_ds}(t) = u_{S1\_ds}(t_2) + \frac{i_{Lm1}(t_2)}{C_{C1}}(t - t_2). \tag{4}$$

4) *Mode 4 [t_3–t_4]:* At t_3, feedforward diode D_{f2} and output diode D_o start to conduct. The current of output diode D_o increases gradually, whereas the current of clamped diode D_{C1} decreases. Both of their charging rates are controlled by leakage inductance L_{Ka}. Thus, the reverse-recovery problem of diodes is alleviated. Meanwhile, switched capacitor C_{f2} is charged by C_{C1}, L_{1S2}, and L_{2S1}. And C_{f1}, L_{1S1}, L_{2S2}, L_{m1}, L_{ka}, and U_{in} in series charges the output capacitor C_o for high gain. The current

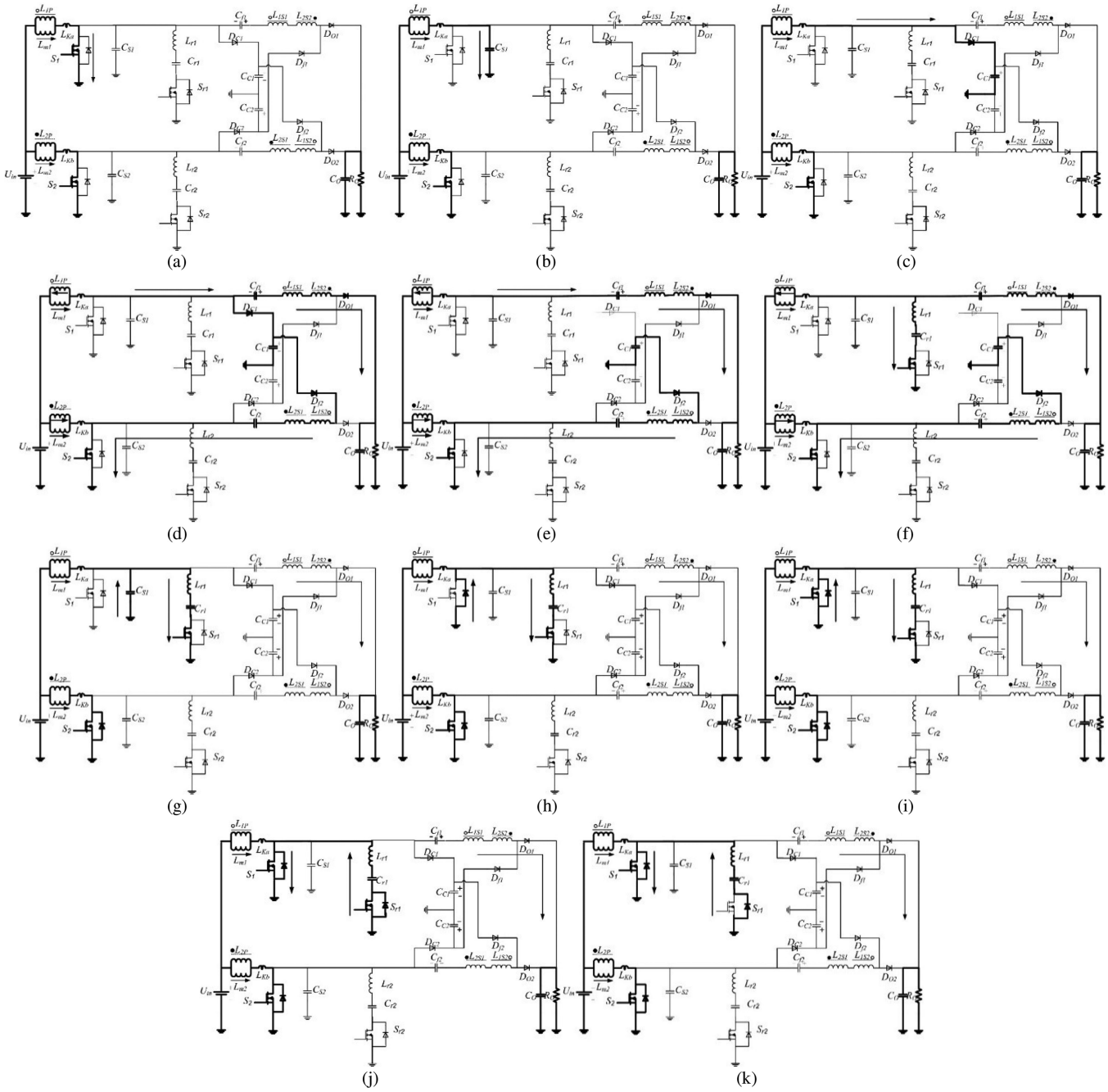

Fig. 5. Operation modes of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9. (j) Mode 10. (k) Mode 11.

expression could be given as

$$\frac{di_{L1P}}{dt} = \frac{di_{L2P}}{dt} = \frac{NU_{CC1} + U_{CC1} + U_{Cf1} - U_O}{N(L_{Ka} + L_{Kb})} \tag{5}$$

$$i_{DO1}(t) = \frac{NU_{CC1} + U_{CC1} + U_{Cf1} - U_O}{2N^2(L_{Ka} + L_{Kb})}(t - t_3) \tag{6}$$

$$i_{Df2}(t) = \frac{NU_{CC1} + U_{CC1} + U_{Cf1} - U_O}{2N^2(L_{Ka} + L_{Kb})}(t - t_3) \tag{7}$$

$$i_{DC1}(t) = i_{Lm1}(t) - (N+1)i_{DO1}(t) - Ni_{Df2}(t) \tag{8}$$

$$i_{S2} = i_{Lm2}(t) + Ni_{DO1}(t) + (N+1)i_{Df2}(t). \tag{9}$$

5) *Mode 5 [t_4–t_5]:* As shown in Fig. 5(e). This mode starts at t_4, when the current of clamp diode D_{C1} decreases down to zero and D_{C1} will be reverse biased. The mode lasts until auxiliary switch S_{r1} is turned ON. The current

expression could be calculated as

$$\frac{di_{L1P}}{dt} = \frac{di_{L2P}}{dt} = \frac{U_O - U_{Cf1}}{L_{Ka} + L_{Kb}} + \frac{(1+N)(U_{CC1} - U_{Cf2})}{N(L_{Ka} + L_{Kb})} \tag{10}$$

$$i_{DO1}(t) = i_{DO1}(t_4) + \frac{N(U_O - U_{Cf1}) + (1+N)(U_{CC1} - U_{Cf2})}{N(L_{Ka} + L_{Kb})} \cdot (t - t_4) \tag{11}$$

$$i_{Df2} = i_{Df2}(t_4) + \frac{1-N}{N} \cdot \frac{N(U_O - U_{Cf1}) + (U_{CC1} - U_{Cf2})(1+N)}{N(L_{Ka} + L_{Kb})}(t - t_4). \tag{12}$$

6) *Mode 6 [t_5–t_6]:* At t_5, auxiliary switch S_{r1} is turned ON. The resonant unit with L_{r1} and C_{r1} in series will be excited by the constant voltage of V_{Cs1} clamped by branch circuit 1. The drain-source current of S_{r1}, which is controlled by resonant inductors L_{r1}, increases in resonance. Thus, S_{r1} is turned ON under ZCS condition. Meanwhile, the current of diodes D_{f2} and D_o decreases in resonance as well. Resonant period T_{o1} could be obtained as

$$T_{o1} = 2\pi\sqrt{L_{r1} \cdot C_{r1}}. \tag{13}$$

7) *Mode 7 [t_6–t_7]:* At t_6, when the resonant current rises up to be larger than branch current i_{Lk1}, diodes D_{f2} and D_o will be reverse-biased. Meanwhile, absorption capacitors C_{S1}, resonant inductors L_{r1}, and resonant capacitors C_{r1} will compose a new resonant loop. U_{S1_ds} begins to decreases in resonance. Resonance period T_{o2}, different with mode 6, is obtained as

$$T_{o2} = 2\pi\sqrt{L_{r1} \cdot \frac{C_{s1} \cdot C_{r1}}{C_{s1} + C_{r1}}}. \tag{14}$$

8) *Mode 8 [t_7–t_8]:* At t_7, U_{S1_ds} has decreased down to zero, and body diode of S_1 starts to conduct. Another new resonant loop, composed of resonant inductors L_{r1} and resonant capacitors C_{r1} will be established up. The resonance period frequency is same as that in mode 6.
9) *Mode 9 [t_8–t_9]:* As shown in Fig. 5(i). At t_8, main switch S_1 is turned ON under ZVS condition, because its body diode has conducted before.
10) *Mode 10 [t_9–t_{10}]:* As shown in Fig. 5(j). At t_9, the drain-source current of S_{r1} reverses its direction. The body diode of S_{r1} starts to conduct.
11) *Mode 11 [t_{10}–t_{11}]:* As shown in Fig. 5(k). At t_{10}, auxiliary switch S_{r1} is turned OFF under ZVS condition, because it body diode has conducted before.

A similar operation occurs in the other eleven modes of one switching period.

III. Performance Analysis and Design

A. Voltage Gain

The duty cycle of the control signal is defined as

$$D = \frac{T_1}{T} \tag{15}$$

where T and T_1 are the switching period of main switch and conduction time of main switch S_1 (S_2) in one switching period, respectively. D denotes the duty cycle of main switch S_1 (S_2). And it is obvious that the duty cycle should satisfy $0.5 < D < 1$ to maintain high gain because no voltage will be outputted during the turn-OFF of both main switches.

To simplify the circuit performance analysis, leakage inductance L_k is neglected, and assume that $L_{m1} = L_{m2}$, $C_{C1} = C_{C2}$, and $C_{f1} = C_{f2}$ because of the symmetry of the topology. Also, the voltage ripple across clamped-capacitor and switched-capacitor is neglected since the clamped-capacitor and switched-capacitor are taken as constant voltage sources over the whole switching period. It is worth mentioning that the auxiliary resonant circuit will not bring effect to the voltage gain of the proposed converter because it never locates at power transferring path, which would be verified by following formulas and experimental results in Section V.

When main switch S_1 is turned ON, the charging voltage of magnetizing inductance L_{m1} is given by

$$U_{Lm1\_\mathrm{char}} = U_{\mathrm{in}}. \tag{16}$$

When main switch S_1 is turned OFF, considering symmetry, the discharging voltage of magnetizing inductance L_{m1} is given by

$$U_o = (N+1)U_{Lm1\_\mathrm{dischar}} + (N+1)U_{\mathrm{in}} + U_{Cf1} \tag{17}$$

$$U_{Cf2} = NU_{Lm1\_\mathrm{dischar}} + NU_{\mathrm{in}} + U_{CC1} \tag{18}$$

$$U_{\mathrm{in}} + U_{Lm1\_\mathrm{dischar}} - U_{CC1} = 0 \tag{19}$$

$$U_{Cf1} = U_{Cf2}. \tag{20}$$

With combination formulas (17)–(20) and by applying the voltage–second balance principle to the magnetizing inductance L_{m1}, the voltage gain and voltage across clamped-capacitor and switched-capacitor are obtained as, respectively

$$M = \frac{U_o}{U_{\mathrm{in}}} = \frac{2(1+N)}{1-D} \tag{21}$$

$$U_{Cc1} = U_{Cc2} = U_{Cc} = \frac{U_{\mathrm{in}}}{1-D} \tag{22}$$

$$U_{Cf1} = U_{Cf2} = U_{Cf} = \frac{1+N}{1-D}U_{\mathrm{in}}. \tag{23}$$

From formula (21), it is obvious that voltage gain M depends on duty cycle D and turns ratio N. The relationship curve of voltage gain versus duty cycle with different turns ratio is shown in Fig. 6. At certain turns ratio N, as duty cycle D increases, voltage gain M will increase. Also, the gain rises with the turns ratio increasing. It can avoid the use of extreme duty cycle in high gain applications, reducing current ripple and switching loss.

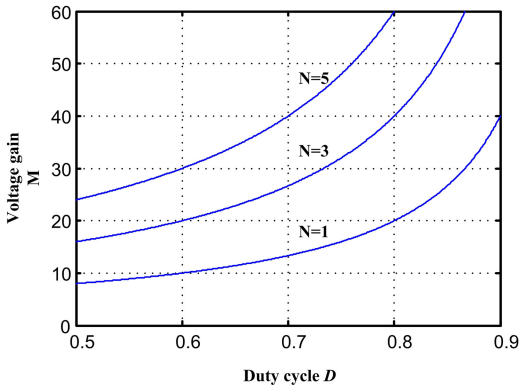

Fig. 6. Relationship curve of voltage gain versus duty cycle with different N.

Known from above-mentioned analysis, the auxiliary resonant circuit very leads little gain loss to the converter.

Considering the effect of the leakage inductance, the output voltage gain is given by

$$M = \frac{2(N+1)}{1-D} \cdot \frac{1}{1+8N^2 k_m/(1-D)^2} \tag{24}$$

where $k_m = L_{Lk1'} \cdot f_s/R_o$. f_s is the switching frequency and $L_{Lk1'}$ is the summation of the leakage inductances, including the primary leakage inductance and reflected leakage inductance of the second and third windings. The detailed analysis could be referred in [25], which is ignored here.

B. Voltage and Current Across Power Devices

Considering the symmetrical parameters in two branches, the voltage/current stress across main switches S_1 and S_2, auxiliary switches S_{r1} and S_{r2}, and clamped diodes D_{C1} and D_{C2} are all equal, the same as the voltage/current stress across clamped capacitors C_{C1} and C_{C2}, and coupled inductors L_1 and L_2.

It is obvious that the main switches, auxiliary switches, clamped diodes, and clamped capacitors suffer the same voltage stress

$$U_S = U_{Sr} = U_{D_c} = \frac{U_{\text{in}}}{1-D} = \frac{U_o}{2(1+N)} = U_{C_C}. \tag{25}$$

The voltage stress across output diodes D_{O1} and D_{O2} can be derived as

$$U_{Do} = U_o - U_{C_C} = \frac{1+2N}{1-D}U_{\text{in}} = \frac{1+2N}{2(1+N)}U_o. \tag{26}$$

As shown in (24) and (25), the voltage stress across main switches and output diode are both determined by the turns ratio at desired output voltage. The plot of normalized switch/output diode voltage stress versus turns ratio is shown in Fig. 7. As the turns ratio increases, the voltage stress of main switches with the maximum voltage stress of halved output voltage decreases gradually. Therefore, the low rated voltage MOSFET with small ON-resistance could be utilized in high voltage gain application, which reduces conduction loss significantly. Meanwhile, as the turns ratio increases, the voltage stress across output diodes increases gradually. But the voltage stress across output diodes

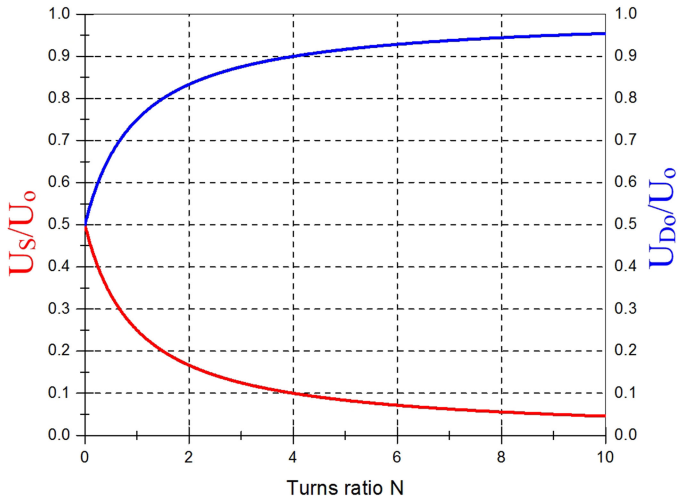

Fig. 7. Plot of normalized switch/output diode voltage stress versus turns ratio.

is always lower than output voltage and the minimum voltage stress halves output voltage.

The voltage stress U_{Df} across the feedforward diodes D_{f1} and D_{f2} equals to voltage stress of output diodes, which can be derived as

$$U_{Df} = U_{Df1} = U_{Df2} = U_o - U_{C_C} = \frac{1+2N}{1-D}U_{\text{in}} = \frac{1+2N}{2(1+N)}U_o. \tag{27}$$

According to the ampere–second balance principle, the average current of output capacitor will be zero in whole switching period. Thus, the average current of output diode D_o equals to output current I_o.

To simplify the analysis, assume that the charging/discharging current in the loops approaches linear mode. Consequently, the peak value of the output diode current could be derived as

$$i_{D_{o1\_\text{peak}}} = \frac{I_o}{1-D}. \tag{28}$$

Similarly, the peak value of feedforward diodes is given as

$$i_{D_{f1\_\text{peak}}} = \frac{I_o}{1-D}. \tag{29}$$

The peak value of main switch S_1 can be expressed as

$$i_{S1\_\text{peak}} = \frac{MI_o}{2} + Ni_{D_{f1\_\text{peak}}} + Ni_{D_{o2\_\text{peak}}}. \tag{30}$$

By substituting (20) into (21), the peak value of the main switch can be given out

$$i_{S1\_\text{peak}} = \left(\frac{M}{2} + \frac{N}{D(1-D)}\right) I_o. \tag{31}$$

The current stress of auxiliary switch is determined by resonant loop

$$i_{Sr1\_\text{peak}} = \frac{U_{Cc1}}{Z_{o1}}. \tag{32}$$

Moreover, the RMS current of main switches, auxiliary switches, capacitors, and coupled inductors can be derived by (33) shown at the bottom of this page

$$I_{S_{r1\_\mathrm{rms}}} = \frac{[(1+N)D+N]\,I_o}{\sqrt{2D\,(1-D)}} \tag{34}$$

$$I_{Cf1\_\mathrm{rms}} = \frac{\sqrt{3}}{3} I_o \sqrt{2\,(1-D)} \tag{35}$$

$$I_{Lm1\_\mathrm{rms}} = \frac{MI_o}{2}. \tag{36}$$

Furthermore, the diodes suffers the same average current, which can be derived by

$$I_{Do1\_ave} = I_{Dc1\__{ave}} = I_{Df1\__{ave}} = \frac{I_o}{2}\,(1-D)\,. \tag{37}$$

C. Design of Coupled Inductor and Capacitors

The coupled-inductor design should make sure the converter work in continuous current mode. The peak current of magnetizing inductance at boundary current mode (BCM) could be given by

$$i_{L_m\_\mathrm{peak}} = \frac{U_{\mathrm{in}} D}{L_m f_s}. \tag{38}$$

Correspondingly, at BCM mode, the average current of magnetizing inductance is obtained as

$$i_{L_m\_ave} = \frac{i_{L_m\_\mathrm{peak}}}{2} = \frac{(N+1)I_o}{2(1-D)} + \frac{NI_o}{2D} = \frac{(N+D)I_o}{2D(1-D)}. \tag{39}$$

Thus, considering formulas (21), (31), and (32), the boundary magnetizing inductance could be derived out

$$L_m = \frac{R_{oB} D^2 (1-D)^2}{2f_s(N+1)(N+D)} \tag{40}$$

where R_{oB} is the load at the boundary condition. Usually, 20% of full load is taken for the BCM.

Finally, a toroidal sendust cores with 37 turns in the primary winding and 37 turns in the second winding is utilized for the proposed converter in the prototype.

Depending on switching frequency f_s and their voltage ripple, the value of capacitors $C_{f1}, C_{f2}, C_{C1}, C_{C2}$, and C_o is designed. The corresponding equations are given by

$$\begin{cases} C_{f1} \geq \frac{I_o(1-D)}{2f_s \Delta U_{Cf1}}, C_{f2} \geq \frac{I_o(1-D)}{2f_s \Delta U_{Cf2}} \\ C_{Cc1} \geq \frac{I_o(1-D)}{2f_s \Delta U_{Cc1}}, C_{Cc2} \geq \frac{I_o(1-D)}{2f_s \Delta U_{Cc2}} \\ C_o \geq \frac{I_o D}{2f_s \Delta U_o} \end{cases} \tag{41}$$

where $\Delta V_{Cf1}, \Delta V_{Cf2}, \Delta V_{Cc1}, \Delta V_{Cc2}$, and ΔV_{Co} are the voltage ripple of capacitors C_{f1}, C_{f2}, C_{c1}, C_{c2}, and C_o, respectively. Generally speaking, a large capacitor helps to reduce the voltage ripple, however, the bulky size and expensive cost may be inevitable. Hence, the tradeoff should be considered when selecting a capacitor.

In order to achieve ZVS for main switches S_1 and S_2, the turn-OFF interval of the main switch should be shorter than the half of resonant period, which is determined by the leakage inductance and clamped capacitor. The corresponding equation could be yielded as

$$C_{r1} \geq \frac{(1-D_{\max})^2}{\pi^2 L_{r1} {f_s}^2} \tag{42}$$

where $D_{\max}$ is the maximum value of duty cycle.The voltage rising ratio should be less than turn-OFF ratio of the MOSFETs to guarantee ZVS under rated output power, hence, the value of absorption capacitance yields

$$C_{s1} = \frac{I_{Lka} t}{2U_{Cc1}} > \frac{MI_{0\_\mathrm{rated}} t_{\mathrm{off}}}{4U_{Cc1}} \tag{43}$$

where t_{off} denotes the turn-OFF time of utilized MOSFETs.

D. Efficiency Analysis

To verify the converter performance, the loss mechanism for the proposed converter is analyzed. Before that, some assumptions are made: switching loss is ignored because of ZVS turn-ON/OFF, C_r is negligible considering ZVS turn-ON of MOSFET, the influence from the current ripple of L_m is negligible, loss in auxiliary circuit is negligible, two branches have the symmetric parameters. Meanwhile, it is assumed that $V_{F,D}$ denotes the forward voltage of diode, r_S represents the conduction resistance of MOSFET, r_{Lm} denotes the equivalent series resistance (ESR) of coupled inductor, and r_C denotes the ESR of capacitor.

The power loss of the proposed converter include loss related to switches, diodes, magnetic, and capacitor components. Next, calculate loss distributed in different components.

The conduction loss of S_1 is calculated as follows:

$$\begin{aligned} P_{\mathrm{Cond},S1} = {} & \left\{ (2D-1)\left[\left(\frac{MI_o}{2}\right)^2 + 2\left(\frac{U_{\mathrm{in}}(1-D)T_s}{2L_M}\right)^2\right] \right. \\ & + (1-D)\left\{ \frac{U_{\mathrm{in}}(1-D)T_s MI_o}{2L_M} - \frac{[U_{\mathrm{in}}(1-D)T_s]^2}{6{L_M}^2} \right. \\ & \left.\left. + \left[\frac{MI_o}{2} - \frac{U_{\mathrm{in}}(1-D)T_s}{2L_M}\right]^2 \right\} \right\} r_S. \end{aligned} \tag{44}$$

Considering forward voltage $V_{F,D}$, the conduction loss of diode D_{o1} yields

$$P_{\mathrm{Cond},D_{o1}} = \frac{(1-D)V_{F,D} I_o}{2}. \tag{45}$$

$$I_{S1\_\mathrm{rms}} = \sqrt{\begin{array}{c} (2D-1)\left[\left(\frac{MI_o}{2}\right)^2 + 2\left(\frac{U_{\mathrm{in}}(1-D)T_s}{2L_M}\right)^2\right] \\ + (1-D)\left\{\frac{U_{\mathrm{in}}(1-D)T_s MI_o}{2L_M} - \frac{[U_{\mathrm{in}}(1-D)T_s]^2}{6{L_M}^2} + \left[\frac{MI_o}{2} - \frac{U_{\mathrm{in}}(1-D)T_s}{2L_M}\right]^2\right\} \end{array}} \tag{33}$$

Similarly, the conduction loss of diode D_{C1} and D_{f1} yields, respectively

$$P_{\mathrm{Cond},D_{c1}} = \frac{(1-D)V_{F,D}I_o}{2} \tag{46}$$

$$P_{\mathrm{Cond},D_{f1}} = \frac{(1-D)V_{F,D}I_o}{2}. \tag{47}$$

Considering the ESR of capacitor r_C, the conduction loss of switched capacitor C_{f1} yields

$$P_{Cf1} = (1-D)\frac{4}{3}{I_o}^2 r_c. \tag{48}$$

The loss of coupled inductor comes from winding loss and core loss. As to winding loss P_{Lm1}, it depends on the parasitic resistance

$$P_{Lm1} = \frac{M^2 {I_o}^2}{4} r_{Lm}. \tag{49}$$

Referred the analysis method, the core loss density P_C is calculated as

$$P_C = k \cdot f_s^{\alpha} \cdot B_m^{\beta} \tag{50}$$

where the unit of P_C is *W/m*^{3}, α, β, and k are *Steinmetz* parameter, which are determined by core material and provided by manufacturer. For ferrite core material, typical value of α ranges from 1 to 2.

According to Faraday's law, it yields

$$V_{L_m} = N_p \frac{d\varphi(t)}{dt} = N_p \cdot A_c \frac{dB(t)}{dt} \tag{51}$$

where A_c represents the sectional area of different core materials and N_p denotes the turns number of the winding.

Combing the above-stated formulas and voltage waveform of the excitation inductor, the maximum magnetic flux density of coupled inductor ΔB could be obtained as

$$\Delta B = \frac{1}{N_p \cdot A_c}\int_0^{DT_s} U_{Lm}\,dt = \frac{1}{N_p \cdot A_c}\int_0^{DT_s} U_{\mathrm{in}}\,dt = \frac{U_{\mathrm{in}}DT_s}{N_p \cdot A_c}. \tag{52}$$

The core loss of coupled inductor satisfies $P_{\mathrm{Core}} = P_C V_c$ where V_c denotes the volume of coupled inductor. Hence, considering $B_m = \Delta B$, the total core loss can be expressed as

$$P_{\mathrm{Core}} = 2P_C \cdot V_c = 2k \cdot f_s^{\alpha} \cdot B_m^{\beta} \cdot V_c = k \cdot f_s^{\alpha} \cdot \left\{\frac{U_{\mathrm{in}}DT_s}{N_p \cdot A_c}\right\}^{\beta} \cdot V_c. \tag{53}$$

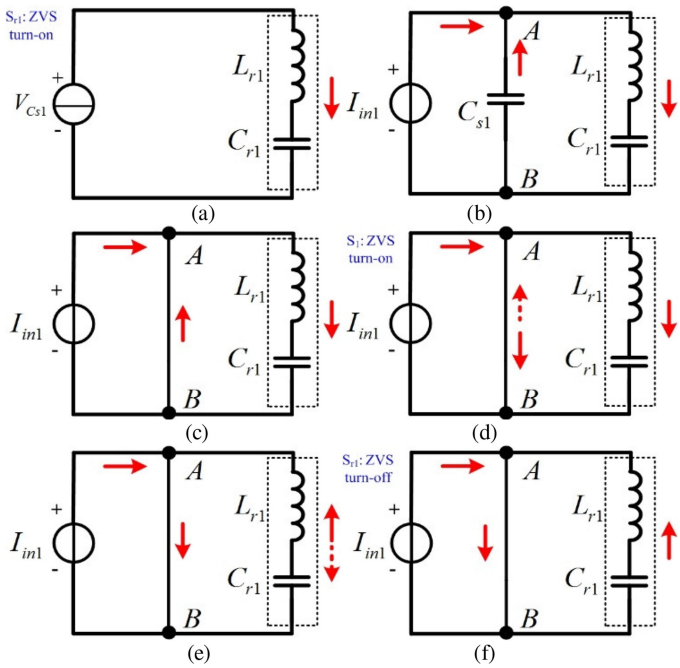

Fig. 8. Equivalent circuits at resonant modes. (a) Mode 6. (b) Mode 7. (c) Mode 8. (d) Mode 9. (e) Mode 10. (f) Mode 11.

The resonance loss is calculated as

$$P_{\mathrm{res}} = \left\{\frac{[(1+N)D+N]\,I_o}{\sqrt{2D(1-D)}}\right\}^2 \cdot r_S \cdot \frac{T_{r1}}{T_s}. \tag{54}$$

To sum up, the power loss of the proposed converter in one switching period yields

$$P_{\mathrm{Loss}} = 2(P_{\mathrm{Cond},S1} + P_{\mathrm{Cond},D_{o1}} + P_{\mathrm{Cond},D_{c1}} + P_{\mathrm{Cond},D_{f1}} + P_{Cf1} + P_{Lm1} + P_{\mathrm{Core}} + P_{\mathrm{res}}). \tag{55}$$

Finally, the efficiency of the proposed converter can be obtained as (56) shown at the bottom of this page, where P_o represents the output power and $P_o = U_o I_o$.

IV. Soft Switching

A. Soft-Switching Condition

For active switches, with the help of the auxiliary resonant circuit, main switches S_1 and S_2 can achieve ZVS turn-ON and ZVS turns-OFF. The equivalent circuits at resonant modes are shown in Fig. 8 where points A and point B connect in short at ON-state of S_1. Due to relatively short interval for resonant period and large inductance for coupled inductor, $I_{\mathrm{in}1}$ could be taken as a constant current source. For diodes, the current rising

$$\eta = \frac{P_o}{P_o + P_{\mathrm{Loss}}} = \frac{P_o}{P_o + \left(\begin{array}{l} 2((2D-1)((\frac{MI_o}{2})^2 + (\frac{U_{\mathrm{in}}(1-D)T_s}{L_M})^2) + (1-D)(\frac{U_{\mathrm{in}}(1-D)T_s M I_o}{L_M} \\ -\frac{(U_{\mathrm{in}}(1-D)T_s)^2}{3{L_M}^2} + 2(\frac{MI_o}{2} - \frac{U_{\mathrm{in}}(1-D)T_s}{2L_M})^2)) + \frac{[(1+N)D+N]^2 {I_o}^2 T_{r1}}{D^2(1-D)^2 T_s} \end{array}\right) r_S + 3(1-D)V_{F,D}I_o + \frac{4(1-D){I_o}^2 r_C}{3} + \frac{M^2 {I_o}^2 r_{Lm}}{2} + 2k \cdot f_s^{\alpha}\left\{\frac{V_i DT_s}{N_p \cdot A_c}\right\}^{\beta} V_c} \tag{56}$$

rate of clamp diodes, output diodes, and feedforward diodes is controlled by leakage inductance. Therefore, there is alleviated reverse-recovery problem for them.

When main switch S_1 is turned OFF at mode 2, it realizes the ZVS operation due to the absorption capacitor. In mode 6, S_{r1} could be turned on under the ZCS condition. Resonance unit of L_{r1} and C_{r1} in series will resonate with different sub-circuits during modes 6 to 8, as shown in Fig. 5(f)–(h). Corresponding equivalent resonant circuits are shown in Fig. 8(a)–(c). Then, when the absorption capacitor is discharged by the resonant inductor completely, the ZVS turn-ON condition will be created for main switch S_1 because its anti-parallel body diode has conducted. Next, when resonant capacitor C_{r1} is discharged with reverse current direction, the condition of ZVS turn-OFF for auxiliary S_{r1} has produced.

Based on above-mentioned analysis, in order to realize soft switching, there are some constraint conditions to be considered. First, main switch S_1 should be turned ON after its body diode conducts, as shown in Fig. 4(g). Due to relative transient interval for mode 7, it yields

$$t_l = t_8 - t_5 \le \frac{1}{2}T_{o1} \tag{57}$$

where t_l is the interval time between rising edge of gate signal for S_{r1} and that for S_1. Namely, t_l denotes the leading turn-ON time between S_{r1} and S_1. T_{01} represents the resonant period.

Second, S_{r1} should be turned OFF timely to make sure the interval of turn-ON $t_{\text{on\_}Sr1}$ is shorter than the whole resonant period but more than the half of resonant period, as shown in Fig. 5(f) and (g), respectively. The responding equations are given by

$$\frac{1}{2}T_{o1} \le t_{10} - t_5 = t_{\text{on\_}Sr1} \le T_{o1}. \tag{58}$$

Finally, the absorption capacitor should be discharged completely by the resonant inductor to guarantee conduction for anti-parallel body diode of main switch S_1

$$\frac{1}{2}L_{r1}(i_{Lr1}(t_6) - i_{Lka}(t_6))^2 \ge \frac{1}{2}C_{s1}{U_{Cs1}}^2(t_6). \tag{59}$$

Noticing that

$$\begin{cases} U_{Cs1}(t_6) = U_{Cc1} \\ i_{Lka}(t_6) = i_{Lka}(t_7) \approx i_{Lm1} - N(i_{Df2} + i_{Do1}) \\ \qquad\quad = (\frac{M}{2} - \frac{N}{1-D})I_o. \end{cases} \tag{60}$$

And the currents of resonant inductor i_{Lr1} at t_6 and t_7 can be obtain as

$$\begin{cases} i_{Lr1}(t_6) = \frac{U_{Cs1}(t_6)}{Z_{o1}} \sin\omega_{o1}(t_6 - t_5) \\ i_{Lr1}(t_7) = i_{Lr1}(t_6)\cos(\omega_{o2}(t_7 - t_6)) \\ \qquad\quad - \frac{U_{Cr1}(t_6)}{Z_{o2}} \sin(\omega_{o2}(t_6 - t_5)) \end{cases} \tag{61}$$

where $\omega_{o1}=1/\sqrt{L_{r1}\cdot C_{r1}}$, $Z_{o1}=\sqrt{L_{r1}/C_{r1}}$, $\omega_{o2}=1/\sqrt{L_{r1}\cdot C_{r1}\cdot C_{S1}/(C_{r1}+C_{S1})}$, $Z_{o2}=\sqrt{L_{r1}\cdot C_{S1}/C_{r1}(C_{r1}+C_{S1})}$.

Considering the relatively short interval for mode 7, it is ignored in the resonant process. And i_{Lka} is established mainly during mode 6 (t_5–t_6). At t_7, end of mode 7, if the current of resonant inductor i_{Lr1} reaches its maximum value and is more than the current of leakage inductance i_{Lka}, the critical condition of ZVS turn-ON would be produced for the main switch. Hence, it should satisfy the following expression at least:

$$i_{Lr1}(t_7) \approx i_{Lr1}(t_6) \approx \frac{U_{Cs1}(t_6)}{Z_{o1}} \sin\frac{\pi}{2} = \frac{U_{Cs1}(t_6)}{Z_{o1}}. \tag{62}$$

With combination of formulas (59)–(62), it yields

$$\frac{U_o(1-D)}{2(1+N)}\left(\sqrt{\frac{C_{r1}}{L_{r1}}} - \sqrt{\frac{C_{s1}}{L_{r1}}}\right) = U_{\text{in}}\left(\sqrt{\frac{C_{r1}}{L_{r1}}} - \sqrt{\frac{C_{s1}}{L_{r1}}}\right) \ge I_o. \tag{63}$$

It is revealed that the smaller value of resonant inductor guarantees ZVS turn-ON for the main switch under the given parameters and load current.

To sum up, if the soft-switching operation is implemented, formulas (57), (58), and (63) should be satisfied.

From (45), it is obvious that the ZVS turn-ON condition for main switch S_1 is dependent on resonance inductance rather than load. The boundary cure between ZVS and non-ZVS range against L_{r1} is shown in Fig. 9. Considering the parameters based on design in Sections III-B and C, if it is guaranteed to realize ZVS turn-ON condition for the main switch from light load to full load, the boundary of resonant inductance $L_{r1\max\_ZVS}$ is 2 μH, as the red arrow shown in the curve. On the other hand, the ZVS will be lost below the resonant inductance value of 2 μH. Thus, it seems that a small resonant inductance is preferable to a wide ZVS range. However, small resonant inductance will make much current stress for auxiliary switch, bringing about unnecessary switching loss in auxiliary circuit. Therefore, L_{r1} should be designed reasonably.

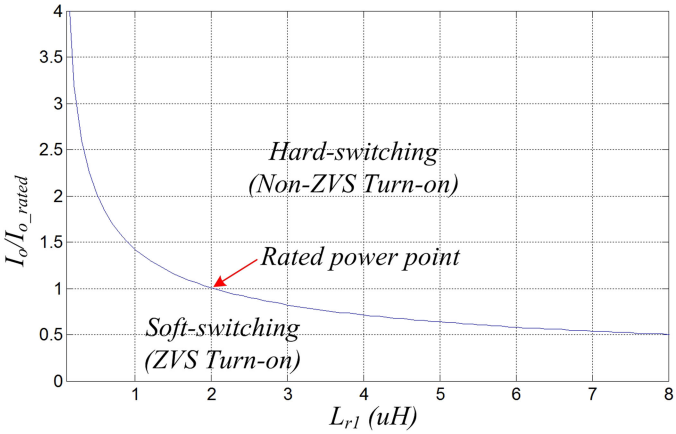

Fig. 9. ZVS load boundary according to resonant inductance.

B. General Soft-Switching Method for High-Step-Up Converter

To provide a general soft-switching method for high step-up converter, one branch of the proposed topology is given equivalence further to denote the general high step-up converter, as shown in Fig. 10. Correspondingly, considering some modes have short internal, the key waveforms of the proposed converter,

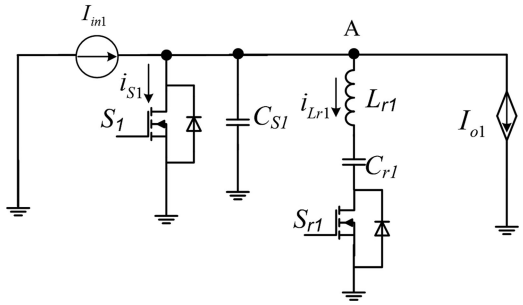

Fig. 10. Equivalent circuit of one branch in the proposed converter.

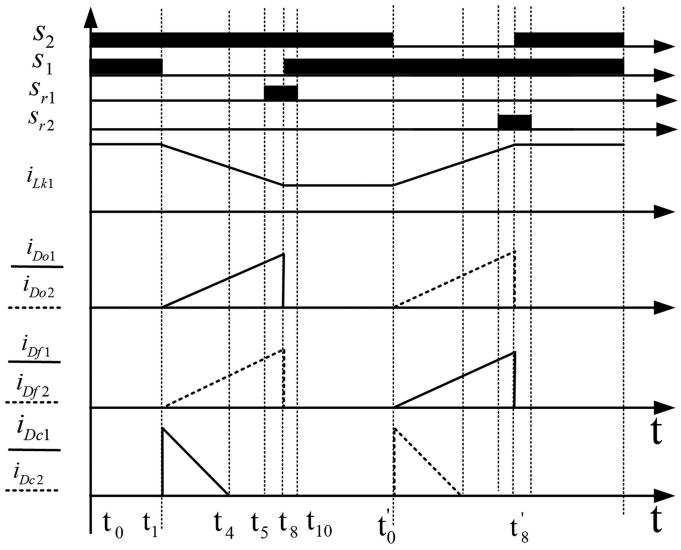

Fig. 11. Simplified operation waveforms.

TABLE I
PROTOTYPE PARAMETERS AND COMPONENTS

Parameters	Value/Description
Input voltage (U_{in})	15~30 V
Output voltage (U_o)	270 V
Maximum output power(P_o)	1000 W
Switching frequency of main switch (f_s)	50 kHz
Duty cycle of main switch (D)	0.55~0.80 (D=0.7 at U_{in}=21 V)
MOSFET	IXFP76N15T2 (r_S =0.02 Ω)
Coupled-inductor	KDM's iron Silico aluminum powder ring core KS226-060A(r_{Lm} =0.025 Ω, V_e =44.5 cm^3, A_c= 2.29 cm^2, L_m = 100 μH, N= 1, N_p =27, L_k=3.5 μH)
Resonant inductor (L_{r1}/ L_{r2})	2 μH
Resonant capacitor(C_{r1} /C_{r2})	180 nF
Absorption capacitor(C_{s1} /C_{s2})	30 nF
Clamped/switched capacitor(C_{C1},C_{C2},C_{f1},C_{f2})	5×1 μF film capacitor (r_C= 0.015 Ω)
Output capacitor(C_o)	2×47 μF electrolytic cap.//3× 1 μF film cap. (r_C= 0.01 Ω)
Clamped/feedback/ output diode(D_{C1},D_{C2},D_{f1},D_{f2}, D_{o1},D_{o2})	MUR1560T(V_{FD}=1.0 V)
Interval time between the gate signal of S_{r1} and that of S_1 (T_l)	1.5 μs
Turn-on time of auxiliary switch (T_{r1})	1 μs

as shown in Fig. 11, could be simplified for better understanding the general soft-switching principle.

The input current source $I_{\rm in1}$ and the controlled current source I_{o1} yields based on Fig. 10 and 11

$$I_{\rm in1}=i_{Lk1}=\begin{cases}\bar{I}_{\rm in1}+0.5\cdot D\cdot T\cdot\frac{V_{\rm in}}{L_{m1}}-\frac{V_{\rm in}}{L_{m1}}\cdot t, t\in(t_4,t_8)\\ \bar{I}_{\rm in1}+0.5\cdot D\cdot\frac{V_{\rm in}}{L_{m1}}, t\in(t_1,t_4)\\ \bar{I}_{\rm in1}-0.5\cdot D\cdot T\cdot\frac{V_{\rm in}}{L_{m1}}+\frac{V_{\rm in}}{L_{m1}}\cdot t, t\in(t'_0,t'_8)\\ \bar{I}_{\rm in1}-0.5\cdot D\cdot\frac{V_{\rm in}}{L_{m1}}, t\in(t_8,t'_0)\end{cases} \tag{64}$$

$$I_{o1}=f(i_{Do1},i_{Dc1})=\begin{cases}i_{Do1}+i_{Dc1}, t\in(t_1,t_4)\\ i_{Do1}, t\in(t_4,t_8)\\ i_{Df1}, t\in(t'_0,t'_8)\\ 0, \text{else}\end{cases} \tag{65}$$

where $\bar{I}_{\rm in1}$ denotes the average current and it equals to $0.5MI_o$. For the controlled current source I_{o1}, it is determined by i_{Do1}, i_{Df1}, and i_{Dc1}. Notice that there is only current of i_{Do1} at the beginning of resonant period and zero current at the end of resonant period. Here, parasitic capacitance of S_1 could be employed as a part or whole C_{s1}, which not only takes part in the ZVS-OFF process but also helps feed energy to resonance network. If i_{Lr1} reaches over $I_{\rm in1}$ during the resonant process, ZVS-ON will be achieved. Namely, the resonant circuit acts as an "electronics load" to absorb $I_{\rm in1}$ and provides a negative current in S_1, which guarantee ZVS-ON in essence. Hence, the soft-switching method could be extended to other high step-up converters conveniently.

V. EXPERIMENTAL RESULTS

To verify the performance of the proposed converter, a 1000-W prototype is implemented in the laboratory. The KDM's iron Silico aluminum powder ring core KS226-060A are used as the cores of coupled inductors. Specifications of the prototype are listed in Table I where the resonant parameters are based on soft-switching analysis in Section IV and other parameter are according to performance analysis in Section III. In general, they keep in according with the parameters of the reported converter in [25], except parameter in auxiliary circuit. Fig. 12 provides a photograph of prototype in test platform.

The typical operation waveforms are shown in Fig. 13. The driving signal waveforms of main switch S_1 and auxiliary switch S_{r1} are shown in Fig. 13(a). The voltage stress across main switch S_1 and clamp capacitor C_{c1} are shown in Fig. 13(b). It is obvious that the voltage stress on S_1 is clamped to be

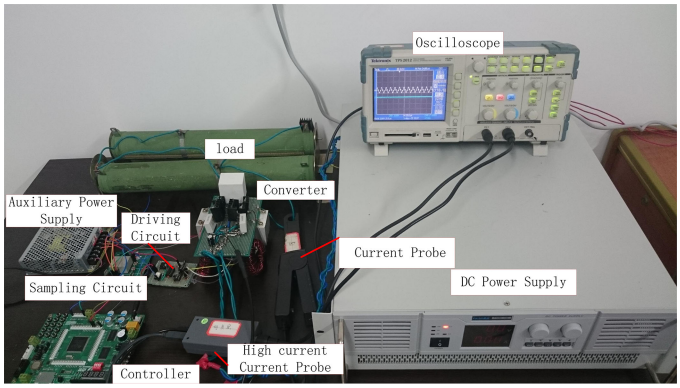

Fig. 12. Photograph of prototype in test platform.

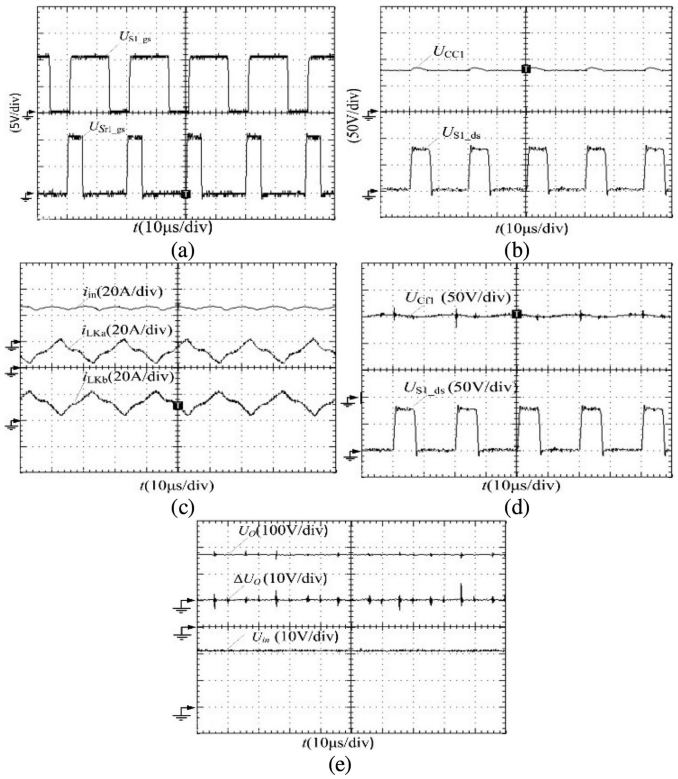

Fig. 13. Typical operation waveforms. (a) U_{S1_gs} and U_{Sr1_gs}. (b) U_{S1_ds} and U_{CC1}. (c) $i_{\rm in}$ and i_{LKa}, i_{LKb}. (d) U_{S1_ds} and U_{Cf1}. (e) $U_{\rm in}$, $U_{\rm o}$, and ΔU_o.

about 80 V by clamped capacitor C_{c1}, much lower than output voltage. The input current $i_{\rm in}$ and two branch currents i_{LKa} and i_{LKb} are shown in Fig. 13(c). The input current suffers small ripple due to the interleaved branch currents. Fig. 13(d) shows the voltage stress on S_1 and switched-capacitor C_{f1} where the voltage across switched-capacitor halves output voltage. The waveforms of input and output voltages are shown in Fig. 13(e) where the input and output voltages approach 21 and 270 V, respectively. Obviously, a high voltage gain of 12.86 reaches a little less than the theoretical value of 13.33. This difference comes from the voltage drop resulting from circuit resistance and leakage inductance.

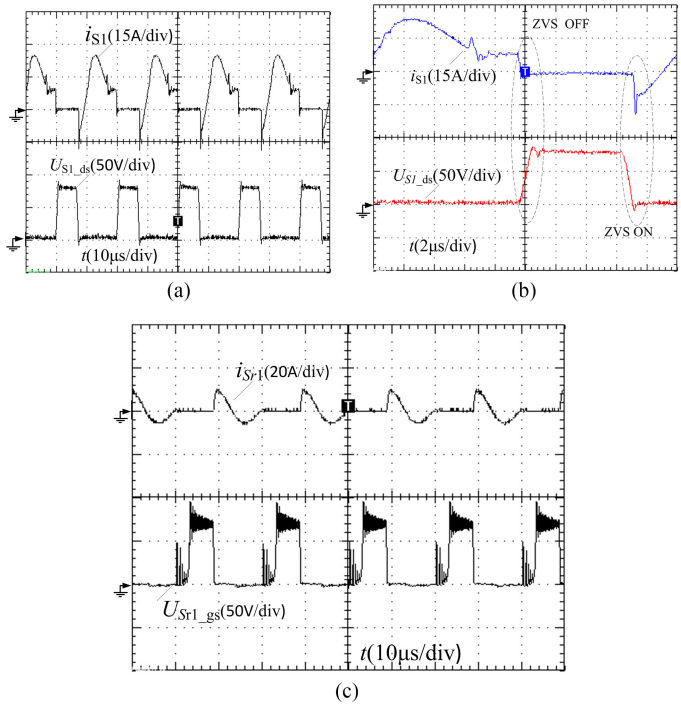

Fig. 14. Soft-switching waveforms. (a) i_{S1} and U_{S1_ds}. (b) Zoom-in waveforms of i_{S1} and U_{S1_ds}. (c) i_{Sr1} and U_{Sr1_ds}.

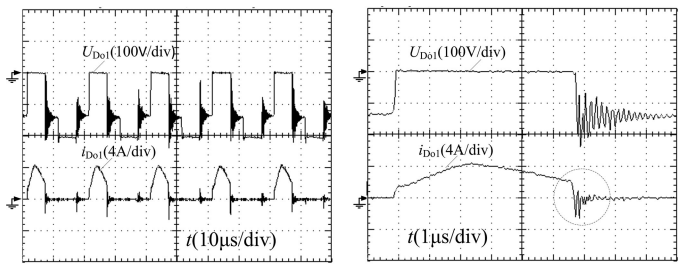

Fig. 15. Diode operation waveforms. (a) Current and voltage of D_{O1}. (b) Zoom-in waveforms of D_{O1}.

Fig. 14 reveals the soft-switching waveforms. The current and voltage waveforms of the main switch are shown in Fig. 14(a). And its zoom-in waveforms are shown in Fig. 14(b). During the turn-OFF process, the drain-source voltage of S_1 increases slowly before the current through S_1 slows down to zero rapidly, ZVS operation is realized for S_1. When S_1 is turned ON, anti-parallel diode of S_1 conducts with negative current through S_1, and S_1 is turned-ON under ZVS condition. Fig. 14(c) shows the current and voltage waveforms of the auxiliary switch. Before the auxiliary switch is turned ON, its anti-body diode has conducted. Thus, the auxiliary switch can achieve ZVS turn-OFF as well. Meanwhile, it is obvious that the ZCS turn-ON is achieved due to the resonant inductor.

One of the merits for the proposed is alleviated diode reverse-recovery converter and its waveforms are shown in Fig. 15. The voltage and current of output diode D_{O1} are shown in Fig. 15(a). And its zoom-in waveforms is shown in Fig. 15(b).The voltage stress of output diode is about quarter of output voltage. The current falling rate of output diode is controlled effectively to

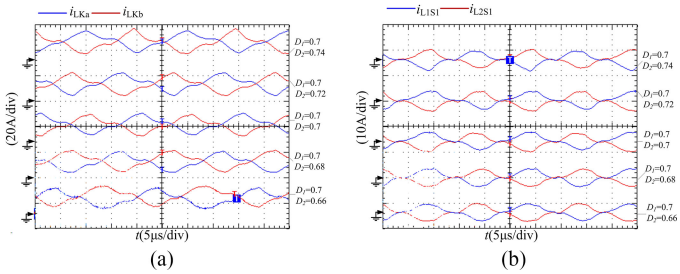

Fig. 16. Current waveforms at asymmetrical duty cycle. (a) i_{LKa} , i_{LKb}. (b) i_{L1S1} , i_{L2S1}.

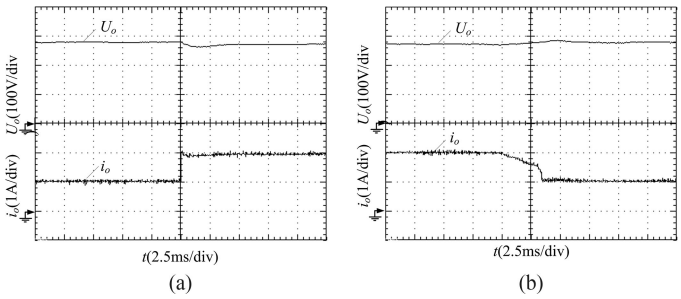

Fig. 17. Dynamic waveforms of U_O and i_O. (a) Step-up change. (b) Step-down change.

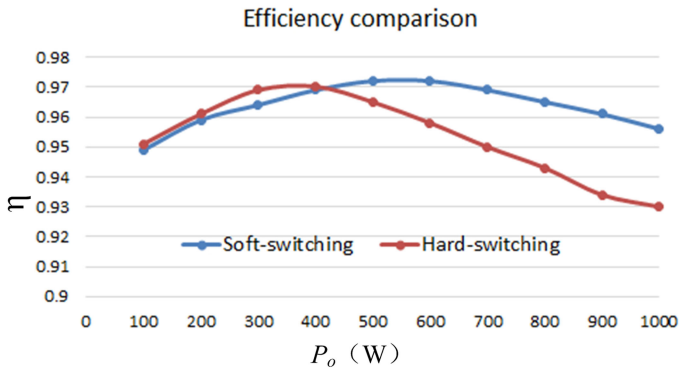

Fig. 18. Measured efficiency comparison.

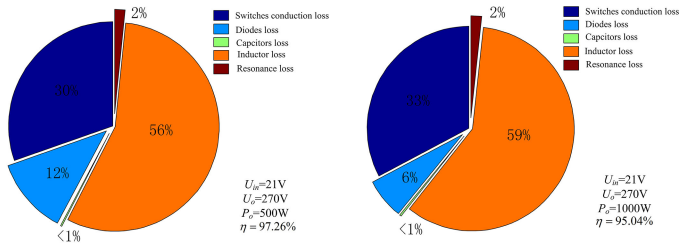

Fig. 19. Loss breakdown and efficiency of the prototype at different output power with the same input/output voltage. (a) 500 W. (b) 1000 W.

approximately 16 A/μs, which alleviates reverse-recovery problem successfully. Insufficiently, there is parasitic capacitance for output diode D_{o1} and non-ignorable stray inductance in circuit. Thus, ringing is easy to be triggered.

Considering the main asymmetrical factor, the branch currents at asymmetrical duty cycle is taken insight. When the duty cycle of S_1 and S_2 is asymmetrical, the waveforms of two branch currents i_{LKa} and i_{LKb}, and secondary current of coupled inductors i_{L1S1} and i_{L2S1} are shown in Fig. 16(a) and (b), respectively. Known from the experimental results, there is little unbalance difference. Hence, the soft-switching operation maintains the auto-balance characteristics well.

Fig. 17(a) and (b) are the experimental waveforms of output voltage and output current under load step-change. From Fig. 17(a), it can be seen that output voltage can enter steady state in 2.5 ms when the output power step from 270 to 540 W. Similarly, from Fig. 17(b), it can be seen that the output voltage can enter steady state in no more than 5 ms when the output power steps from 540 to 270 W. It is concluded that the dynamic performance would never be effected by the auxiliary soft-switching circuit.

Under different output power with changing load and fixed output voltage, the measured efficiency comparison between converter without soft switching in [25] and the proposed converter with soft switching is shown in Fig. 18, the peak efficiency of the proposed converter could reach up to 97.2% at P_o of 500 W. Referring to efficiency calculation method in Section III-D, efficiency at P_o of 500 and 1000 W reaches up to 97.26% and 95.04%, respectively, as shown in Fig. 19, which agree with the theory efficiency even a little deviation. Under high current flow, a tiny measured deviation of parasitic resistance in the components may lead large loss error. Meanwhile, Fig. 19(a) and (b) show the loss breakdown as well. Obviously, the dominate loss of the proposed converter is the wire loss of coupled inductor. Actually, when the switching loss is neglect, the winding conduction loss gets dominant in high voltage gains and high output powers, which is due to its corresponding high current flow. Therefore, it is important to employ better-graded wires for coupled inductors to further enhance the conversion efficiency and the copper belt is utilized as the winding wire.

Compared with the hard-switching operation in [25], the efficiency has promoted significantly at heavy load range, but little improvement even drop at light load because the switching loss has small weight in total loss at light load. Namely, the loss of auxiliary circuit itself exceeds the reduced switching loss of main switch at light load. However, the switching loss have rising weight with the current increasing, thus, the soft-switching operation could significantly enhance the efficiency under heavy load. To obtain high efficiency at light load, the auxiliary switches could be kept OFF-state, which is reason to be called plug-play soft technology. Fortunately, the light-load operation is relatively infrequent. Moreover, the heat stress will be lower even with low efficiency under light-load condition because the absolute total loss is relatively small.

VI. Conclusion

This paper has developed a plug-play active soft-switching method for the current-auto-balance interleaved high step-up dc/dc converter. With the employment of active soft-switching method, ZVS turn-ON and ZVS turn-OFF are both realized for

the main switches. Besides, the auxiliary switches obtain ZCS turn-ON and ZVS turn-OFF operation as well. Hence, the soft-switching method not only contributes to reduce switching loss of main switches but also brings small extra loss from the auxiliary circuit. Meanwhile, the operation modes of the primary converter will never be invaded, accordingly, several topology features, such as extremely high voltage gain but low voltage stress on power devices, complete current-auto-balance, alleviated diode reverse-recovery problem, reduced input current ripple, and output voltage ripple are well maintained. Based on the theory analysis and measurement for efficiency, the proposed converter is validated an efficiency enhancement at relatively heavy load compared with the converter with hard-switching operation. Thus, the soft-switching operation could be plugged-played according to the load. Finally, the soft-switching essence of high step-up converters is revealed and this paper provides a general soft-switching method for the kind of high step-up converters.

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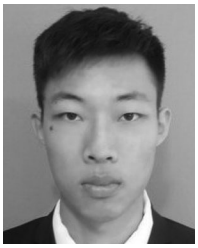

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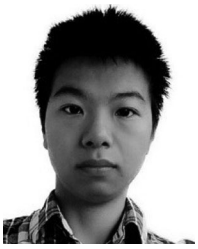

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