A Novel Discontinuous Modulation Strategy With Reduced Common-Mode Voltage and Removed DC Offset on Neutral-Point Voltage for Neutral-Point-Clamped Three-Level Converter

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***Abstract*—In this paper, a novel discontinuous pulsewidth modulation (DPWM) modulation strategy for a neutral-point-clamped (NPC) three-level converter (TLC) is proposed to reduce the switching loss, reduce common-mode voltage (CMV), and remove dc offset from the neutral-point (NP) voltage simultaneously, which is named as RCMV_DPWM. Based on the space vector diagram with reduced CMV, all clamping modes under RCMV_DPWM are revealed. Then, the NP voltage is controlled by selecting proper clamping mode. The realization of RCMV_DPWM is also discussed. Moreover, the performances of RCMV_DPWM are analyzed and compared with other PWM strategies in term of the NP voltage ripple, switching loss, and waveform quality. Finally, the feasibility and superiority of RCMV_DPWM are verified by experiments.**

***Index Terms*—Modulation strategy, neutral-point voltage balance, switching loss, three-level converter.**

I. Introduction

With the development of power electronics technology, the neutral-point-clamped (NPC) three-level converter (NPC TLC) has attained a lot of attention [1]–[3], which has some advantages over the conventional two-level converter, such as reduced total harmonic distortion (THD), reduced voltage stress across switching devices, and high conversion efficiency. Due to these attractive characteristics, a NPC TLC has been widely used in several applications, such as motor drive and renewable energy source [4]–[6].

Various modulation methods have been proposed for the NPC TLC, which can be classified as carrier-based pulsewidth modulation (PWM) (CBPWM) and space vector PWM (SVPWM)

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proposed. However, this method is only suitable for inverters with seven or more levels.

All of these CMV reduction or elimination methods [20]–[23] are based on selecting the vectors corresponding to lower or zero CMV, but the NP voltage oscillation is not considered.

In this paper, a novel DPWM is proposed, and the three goals of reducing the CMV, reducing switching losses, and controlling the NP voltage, can be meanwhile achieved. Hereafter, it is called as RCMV_DPWM. It is necessary to prioritize the aforementioned three goals. In this paper, they are prioritized as follows.

1) Reduce the CMV within $\pm u_{\rm dc}/6$.
2) Reduce the switching loss, i.e., one phase is clamped to the positive bus (PB), negative bus (NB), or NP. This phase has no switching action, and only four switching actions (conventional CBPWM or SVPWM has six switching actions) in one switching cycle. It is worth noting that, because of the requirement to reduce CMV and control NP voltage, the phase without switching action maybe not corresponding to the maximum current. Therefore, the switching loss reduction capability cannot reach the maximum.
3) Control the NP voltage, in particular, the dc offset on the NP voltage should be eliminated, and the ac variation should be reduced as much as possible.

II. NPC TLC and Its Modulation Model

A. NPC TLC

Three phase voltages u_a, u_b, and u_c and three phase currents i_a, i_b, and i_c can be expressed as

$$\begin{cases} u_a = mu_{\rm dc}\cos\omega t \\ u_b = mu_{\rm dc}\cos(\omega t - 2\pi/3) \\ u_c = mu_{\rm dc}\cos(\omega t - 4\pi/3) \end{cases} \tag{1}$$

$$\begin{cases} i_a = I_m\cos(\omega t - \varphi) \\ i_b = I_m\cos(\omega t - 2\pi/3 - \varphi) \\ i_c = I_m\cos(\omega t - 4\pi/3 - \varphi) \end{cases} \tag{2}$$

where $\omega t \in [0, 2\pi]$ is the phase angle of voltage of phase A, $m \in [0, 1.1547]$ is the modulation index, I_m is the peak value of the phase current, and φ is the Pf angle of load. In this paper, the positive direction of the phase current is defined as flowing from the converter.

The topology of the NPC TLC is shown in Fig. 1(a). Each phase is composed of four switch devices with antiparalleled free-wheel diode and two clamping diodes. Two capacitors C_1 and C_2 serve as a voltage divider. When the capacitor voltage is balanced, the voltage of the dc bus is $u_{\rm dc}$ and $u_{C1} = u_{C2} = u_{\rm dc}/2$. To simplify the analysis, $u_{\rm dc} = 1$ is assumed. Choosing the negative bus as the reference point, the output voltage is u_{C1}, while S_1 and S_2 are gated ON, defined as level 1; the output voltage is 0, while S_2 and S_3 are gated ON, defined as level 0; the output voltage is $-u_{C2}$, while S_3 and S_4 are gated ON, defined as level –1.

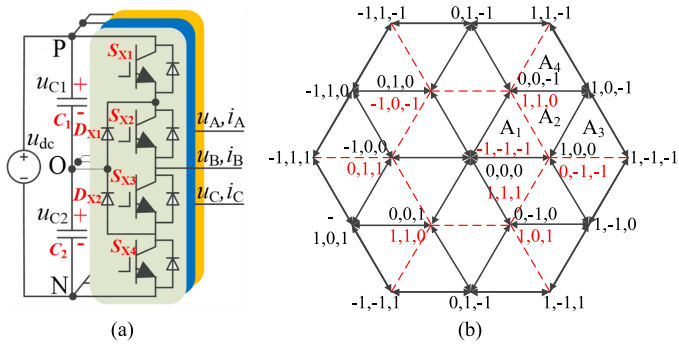


Fig. 1. Topology and space vector diagram with reduced CMV of the NPC TLC. (a) NPC TLC. (b) Space vector diagram with reduced CMV.

Substituting phase voltages into (3), 27 basic voltage vectors can be obtained. Then, the space vector diagram for the NPC TLC is given as Fig. 1(b).

$$\boldsymbol{u} = \sqrt{2/3}(u_A\boldsymbol{e}^{j0} + u_B\boldsymbol{e}^{j2\pi/3} + u_C\boldsymbol{e}^{j4\pi/3}). \tag{3}$$

According to the vector length, the basic voltage vectors can be divided into zero-voltage vectors (ZVVs), large-voltage vectors (LVVs), medium-voltage vectors (MVVs), and small-voltage vectors (SVVs). Taking the phase voltage given by (1) into (3), reference vector $\boldsymbol{u}_{\rm ref}$ can be acquired. In one switching cycle, $\boldsymbol{u}_{\rm ref}$ is synthesized by the basic voltage vectors according to the volt–second equilibrium principle. For example, when $\boldsymbol{u}_{\rm ref}$ is located in the subsector A2, as shown in Fig. 1(b), the basic voltage vectors $[0, -1, -1]$, $[0, 0, -1]$, $[1, 0, -1]$, $[1, 0, 0]$, and $[1, 1, 0]$ can be selected to synthesize $\boldsymbol{u}_{\rm ref}$, where $[0, -1, -1]$ and $[1, 0, 0]$, $[0, 0, -1]$ and $[1, 1, 0]$ are redundant basic voltage vector pairs.

According to the nearest three vector (NTV) principle of SVPWM, the synthesis rule for $\mathbf{u}_{\rm ref}$ in subsector A2 is

$$\begin{cases} \left\{\begin{matrix}[0,-1,-1]\\ [1,0,0]\end{matrix}\right\} d_1 + [1,0,-1]d_2 + \left\{\begin{matrix}[0,0,-1]\\ [1,1,0]\end{matrix}\right\} d_3 = \boldsymbol{u}_{\rm ref} \\ d_1 + d_2 + d_3 = 1 \end{cases} \tag{4}$$

where d_1, d_2, and d_3 denotes the duty ratio of the corresponding vectors, respectively.

B. CMV for NPC TLC

The CMV of the NPC TLC can be defined as

$$V_{\rm CMV} = \frac{L_A + L_B + L_C}{3}\frac{u_{\rm dc}}{2} \tag{5}$$

where L_A, L_B, and L_C denote the three phases output level.

Taking the three-phase output level into (5), the CMV of each basic voltage vector can be obtained as Table I. Because SVVs(B) and ZVVs(B) introduce higher CMVs, these vectors are not selected in vector synthesis for the purpose of reducing the CMV. After discarding these vectors, the space vector with reduced CMV is shown in Fig. 1(b). It is worth noting that the original vector arrival relationship has changed when the SVVs(B) and ZVVs(B) are discarded. For example, the vector

TABLE I
VECTOR CLASSIFICATION AND CORRESPONDING CMV

group	Vector	CMV
LVVs	[1,-1,-1], [1,1,-1], [-1,1,-1], [-1,1,1], [-1,-1,1], [1,-1,1]	$\pm u_{dc}/6$
MVVs	[1,0,-1], [0,0,-1][0,1,-1], [-1,1,0], [-1,0,1], [0,-1,1]	0
SVVs(A)	[1,0,0], [0,0,-1], [0,1,0], [-1,0,0], [0,0,1], [0,-1,0],	$\pm u_{dc}/6$
SVVs(B)	[0,-1,-1], [1,1,0], [-1,0,-1], [0,1,1], [-1,-1,0], [1,0,1],	$\pm u_{dc}/3$
ZVV(A)	[0,0,0]	0
ZVVs(B)	[1,1,1], [-1,-1,-1]	$\pm u_{dc}/2$

$[1,-1,-1]$ cannot reach the vector $[0,-1,-1]$ if only one switching action during commutation is admitted. In Fig. 1(b), the reachable vectors are connected by black solid lines, and non-reachable vectors are connected by red dash lines.

In general, only LVVs, MVVs, SVVs(A), and ZVV(A) should be selected to synthesize the reference vector for the purpose of reducing the CMV.

After discarding SVVs(B) and ZVVs(B), the vector synthesis relationship in subsector A2 is

$$\begin{cases} [1,0,0]d_1 + [1,0,-1]d_2 + [0,0,-1]d_3 = \boldsymbol{u}_{\text{ref}} \\ d_1 + d_2 + d_3 = 1. \end{cases} \tag{6}$$

Compared to the vector synthesis relationship given by (4), the vector synthesis relationship given by (6) has the following differences: 1) CMVs are reduced within $\pm u_{\text{dc}}/6$; and (2) B phase is always clamped to the NP and the switching loss is reduced. The goal that reduces the CMV by DPWM is achieved so it is called as RCMV_DPWM.

C. NP Voltage for NPC TLC

When the output level of one phase is 0, the phase current will be injected into or out from the NP and the NP voltage will change. In one switching cycle, the duty ratio of level 0 of the phase *X* is d_{X0}, and the average of the NP current introduced by phase *X* is

$$i_{\text{NP},X} = i_X d_{X0}. \tag{7}$$

The average NP currents introduced by the three phases in one switching cycle is

$$i_{\text{NP}} = \sum_{X=A,B,C} i_X d_{X0} = I_m \sum_{X=A,B,C} i_{\text{X}}^* d_{X0} = I_m i_{\text{NP}}^*$$

$$i_{\text{NP}}^* = \sum_{X=A,B,C} i_{\text{X}}^* d_{X0} \tag{8}$$

where i_{NP}^* is the normalized NP current in one switching cycle. The relationship between the NP current and the NP voltage variation is

$$\Delta u_{\text{NP}} = u_{C2} - u_{C1} = -\frac{T_s}{C_1 + C_2} \sum_{X=A,B,C} i_X d_{X1}$$

$$= -\frac{T_s I_m}{C_1 + C_2} i_{\text{NP}}^*. \tag{9}$$

TABLE II
REARRANGED PHASE VOLTAGES AND CURRENTS WITH RESPECT TO ωt

	[0, π/3]	[π/3, 2π/3]	[2π/3, π]	[π, 4π/3]	[4π/3, 5π/3]	[5π/3, 2π]
$u_{\max}$, $i_{\max}$	u_a, i_a	u_b, i_b	u_b, i_b	u_c, i_c	u_c, i_c	u_a, i_a
u_{mid}, i_{mid}	u_b, i_b	u_a, i_a	u_c, i_c	u_b, i_b	u_a, i_a	u_c, i_c
$u_{\min}$, $i_{\min}$	u_c, i_c	u_c, i_c	u_a, i_a	u_a, i_a	u_b, i_b	u_b, i_b

The positive NP current will make the NP voltage decrease and the negative NP current will make the NP voltage increase.

Correspond to (4), k_1 and k_2 are the distribution coefficients of the redundant vector pairs $\{[0,-1,-1],[1,0,0]\}$ and $\{[0,0,-1],[1,1,0]\}$, respectively. i_{NP}^* is

$$i_{\text{NP}}^* = i_A^*[2k_1 - 1]d_1 + i_B^* d_2 + i_C^*(2k_2 - 1)d_3. \tag{10}$$

In order to reduce the number of switches, one of k_1 and k_2 is generally set as one or zero, so the NP voltage can be controlled by changing the distribution coefficients. Therefore, there is one freedom to control the NP voltage under SVPWM.

Correspond to (6), i_{NP}^* can be expressed as

$$i_{\text{NP}}^* = -i_A^* d_1 + i_B^* d_2 - i_C^* d_3. \tag{11}$$

From the aforementioned equation, it can be seen that there is no freedom to control the NP voltage in one switching cycle under RCMV_DPWM. However, the NP voltage can still be controlled within a certain range by selecting different RCMV_DPWM modes. In particular, the dc offset of the NP voltage can be eliminated. This will be explained in detail in the following sections.

III. RCMV_DPWM

Although RCVM_DPWM based on the space vector diagram has been determined, there is no freedom to control NP voltage. Therefore, its applications are limited in some cases.

For the purpose of controlling the NP voltage, all possible RCMV_DPWM sequences must be first explored. For simplicity, the three phase voltages can be rearranged as

$$\begin{cases} u_{\max} = \max(u_a, u_b, u_c) \\ u_{\min} = \min(u_a, u_b, u_c) \\ u_{\text{mid}} = \text{mid}(u_a, u_b, u_c). \end{cases} \tag{12}$$

When $\omega t \in [0, \pi/3]$, u_a, u_b, and u_c correspond to $u_{\max}, u_{\text{mid}}$, and $u_{\min}$, respectively. The other cases can refer to Table II. Assuming $i_{\max}, i_{\text{mid}}$, and $i_{\min}$ denote the current of the phase corresponding to $u_{\max}, u_{\text{mid}}$, and $u_{\min}$, respectively.

Based on the space vector diagram, the first step is to determine the region in which the reference vector located in, and then, select the basic voltage vectors to synthesize reference vector, and the last, calculate the corresponding action time. In Fig. 1(b), there are two types of synthesis methods. One is based on the NTV synthesis method, and the selected vectors consist of equilateral triangle, such as [0, 0, −1], [0, 0, 0], and [1, 0, 0]. The second is based on the non-NTV (NNTV) method, and the selected vectors consist of isosceles triangles, such as [1, 0, 0], [1, 0, −1], and [1, 1, −1].

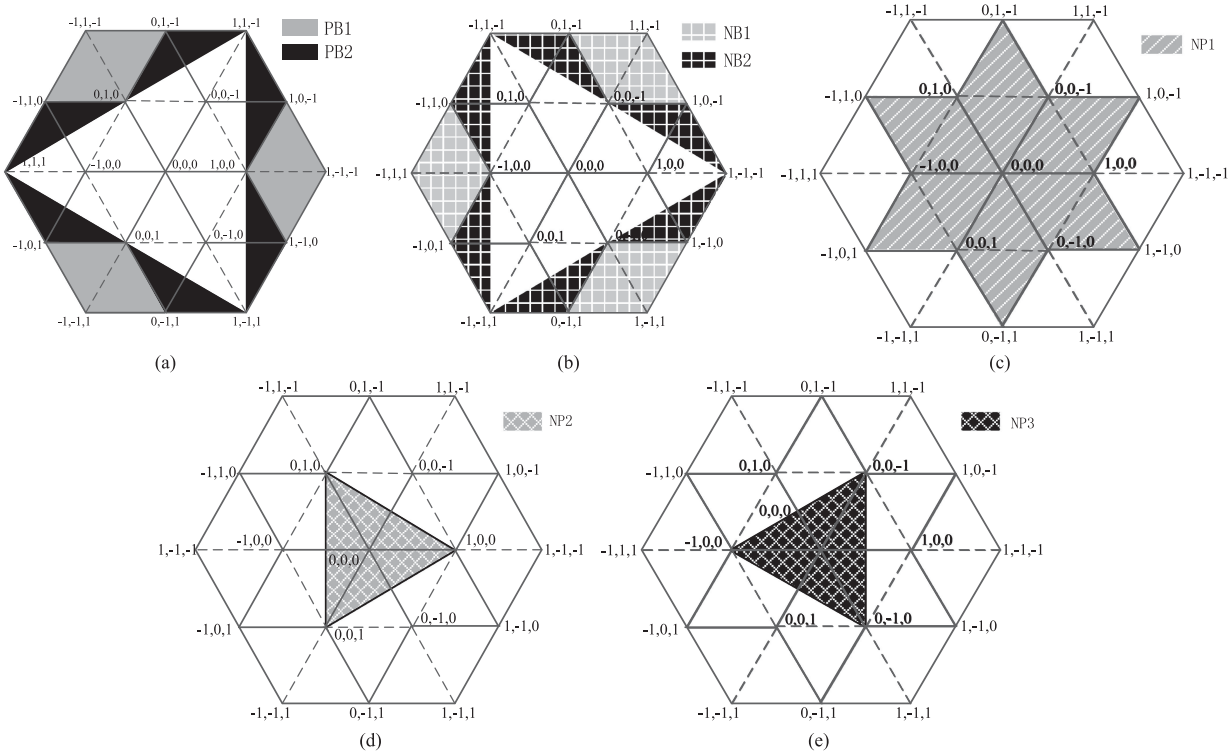


Fig. 2. Applicable areas for all clamping modes of RCMV_DPWM. (a) PB1 and PB2. (b) NB1 and NB2. (c) NP1. (d) NP2. (e) NP3.

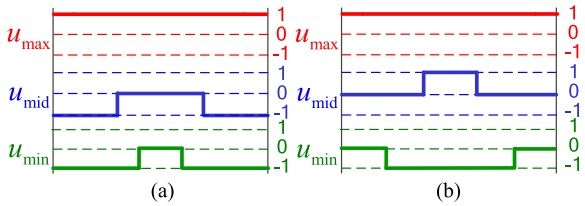


Fig. 3. Switching sequences of PB1 and PB2.

Fig. 2 shows the applicable areas for all clamping modes of RCMV_DPWM. Fig. 2(a) shows the applicable areas where $u_{\max}$ is clamped to the PB. In the areas colored as ▭ the corresponding switching sequence is shown in Fig. 3(a), and this mode is called as PB1. In the area colored as ■ the corresponding switching sequence is shown Fig. 3(b), and this mode is called as PB2. The former uses the NTV method and the latter uses the NNTV method. It can be seen that the $u_{\max}$ is clamped to the PB in the two modes, and the CMVs are also reduced within $\pm u_{\rm dc}/6$.

Taking PB1 as example, the all duty ratios of each level of each phase are

$$\begin{aligned} d_{\max,1} &= 1, \quad d_{\max,0} = 0, \quad d_{\max,-1} = 0 \\ d_{\rm mid,1} &= 0, \quad d_{\rm mid,0} = 2 - u_{\max} + u_{\rm mid}, \\ d_{\rm mid,-1} &= u_{\max} - u_{\rm mid} - 1 \\ d_{\rm min,1} &= 0, \quad d_{\rm min,0} = 2 - u_{\max} + u_{\rm min}, \\ d_{\rm min,-1} &= u_{\max} - u_{\rm min} - 1 \end{aligned} \tag{13}$$

where $d_{X,n}(X = \max, \min, \text{and mid and} \, n = -1, 0, 1)$ denotes the duty ratio of level n of phase X.

And, the condition for PB1 is

$$u_{\max} - u_{\rm mid} > 1 \ \text{ and } \ 1 > u_{\rm mid} - u_{\rm min} > 0. \tag{14}$$

The average NP current in one switching cycle for PB1 can be expressed as

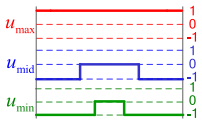
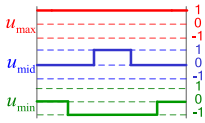
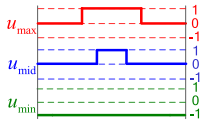
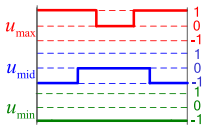
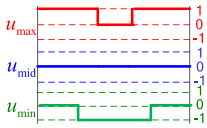
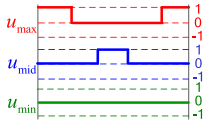
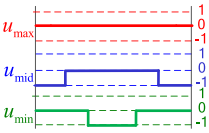
$$\begin{aligned} i_{\rm NP,PB1} &= d_{\rm mid,0} i_{\rm mid} + d_{\rm min,0} i_{\rm min} \\ &= (2 - u_{\max} + u_{\rm mid}) i_{\rm mid} + (2 - u_{\max} + u_{\rm min}) i_{\rm min}. \end{aligned} \tag{15}$$

Similarly, when $u_{\rm min}$ is clamped to the NB, the applicable areas are shown in Fig. 2(b). There are also two clamping modes corresponding to NTV and NNTV, named as NB1 and NB2. When the phase corresponding to $u_{\rm mid}$, $u_{\rm min}$, and $u_{\max}$ is clamped to the NP, the applicable areas are shown in Fig. 2 (c)–(e), named as NP1, NP2, and NP3, respectively. Table III summarizes the conditions, switching sequences, duty ratios, and NP current for the all clamping modes.

It be seen from Fig. 2, that there are many overlapping areas for these clamping modes. Fig. 4 shows the overlapping areas of clamping modes of RCMV_DPWM. It can be seen that there is at least one clamping mode in the whole areas, and there are even three clamping modes in some areas.

The existing of overlapping areas provides the possibility to achieve the NP voltage control under RCMV_DPWM.

TABLE III
CONDITIONS, SWITCHING SEQUENCES, DUTY RATIOS, AND NP CURRENT FOR ALL THE CLAMPING MODES UNDER RCMV_DPWM

Mode	Sequence	Condition	Duty ratio	NP current
PB1		$u_{max}-u_{mid}>1$ $u_{mid}-u_{min}<1$	$d_{max,1}=1,\ d_{max,0}=0,\ d_{max,-1}=0$ $d_{mid,1}=0,\ d_{mid,1}=2-u_{max}+u_{mid},\ d_{mid,-1}=u_{max}-u_{mid}-1$ $d_{min,1}=0,\ d_{min,0}=2-u_{max}+u_{min},\ d_{min,-1}=u_{max}-u_{min}-1$	$i_{NP,PB1}=(2-u_{max}+u_{mid})i_{mid}$ $+(2-u_{max}+u_{min})i_{min}$
PB2		$u_{max}-u_{mid}<1$ $u_{max}-u_{min}>1$ $2u_{max}-u_{mid}-u_{min}>2$	$d_{max,1}=1,\ d_{max,0}=0,\ d_{max,-1}=0$ $d_{mid,1}=1-u_{max}+u_{mid},\ d_{mid,0}=u_{max}-u_{mid},\ d_{mid,-1}=0$ $d_{min,1}=0,\ d_{min,0}=2-u_{max}+u_{min},\ d_{min,-1}=u_{max}-u_{min}-1$	$i_{NP,PB2}=(u_{max}-u_{mid})i_{mid}$ $+(2-u_{max}+u_{min})i_{min}$
NB1		$u_{max}-u_{min}>1$ $u_{mid}-u_{min}>1$ $1>u_{max}-u_{mid}$	$d_{max,1}=u_{max}-u_{min}-1,\ d_{max,0}=2-u_{max}+u_{min},\ d_{max,-1}=0$ $d_{mid,1}=u_{mid}-u_{min}-1,\ d_{mid,0}=2-u_{mid}+u_{min},\ d_{mid,-1}=0$ $d_{min,1}=0,\ d_{min,0}=0,\ d_{min,-1}=1$	$i_{NP,NB1}=(2-u_{max}+u_{min})i_{max}$ $+(2-u_{mid}+u_{min})i_{mid}$
NB2		$u_{max}-u_{min}>1$ $u_{mid}-u_{min}<1$ $u_{max}+u_{mid}-2u_{min}>2$	$d_{max,1}=u_{max}-u_{min}-1,\ d_{max,0}=2-u_{max}+u_{min},\ d_{max,-1}=0$ $d_{mid,1}=0,\ d_{mid,0}=u_{mid}-u_{min},d_{mid,-1}=1-u_{mid}+u_{min}$ $d_{min,1}=0,\ d_{min,0}=0,d_{min,-1}=1$	$i_{NP,NB2}=(2-u_{max}+u_{min})i_{max}$ $+(u_{mid}-u_{min})i_{mid}$
NP1		$1>u_{max}-u_{mid}$ $1>u_{mid}-u_{min}$	$d_{max,1}=u_{max}-u_{mid},\ d_{max,0}=1-u_{max}+u_{mid},\ d_{max,-1}=0$ $d_{mid,1}=0,\ d_{mid,0}=1,\ d_{mid,-1}=0$ $d_{min,1}=0,\ d_{min,0}=1-u_{mid}+u_{min},d_{min,-1}=u_{mid}-u_{min}$	$i_{NP,NP1}=(1-u_{max}+u_{mid})i_{max}$ $+i_{mid}+(1-u_{mid}+u_{min})i_{min}$
NP2		$1>u_{max}-u_{min}$ $1>u_{mid}-u_{min}$ $1>u_{max}+u_{mid}-2u_{min}$	$d_{max,1}=u_{max}-u_{min},\ d_{max,0}=1-u_{max}+u_{min},\ d_{max,-1}=0$ $d_{mid,1}=u_{mid}-u_{min},\ d_{mid,0}=1-u_{mid}+u_{min},\ d_{mid,-1}=0$ $d_{min,1}=0,\ d_{min,0}=1,\ d_{min,-1}=0$	$i_{NP,NP2}=(1-u_{max}+u_{min})i_{max}$ $+(1-u_{mid}+u_{min})i_{mid}+i_{min}$
NP3		$1>u_{max}-u_{min}$ $1>2u_{max}-u_{mid}-u_{min}$	$d_{max,1}=0,\ d_{max,0}=1,\ d_{max,-1}=0$ $d_{mid,1}=0,\ d_{mid,0}=1-u_{max}+u_{mid},\ d_{mid,-1}=u_{max}-u_{mid}$ $d_{min,1}=0,\ d_{min,0}=1-u_{max}+u_{min},\ d_{min,-1}=u_{max}-u_{min}$	$i_{NP,NP3}=(1-u_{max}+u_{min})i_{min}$ $+(1-u_{max}+u_{mid})i_{mid}+i_{max}$

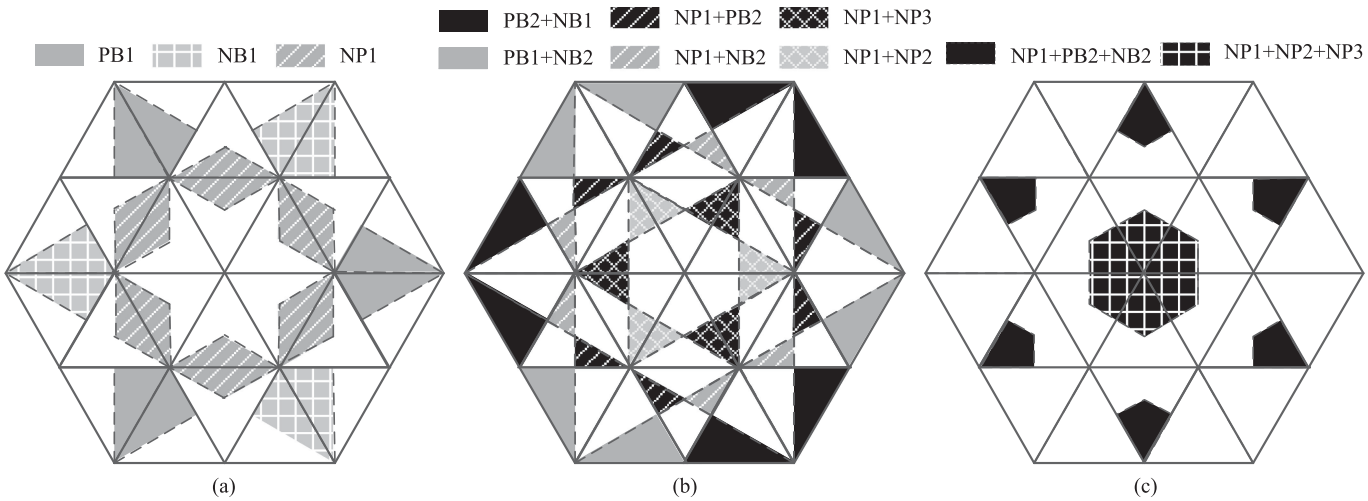


Fig. 4. Overlapping areas of clamping modes under RCMV_DPWM. (a) Single clamping mode areas. (b) Overlapping areas of two clamping modes. (c) Overlapping areas of three clamping modes.

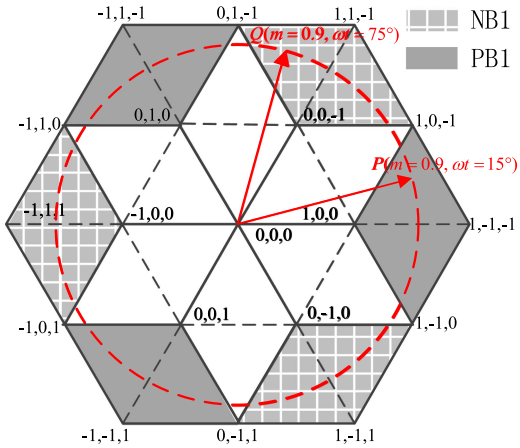


Fig. 5. Duality of NP currents introduced by PB1 and NB1 modes.

IV. NP Voltage Control Under RCMV_DPWM

A. Self-Equilibrium for RCMV_DPWM

Before discussing the NP voltage control for RCMV_DPWM, it is critical to pay attention to the NP voltage self-equilibrium. The NP voltage self-equilibrium is that the NP voltage variation in a certain time is theoretically zero even if any active NP voltage control is not used.

The NP currents $i_{\mathrm{NP,PB1}}$ and $i_{\mathrm{NP,NB1}}$ under PB1 and NB1 are related to m, φ, and ωt. When $m = 0.9$ and $\omega t = \pi/12$, which is corresponding to the point P in Fig. 5, the clamping mode PB1can only be selected in order to reduce the CMV; and when $m = 0.9$ and $\omega t = 5\pi/12$, which is corresponding to the point Q in Fig. 5, the clamping mode NB1 can only selected. Taking (1) and (2) into the NP current expression given in Table III and considering Table II, $i_{\mathrm{NP,PB1}}$ and $i_{\mathrm{NP,NB1}}$ can be expressed as

$$\begin{aligned} &i_{\mathrm{NP,PB1}}(m,\varphi)|_{\omega t=\theta} \\ &= [2 - m\cos\theta + m\cos(\theta - 2\pi/3)]I_m\cos(\theta - 2\pi/3 - \varphi) \\ &+ [2 - m\cos\theta + m\cos(\theta - 4\pi/3)]I_m\cos(\theta - 4\pi/3 - \varphi) \end{aligned} \tag{16}$$

$$\begin{aligned} &i_{\mathrm{NP,NB1}}(m,\varphi)|_{\omega t=\theta+\pi/3} \\ &= [2 - m\cos(\theta - \pi/3) + m\cos(\theta - \pi)]I_m\cos(\theta - \pi/3 - \varphi) \\ &+ [2 - m\cos(\theta + \pi/3) + m\cos(\theta - \pi)]I_m\cos(\theta + \pi/3 - \varphi). \end{aligned} \tag{17}$$

From (16) and (17), it can be seen that

$$i_{\mathrm{NP,PB1}}(m,\varphi)|_{\omega t=\theta} + i_{\mathrm{NP,NB1}}(m,\varphi)|_{\omega t=\theta+\pi/3} = 0. \tag{18-1}$$

Similarly, the following conditions can be obtained:

$$i_{\mathrm{NP,PB2}}(m,\varphi)|_{\omega t} + i_{\mathrm{NP,NB2}}(m,\varphi)|_{\omega t+\pi/3} = 0 \tag{18-2}$$

$$i_{\mathrm{NP,NP1}}(m,\varphi)|_{\omega t} + i_{\mathrm{NP,NP1}}(m,\varphi)|_{\omega t+\pi/3} = 0 \tag{18-3}$$

$$i_{\mathrm{NP,NP2}}(m,\varphi)|_{\omega t} + i_{\mathrm{NP,NP3}}(m,\varphi)|_{\omega t+\pi/3} = 0. \tag{18-4}$$

Under these conditions, the NP voltage variations at ωt and $\omega t + \pi/3$ are reversed and they can be offset with each other, and these two clamping modes are called as complementary modes.

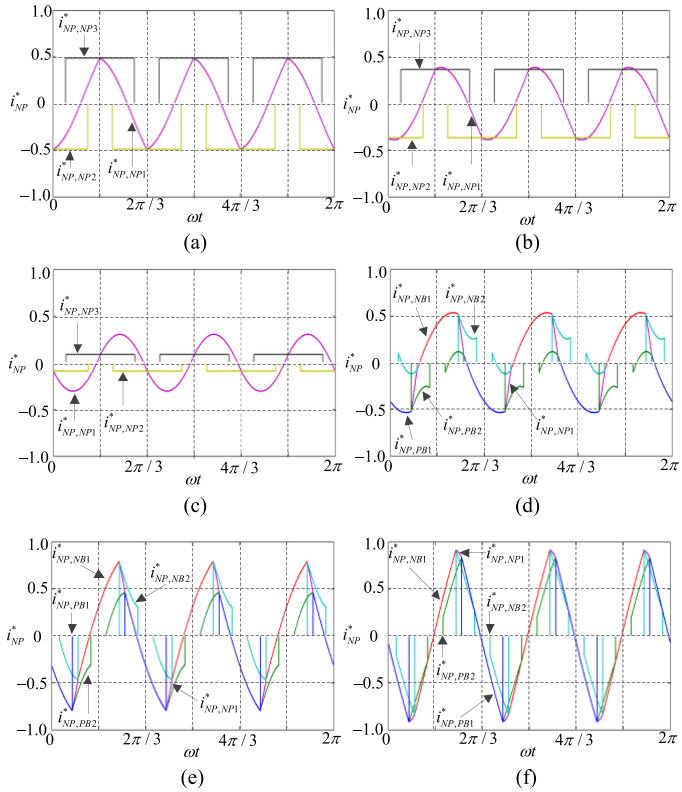


Fig. 6. NP currents under different clamping modes with respect to m and φ. (a) $m = 0.3$, $\varphi = \pi/9$. (b) $m = 0.3$, $\varphi = \pi/4$. (c) $m = 0.3$, $\varphi = 4\pi/9$. (d) $m = 1.05$, $\varphi = \pi/9$. (e) $m = 1.05$, $\varphi = \pi/4$. (f) $m = 1.05$, $\varphi = 4\pi/9$.

So, PB1 and NB1, PB2 and NB2, NP1 and NP1, and NP2 and NP3 are complementary modes with each other, respectively.

It is easy to imagine that the NP voltage self-equilibrium condition for RCMV_DPWM is that: under a certain m, PB1, PB2, NP1, and NP2 are used when $\omega t = \theta$, and NB1, NB2, NP1, and NP3 should be used when $\omega t = \theta + \pi/3$, or vice versa.

Taking the NP voltage self-equilibrium into account, the accumulative NP voltage variation during $\omega t \in [\theta, \theta + \pi/3]$ will be able to be compensated during $\omega t \in [\theta + \pi/3, \theta + 2\pi/3]$, and the NP voltage will exhibit fluctuation with triple fundamental frequency. If small ac fluctuation on the NP voltage is allowed, the main purpose of the NP voltage control is to eliminate the dc offset.

B. NP Voltage Control for RCMV_DPWM

For different m and φ, Fig. 6 shows i_{NP} with respect to ωt under different clamping modes. By comprehensively comparing, the following cases shown in Fig. 7 can be found.

1) If there is only one clamping mode and the NP current under this clamping mode is positive or negative, and the NP voltage will decrease or increase, which is recorded as cases 1 and 2, respectively.
2) If there are multiple clamping modes and the NP currents of these clamping modes are all positive or negative, and the NP voltage will decrease or increase, but the slew

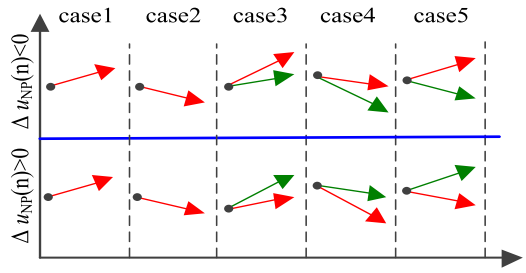


Fig. 7. NP voltage adjustment in different cases.

TABLE IV
CLAMPING MODE SELECTION RULE TO ACHIEVE NP VOLTAGE CONTROL FOR RCMV_DPWM

$\Delta u_{NP}=u_{C2}-u_{C1}>0$	$\Delta u_{NP}=u_{C2}-u_{C1}<0$
Mode with the largest NP current	Mode with the smallest NP current

rates are different when different clamping modes used, denoted as cases 3 and 4, respectively.

3) If there are multiple clamping modes, the NP currents of some clamping modes are positive and others correspond to negative, then the NP voltage can be adjusted bi-directionally, denoted as case 5.

Under cases 1 and 2, the NP voltage cannot be controlled in these two cases. However, taking complementary modes into account, as shown in Fig. 4(a), the NP voltage self-equilibrium condition is satisfied.

In the clamping mode overlapping area, the NP voltage may be controlled by selecting an appropriate clamping mode. In one switching cycle, if the initial offset of the NP voltage $\Delta u_{\rm NP} = u_{C2} - u_{C1} > 0$ is detected, then it is desirable that the NP voltage should decrease with a maximum rate or increase with minimum rate. Specifically speaking, when $\Delta u_{\rm NP} = u_{C2} - u_{C1} > 0$, the NP voltage control rules are given as follows.

1) If one or more clamping modes are accompanied with positive NP current modes, the NP voltage will decrease under these clamping. The clamping mode with the largest NP current should be selected to recover the NP voltage as quickly as possible.
2) If all clamping modes are accompanied with the negative NP current, the NP voltage will increase under these clamping modes. The clamping mode with the smallest NP current should be selected to make the NP voltage offset as slowly as possible.

In summary, the NP voltage control for RCMV_DPWM can be summarized as Table IV.

It can be seen that the NP voltage control under RCMV_DPWM is realized by choosing the clamping mode with the largest NP current or smallest NP current. If the clamping mode with the largest NP current is always used in one fundamental cycle, the maximum decreasing ability can be acquired. Similarly, if the clamping modes with the smallest NP current are always used in one fundamental cycle, the maximum increasing ability can be acquired. Define the evaluation

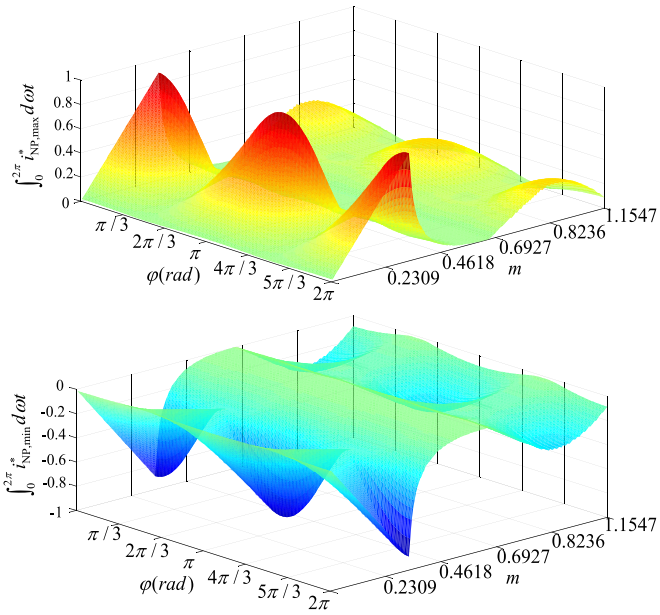


Fig. 8. $\bar{i}^*_{\rm NP,min}$ and $\bar{i}^*_{\rm NP,max}$ with respect to m and φ.

function of the NP voltage recovery ability for the negative and positive NP voltage offset in one fundamental period as $f_{\rm INC}$ and $f_{\rm DEC}$

$$\begin{aligned} f_{\rm INC} &= \frac{1}{2f_s}\int_0^{2\pi} i^*_{\rm NP,min} d\omega t = \frac{1}{2f_s}\bar{i}^*_{\rm NP,min} \\ f_{\rm DEC} &= \frac{1}{2f_s}\int_0^{2\pi} i^*_{\rm NP,max} d\omega t = \frac{1}{2f_s}\bar{i}^*_{\rm NP,max}. \end{aligned} \tag{19}$$

Fig. 8 shows $\bar{i}^*_{\rm NP,min}$ and $\bar{i}^*_{\rm NP,max}$ with respect to m and φ. The following conclusions can be drawn from Fig. 8.

1) When the clamping mode with the largest NP current is always selected, $\bar{i}^*_{\rm NP,max} > 0$, which means that the NP voltage shows a downward trend in a fundamental cycle; when the clamping mode with the smallest NP current is always selected, $\bar{i}^*_{\rm NP,min} < 0$, which means that the NP voltage shows an upward trend in a fundamental cycle. And, the absolute value of $\bar{i}^*_{\rm NP,max}$ and $\bar{i}^*_{\rm NP,min}$ at the same m and φ are equal, indicating that the algorithm has the same recovery ability under the positive or negative unbalanced NP voltage.
2) With a higher Pf and lower m, the algorithm has better ability to recover the NP voltage than other conditions.
3) When m is 0.577, the algorithm has the worst ability to recover the NP voltage. This is because most of operation points belong to one clamping mode areas, as shown in Fig. 4.

V. REALIZATION OF RCMV_DPWM

A. Preprocessing

It should be noted that three phase currents are involved in the calculation of the NP current in Table III. In order to calculate the NP current in the next switching cycle, the phase currents in the next switching cycle should be predicted by using the phase currents in the present switching cycle. The predictive method is as follows.

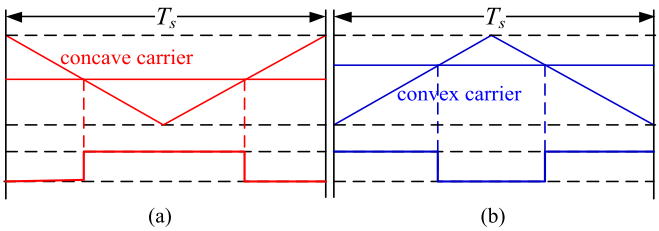


Fig. 9. Two carrier types. (a) Concave carrier. (b) Convex carrier.

First, the current vector in the ABC stationary frame is transformed into the current vector in the stationary $\alpha\beta$ reference frame by using the Clarke transformation, which is

$$[i_\alpha, i_\beta, i_0]^T = C_{3S/2S}[i_a, i_b, i_c]^T. \tag{20}$$

Then, a rotation transformation is used to predict the current vector in the stationary $\alpha\beta$ reference frame in the next switching cycle, which is

$$[i'_\alpha, i'_\beta, i'_0]^T = C_{\omega T_S}[i_\alpha, i_\beta, i_0]^T. \tag{21}$$

At last, the predicted current vector in the ABC stationary frame in the next switching cycle can be acquired by using the anti-Clarke transformation, which is

$$[i'_a, i'_b, i'_c]^T = C_{2S/3S}[i'_\alpha, i'_\beta, i'_0]^T. \tag{22}$$

So, the phase currents predictive method can be acquired as

$$[i'_a, i'_b, i'_c]^T = C_{2S/3S}\left[C_{\omega T_S}\left(C_{3S/2S}[i_a, i_b, i_c]^T\right)\right]. \tag{23}$$

In (20)–(23), the transformation matrixes are

$$\mathbf{C}_{3S/2S} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1 & 1 & 1 \end{bmatrix}$$

$$\mathbf{C}_{\omega T_S} = \begin{bmatrix} \cos\omega T_S & \sin\omega T_S & 0 \\ -\sin\omega T_S & \cos\omega T_S & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

and $\mathbf{C}_{2S/3S} = \mathbf{C}_{3S/2S}{}^{-1}$.

B. Determine Carrier and Modulation Waves

Because carrier-based PWM compares carrier with modulation wave to generate the PWM sequences and it is easy to be implemented. The carriers can be divided into two types: the concave carrier, as shown in Fig. 9(a); and the convex carrier, as shown in Fig. 9(b).

RCMV_DPWM can be realized by comparing the carriers with the three-phase modulation waves. According to the geometric relationship, the modulation wave for phase *X* are easily obtained as

$$\begin{aligned} u_X &= (1 + d_{X,1})u_{\mathrm{dc}} \quad (\text{if } d_{X,-1} = 0) \\ u_X &= (1 - d_{X,-1})u_{\mathrm{dc}} \quad (\text{if } d_{X,1} = 0). \end{aligned} \tag{24}$$

For example, the carrier-based realization of PB1 and PB2 of RCMV_DPWM is shown in Fig. 10. For other clamping modes, the carrier types can be referred to Table V.

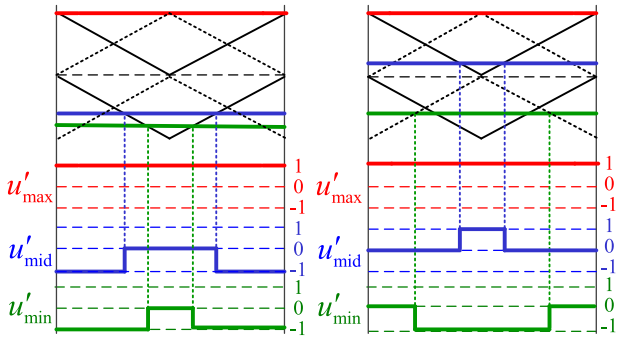


Fig. 10. Realization of PB1 and PB2 of RCMV_DPWM.

TABLE V
CARRIER TYPES FOR DIFFERENT CLAMPING MODES

Mode	Carrier for $u_{\max}$	Carrier for u_{mid}	Carrier for $u_{\min}$
PB1	concave	concave	concave
PB2	concave	concave	convex
NB1	concave	concave	concave
NB2	convex	concave	convex
NP1	convex	convex	convex
NP2	convex	concave	concave
NP3	convex	concave	convex

According to the analysis, the realization of RCMV_DPWM contains the following three considerations: 1) preprocessing; 2) selecting clamping mode to control the NP voltage and reduce CMV; and 3) generating the specific PWM sequence. Finally, the flow chart of RCMV_DPWM is shown in Fig. 11.

VI. PERFORMANCE ANALYSIS

A. AC Ripple on the NP Voltage

The NP voltage Δu_{NP} can be expressed as the function of I_m, m, and φ.

$$\Delta u_{\mathrm{NP}}(\omega t) = \frac{I_m \int i^*_{\mathrm{NP}}(\omega t)d\omega t}{2\pi f(C_1 + C_2)} = \frac{I_m \Delta u^*_{\mathrm{NP}}(\omega t)}{2\pi f(C_1 + C_2)} \tag{25}$$

where $\Delta u^*_{\mathrm{NP}}(\omega t) = \int i^*_{\mathrm{NP}}(\omega t)d\omega t$ is a normalized function of the NP voltage. The normalized ac ripple on the NP voltage can be expressed as

$$\Delta \tilde{u}^*_{\mathrm{NP}} = \max(\Delta u^*_{\mathrm{NP}}) - \min(\Delta u^*_{\mathrm{NP}}). \tag{26}$$

$\Delta \tilde{u}^*_{\mathrm{NP}}$ is related to m and φ, which can be used to evaluate the ac ripple on the NP voltage under different PWM strategies.

The $\Delta \tilde{u}^*_{\mathrm{NP}}$ under SVPWM, SPWM, TRIPWM, RCMV_DPWM, and DPWM I–IV with respect to m and φ are shown in Fig. 12. The maximum value of $\Delta \tilde{u}^*_{\mathrm{NP}}$ for SVPWM, TRIPWM, and SPWM is about 0.075, while $m = 1.154$ ($m = 1$ for SPWM) and $\varphi = \pm\pi/2$. The maximum value of $\Delta \tilde{u}^*_{\mathrm{NP}}$ for DPWM I–IV is about 0.15, while $m = 0.577$ and $\varphi = 0$. The maximum value of $\Delta \tilde{u}^*_{\mathrm{NP}}$ for RCMV_DPWM is about 0.065, while $m = 0.577$ and $\varphi = 0$. It can be seen that the ac ripple on the NP voltage cannot be suppressed fully under RCMV_DPWM but with minimum amplitude compared to other DPWM strategies.

In this subsection, only ac ripple on the NP voltage is studied. It should be noted that there are not only ac ripple but also

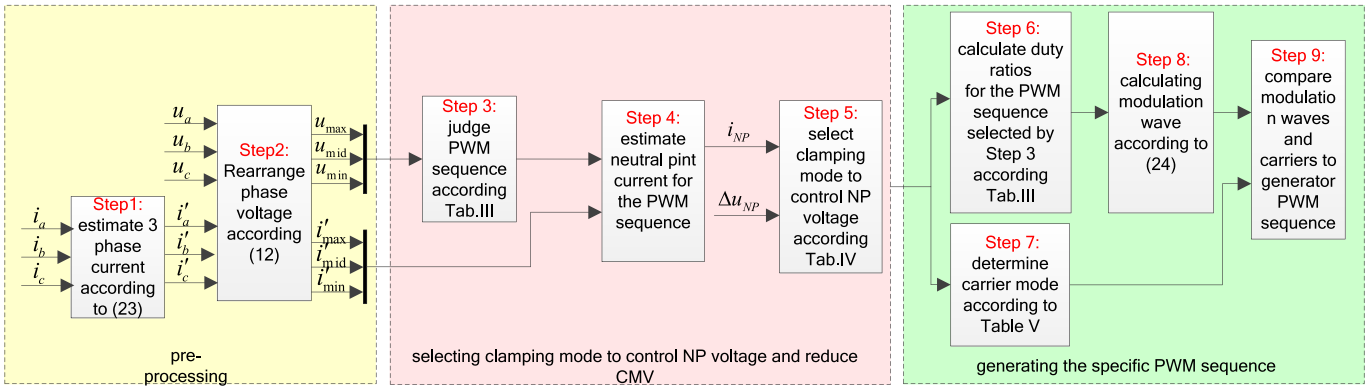


Fig. 11. Flowchart of RCMV_DPWM.

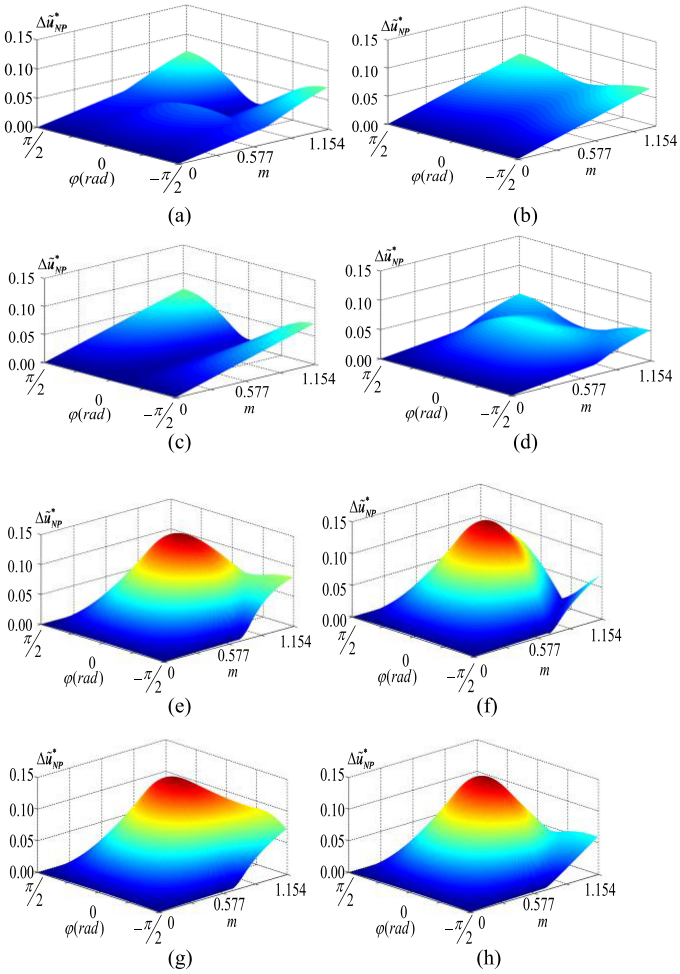


Fig.12. $\Delta\tilde{u}^*_{\rm NP}$ with respect to m and φ under different PWM strategies. (a) SVPWM. (b) SPWM. (c)TRIPWM. (d) RCMV_DPWM. (e) DPWM I. (f) DPWM II. (g) DPWM III. (h) DPWM IV.

dc offset on the NP voltage under DPWM I–IV. The dc offset under DPWM I–IV cannot be calculated by using simulation because it is related to too many non-ideal factors. However, the dc offset on the NP voltage can be completely removed under RCMV_DPWM. The phenomena can be found in experimental results.

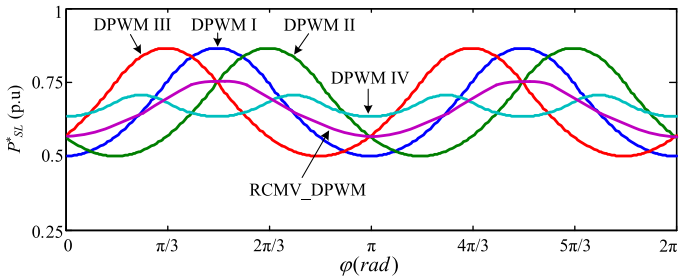


Fig. 13. $P^*_{\rm SL}$ under different PWM strategies.

B. Switching Loss

Conduction losses for different PWMs strategies are approximately equal but the switching losses are quite different from each other. So, for the loss comparison under different PWM strategies, the switching loss is significant and the conduction loss cannot be considered. The average switching loss over the fundamental cycle can be calculated as

$$p_{\rm loss} = \frac{1}{f}\frac{u_{\rm dc}(t_{\rm on}+t_{\rm off})}{2T_S}\int_0^{2\pi}\sum_{X=A,B,C} k_X i_X(\omega t)d\omega t \quad (27)$$

where $t_{\rm on}$ and $t_{\rm off}$ represent the turn-ON and turn-OFF times of the switching devices, respectively, k_X is the number of switching actions of phase X in one switching cycle, which is related to sequences. Unedr SVPWM, TRIPWM, and SPWM, $k_X = 1$, and under DPWM I–IV and RCMV_DPWM, $k_X = 1$ or 0.

The calculation results of the three phase switching losses in a fundamental cycle with respect to m and φ for SVPWM and DPWM I–IV and RCMV_DPWM are obtained. It is more important to compare switching loss under different PWM strategies. Let the total switching losses for SVPWM as the baseline, the three phase switching losses for DPWM I–IV and the RCMV_DPWM can be normalized as

$$P^*_{\rm SL} = P_{\rm SL}/P_{\rm SL\_SVPWM}. \quad (28)$$

The curves of $P^*_{\rm SL}$ under different PWM strategies are shown in Fig. 13. The maximum and minimum $P^*_{\rm SL}$ under DPWM I–III is about 0.86 and 0.5, respectively. The maximum and minimum $P^*_{\rm SL}$ under DPWM IV is about 0.75 and 0.68, respectively.

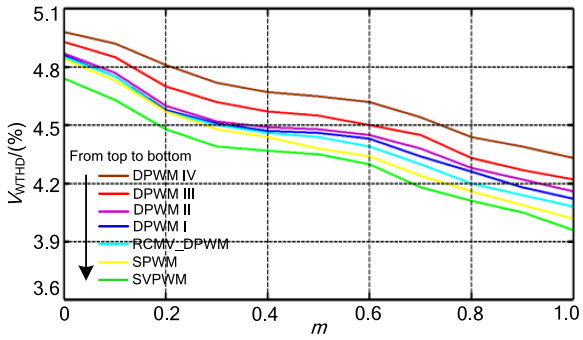


Fig. 14. V_{WTHD} with respect to m under different modulation strategies.

TABLE VI
KEY PARAMETERS OF THE SYSTEM

Parameter	Value
dc-link voltage	200V
upper and lower dc-link capacitor	1000μF
resistive-inductive load 1 for high power factor (Z_{H1})	$1.8e^{j\pi/9}\Omega$
resistive-inductive load 2 for high power factor (Z_{H2})	$6.2e^{j\pi/9}\Omega$
resistive-inductive load 1 for low power factor (Z_{L1})	$1.8e^{j4\pi/9}\Omega$
resistive-inductive load 2 for low power factor (Z_{L2})	$6.2e^{j4\pi/9}\Omega$
switching frequency	6000Hz
fundamental frequency	50Hz

The maximum P^*_{SL} under RCMV_DPWM is about 0.75, and the minimum P^*_{SL} under RCMV_DPWM is about 0.57. Therefore, RCMV_DPWM can combine the advantages of DPWM I–III and IV.

C. Output Performance

The weighted total harmonic distortion V_{WTHD} is usually used to evaluate the harmonic characteristics of the output voltage, and can be expressed as

$$V_{\mathrm{WTHD}} = \sqrt{\sum_{h=2}^{\infty} (V_h/h)^2}/V_1 \tag{29}$$

where V_1 and V_h are the rms value of the fundamental and the hth harmonic components of the outputted line-to-line voltage. Fig. 14 shows the curves of V_{WTHD} related to m under different PWM strategies. It can be seen that with m increasing, V_{WTHD} under SVPWM, SPWM, RCMV_DPWM, and DPWM I decreases. V_{WTHD} under SVPWM has a smallest value. It is obvious that V_{WTHD} of DPWM I–IV are higher than that of RCMV_DPWM. Consider that there is significant dc offset on the NP voltage under DPWM, the V_{WTHD} will increase further.

VII. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a prototype of the NPC TLC is built in the lab. The key system parameters are listed in Table VI, and the main control chip is Freescale's DSP MC56F8345.

Fig. 15 shows the steady-state experimental results of DPWM I and RCMV_DPWM under different m and loads, where $u_{c1}, u_{c2}, u_A, u_B, u_C, u_{\mathrm{AB}}$, and u_{CMV}, respectively, stand for the

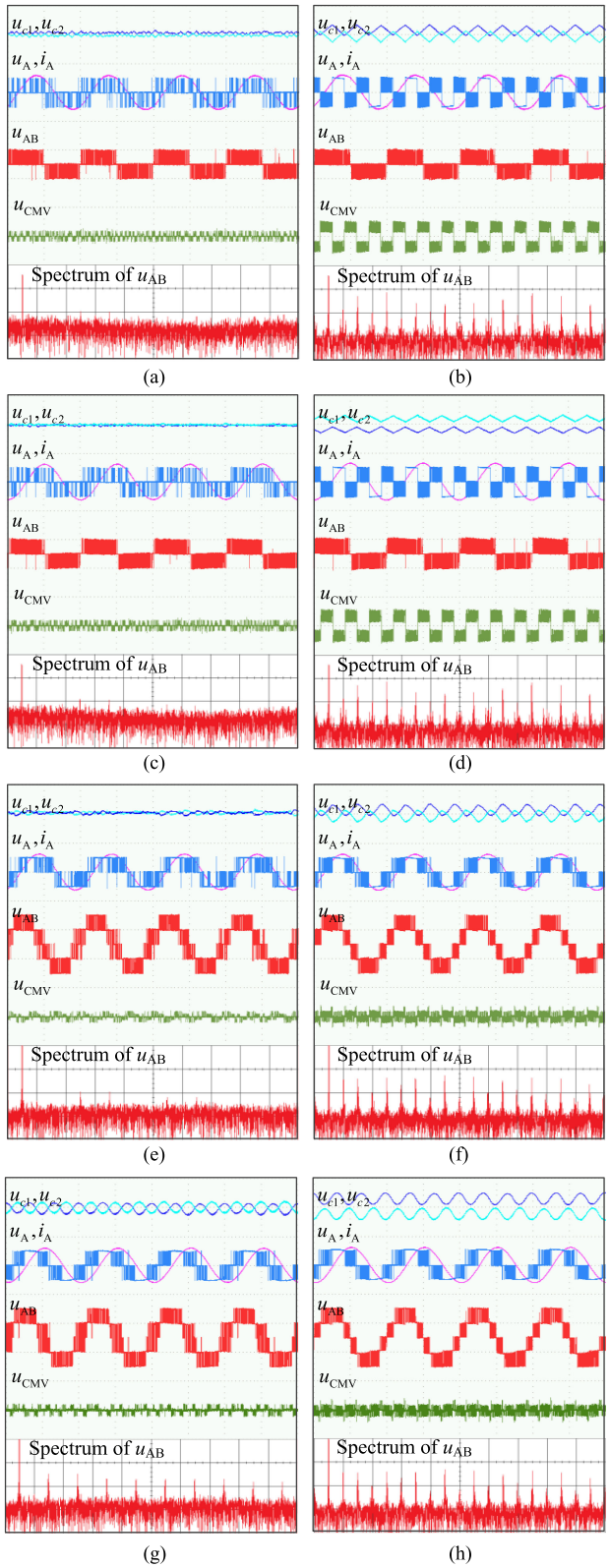


Fig. 15. Steady-state experimental results. (u_{C1} and u_{C2} : 20 V/div; u_A, u_{AB}, and u_{CMV} : 200 V/ div; i_A : 20 A/ div; time: 10 ms/div; spectrum of u_{AB}: 20 dB/ div; and frequency: 100 Hz/div.) (a) RCMV_DPWM with $m = 0.3, Z_{H1}$. (b) DPWM I with $m = 0.3, Z_{H1}$. (c) RCMV_DPWM with $m = 0.3, Z_{L1}$. (d) DPWM I with $m = 0.3, Z_{L1}$. (e) RCMV_DPWM with $m = 1.05, Z_{H2}$. (f) DPWM I with $m = 1.05, Z_{H2}$. (g) RCMV_DPWM with $m = 1.05, Z_{L2}$. (h) DPWM I with $m = 1.05, Z_{L2}$.

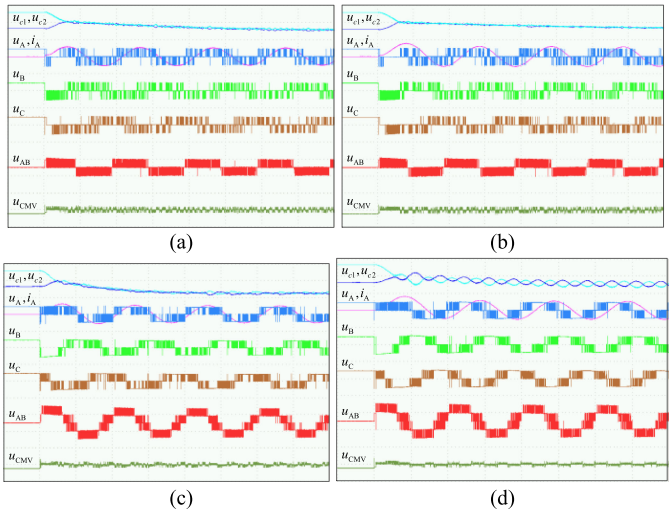


Fig. 16. NP voltage recovery process of RCMV_DPWM under different operating conditions. (u_{C1} and u_{C2} : 20 V/ div; u_A, u_B, u_C, $u_{\rm AB}$ and $u_{\rm CMV}$ 200 V/ div; i_A : 20 A/ div; and time : 10 ms/ div.) (a) $m = 0.3, Z_{H1}$. (b) $m = 0.3, Z_{L1}$. (c) $m = 1.05, Z_{H2}$. (d) $m = 1.05, Z_{L2}$.

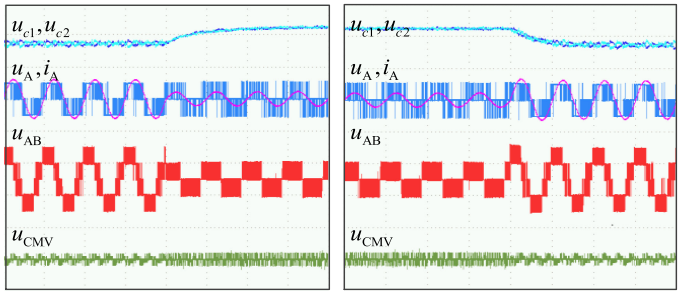


Fig. 17. Dynamic experimental results of RCMV_DPWM. (u_{C1} and u_{C2}: 20 V/div; u_A, $u_{\rm AB}$ and $u_{\rm CMV}$: 200 V/ div; i_A : 20 A/ div; and time: 10 ms/div.)

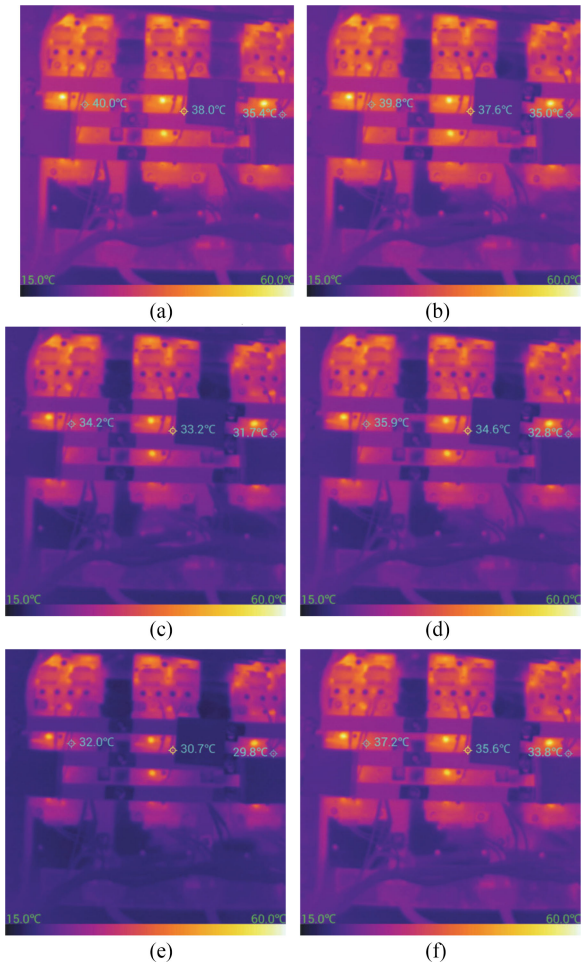


Fig. 18. Infrared thermograph of power devices under different PWM strategies. (a) SVPWM with $m = 1.05, Z_{H2}$. (b) SVPWM with $m = 1.05, Z_{L2}$. (c) RCMV_DPWM with $m = 1.05, Z_{H2}$. (d) RCMV_DPWM with $m = 1.05, Z_{L2}$. (e) DPWM I with $m = 1.05, Z_{H2}$. (f) DPWM I with $m = 1.05, Z_{L2}$.

voltage of upper capacitor, lower capacitor, phase A, phase B, phase C, phase A to B, and CMV, and i_a stands for the current of phase A. Moreover, the spectrums of $u_{\rm AB}$ are also shown. As shown in Fig. 15, for DPWM I, the NP voltage shows a relatively large fluctuation. While smaller capacitance is applied, a larger ac NP voltage fluctuation will be further caused. Therefore, a 1-mF capacitor is adopted for experiments. Comparing to DPWM I, the NP voltage of RCMV_DPWM can be better controlled with a smaller ac ripple, and the dc offset is almost eliminated. Moreover, for all conditions, CMVs are always reduced within $\pm u_{\rm dc}/6$ under RCMV_DPWM, which is much less than that under DPWM I. And from the spectrum of $u_{\rm AB}$, it found that there are many low-order harmonics once the NP voltage is not well controlled, especially in DPWM I.

By using RCMV_DPWM, it can be seen from Fig. 15 that not only the NP voltage can be well controlled, but also the CMV can be reduced. It verifies that RCMV_DPWM proposed in this paper has better performances compared to the traditional DPWM.

The NP voltage recovery processes under different operating conditions with unbalanced initial state are shown in Fig. 16. The experimental results prove that RCMV_DPWM has the good recovery ability on the NP voltage balance, and the dc offset can be quickly eliminated. Moreover, the CMV is always limited within $\pm u_{\rm dc}/6$ during the recovery processes.

In addition, the dynamic experimental results are provided in Fig. 17, where m is changed between 0.3 and 1.05. It can be seen that the NP voltage can be always well controlled and CMVs are limited within $\pm u_{\rm dc}/6$ during the dynamic processes.

Under the same environmental temperature (15°C) and cooling condition, the infrared thermal images of power devices after 2-h operation under the conditions of $m = 1.05, Z_{H2}$ or Z_{L2}, and 12-A peak phase current are given in Fig. 18. The infrared thermal images under SVPWM, RCMV_DPWM, and DPWM I are shown in Fig. 18(a)–(f), respectively. Under the condition of $m = 1.05, Z_{H2}$, it can be seen that SVPWM has the highest temperature rise (about 25 °C), and DPWM I has the lowest temperature rise (about 17 °C). For RCMV_DPWM, the temperature rise is about 19.2 °C, which is between that under SVPWM and DPWM I. Under the condition of $m = 1.05, Z_{L2}$, SVPWM still has the highest temperature rise (about 24.8 °C), and the temperature rise under RCMV_DPWM is about 21 °C, which

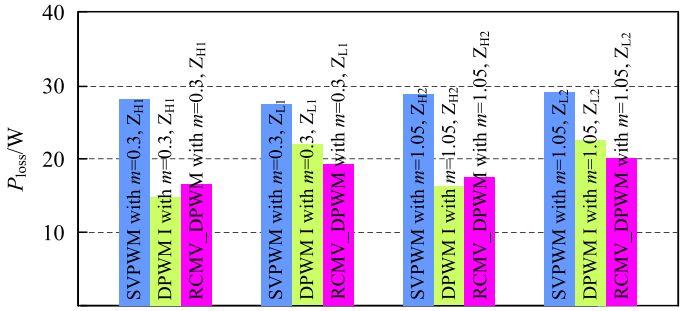


Fig. 19. Measured switching losses under different PWM strategies.

is a little lower than that under DPWM I (about 22.2 °C). From Fig. 18, it can be seen that the proposed RCMV_DPWM can reduce switching loss like the traditional DPWM. The temperature rise under different PWM strategies is consistency with the loss analysis given by Section VI-B. Moreover, the measured switching losses under different PWM strategies are given in Fig. 19. From Fig. 19, it can be seen that the switching loss under SVPWM is highest in all conditions, and the switching loss under RCMV_DPWM is a little higher than that of DPWM I with load of higher Pf, and the switching loss under RCMV_DPWM is a little lower than that of DPWM I with load of lower Pf.

VIII. Conclusion

In order to reduce the CMV, switching loss, and balance NP voltage simultaneously, RCMV_DPWM is proposed in this paper for the NPC TLC. The three goals are achieved by choosing a proper clamping mode. The performances of the NP voltage, switching loss, and outputted line-to-line voltage are analyzed. The experimental results verify the advantages of RCMV_DPWM in terms of the CMV, switching loss, and NP voltage.

For RCMV_DPWM, it should be noted that the NP voltage ac ripple is still not well controlled in the conditions of a high MI and a low pf. That is because the NP voltage cannot be adjusted bidirectionally in those conditions. Moreover, the algorithm of the proposed RCMV_DPWM is a bit complicated, which may be limited in practice.

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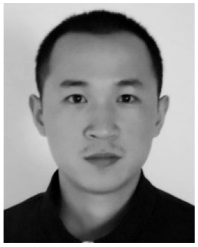

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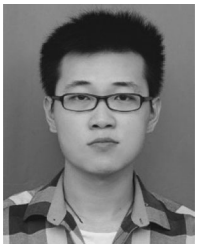

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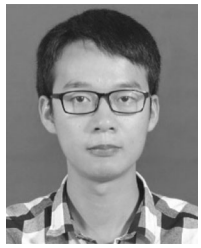

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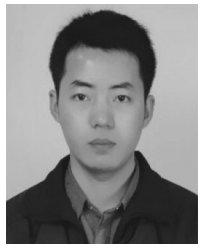

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