A New Two Input-Single Output High Voltage Gain Converter With Ripple-Free Input Currents and Reduced Voltage on Semiconductors

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***Abstract*—In this paper, a new non-isolated two-input single-output dc–dc converter with high voltage gain is proposed. In the proposed converter, there are two three-winding coupled inductors used to achieve a high voltage gain and ripple-free input currents. The proposed converter has two switches, and their control pulses are the same as the control pulses of the two-phase interleaved converters with a phase shift equal to 180°. The voltage stresses of switches and diodes are reduced and are always lower than the high output voltage. The proposed converter is extendable to a four-input single-output converter in which the switches have the control pulses the same as those in four-phase converters with phase shifts equal to 90°. In this paper, the proposed topology is analyzed in all operating modes, and the values of current and voltage stresses of all switches and diodes, voltage gain, and required conditions for input current ripple cancelation are calculated during a switching period. Finally, the accuracy performance of the proposed converter is reconfirmed through experimental results for 225- and 298-W prototypes.**

***Index Terms*—DC–DC non-isolated converter, high voltage gain, reduced voltage stresses of switches and diodes, ripple-free input currents, two input boost stages.**

I. Introduction

RENEWABLE energy sources such as fuel cells and photovoltaic (PV) systems have attracted a lot of attention in recent years due to the air pollution caused by fossil energy sources [1]. In fact, the reliability and availability of these energy sources are low. As a result, to obtain constant energy from these energy sources such as PV cells, these have to be combined with each other to increase their reliability. As an interface to combine these different energy sources with different voltage and current features, the dual-input dc converters are required [2]–[3]. Then, these can become a reliable energy source for high-intensity-discharge lamps of automobile head-

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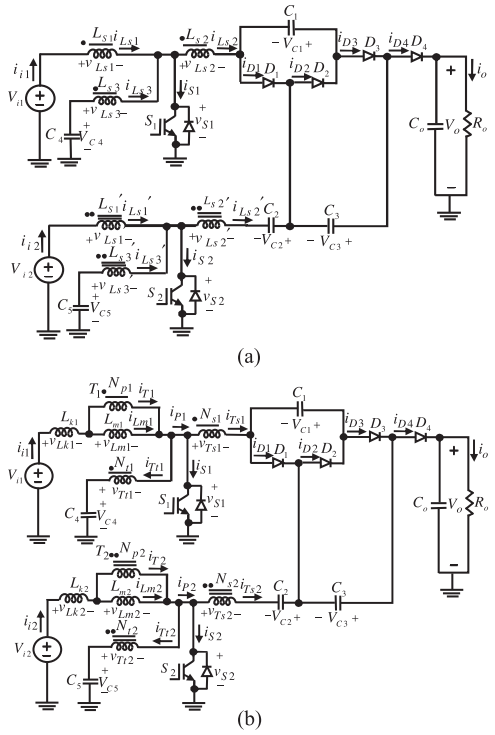

Fig. 1. (a) Proposed high voltage gain converter. (b) Power circuit of the proposed converter by using a transformer model of coupled inductors.

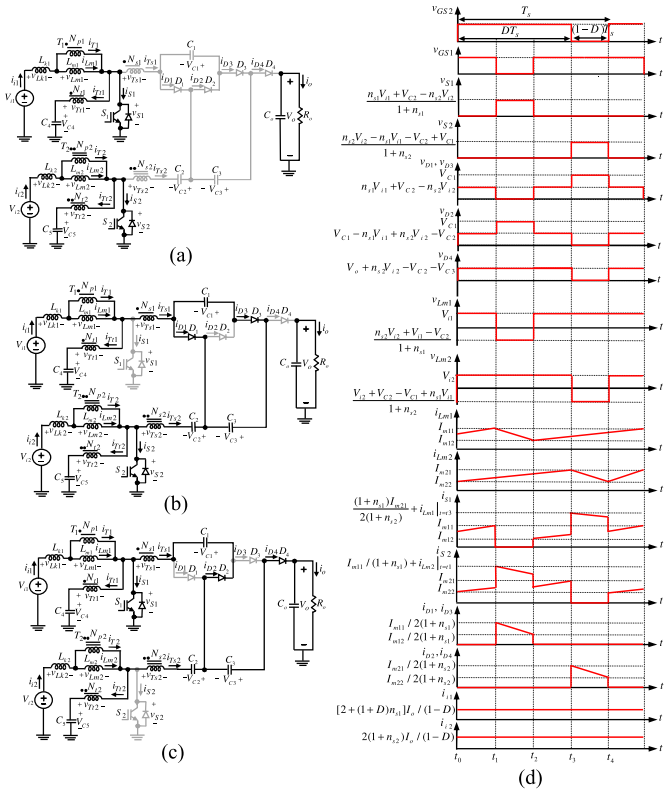

Fig. 2. Equivalent circuits and waveforms of the proposed converter. (a) Modes 1 and 3. (b) Mode 2. (c) Mode 4. (d) Waveforms.

dc converter with input current ripple cancelation is presented, which uses a three-winding coupled inductor to increase the voltage gain and eliminate input current ripples. In [27] and [28], two bidirectional dc–dc converters are presented, which their conversion ratios can be increased by adding the turn ratios of the implemented coupled inductors. Also, there are two interleaved dc–dc bidirectional converters presented in [29], which have the capability of eliminating the input current ripples only for the duty ratio of 0.5, which is common among interleaved structures.

In this paper, a new two input-single output non-isolated high-voltage-gain converter with ripple-free input currents is proposed. In this paper, the proposed topology is analyzed theoretically, and the values of current and voltage stresses of all switches and diodes, the voltage gain, and required conditions for input current ripple cancelation are calculated. Finally, the accuracy performance of the proposed converter is verified through experimental results.

II. Proposed Converter

The power circuit of the proposed high-voltage-gain converter and its transformer model is shown in Fig. 1(a) and (b), respectively. In the proposed converter first coupled inductor is considered with inductances L_{S1} as the first winding, L_{S2} as the second winding, and L_{S3} as the third winding, and the inductances M_{12}, M_{13}, and M_{23} as coupling inductances between two windings, and second coupled inductor is considered with inductances L'_{S1} as the first winding, L'_{S2} as the second winding, and L'_{S3} as the third winding, and the inductances M'_{12}, M'_{13}, and M'_{23} as coupling inductances between two windings.

The coupled inductors are modeled with the magnetizing inductances L_{m1} and L_{m2}, the leakage inductances L_{k1} and L_{k2} and the transformers T_1 and T_2, as shown in Fig. 1(b). The turns ratio of the secondary winding of transformers is considered as $n_{s1} = N_{s1}/N_{p1}$ and $n_{s2} = N_{s2}/N_{p2}$. Also, the turns ratio of the third winding is considered as $n_{t1} = N_{t1}/N_{p1}$ and $n_{t2} = N_{t2}/N_{p2}$. Since the capacitors are large enough, they can be considered as constant voltage sources of V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5}. In the steady state, the voltages of the capacitors C_4 and C_5 are equal to V_{i1} and V_{i2}, respectively. The equivalent circuits of the proposed converter and the voltage and current waveforms of the proposed converter during a switching period (T_s) are shown in Fig. 2. This figure shows the proposed converter as a type of two-phase converter and the switches' pulses are applied with a phase shift equal to 180°. The proposed converter is analyzed for $D > 0.5$. Based on the waveform of the current i_{Lm1} from Fig. 2(d), it can be seen that I_{m12} and I_{m11} are the minimum and maximum values of the current i_{Lm1} at moments t_2 and t_1, respectively. Moreover, based on the waveform of the current i_{Lm2} in Fig. 2(d), it can be seen that I_{m22} and I_{m21} are the minimum and maximum values of the current i_{Lm2} at moments t_0 and t_3, respectively.

A. First and Third Operating Modes [$(t_0 \le t < t_1)$, $(t_2 \le t < t_3)$]

The equivalent circuit of the first and third operating modes is shown in Fig. 2(a). By considering Fig. 2(a), the voltages v_{Lm1}, v_{Lk1}, v_{Lm2}, and v_{Lk2} are obtained as V_{i1}/n_{t1}, $(V_{i1} - V_{i1}/n_{t1})$,

V_{i2}/n_{t2}, and $(V_{i2} - V_{i2}/n_{t2})$, respectively. Therefore, the currents equations are obtained as follows:

$$i_{Lm1} = [V_{i1}(t - t_2)]/(n_{t1}L_{m1}) + I_{m12} \quad (1)$$

$$i_1 = [(n_{t1} - 1)V_{i1}(t - t_2)]/(n_{t1}L_{k1}) + i_{Lk1}\,|_{t=t2} \quad (2)$$

$$i_{Lm2} = [V_{i2}(t - t_0)]/(n_{t2}L_{m2}) + I_{m22} \quad (3)$$

$$i_2 = [(n_{t2} - 1)V_{i2}(t - t_0)]/n_{t2}L_{k2} + i_{Lk2}\,|_{t=t0}\,. \quad (4)$$

$$i_{C4} = i_{Tt1} = (i_1 - i_{Lm1})/n_{t1} \quad (5)$$

$$i_{C5} = i_{Tt2} = (i_2 - i_{Lm2})/n_{t2} \quad (6)$$

$$i_{Co} = -I_o \quad (7)$$

$$i_{S1} = i_1 - i_{Tt1} = [(n_{t1} - 1)/n_{t1}]i_1 + i_{Lm1}/n_{t1} \quad (8)$$

$$i_{S2} = i_2 - i_{Tt2} = [(n_{t2} - 1)/n_{t2}]i_2 + i_{Lm2}/n_{t2}. \quad (9)$$

B. Second Operating Mode ($t_1 \le t < t_2$)

The equivalent circuit of this mode is shown in Fig. 2(b). During this mode, the same as the first mode, (3), (4), and (6) are obtained. By considering $V_{C4} = V_{i1}$, the voltages v_{Lm1} and v_{Lk1} are obtained as $v_{Lm1} = [(n_{s2}/n_{t2})V_{i2} + V_{i1} - V_{C2}]/(n_{s1} + n_{t1})$ and $v_{Lk1} = -(1 - n_{t1})v_{Lm1}$, respectively. Therefore, the currents i_{Lm1} and i_1 are obtained as follows:

$$i_{Lm1} = [(n_{s2}/n_{t2})V_{i2} + V_{i1} - V_{C2}](t - t_1)/ [L_{m1}(n_{s1} + n_{t1})] + I_{m11} \quad (10)$$

$$i_1 = \frac{(n_{t1} - 1)[(n_{s2}/n_{t2})V_{i2} + V_{i1} - V_{C2}]}{L_{k1}(n_{s1} + n_{t1})} \times (t - t_1) + i_{Lk1}\,|_{t=t1}\,. \quad (11)$$

Based on Fig. 2(b), the relation between the currents of the three windings of the transformers T_1 and T_2 is written as $i_{T1} - n_{t1}i_{Tt1} + n_{s1}i_{Ts1} = 0$ and $i_{T2} - n_{t2}i_{Tt2} + n_{s2}i_{Ts2} = 0$, respectively. By applying the Kirchhoff's Current Law (KCL) the currents i_{C1}, i_{C2}, i_{C4}, i_{C5}, and i_{S2}, and diode's currents are obtained as follows:

$$i_{C2} = [i_{Lm1} - (1 - n_{t1})i_1]/(n_{t1} + n_{s1}) \quad (12)$$

$$i_{C4} = i_{Tt1} = i_1 - [i_{Lm1} - (1 - n_{t1})i_1]/(n_{t1} + n_{s1}) \quad (13)$$

$$i_{C5} = \frac{i_2 - i_{Lm2} + n_{s2}[(1 - n_{t1})i_1 - i_{Lm1}]/(n_{t1} + n_{s1})}{n_{t2}} \quad (14)$$

$$i_{S2} = \frac{1}{n_{t2}}\left\{ i_{Lm2} + (n_{t2} - 1)i_2 + \frac{(n_{t2} + n_{s2})[(n_{t1} - 1)i_1 + i_{Lm1}]}{n_{t1} + n_{s1}} \right\} \quad (15)$$

$$-i_{C1} = i_{D1} = i_{D3} = [i_{Lm1} - (1 - n_{t1})i_1]/[2(n_{t1} + n_{s1})]. \quad (16)$$

The current value of i_{Co} by considering Fig. 2(b) is obtained as (7).

C. Fourth Operating Mode ($t_3 \le t < t_4$)

The equivalent circuit of this mode is shown in Fig. 2(c). In this mode, similar to the first mode, (1) and (2) are obtained. By considering $V_{C5} = V_{i2}$, the voltages v_{Lm2} and v_{Lk2} are obtained as $v_{Lm2} = [V_{i2} + V_{C2} - V_{C1} + (n_{s1}/n_{t1})V_{i1}]/(n_{s2} + n_{t2})$ and $v_{Lk2} = (1 - n_{t2})v_{Lm2}$, respectively. Therefore, the currents i_{Lm2} and i_2 are obtained as follows:

$$i_{Lm2} = \frac{[V_{i2} + V_{C2} - V_{C1} + (n_{s1}/n_{t1})V_{i1}](t - t_3)}{L_{m2}(n_{s2} + n_{t2})} + I_{m21} \quad (17)$$

$$i_2 = \frac{(n_{t2} - 1)[V_{i2} + V_{C2} - V_{C1} + (n_{s1}/n_{t1})V_{i1}]}{L_{k2}(n_{s2} + n_{t2})} \times (t - t_3) + i_{Lk2}\,|_{t=t3}\,. \quad (18)$$

In this mode, the currents of capacitors, switches, and diodes are as follows:

$$i_{C1} = i_{D2} = i_{D4} = [i_{Lm2} - (1 - n_{t2})i_2]/[2(n_{t2} + n_{s2})] \quad (19)$$

$$i_{S1} = \frac{1}{n_{t1}}\left[i_{Lm1} + (n_{t1} - 1)i_1 + (n_{t1} + n_{s1}) \times \frac{i_{Lm2} - (1 - n_{t2})i_2}{2(n_{t2} + n_{s2})} \right] \quad (20)$$

$$i_{Co} = i_{D4} - I_o = [i_{Lm2} - (1 - n_{t2})i_2]/[2(n_{t2} + n_{s2})] - I_o \quad (21)$$

$$i_{C4} = \frac{i_1 - i_{Lm1} + n_{s1}[-i_{Lm2} + (1 - n_{t2})i_2]/[2(n_{t2} + n_{s2})]}{n_{t1}} \quad (22)$$

$$i_{C5} = i_2 - [i_{Lm2} - (1 - n_{t2})i_2]/(n_{t2} + n_{s2}). \quad (23)$$

III. Inductors Current Calculation

Considering (2), (4), (11), and (18), the required condition for canceling input current ripples of i_1 and i_2 is obtained as follows:

$$n_{t1} = n_{t2} = 1, L_{k1} \neq 0, \text{and } L_{k2} \neq 0. \quad (24)$$

Based on the current-balance law of the capacitors, and by considering (16) and (19) for i_{C1}, (7) and (21) for i_{Co}, (5), (13), and (22) for i_{C4}, and (6), (14), and (23) for i_{C5}, the average value of the currents i_{C1}, i_{Co}, i_{C4}, and i_{C5} under $n_{t1} = n_{t2} = 1$ is made equal to zero in the following equations:

$$(1 - D)T_s I_{Lm2}/[2(1 + n_{s2})] + (1 - D)T_s(-I_{Lm1})/[2(1 + n_{s1})] = 0 \quad (25)$$

$$DT_s(-I_o) + (1 - D)T_s\,(I_{Lm2}/[2(1 + n_{s2})] - I_o) = 0 \quad (26)$$

$$(2D - 1)T_s(I_1 - I_{Lm1}) + (1 - D)T_s[I_1 - I_{Lm1}/(1 + n_{s1})] + (1 - D)T_s[I_1 - I_{Lm1} - n_{s1}I_{Lm2}/[2(1 + n_{s2})] = 0 \quad (27)$$

$$(2D - 1)T_s(I_2 - I_{Lm2}) + (1 - D)T_s\,[I_2 - I_{Lm2}/(1 + n_{s2})] + (1 - D)T\,[I_2 - I_{Lm2} - n_{s2}I_{Lm1}/(1 + n_{s1})] = 0. \quad (28)$$

As a result, the average value of the currents i_{Lm1} and i_{Lm2} (I_{Lm1} and I_{Lm2}), and the average value of the input currents

TABLE I
VOLTAGE STRESSES OF SWITCHES AND DIODES

The voltage stresses on switches	$v_{S1}=\frac{n_{s1}V_{i1}+V_{C2}-n_{s2}V_{i2}}{1+n_{s1}}=\frac{(1+n_{s1})V_{i1}}{(1+n_{s2})(1-D)}$, $v_{S2}=\frac{n_{s2}V_{i2}-n_{s1}V_{i1}-V_{C2}+V_{C1}}{1+n_{s2}}=\frac{V_{i2}}{1-D}$
The maximum and minimum voltage stresses on diodes	$v_{D1}\big\|_{\min}=v_{D3}\big\|_{\min}=n_{s2}V_{i2}-n_{s1}V_{i1}-V_{C2}=-\frac{n_{s1}+1}{1-D}V_{i1}$; $v_{D1}\big\|_{\max}=v_{D2}\big\|_{\max}=v_{D3}\big\|_{\max}=-V_{C1}=-\frac{(1+n_{s1})V_{i1}}{1-D}-\frac{(1+n_{s2})V_{i2}}{1-D}$; $v_{D2}\big\|_{\min}=n_{s1}V_{i1}-n_{s2}V_{i2}+V_{C2}-V_{C1}=-\frac{n_{s2}+1}{1-D}V_{i2}$, $v_{D4}=-\frac{(1+n_{s2})V_{i2}}{1-D}$

(i_{i1} and i_{i2}), switches and diodes are obtained as follows:

$$I_{Lm1}=[2(1+n_{s1})/(1-D)]I_o=(I_{m11}+I_{m12})/2 \quad (29)$$

$$I_1=[2+(1+D)n_{s1})]I_o/(1-D) \quad (30)$$

$$I_{S2}=I_2=I_{Lm2}=[2(1+n_{s2})/(1-D)]\times I_o=(I_{m21}+I_{m22})/2 \quad (31)$$

$$I_{S1}=I_1-I_o=[1+(1+D)n_{s1}+D]I_o/(1-D) \quad (32)$$

$$I_{D1}=I_{D2}=I_{D3}=I_{D4}=I_o. \quad (33)$$

The maximum and minimum values of the currents i_{Lm1} and i_{Lm2} can be written as follows:

$$I_{m11}=[2(1+n_{s1})/(1-D)]I_o+V_{i1}DT_s/(2L_{m1}) \quad (34)$$

$$I_{m12}=[2(1+n_{s1})/(1-D)]I_o-V_{i1}DT_s/(2L_{m1}) \quad (35)$$

$$I_{m21}=[2(1+n_{s2})/(1-D)]I_o+V_{i2}DT_s/(2L_{m2}) \quad (36)$$

$$I_{m22}=[2(1+n_{s2})/(1-D)]I_o-V_{i2}DT_s/(2L_{m2}). \quad (37)$$

IV. VOLTAGE GAIN CALCULATION

Based on the voltage-balance law of the inductances L_{m1} and L_{m2}, and based on the waveform of the voltages v_{Lm1} and v_{Lm2} from Fig. 2(d), and considering $n_{t1}=n_{t2}=1$, the following equations can be obtained:

$$DV_{i1}+(1-D)(n_{s2}V_{i2}-V_{C2}+V_{i1})/(n_{s1}+1)=0 \quad (38)$$

$$DV_{i2}+(1-D)(V_{i2}+V_{C2}-V_{C1}+n_{s1}V_{i1})/(n_{s2}+1)=0. \quad (39)$$

As a result, based on $V_{C3}=V_{C1}$ and $V_o=V_{C3}+V_{C1}-n_{s1}V_{i1}=2V_{C1}-n_{s1}V_{i1}$, the voltage across the capacitors and the output voltage for $n_{t1}=n_{t2}=1$ are obtained as follows:

$$V_{C2}=(1+n_{s1}D)V_{i1}/(1-D)+n_{s2}V_{i2} \quad (40)$$

$$V_{C1}=V_{C3}=[(1+n_{s1}D)V_{i1}+(1+n_{s2})V_{i2}]/(1-D) \quad (41)$$

$$V_o=\{[2+n_{s1}(1+D)]V_{i1}+2(1+n_{s2})V_{i2}\}/(1-D). \quad (42)$$

Considering Fig. 2, the voltage stresses on switches and diodes for $n_{t1}=n_{t2}=1$ can be summarized as shown in Table I.

TABLE II
USED PARAMETERS FOR VOLTAGE GAIN EQUATION

a, b, c, d, e, f, g, h and j	$a=n_{s1}(1-D)(r_{Tt1}+r_{C4})+2(1+ns_1)r_{S1}$, $b=2(1+ns_2)r_{S2}$; $c=2[n_{s2}(r_{Tt2}+r_{C5})+r_{S2}(2+n_{s2})]$; $d=2n_{s2}[n_{s2}(r_{Tt2}+r_{C5})+(2+n_{s2})r_{S2}]+2(1+n_{s2})r_{S2}+r_{D1}$; $+2(r_{Ts1}+r_{Ts2}+r_{C2}+r_{S2}+r_{Tt1}+r_{C4})-[2+(1+D)n_{s1}](r_{Tt1}+r_{C4})$; $e=n_{s1}(2-D)(r_{Tt1}+r_{C4})+3(1+ns_1)r_{S1}$; $f=e\cdot ns_1+3(1+ns_1)r_{S1}+r_{D2}+r_{Ts1}+r_{C1}+2r_{Ts2}+2r_{C2}+r_{S2}+r_{Tt1}-2n_{S2}(r_{Tt2}+r_{C5})$; $j=e\cdot n_{s1}+3(1+ns_1)r_{S1}+r_{D2}+r_{D1}-r_{D4}-r_{D3}+r_{Ts1}-2r_{C3}$; $h=d+[e+a\cdot(2D-1)](1+ns_1)+f+[c+b\cdot(2D-1)/(1-D)](1+ns_2)$; $g=d+[e+a\cdot(2D-1)](1+ns_1)$
V_{C1}	$V_{C1}=\frac{1+n_{s1}}{1-D}V_{i1}+\frac{1+n_{s2}}{1-D}V_{i2}-(V_{FD1}+V_{FD2})-\frac{V_{FS1}+V_{FS2}}{1-D}-\frac{I_o}{1-D}h$
V_{C2}	$V_{C2}=\frac{1+n_{s1}D}{1-D}V_{i1}-\frac{DV_{FS1}}{1-D}-\frac{I_o}{1-D}g+n_{s2}V_{i2}-V_{FD1}-V_{FS2}$
V_{C3}	$V_{C3}=\frac{1+n_{s1}}{1-D}V_{i1}+\frac{1+n_{s2}}{1-D}V_{i2}-\frac{V_{FS1}+V_{FS2}}{1-D}-\frac{(h+r_{C1}+r_{C3})I_o}{1-D}-(V_{FD2}+V_{FD3})$

In this part, the voltage gain of the proposed converter is calculated by considering the equivalent series resistance (ESR) of all components and forward voltage drops of switches and diodes. For this purpose, in the power circuit of the proposed converter in Fig. 1(b), a series resistance is placed in series with capacitors (r_C), inductors ($r_{Lp1}, r_{Tt1}, r_{Ts1}, r_{Lp2}, r_{Tt2}, r_{Ts2}$), switches ($r_S$), and diodes ($r_D$). Moreover, the on-state forward voltage drop of the diodes ($V_{\rm FD}$) and switches ($V_{\rm FS}$) is considered in series with them. Therefore, in this condition, the steady-state analysis of the proposed converter is rewritten. As a result, the output voltage considering ESRs of all components and forward voltage drops of switches and diodes is calculated as follows:

$$V_o=\frac{\begin{bmatrix}\frac{2+n_{s1}(1+D)}{1-D}V_{i1}+\frac{2(1+n_{s2})}{1-D}V_{i2}+V_{\rm FS1}(1+n_{s1})\\ -2\frac{V_{\rm FS1}+V_{\rm FS2}}{1-D}-(V_{\rm FD1}+V_{\rm FD2}+V_{\rm FD3}+V_{\rm FD4})\end{bmatrix}}{1+\frac{h-j}{R_o(1-D)}} \quad (43)$$

where the parameters a, b, c, d, e, f, g, h, and j are given in the first row of Table II. Furthermore, the voltages of capacitors considering ESRs of components are calculated as given in the second row of Table II.

V. DEVELOPED CONVERTER

The proposed converter in Fig. 1(a) can be extended to a four input single-output converter as shown in Fig. 3(a). The control signals of the four used switches S_1, S_2, S_3, and S_4 should be adjusted similarly to four-phase converters, as shown in Fig. 3(b). In the proposed converter, the obtained voltage gain for a duty cycle more than $0.75(D\geq 0.75)$ is higher than that for a duty cycle lower than 0.75. The dc characteristics of the proposed converter for $D\geq 0.75$ are obtained as given in Table III.

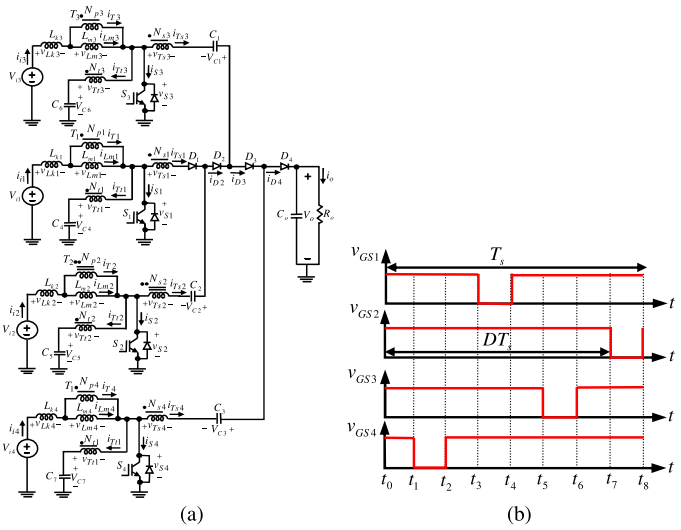

Fig. 3. (a) Power circuit of the proposed developed converter. (b) Trigger signals of the switches for the proposed developed converter.

TABLE III
CHARACTERISTICS OF THE PROPOSED DEVELOPED CONVERTER

Voltages of the capacitors	$V_{C1}=[(1+n_{s1}D)V_{i1}+(1+n_{s2})V_{i2}]/(1-D)+n_{s3}V_{i3}$ $V_{C2}=(1+n_{s1}D)V_{i1}/(1-D)+n_{s2}V_{i2}$ $V_{C3}=[(1+n_{s1}D)V_{i1}+(1+n_{s2})V_{i2}+(1+n_{s3})V_{i3}]/(1-D)+n_{s4}V_{i4}$
Voltage stresses on switches	$v_{S1}=V_{i1}/(1-D)$, $v_{S2}=V_{i2}/(1-D)$, $v_{S3}=V_{i3}/(1-D)$, $v_{S4}=V_{i4}/(1-D)$
Maximum voltage stresses on diodes	$v_{D1-\max}=-\frac{(1+n_{s1})V_{i1}}{1-D}-\frac{(1+n_{s2})V_{i2}}{1-D}$, $v_{D2}\big\vert_{\max}=-\frac{(1+n_{s2})V_{i2}}{1-D}-\frac{(1+n_{s3})V_{i3}}{1-D}$ $v_{D3}\big\vert_{\max}=-\frac{(1+n_{s4})V_{i4}}{1-D}-\frac{(1+n_{s3})V_{i3}}{1-D}$, $v_{D4}=-(1+n_{s4})V_{i4}/(1-D)$
Average input and inductors currents	$I_{Lm1}=(1+n_{s1})I_o/(1-D)$, $I_1=(1+n_{s1}D)I_o/(1-D)$ $I_2=I_{Lm2}=(1+n_{s2})I_o/(1-D)$, $I_3=I_{Lm3}=(1+n_{s3})I_o/(1-D)$, $I_{Lm4}=(1+n_{s4})I_o/(1-D)$

Therefore, the output voltage is obtained as follows:

$$V_o=\frac{1+n_{s1}D}{1-D}V_{i1}+\frac{1+n_{s2}}{1-D}V_{i2}+\frac{1+n_{s3}}{1-D}V_{i3}+\frac{1+n_{s4}}{1-D}V_{i4}. \quad (44)$$

In this proposed converter, similar to the main proposed converter in Fig. 1(a), the required conditions for achieving ripple-free input currents are calculated as (24).

VI. DESIGN CONSIDERATION

To verify the proposed converter operating in a continuous conduction mode (CCM), the average value of the current through the inductances L_{m2} and L_{m1} has to be higher than half of their current ripple. Therefore, the values of the inductances L_{m1} and L_{m2} by considering (29), (31), and (34)–(37) are obtained as follows:

$$L_{m1}>[R_o(1-D)DV_{i1}]/[2f_s(1+n_{s1})V_o] \quad (45)$$

$$L_{m2}>[R_o(1-D)DV_{i2}]/[2f_s(1+n_{s1})V_o]. \quad (46)$$

TABLE IV
AVERAGE CAPACITOR CURRENTS DURING A SWITCHING PERIOD

$$I_{C1}=\begin{cases}-I_o/(1-D) & during\ Mode\ 2\\ I_o/(1-D) & during Mode\ 4\end{cases},\ I_{C2}=\begin{cases}2I_o/(1-D) & during\ Mode\ 2\\ -2I_o/(1-D) & during Mode\ 4\end{cases}$$

$$I_{Co}=\begin{cases}-I_o & during\ Modes\ 1,2,3\\ DI_o/(1-D) & during Mode\ 4\end{cases},\ I_{C3}=\begin{cases}I_o/(1-D) & during\ Mode\ 2\\ -I_o/(1-D) & during Mode\ 4\end{cases}$$

$$I_{C5}=\begin{cases}\frac{-2n_{S2}I_o}{1-D} & during\ Mode\ 2\\ \frac{2n_{S2}I_o}{1-D} & during Mode\ 4\end{cases},\ I_{C4}=\begin{cases}\frac{[(1+D)n_{S1}]I_o}{1-D} & during\ Mode\ 2\\ I_1-I_{Lm1}=-n_{S1}I_o & during\ Modes\ 1,3\\ \frac{-[(2-D)n_{S1}]I_o}{1-D} & during Mode\ 4\end{cases}$$

The voltages across the first, second, third, and fourth windings of the utilized first coupled inductor in Fig. 1(a) can be written as follows:

$$v_{Ls1}=L_{s1}(di_{Ls1}/dt)+M_{21}(di_{Ls2}/dt)+M_{31}(di_{Ls3}/dt) \quad (47)$$

$$v_{Ls2}=M_{12}(di_{Ls1}/dt)+L_{s2}(di_{Ls2}/dt)+M_{32}(di_{Ls3}/dt) \quad (48)$$

$$v_{Ls3}=M_{13}(di_{Ls1}/dt)+M_{23}(di_{Ls2}/dt)+L_{s3}(di_{Ls3}/dt). \quad (49)$$

Then, considering $n_{t2}=n_{t1}=1$, $L_{k1}\neq 0$, and $L_{k2}\neq 0$, and (45) and (46) for achieving ripple-free input currents and CCM operation, the inductances of coupled inductors in Fig. 1(a) can be simplified as $L_{S1}=L_{m1}+L_{k1}=L_{m1}/K^2$, $L_{S2}=n_{s1}{}^2L_{m1}$, $L_{S3}=L_{m1}$, $M_{13}=M_{31}=L_{m1}$, and $M_{12}=M_{21}=M_{23}=M_{32}=n_{s1}L_{m1}$. In the same way, in the second coupled inductor, inductances can be replaced with $L'_{S1}=L_{m2}+L_{k2}=L_{m2}/K^2$, $L'_{S2}=n_{s2}{}^2L_{m2}$, $L'_{S3}=L_{m2}$, $M'_{13}=M'_{31}=L_{m2}$, and $M'_{12}=M'_{21}=M'_{23}=M'_{32}=n_{s2}L_{m2}$, where K the coupling coefficient of coupled inductors, which is defined as $K=\sqrt{L_m/(L_k+L_m)}$ in the realistic condition, is always lower than 1 and close to 1 in the range $0\ll K<1$.

Considering [1] and [30], the real voltage ripple across the output capacitor is obtained as $\Delta V_{Co}=0.01V_o-r_{Co}\Delta I_{Co}$. Considering Table IV, ΔI_{Co} is obtained as $\Delta I_{Co}=I_{Co}\big\vert_{\mathrm{mod}\,e2}-I_{Co}\big\vert_{\mathrm{mod}\,e1}=I_o/(1-D)$. Therefore, the minimum value of the capacitor C_o is calculated as follows:

$$C_{o\_\min}\big\vert_{\mathrm{ESR}}=D/[\{0.01-r_{Co}/[R_o(1-D)]\}R_of_s]. \quad (50)$$

On the other hand, based on [1], if the load changes equal to the full load, $\Delta I_o=V_o/R_o$, the value of the capacitor C_o has to be at least

$$C_{o\_\min}\big\vert_{\text{transient holding time}}=V_o/[0.01V_oR_o(0.1f_s)]. \quad (51)$$

Consequently, the minimum value of output capacitor can be obtained from the following inequality:

$$C_{o\_\min}>\max\{C_{o\_\min}\big\vert_{\mathrm{ESR}},\ C_{o\_\min}\big\vert_{\text{transient holding time}}\}. \quad (52)$$

The accurate design of the capacitors C_1, C_2, C_3, C_4, and C_5 includes only the ESR of capacitors. Based on Table IV, $V_{C4}=V_{i1}$, $V_{C5}=V_{i2}$, (40) and (41), the minimum

TABLE V
MINIMUM VALUES OF CAPACITORS

C_{1_min} C_{3_min}	$1/\{[(1\%)V_{C1}/V_o - 2r_C/[R_o(1-D)]]R_o f_s\}$
C_{2_min}	$2/\{[(1\%)V_{C2}/V_o - 4r_C/[R_o(1-D)]]R_o f_s\}$
C_{4_min}	$(1+D)n_{s1}/\{[(1\%)V_{i1}/V_o - 3n_{s1}r_C/[R_o(1-D)]]R_o f_s\}$
C_{5_min}	$2n_{s2}/\{[(1\%)V_{i2}/V_o - 4n_{s2}r_C/[R_o(1-D)]]R_o f_s\}$

TABLE VI
RMS CURRENTS OF THE WINDINGS OF COUPLED INDUCTORS IN FIG. 1(a)

RMS currents of the first coupled inductor	$I_{Ls1-rms} = \frac{2+(1+D)n_{s1}}{(1-D)} I_o$, $I_{Ls2-rms} = \sqrt{\frac{5I_o^2}{1-D}}$, $I_{Ls3-rms} = \sqrt{\frac{(n_s I_o)^2[(2D-1)(1-D)+(1+D)^2+(2-D)^2]}{1-D}}$
RMS currents of the second coupled inductor	$I_{L's1-rms} = \frac{2(1+n_{s2})}{(1-D)} I_o$, $I_{L's2-rms} = \sqrt{\frac{5I_o^2}{1-D}}$, $I_{L's3-rms} = \sqrt{\frac{8(n_s I_o)^2}{1-D}}$

value of these capacitors for their maximum voltage ripple of $\Delta V_C = (1\%)V_C - r_C \Delta I_C$ should verify the inequalities given in Table V. The total saved energy in the three windings of coupled inductors in Fig. 1(a), E_L, and in the capacitors, E_C, is obtained as follows:

$$\begin{aligned} E_L &= \frac{1}{2}(L_{s1} I_{Ls1-\mathrm{rms}}{}^2 + L_{s2} I_{Ls2-\mathrm{rms}}{}^2 + L_{s3} I_{Ls3-\mathrm{rms}}{}^2 \\ &\quad + L'_{s1} I_{L's1-\mathrm{rms}}{}^2 \\ &\quad + L'_{s2} I_{L's2-\mathrm{rms}}{}^2 + L'_{s3} I_{L's3-\mathrm{rms}}{}^2) \\ &= \frac{\left\{\frac{[2+(1+D)n_s]^2}{K^2(1-D)4} + \frac{(25+D)n_s{}^2}{4} + \frac{(1+n_s)^2}{1-D}\right\} D(1-D)T_s P_o}{(1+n_s)[4+n_s(3+D)]} \end{aligned} \tag{53}$$

$$\begin{aligned} E_C &= \sum_{i=1,2,3,4,5} E_{Ci} + E_{Co} = \frac{1}{2} \sum_{i=1,2,3,4,5} C_i V_{Ci}{}^2 + \frac{1}{2} C_o V_{Co}{}^2 \\ &= \left\{ \frac{6(1+n_s)}{1-D} + n_s(3+D) + DG \right\} \frac{50(1-D)T_s P_o}{4+n_s(3+D)} \end{aligned} \tag{54}$$

where, in (53), the values of inductances of coupled inductors that depend on the their transformer model parameters ($n_{s1} = n_{s2} = n_s$, L_{m1}, L_{m2}, K) are replaced. The root mean square (rms) currents of inductors are summarized in Table VI.

VII. COMPARING THE PROPOSED CONVERTER WITH THE PRESENTED CONVERTERS IN LITERATURE

To confirm the performance of the proposed dc–dc converter, in Table VII, it is compared with two other dual input–single output dc–dc converters presented in [3] and [16]. The differences between these converters from different aspects, including the output voltage (V_o), the capability of achieving ripple-free input currents ($\Delta i_1 = \Delta i_2 = 0$), the normalized voltage stresses across power switches (V_S/V_o) and diodes (V_D/V_o), the normalized current stresses of switches $[I_S/(I_1+I_2)]$ and diodes

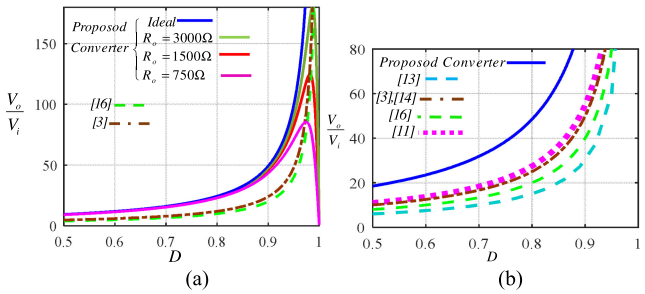

Fig. 4. (a) Voltage gain of the proposed converter and converters in [3] and [16]. (b) Voltage gain of an interleaved converters.

$[I_D/(I_1+I_2)]$, the number of switches (N_S), diodes (N_D), coupled inductors (N_{CI}), typical inductors (N_I), and capacitors (N_C), and the total normalized saved energy on inductors ($E_{L,N} = E_L/T_s P_o$) and capacitors ($E_{C,N} = E_C/T_s P_o$), are presented. The proposed converter is also compared with other single input–single output converters that have used coupled inductors in their structures, as presented in Table VIII. The voltage gain of the proposed converter, including ESRs of components ($r_{Lp1} = r_{Ts1} = r_{Tt1} = r_{Lp2} = r_{Ts2} = r_{Tt2} = r_L = 0.1\,\Omega$,$r_{S2} = r_{S1} = 0.04\,\Omega$, and $r_{D1} = r_{D2} = r_{D3} = r_{D4} = r_D = 0.1\,\Omega$) and the forward voltage drop of switches and diodes ($V_{\mathrm{FS1}} = V_{\mathrm{FS2}} = 0.8$ V and $V_{\mathrm{FD1}} = V_{\mathrm{FD2}} = V_{\mathrm{FD3}} = V_{\mathrm{FD4}} = 0.8\,V$), is plotted in Fig. 4(a). The output load is selected as $R_o = 3000\,\Omega$, $R_o = 1500\,\Omega$, and $R_o = 750\,\Omega$, which have been plotted based on (43). The ideal voltage gain of the two input converters presented in [3] and [16] is lower than even the voltage gain of the proposed converter considering ESRs of components. To plot this figure, other parameters selected are $n_{s1} = n_{s2} = 1.5$, $V_{i1} = 20$ V, and $V_{i2} = 30$ V. The proposed converter with an interleaved structure [as a one-input/one-output converter ($V_{i1} = V_{i2} = V_i$)] and the interleaved converters in [11], [13], and [14], which have the same feature of applying two three-winding coupled inductors for achieving a high voltage gain, are compared in Table VII. Based on this figure and Table VII, it can be seen that the voltage gain of the proposed converter with an interleaved structure is higher than that of the interleaved converters in [11], [13], and [14] by using a lower number of components. Compared to the converters presented in [3], [16], [11], [13], and [14], the proposed converter has the capability of canceling input current ripples Fig. 5(a)–(f) shows V_S/V_o, the total maximum normalized voltage stresses on diodes ($\sum V_D/V_o$), $I_S/(I_1+I_2)$, $I_D/(I_1+I_2)$, the total normalized energy on reactive components ($E_{\mathrm{total\_}N} = E_{C,N} + E_{L,N}$), and the voltage gain over the total normalized energy on reactive components ($G/E_{\mathrm{total\_}N}$) versus duty cycle, respectively. Fig. 5(a) is plotted by considering $V_{i2} = V_{i1}$ and $n_{s1} = n_{s2} = n_s$. Considering Fig. 5(a), V_S/V_o in the proposed converter is lower than the converters presented in [3], [11], [13], [14], and [16], and it can be further decreased by increasing the turns ratio of transformers n_s. According to Fig. 5(b), the $\sum V_D/V_o$ in the proposed converter is close to that of the converters in [3] and [16] and lower than that of the converters presented in [11], [13], and [14]. Fig. 5(c) shows that the

TABLE VII
COMPARING THE PROPOSED TWO BOOST STAGES CONVERTERS

Two boost stages converters	V_o	$\Delta i_1 = \Delta i_2 = 0$	$\frac{V_S}{V_o}$	$\frac{V_{D-\max}}{V_o}$	$\frac{I_S}{I_1+I_2}$	$\frac{I_D}{I_1+I_2}$	$\frac{E_{C,N}}{E_{L,N}}$	N	N_D	N_{CI}	N_I	N_C	N_{Total}
[3]	$\frac{3V_{i1}+2V_{i2}}{1-D}$	No	$\frac{1}{5}$	$D_{1,2,3,4}:\frac{2}{5}$ $D_5:\frac{1}{5}$	$S_1:\frac{2+D}{5}$ $S_2:\frac{2}{5}$	$\frac{1-D}{5}$	$E_{C,N}:10(10+5D)$ $E_{L,N}:D/4$	2	5	-	2	5	14
[16]	$\frac{2(V_{i1}+V_{i2})}{1-D}$	No	$\frac{1}{4}$	$D_{1,2,3}:\frac{1}{2}$ $D_4:\frac{1}{4}$	$S_1:\frac{1+D}{4}$ $S_2:\frac{1}{2}$	$\frac{1-D}{4}$	$E_{C,N}:50(1.5+D)$ $E_{L,N}:D/4$	2	4	-	2	4	12
Proposed converter	$\frac{2+n_{s1}(1+D)}{1-D}V_{i1}$ $+\frac{2(1+n_{s2})}{1-D}V_{i2}$	Yes	$\frac{1}{4+n_{s1}(3+D)}$	$D_{1,2,3}:\frac{2(1+n_{s1})}{4+n_{s1}(3+D)}$ $D_4:\frac{1+n_{s1}D}{4+n_{s1}(3+D)}$	$S_1:\frac{(1+n_{s1})(1+D)}{4+n_{s1}(3+D)}$ $S_2:\frac{2(1+n_{s1})}{4+n_{s1}(3+D)}$	$\frac{1-D}{4+n_{s1}(3+D)}$	$E_{C,N}=\frac{E_C}{T_sP_o}$ E_C: Eq. (88) $E_{L,N}=\frac{E_L}{T_sP_o}$ E_L: Eq. (87)	2	4	2	-	6	14

TABLE VIII
COMPARING AN INTERLEAVED COUPLED INDUCTOR-BASED CONVERTERS IN THE LITERATURE

Interleaved dc-dc converters	$\frac{V_o}{V_i}$	$\Delta i = 0$	$\frac{V_S}{V_o}$	$\frac{V_{D-\max}}{V_o}$	$\frac{I_S}{I_i}$	$\frac{I_D}{I_i}$	N_S	N_{CI}	N_D	N_C	N_{Total}
[11]	$(1+3n)/(1-D)$	No	$1/(1+3n)$	6 diodes: $2n/(1+3n)$ 2 diodes: $1/(1+3n)$	$(D+3n)/(2+6n)$	$\frac{1-D}{2+6n}$	2	2	8	5	17
[14]	$\frac{2(1+n)}{1-D}$	No	$\frac{1}{2(1+n)}$	4 diodes: $(2n+1)/(2+2n)$ 2 diodes: $1/(2+2n)$	$\frac{D+2n+1}{8(1+n)}$	$\frac{1-D}{4(1+n)}$	2	2	6	4	14
[13]	$N_2+\frac{2DN_3+2-D}{(1-D)}$	No	$\frac{1}{N_2(1-D)+2DN_3+2-D}$	2 diodes: $\frac{1}{N_2(1-D)+2DN_3+2-D}$ diodes: $\frac{1+N_2}{N_2(1-D)+2DN_3+2-D}$ diodes: $\frac{N_3}{N_2(1-D)+2DN_3+2-D}$	$\frac{[N_2(1-D)+2DN_3+1]}{2[N_2(1-D)+2DN_3+2-D]}$	-	2	6	2	5	15
Interleaved form of proposed converter	$\frac{4+n(3+D)}{1-D}$	Yes	$\frac{1}{4+3n+nD}$	3 diodes: $\frac{2(1+n_{s1})}{4+n_{s1}(3+D)}$ 1 diode: $\frac{1+n_{s1}D}{4+n_{s1}(3+D)}$	$S_1:\frac{(1+n_{s1})(1+D)}{4+n_{s1}(3+D)}$ $S_2:\frac{2(1+n_{s1})}{4+n_{s1}(3+D)}$	$\frac{1-D}{4+n_{s1}(3+L}$	2	2	4	3	11

$I_S/(I_1+I_2)$ in the proposed converter is close to that of the converters in [3] and [16] and higher than that of the converters presented in [11], [13], and [14]. On the other hand, Fig. 5(d) shows that the $I_D/(I_1+I_2)$ in the proposed converter is close to that of the converters presented in [11] and [13] and lower than that of the converters presented in [3] and [16]. Fig. 5(f) shows that the $G/E_{\text{total\_N}}$ in the proposed converter is higher than that of the converters presented in [3] and [16]. As a result, the proposed converter has the best performance from this point of view.

VIII. EXPERIMENTAL RESULTS

In this part, the experimental results are obtained under two different conditions of duty cycle and output power. The values of different elements are summarized in Table IX.

TABLE IX
USED PARAMETERS

$L_{k1}=50\ \mu H$, $L_{m1}=220\ \mu H$	$V_{i1}=20\ V$
$L_{k2}=60\ \mu H$, $L_{m2}=250\ \mu H$	$V_{i2}=30\ V$
$C_1=C_2=C_3=C_4=C_5=C_o=100\ \mu F$	$n_{s2}=n_{s1}=1.5$
Switches: IRFP260N	Diodes: MUR1540G
$R_o=1500\ \Omega$	$f_s=30\ kHZ$
For $D=0.6$	For $D=0.65$ $P_o=296\ W$

A. Experimental Results for $D = 0.6$ and $P_o = 225$ W

Fig. 6 shows the experimental results of voltage and current stresses of the switches for $D = 0.6$. From the second row of Table II and the parameters given in Table IX, it can be seen that $V_{C1} = 300.28$ V, $V_{C3} = 300.19$ V, $V_{C2} = 134$ V, $V_{C4} = 20$ V, $V_{C5} = 30$ V, and $V_o = 580.37$ V, which are almost the same as the experimental results obtained in Fig. 6(a) and (b). Based on Table I, the voltage stresses for the switches are calculated as $v_{S1} = 50$ V and $v_{S2} = 75$ V, respectively, during $(1-D)T_s = 13.33\ \mu$s. According to Fig. 2(d), the maximum voltage stresses on the diodes D_1, D_2, and D_3 are calculated as $v_{D1}|_{\max} = v_{D2}|_{\max} = v_{D3}|_{\max} = 300.28$ V during $(1-D)T_s$. Moreover, the minimum voltage stresses on the

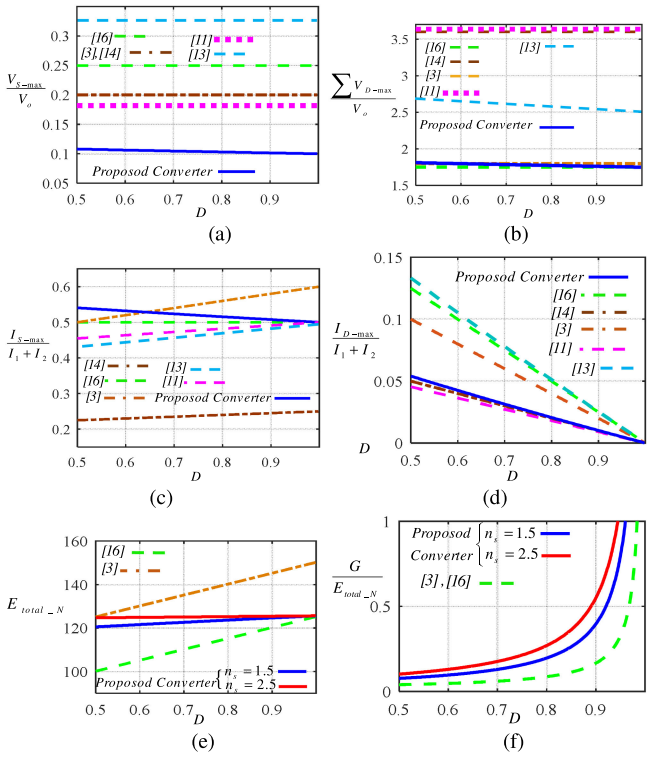

Fig. 5. (a) V_S/V_o. (b) $\sum V_D/V_o$. (c) $I_S/(I_1+I_2)$. (d) $I_D/(I_1+I_2)$. (e) $E_{\text{total\_}N}$; (f) $G/E_{\text{total\_}N}$.

diodes D_1, D_2, and D_3 are calculated as $v_{D1}|_{\min} = v_{D3}|_{\min} = -119$ V and $v_{D2}|_{\min} = 181$ V during $(2D-1)T_s = 6.66\,\mu$s. As shown in Fig. 6(b), the experimental results are very close to the calculated values from analytical results by considering ESRs of components.

Considering (34) and (35), the maximum and minimum values of the inductor current i_{Lm1} is calculated as $I_{m11} = 5.75$ A and $I_{m12} = 3.93$ A, respectively, which are almost the same as the results obtained in Fig. 6(c). Moreover, based on (36) and (37), the maximum and minimum values of the inductor current i_{Lm2} are calculated as $I_{m21} = 6.04$ A and $I_{m22} = 3.64$ A, respectively, which are verified by Fig. 6(c). The average values of the input currents i_{i1} and i_{i2} are calculated as $I_1 = 4.256$ A and $I_2 = 4.84$ A from (30) and (31), respectively, which are almost the same results as obtained in Fig. 6(c). According to (31) and (32), the average currents of switches are obtained as $I_{S1} = 3.869$ A and $I_{S2} = I_2 = 4.84$ A. Considering Fig. 2(d), the maximum and minimum values of the currents i_{D1}, i_{D2}, i_{D3}, and i_{D4} are calculated as $i_{D2}|_{\max} = i_{D4}|_{\max} = 1.208$ A, $i_{D2}|_{\min} = i_{D4} = 0.724$ A, $i_{D1}|_{\max} = i_{D3}|_{\max} = 1.15$ A and $i_{D1}|_{\min} = i_{D3}|_{\min} = 0.786$ A, respectively, which are very close to the results illustrated in Fig. 6(d).

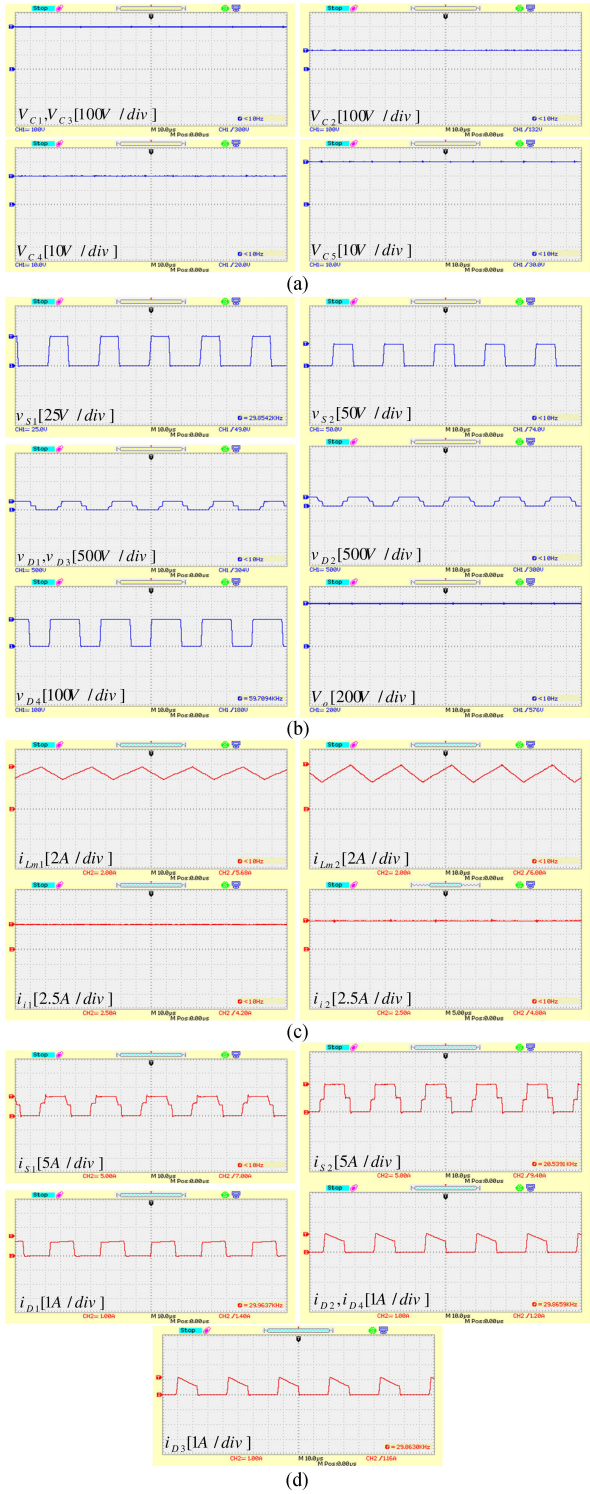

Fig. 6. Experimental results for $D = 0.6$. (a) Voltages of capacitors. (b) Voltages of switches, diodes, and the output voltage. (c) Input currents and inductor's currents. (d) Currents of switches and diodes.

B. *Experimental Results for $D = 0.65$ and $P_o = 296$ W*

Fig. 7 shows the experimental results for $D = 0.65$. The output voltage is calculated as $V_o = 666.56$ V for the parameters given in Table IX, which is equal to the experimental results shown in Fig. 7(a). Based on Table I, the voltage stresses for the switches are calculated as $v_{S1} = 57.14$ V and $v_{S2} = 85.7$ V. The voltage stress on the diode D_4 is calculated as $v_{D4} = 214.28$ V. According to Table I and Fig. 2(d), the maximum and minimum voltage stresses on the diodes D_1, D_2, and D_3 are calculated as $v_{D1}|_{\max} = v_{D2}|_{\max} = v_{D3}|_{\max} = 357.14$ V and $v_{D1}|_{\min} = v_{D3}|_{\min} = 142.85$ V and $v_{D2}|_{\min} = 214.2$ V.

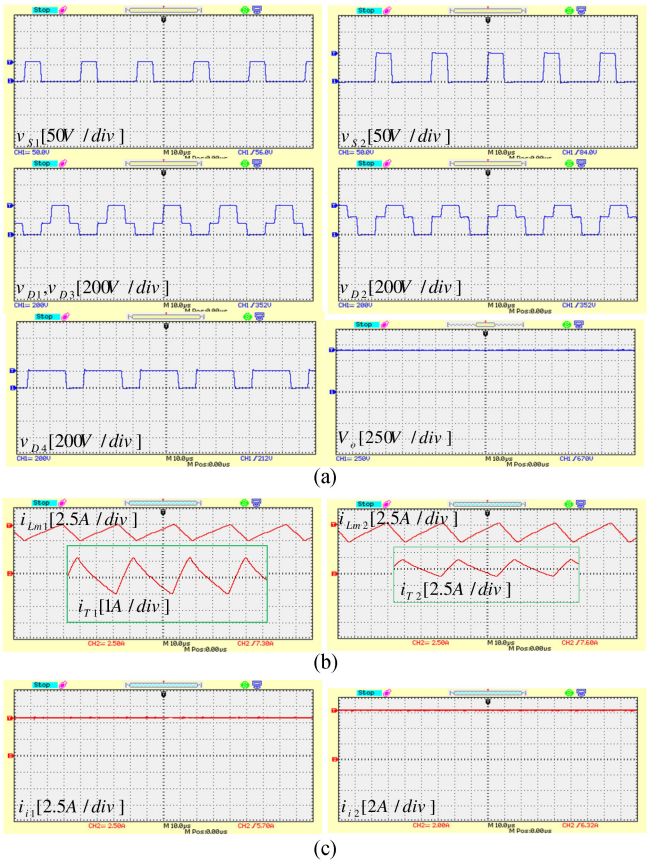

Fig. 7. Experimental results for $D = 0.65$. (a) Voltages of switches and diodes and the output voltage. (b) Input currents and inductor's currents. (c) Currents of switches and diodes.

As shown in Fig. 7(a), the experimental results are very close to the calculated theoretical results. Then, the maximum and minimum values of the inductor currents i_{Lm1} and i_{Lm2} are calculated as $I_{m11} = 7.33$ A and $I_{m12} = 5.36$ A, $I_{m21} = 7.65$ A, and $I_{m22} = 5.05$ A, respectively, which are almost the same as the results obtained in Fig. 7(b). Fig. 7(c) shows that when the current i_{Lm2} is increased, i_{T2} is decreased during DT_s. According to Fig. 1, the sum of the currents i_{Lm2} and i_{T2} is equal to the dc input current i_2, which is shown on the right-hand side of Fig. 7(c). The average value of the input currents i_{i1} and i_{i2} is calculated as $I_1 = 5.68$ A and $I_2 = 6.35$ A from (30) and (31), respectively, which are almost the same as the results shown in Fig. 7(c). Based on the theoretical efficiency calculation adopted in [27] and [28], the parameters of switches from their datasheet are as follows: $V_{\rm FS1} = V_{\rm FS2} = 0.8$ V, $r_{S2} = r_{S1} = 0.04\,\Omega$, $t_{r\_S1} = t_{r\_S2} = 60$ ns, $t_{f\_S1} = t_{f\_S2} = 48$ ns. The parameters of diodes are as follows: $V_{\rm FD1} = V_{\rm FD2} = V_{\rm FD3} = V_{\rm FD4} = 0.8$ V, $r_D = 0.1\ \Omega$, $t_{b-D1} = t_{b-D2} = t_{b-D3} = t_{b-D4} = 60$ ns, and $I_{rr-D1,D2,D3,Da1,Db1,Do1,Do2} = 10\,\mu$A. The efficiency curve of the proposed converter and converters presented in [12] and [13], is plotted in Fig. 8(a). The implemented prototype of the proposed converter is shown in Fig. 8(b).

IX. Conclusion

In this paper, a non-isolated high-voltage-gain two-input single-output boost converter with ripple-free input currents was proposed. The proposed converter uses a D-C-L circuit to obtain a high voltage gain. In the proposed converter, the voltage stresses on switches and diodes are lower than the high output load. In this paper, the values of current and voltage stresses of all switches and diodes, the required condition for canceling input current ripples, and the voltage gain of the proposed converter were calculated. Finally, the accuracy performance of the proposed converter has been verified through experimental results.

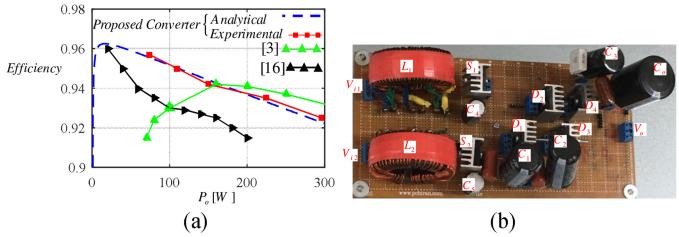

Fig. 8. (a) Efficiency curves versus output power. (b) Implemented prototype of the proposed converter.

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