IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 34, NO. 8, AUGUST 2019

A High-Efficiency Active-Boost-Rectifier-Based Converter With a Novel Double-Pulse Duty Cycle Modulation for PV to DC Microgrid Applications

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***Abstract*—In this paper, a highly efficient isolated resonant converter with a novel modulation method is proposed for delivering power from photovoltaic (PV) modules to the dc microgrid. The proposed modulation method allows the converter to boost low input voltages and regulate a wide input voltage range. The converter design is based on a series resonant converter (SRC) that operates at the resonant frequency to achieve highest efficiency under nominal input voltage condition. Under shadowed or low irradiance conditions of PV panels, the converter will operate with the proposed "double-pulse duty cycle" modulation method to step up the voltage for the dc microgrid connection. With the proposed modulation method, the output switches serve for both synchronous rectification and voltage boost function. This method enables a higher voltage boost ratio than the SRC without adding additional switches while operating at the resonant frequency. A 300-W hardware prototype with gallium-nitride devices is built to verify the performance of the proposed converter and modulation method. The converter achieved a peak efficiency of 98.9% and a California Energy Commission weighted efficiency of 98.7% under nominal input voltage condition.**

***Index Terms*—Active boost rectifier, dc microgrid, dc optimizer, wide-range regulation.**

I. INTRODUCTION

DC microgrid systems have great benefits with regard to energy conservation, which has attracted more and more research in the past decades [1]–[5]. Solar energy is considered as one of the most important energy sources in microgrid systems. In order to effectively maximize energy production from photovoltaic (PV) panels, a paralleled-type dc power optimizer that directly converts low-voltage dc to high-voltage dc is used, as shown in Fig. 1. Presently, the most commonly used PV panels are 60-cell modules [6]–[8]. Therefore, a 300-W dc power optimizer will suffice in most cases. Instead of connecting a string of PV panels or series connecting low-voltage type power optimizers [9], a paralleled-type dc optimizer provides more flexibility. However, a paralleled-type dc optimizer should be able to meet the following requirements.

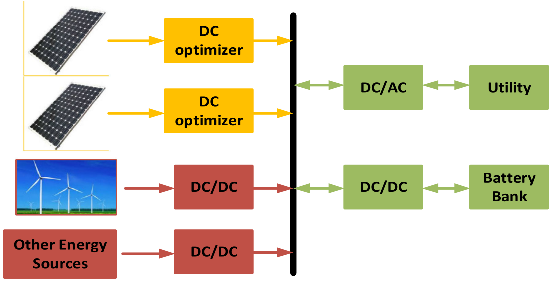

Fig. 1. DC microgrid system.

1) Ability to operate at a wide-range of input voltage.
2) High voltage boost ratio.
3) High efficiency over wide-range operating conditions.

Although isolation is not required because PV panel terminals may not necessarily be grounded [10], the proposed converter also provides galvanic isolation so that the PV panels can be isolated from the dc microgrid during fault conditions. This type of isolated design normally results in a poorer efficiency; however, if the converter operates under soft-switching conditions, it is able to achieve ultrahigh efficiency that is comparable to or is even better than most non-isolated designs [11], [12].

Furthermore, it is well known that the output voltage of PV panels is at nominal voltage under the majority of irradiance conditions and drops under low irradiance and shadowed conditions. Therefore, the converter design should be optimized at the nominal input voltage condition and can also have higher voltage gain at low input voltage conditions. Many circuit topologies have been proposed to meet these requirements [13]–[26]. The most conventional category is flyback and the flyback-derived converter, such as in [13]–[15], where variable gain is achieved by duty adjustment. Although these converters have the advantages of simple structure, ease of control, and low cost, they suffer from low efficiency and low magnetics utilization. Another category is the bridge-based converters, including non-resonant converters [16]–[18] and resonant converters [19]–[26], which have higher magnetics utilization compared with the first category. However, these non-resonant converters have problems with large turn-OFF current on the primary side switches as well as ringing and high voltage spikes caused by the leakage inductance of the transformer. Thus, their efficiencies are also limited. The *LLC* resonant converter is an attractive solution for wide-range regulation when using phase-shift fixed frequency

Manuscript received July 9, 2018; revised September 14, 2018; accepted October 18, 2018. Date of publication October 25, 2018; date of current version May 22, 2019. Recommended for publication by Associate Editor V. Agarwal. *(Corresponding author: Xiaonan Zhao.)*

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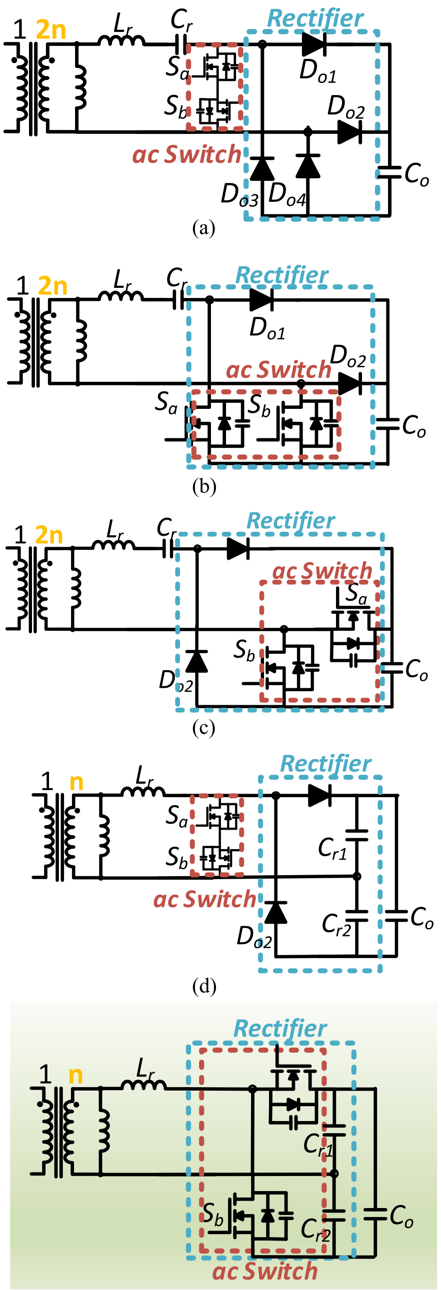
control or variable frequency control to the primary side full bridge. However, phase-shift fixed frequency control can only step down voltage, which is suitable for the conditions only when input voltage is higher than nominal voltage [19], [20]. Only variable frequency control can allow the *LLC* converter achieve higher voltage gains at low input conditions [21]–[23]. Furthermore, the *LLC* converter can achieve soft-switching over a wide operating range. However, to meet the voltage gain range requirement, the ratio of magnetizing inductance over leakage inductance should be selected properly, which will increase circuiting current and sacrifice efficiency when switching at resonant frequency. Moreover, it is complicated to model the *LLC* resonant converter with variable frequency modulation.

Among all of these topologies, resonant converters proposed in [24]–[26] employ a boost rectifier in the secondary side to achieve high voltage gain under low input conditions with fixed-frequency modulation. These converters have shown great performance and high efficiency over a wide input range because of the ability for direct power transfer over the majority of the switching cycle, low circulating energy with fixed-frequency modulation, and soft-switching during the entire operating range. Fig. 2(a)–(d) summarizes the candidate topologies of boost rectifier presented in [24]–[26]. By controlling the ac switch appropriately, a boost circuit is built and the converter can achieve high voltage boost ratio. However, the rectifier configuration of the converter in Fig. 2(a)–(c) is a full–bridge type, containing more devices and requiring twice the turns ratio of transformer when compared to the voltage-doubler configuration. Therefore, it results in a higher leakage inductance and more complicated magnetics design. Although the output configuration is a voltage-doubler as shown in Fig. 2(d), the ac switch is added to serve as the switch of boost circuit. This ac switch stays OFF during entire switching cycle when the input voltage is nominal, which is not fully utilized and increases the cost. In this paper, the output diodes of the voltage-doubler circuit are replaced with active switches for synchronous rectification while serving for voltage boost function, eliminating the ac switch as shown in Fig. 2(e). In other to achieve wide input voltage range regulation and obtain high voltage boost ratio, a new modulation method, referred to as "double-pulse duty cycle," is proposed for low input voltage conditions. Thus, the turns ratio of the transformer is halved compared to the full-bridge-based rectifier, and the number of power devices can be reduced. In this paper, Table I compares the transformer turns ratio and component number among the boost rectifiers in Fig. 2(a)–(d) and the proposed boost rectifier topology in Fig. 2(e). The proposed boost rectifier requires lowest number of devices while maintaining a low transformer turns ratio.



(a)

(b)

(c)

(d)

(e)

Fig. 2. Candidate topologies of boost rectifiers. (a) Full-bridge-based boost rectifier: Type I. (b) Full-bridge-based boost rectifier: Type II. (c) Full-bridge-based boost rectifier: Type III. (d) Half-bridge-based boost rectifier. (e) Proposed half-bridge-based active-boost-rectifier with reduced number of power devices.

Fig. 3 shows the topology of the proposed converter for delivering the energy from the PV modules to the dc microgrid system. Although the circuit looks identical to the *LLC* resonant converter, the design and modulation is entirely different. The major contribution of this paper is the proposal of an active-boost-rectifier with a novel double-pulse duty cycle modulation method. The output switches serve as dual purposes with the proposed modulation technique: voltage boost function and synchronous rectification. Under nominal input voltage condition, the boost function is OFF, and the entire purpose of the duty cycle for the output switches is for synchronous rectification. When the input voltage is lowered due to shadowed or low-irradiance conditions of PV panels, a double-pulse duty cycle modulation method is applied to the output switches for output voltage boost. The first pulse serves as the voltage boost function, and the second pulse serves as synchronous rectification. The proposed active-boost-rectifier with employed modulation method allows the converter to keep the benefits of highly efficient series resonant converter (SRC) converter and, at the same

TABLE I
DEVICE NUMBER COMPARISON IN FIG. 2

Boost rectifier topology	Turns ratio of transformer	Switches	Diodes
Fig.2 (a)	1:2n	2	4
Fig.2 (b)	1:2n	2	2
Fig.2 (c)	1:2n	2	2
Fig.2 (d)	1:n	2	2
Fig.2 (e) Proposed	1:n	2	0

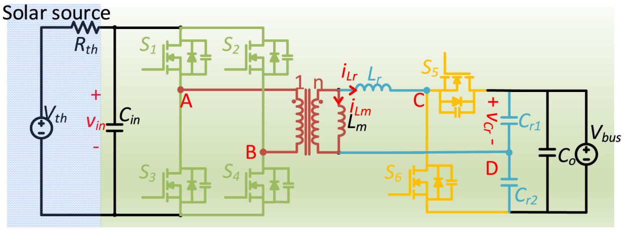


Fig. 3. Topology of the proposed converter.

time, achieve higher voltage boost ratio than the SRC without the need of extra switches while operating at a fixed frequency. The detailed analysis of the proposed modulation scheme as well as the derivation of voltage conversion ratio is depicted in Section II. Section III gives the design procedures and digital implementation of the proposed "double-pulse duty cycle" modulation method. In Section IV, experimental results based on a 300-W prototype are presented. The prototype achieves a peak efficiency of 98.9% and California Energy Commission (CEC) weighted efficiency of 98.7% at the nominal input voltage.

II. CONVERTER OPERATION WITH THE PROPOSED MODULATION SCHEME

A. Topology

The topology looks identical to a conventional full bridge *LLC* resonant converter with synchronous rectification [27]. However, the purpose and design of the proposed converter is entirely different with the *LLC* resonant converter. The input side is a full-bridge comprised of switches $S_{1\text{–}4}$ and output side is an active boost rectifier comprised of switches $S_{5,6}$. Each switch is modeled with a channel, body diode, and the parasitic output capacitance. L_r, C_{r1}, and C_{r2} is the resonant tank network, where L_r is the summation of transformer leakage inductance and external inductor and C_{r1} is equal to C_{r2}. For the high frequency transformer, n is the turns ratio and L_m is the magnetizing inductance.

Unlike the conventional variable frequency operation of the *LLC* resonant converter, the proposed converter operates at a fixed switching frequency that is equal to the series resonant frequency. Hence, the design of L_m only needs to consider zero voltage switching (ZVS) of the input side switches but not necessarily in order to obtain wide voltage gains. Thus, the ratio of L_m/L_r is much larger than conventional variable frequency LLC converters. Therefore, the proposed converter has the advantages of low circulating current, low current switching of the input side switches, and zero-current-switching (ZCS) of the output side switches regardless of input voltage or power compared to the traditional variable frequency *LLC* resonant converter.

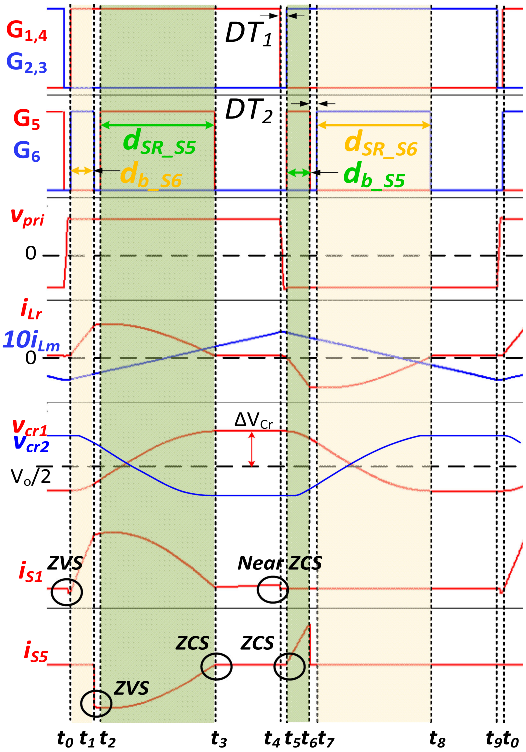


Fig. 4. Steady-state waveforms with double-pulse duty cycle modulation.

The energy is delivered from the input to output through a pure sinusoidal current during entire switching cycle under nominal input condition. The switching frequency is selected to be the same as the resonant frequency, given as

$$f_s = f_r = \frac{1}{2\pi\sqrt{L_r(C_{r1}+C_{r2})}}. \tag{1}$$

Under nominal input condition, the voltage boost ratio is entirely determined by the turns ratio of the transformer, given as

$$n = \frac{V_o}{2V_{\text{in\_}nom}}. \tag{2}$$

B. Proposed Modulation Scheme

A double-pulse duty cycle modulation method is proposed to achieve a higher voltage boost ratio than the nominal boost ratio shown in (2) for low input voltage conditions. With the proposed modulation method, S_5 and S_6 can serve not only for the synchronous rectification but also as voltage boost function.

The main steady-state waveforms with double-pulse duty cycle modulation are shown in Fig. 4. The duty of switches S_5 and S_6 contain two pulses, which are defined as d_b for voltage boost and d_{SR} for synchronous rectification, while the full bridge of the input side $S_{1\text{–}4}$ operates at 0.5 duty with 180° phase shift.

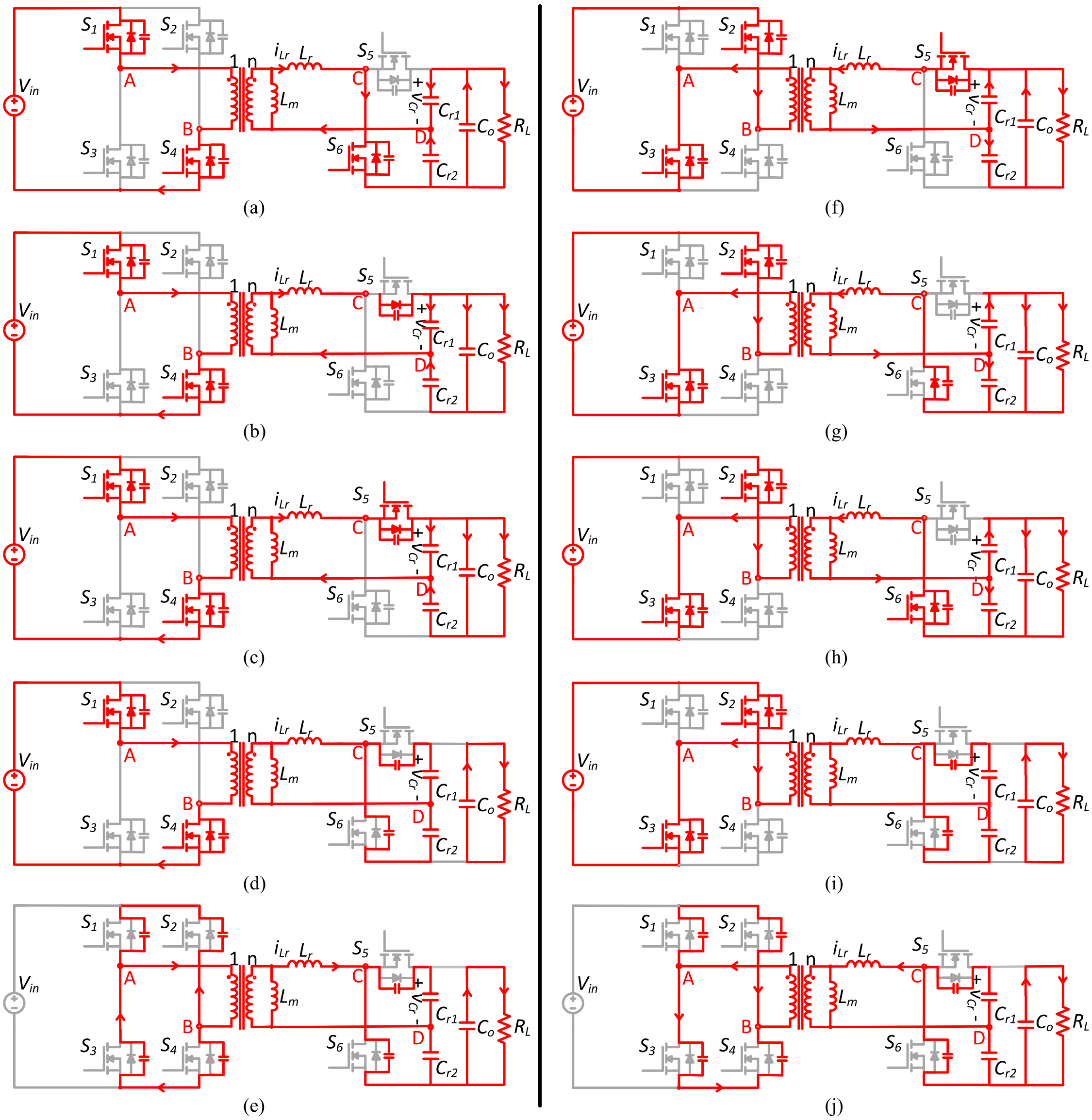


Fig. 5. Modes of operating periods with double-pulse duty cycle modulation. (a) [t0–t1]. (b) [t1–t2]. (c) [t2–t3]. (d) [t3–t4]. (e) [t4–t5]. (f) [t5–t6]. (g) [t6–t7]. (h) [t7–t8]. (i) [t8–t9]. (j) [t9–t0].

Under nominal input condition $d_b = 0$, only d_{SR} is applied to S_5 and S_6, and the converter works as an SRC. When the input voltage drops below nominal voltage $d_b > 0$, S_5 and S_6 serve as an active boost rectifier to achieve boost gain. There are ten operating periods in the whole switching cycle for $d_b > 0$ conditions. The operation of each period is shown in Fig. 5. Since the first half of the switch cycle and the second half switching cycle are symmetrical, only the first five operating periods will be illustrated in the following paragraphs.

Interval [t_0–t_1]: t_0 is the beginning of the switching period. At this time, the initial resonant current i_{Lr} is zero and the resonant voltage v_{Cr} is at minimum value, given as

$$i_{Lr}\left(t_0\right) = 0 \tag{3}$$

$$v_{Cr}\left(t_0\right) = \frac{V_o}{2} - \Delta v_{Cr} \tag{4}$$

where Δv_{Cr} is half of the voltage ripple across the resonant capacitor $C_{r1,2}$

$$\Delta v_{Cr} = \frac{P_o T_s}{8nV_{\mathrm{in}}C_{r1}}. \tag{5}$$

During [t_0–t_1], S_1 and S_4 are ON, as shown in Fig. 5(a), therefore, the positive input voltage is applied to the primary winding of the transformer. For the output side, S_6 turns ON at a ZCS condition. During this period, a boost duty for S_6, d_{b_s6}, is applied and a boost circuit is built. The input voltage source, output capacitor C_o, and resonant capacitors C_{r1} and C_{r2} provide energy to L_r. The mechanism during the period [t_0–t_1] is similar to a conventional boost converter when high side switch is ON and the inductor is charged. In the trajectory path, as shown in Fig. 6, this period represents point a to point b and the equivalent resonant circuit is shown in Fig. 7(a),

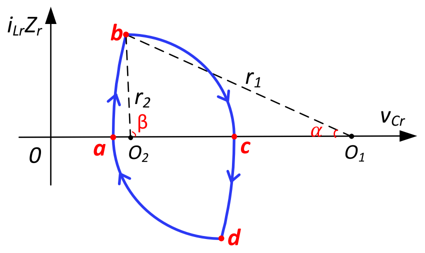
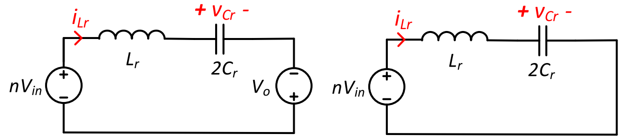


Fig. 6. Trajectory path of the converter operation with the proposed modulation scheme.



(a) (b)

Fig. 7. Equivalent circuits of $[t_0–t_1]$ and $[t_1–t_3]$ periods. (a) $[t_0–t_1]$. (b) $[t_1–t_3]$.

where input voltage and output capacitor voltage serve as voltage source. L_r and $C_{r1,r2}$ make up the series resonant network. In the trajectory path, the center of this period is located at O_1, and the radius is marked as r_1, given as

$$O_1 = nV_{\rm in} + V_o \tag{6}$$

$$r_1 = nV_{\rm in} + \frac{V_o}{2} + \Delta v_{Cr}. \tag{7}$$

The state variables of i_{Lr} and v_{Cr} are expressed in the time domain in (8) and (9), respectively, as

$$i_{Lr}\,(t) \;= \frac{r_1}{Z_r}\sin\left(\pi - \omega_r\,(t - t_0)\right) \tag{8}$$

$$v_{Cr}\,(t) \;= (nV_{\rm in} + V_o) + r_1\cos\left(\pi - \omega_r\,(t - t_0)\right) \tag{9}$$

where Z_r is the impedance of the series resonant network, $Z_r = \sqrt{\frac{L_r}{2C_{r1}}}$.

Interval [t_1–t_2]: This period represents the first dead time between S_5 and S_6, as shown in Fig. 5(b). At t_1, S_6 turns OFF and S_5 remains OFF. Point b in Fig. 6 shows the status of the resonant variables at t_1

$$i_{Lr}\,(t_1) \;= \frac{r_1}{Z_r}\sin\left(\pi - \omega_r\,(t_1 - t_0)\right) \tag{10}$$

$$v_{Cr}\,(t_1) \;= (nV_{\rm in} + V_o) + r_1\cos\left(\pi - \omega_r\,(t_1 - t_0)\right) \tag{11}$$

$$\alpha = \sin^{-1}\left(\frac{Z_r i_{Lr}\,(t_1)}{r_1}\right). \tag{12}$$

Since positive voltage is applied across the transformer, the energy is delivered to the load side through the body diode of S_5 after the output capacitance of S_5 is fully discharged. Therefore, when S_5 turns ON at t_2, ZVS turn ON is achieved.

Interval [t_2–t_3]: The mode of operation is shown in Fig. 5(c). S_5 turns ON when the synchronous rectification duty d_{SR_S5} is applied, and power continues transferring to the output side through S_5. The equivalent circuit of this interval is shown in Fig. 7(b). In the trajectory path figure, the center of this period is located at O_2, and the radius is marked as r_2, given as

$$O_2 = nV_{\rm in} \tag{13}$$

$$r_2 = \frac{V_o}{2} - nV_{\rm in} + \Delta v_{Cr}. \tag{14}$$

The state variables of i_{Lr} and v_{Cr}, in this interval, are expressed in the time domain in (15) and (16), respectively, where β is the initial angle as marked in Fig. 6. β can be derived from point b in the trajectory path as

$$i_{Lr}\,(t) \;= \frac{r_2}{Z_r}\sin\left(\beta - \omega_r\,(t - t_1)\right) \tag{15}$$

$$v_{Cr}\,(t) \;= (nV_{\rm in}) + r_2\cos\left(\beta - \omega_r\,(t - t_1)\right) \tag{16}$$

$$\beta = \pi - \sin^{-1}\left(\frac{Z_r i_{Lr}\,(t_1)}{r_2}\right). \tag{17}$$

The interval ends when the current sensor senses that the resonant current reaches to zero. At this point, S_5 turns OFF with ZCS.

Interval [t_3–t_4]: During this period, there is no more energy delivery to the load, as shown in Fig. 5(d). The converter runs into the idle state (discontinuous current mode (DCM) period) with the magnetizing current freewheeling and small ringing occurring between L_r and output capacitances of S_5 and S_6. At t_4, S_1 and S_4 turn OFF under relatively low magnetizing current as

$$i_{Lm}\,(t_4) = \frac{nV_{\rm in}T_s}{4L_m}. \tag{18}$$

Interval [t_4–t_5]: As shown in Fig. 5(e), the converter enters a dead-time period for the switches on both the primary and secondary sides. At this time, there is no gate signal applied to the switches. The magnetizing current appears as a current source to discharge the parasitic output capacitances of $S_{2,3}$ and charge those of $S_{1,4}$. Once the output capacitances are fully charged and discharged, the body diodes of S_2 and S_3 will be forced to conduct before applying the gate signals. Therefore, the main purpose of designing the magnetizing inductance is to guarantee ZVS turn ON for primary side switches.

Interval [t_5–t_0]: During t_5 through t_0, the circuit analysis is completely symmetrical to the circuit operating in the period of t_0 to t_5.

C. Voltage Conversion Ratio With the Proposed Modulation Scheme

As mentioned in the previous section, the gate signal of S_5 and S_6 is composed of $d_{\rm SR}$ and d_b, as shown in Fig. 4. $d_{\rm SR}$ is responsible for the synchronous rectification, which replaces the diode to minimize conduction loss. $d_{\rm SR}$ has no effect on the voltage gain. With double-pulse duty cycle modulation, the output voltage is regulated only by controlling d_b. In this section, the relationship between d_b, voltage conversion ratio, and converter parameters is derived for further components design.

The trajectory path is necessary for derivation of the voltage conversion ratio. Point b in Fig. 6 represents the intersection of arc ab and arc bc. Therefore, the geometric relationship of the state variables at point b, respectively, can be expressed as

$$\left(v_{Cr}\left(t_1\right)-nV_{\mathrm{in}}-V_o\right)^2+\left(Z_r i_{Lr}\left(t_1\right)\right)^2=r_1^2 \tag{19}$$

$$\left(v_{Cr}\left(t_1\right)-nV_{\mathrm{in}}\right)^2+\left(Z_r i_{Lr}\left(t_1\right)\right)^2=r_2^2. \tag{20}$$

Equation (21) is derived by (19) and (20), where $t_1 = d_b T_s$, as

$$v_{Cr}\left(t_1\right)=nV_{\mathrm{in}}+\frac{V_o}{2}-\frac{nV_{\mathrm{in}}\left(V_o+\Delta V_{Cr}\right)}{V_o}. \tag{21}$$

Combined with (5), (7), (11), and (21), the relationship between duty cycle and voltage conversion ratio can be derived as

$$d_b=\frac{\cos^{-1}\left(\frac{\frac{V_o}{2}+nV_{\mathrm{in}}+\frac{P_o T_s}{4C_{r1}}}{\frac{V_o}{2}+nV_{\mathrm{in}}+\frac{P_o T_s}{8nV_{\mathrm{in}}C_{r1}}}\right)}{\omega_r T_s}. \tag{22}$$

According to (22), the relationship between the duty cycle and the voltage conversion ratio is not only determined by the output power, but also determined by the parameters of resonant tank. Fig. 8(a) and (b) shows the duty cycle versus the input voltage under different power levels and resonant tanks, where V_o sets as 380 V and V_{in_nom} designs at 35 V for PV to dc microgrid application. In Fig. 8(a), the output impedance is fixed at 34 for all cases, and the output power is fixed as 300 W for all cases in Fig. 8(b). Additionally, universal voltage gain curves versus d_b with various qualify factors (Q) are shown in Fig. 8(c), which are not only limited to this application.

III. CONVERTER DESIGN AND IMPLEMENTATION OF THE PROPOSED MODULATION SCHEME

A. Transformer Design

The transformer is optimized at the most efficient point when the converter operates as a pure SRC and d_b is zero under nominal input voltage. The turns ratio is selected in (2).

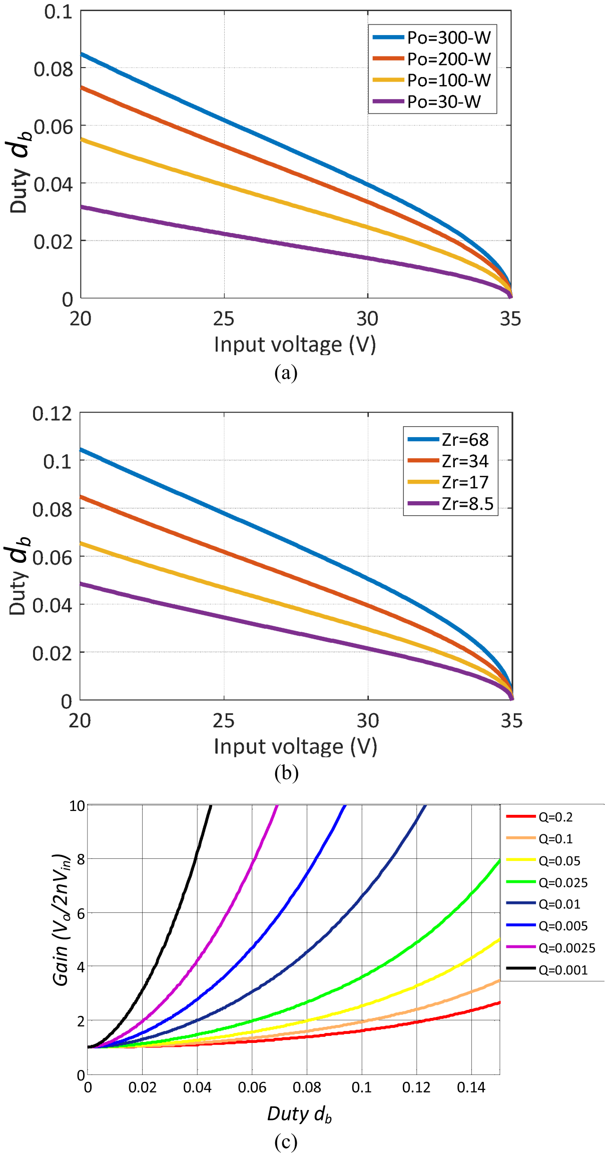
As mentioned in the Section II, the magnetizing inductance, L_m is designed to provide energy to fully charge and discharge output capacitance of input side devices during dead-time period. L_m should meet the requirement of (23) if i_{Lm} is treated as a constant current source during dead-time period [28]. t_d is the length of dead time and C_{oss} is the output capacitance of each input side switch

$$L_m \leq \frac{n^2 t_d}{8 f_s C_{oss}}. \tag{23}$$

Magnetic material 3C95 is selected for 100-kHz range operation and core shape RM14 with low profile is selected because of its relatively large window area. The number of turns is determined by the tradeoff between core loss and winding loss. As per Fig. 9, 4 turns for primary winding and 25 turns for secondary winding were selected.

B. Resonant Tank Design

The impedance design is limited by the length of period $[t_0$–$t_3]$ in Fig. 4. The period $[t_0$–$t_3]$ should be less than $T_s/2$ to guarantee the DCM operation of the converter. Equation (24)



(a)

(b)

(c)

Fig. 8. Voltage conversion ratio curves: The relationship between input voltage and d_b for 380 V fixed output voltage (a) with different output power levels ($Z_r = 34$) and (b) with different resonant tank impedances ($P_o = 300$ W). (c) Relationship between voltage conversion gain and d_b.

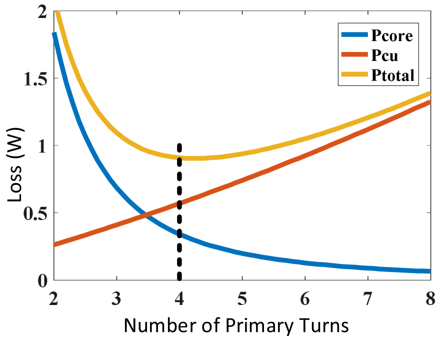


Fig. 9. Power loss curve of transformer for turns number selection.

constrains the inductance selection of L_r. Additionally, the voltage ripple across each resonant capacitor should be less than half of the output voltage (25). The relationship between L_r and C_r should follow (1)

$$T_s/2 \geq d_b T_s + \frac{(\pi - \sin^{-1}(r_1 \sin(d_b \omega_r T_s)))}{\omega_r} \tag{24}$$

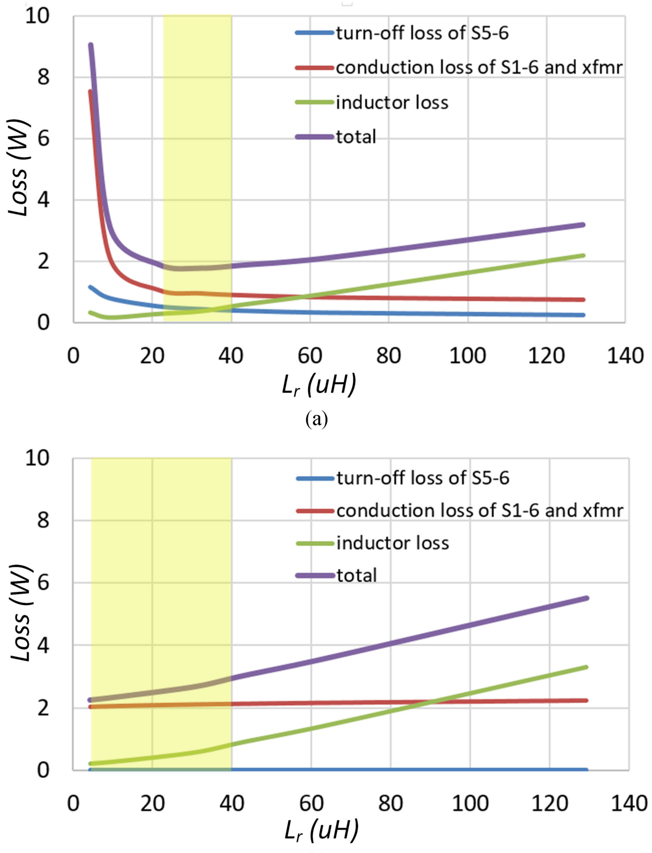
$$\Delta v_{Cr} = \frac{P_o T_s}{8 n V_{\text{in}} C_{r1}} \leq \frac{V_o}{2}. \tag{25}$$

Besides the basic constraints of (24) and (25), the resonant tank design is based on optimizing the system efficiency at nominal and near-nominal conditions. As shown in Fig. 8(b), a larger resonant impedance results in wider boost duty, lower turn-OFF current of $S_{5,6}$, and lower RMS current. However, this can result in a large external inductor and, thus, greater losses as well. Practically, the design of the resonant tank considers the tradeoff between the turn-OFF loss of $S_{5,6}$, converter conduction loss, and losses of the external inductor.

The turn-OFF current of $S_{5,6}$ and the RMS current of i_{Lr} are expressed in (26) and (27) shown at the bottom of this page, respectively, as

$$i_{s5,6\_\text{off}} = i_{Lr}(t_1) = \frac{r_1}{Z_r} \sin(\omega_r d_b T_s) \tag{26}$$

Fig. 10 shows the turn-OFF loss of $S_{5,6}$, conduction losses of the MOSFETs and transformer, and external inductor loss under 32-V/150-W and 35-V/300-W conditions. The operating conditions are selected based on the PV output characteristic curves, as shown in Fig. 18(b). According to Fig. 10, 20–40 μH is a proper range for resonant inductance.



(a)

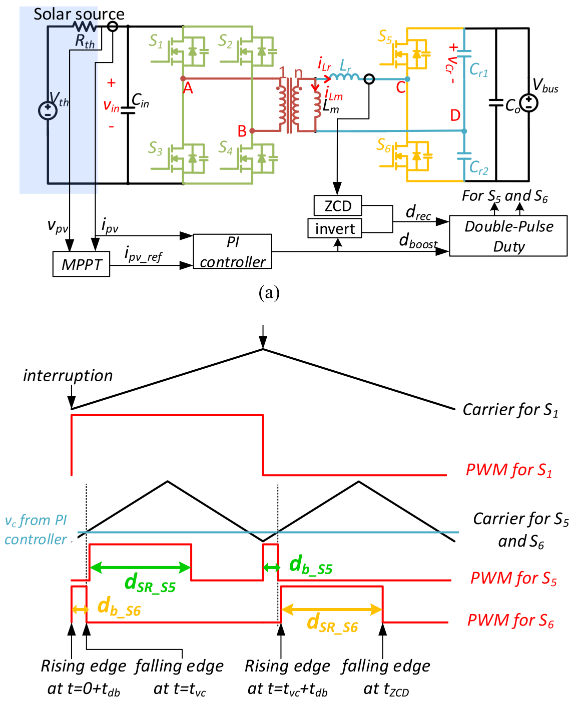
(b)

Fig. 10. Relationship between L_r and converter loss estimation. (a) Under 32-V input, 150-W conditions. (b) Under 35-V input, 300-W conditions.

C. Implementation of the Proposed Modulation in Digital Signal Processor (DSP)

Fig. 11(a) shows the system control diagram of the proposed double-pulse duty cycle modulation. The control is focused on the pulsewidth modulations (PWMs) of S_5 and S_6. The input voltage and input current of the converter are sensed for maximum power point tracking (MPPT). The MPPT function generates a current reference for the input current control. A proportional-integral (PI) controller is designed to regulate the input current. The output of the current control loop is d_b for S_5 and S_6. d_{SR} is generated from both the inverse of the d_b and the zero current detection (ZCD). Fig. 11 shows the details of the implementation of d_{SR} and d_b. Texas Instrument DSP 28026 is employed for the digital control implementation because of its small package and low power dissipation. The two analog comparators in the DSP 28026 are used for positive and negative half cycle ZCD. The frequency of carriers of $S_{5,6}$ is double of the carrier of primary side switches. For each switching cycle of S_1, there are two interrupt events. The first interruption is at the beginning of the switching cycle, and the second is at half of the switching cycle. When the first interruption happens, the PWM of S_6 is set high after dead time, and then set to low when the carrier wave reaches to the output value of the PI controller. At this period, the PWM setting of S_5 is complementary of S_6. Therefore, the PWM of S_5 is set high after the PWM of S_6 becomes low with dead-time delay. The PWM of S_5 is forced to low when the positive half cycle ZCD circuit senses that the resonant current has reached zero. This is implemented in the DSP with an internal analog comparator and an enhanced pulse width modulator (ePWM) trip zone submodule. After the PWM trips to low, it will stay low and is no longer affected by the sensing circuit until the end of half the switching cycle. At the beginning of the other half switching cycle of S_1, the second interruption happens. Now, the output of PI controller is no longer impacting S_6 but S_5. Also, the negative half cycle ZCD will work for the PWM of S_6. The rising edge of the PWM of S_5 is right after the second interruption with dead-time delay, and the falling edge is controlled by the output of the PI controller. The rising edge of the PWM of S_6 is right after the falling edge of the PWM of S_5 with dead-time delay, and its falling edge is dependent on the ZCD.

$$i_{Lr\_RMS} = \sqrt{\frac{2}{T}\left(\int_0^{t1}\left(\frac{r_1}{Z_r}\sin(\omega_r T_s t)\right)^2 dt + \int_{t1}^{t3}\left(\frac{r_2}{Z_r}\sin(\beta - \omega_r T_s (t - d_b))\right)^2 dt\right)} \tag{27}$$



(a)

(b)

Fig. 11. Digital implementation of the proposed double-pulse duty cycle modulation. (a) System control diagram. (b) Implementation in DSP.

D. Dead-Time Design

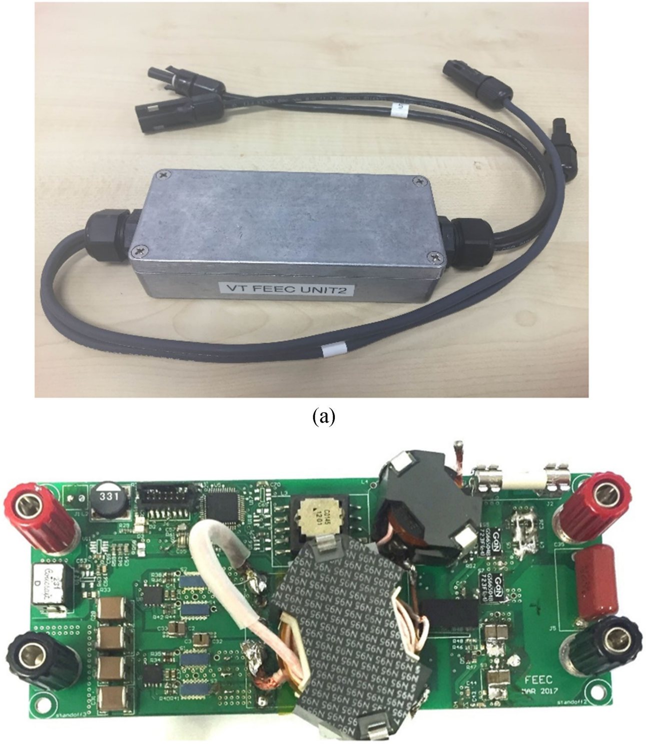
Dead-time design is critical to achieve soft switching for the proposed modulation technique. As shown in Fig. 4, there are two dead times for the half switching cycle in the proposed modulation scheme. One is the dead time between S_1 and S_3, referred to as DT_1, and the other is the dead time between S_5 and S_6, referred to as DT_2.

During DT_1, the magnetizing current can be treated as a current source to fully discharge C_{oss} of $S_{2,3}$ and charge C_{oss} of $S_{1,4}$. S_2 and S_3 can then achieve ZVS turn on when a positive gate signal is applied. Therefore, DT_1 should be designed large enough for this period as

$$DT_1 \geq \frac{8 L_m f_s C_{oss}}{n^2}. \tag{28}$$

Unlike $S_{1\text{–}4}$, the ZVS turn ON of $S_{5,6}$ is achieved by resonant current. During DT_2, the L_r and C_{oss} of $S_{5,6}$ resonate. When the voltage across C_{oss6} resonates to zero, the body diode of S_6 conducts and the voltage is clamped to the forward voltage. The initial resonant current is the turn-OFF current of S_5, which is dependent on the operating conditions. The larger the initial current, the less time is necessary for C_{oss6} to resonate to 0 V. Therefore, the design of DT_2 is based on the worst case conditions when initial current is zero, which means $d_b = 0$ at nominal input voltage condition

$$V_o \cos\left(\frac{1}{\sqrt{2 L_r C_{oss5}}} DT_2\right) = 0. \tag{29}$$



(a)

(b)

Fig. 12. Hardware photograph. (a) Case picture. (b) Board picture.

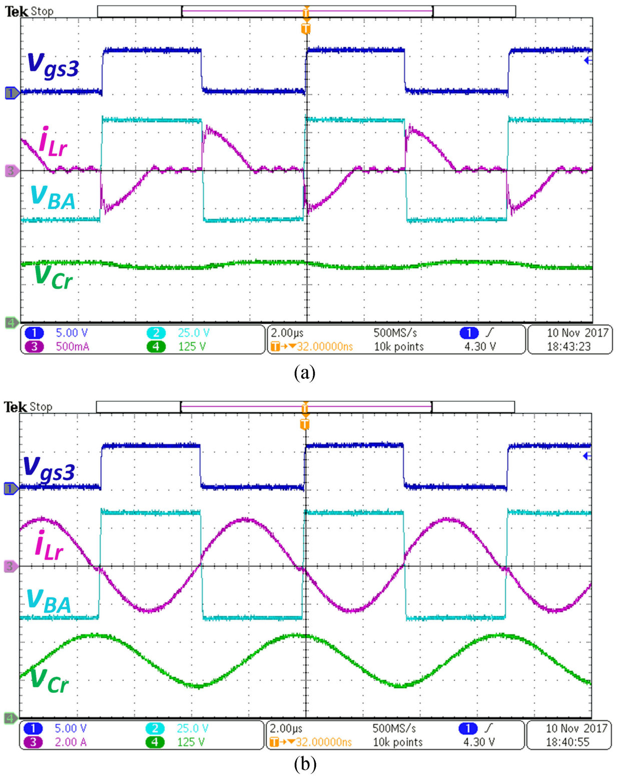
TABLE II
POWER STAGE PARAMETERS

Description	Value
Resonant inductance, L_r	39.5 *uH*
Resonant capacitance, $C_{r1,2}$	16.4 *nF* (600 V, NP0)
Magnitizing inductance, L_m	680 *uH*
Transformer turns ratio, *n*	4: 22
Primary-side switches, S_1-S_4	EPC2021
Secondary-side switches, S_5-S_6	GS66502B

IV. EXPERIMENTAL VERIFICATIONS

A 300-W prototype was built to verify the performance of the proposed converter. Fig. 12 shows the hardware photograph with case. The case dimension is 5.1” length × 2.4” width × 1.4” height. The nominal input voltage is designed at 35 V and the output voltage is fixed at 380 V for the dc microgrid connection. The transformer turns ratio is selected to be 4:22. EPC2021 and GS66502B are selected as the input and output sides switches, respectively. The switching and resonant frequencies are selected to be 140 kHz for the compliance consideration of electromagnetic interference standards that are typically measured from 150 kHz and up. The designed parameters are given in the Table II.

With nominal input voltage, the converter operates as a pure SRC, as shown in Fig. 13. Because of the 0.5 fixed duty of $S_{1\text{–}4}$, the voltage waveform across the primary winding of the transformer is rectangular. The dc voltage of resonant capacitor is half of the output voltage 190 V. Under 30-W conditions, the peak resonant current is 0.5 A, and the peak resonant voltage is



(a)

(b)

Fig. 13. Experimental steady-state waveforms with nominal input voltage (35 V): gate to source voltage of S_3 v_{gs3}, resonant current i_{Lr}, voltage across primary winding of the transformer v_{BA}, and voltage across resonant capacitor v_{Cr}. (a) Under light load condition (30 W). (b) Under full load condition (300 W).

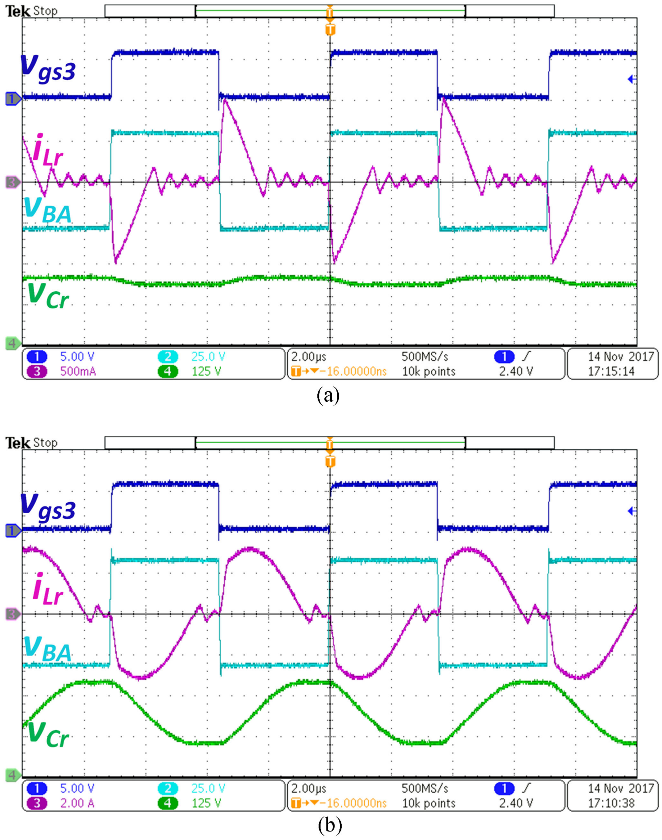
210 V. Under 300-W conditions, the resonant current is purely sinusoidal, as shown in Fig. 13(b). The peak resonant current is 2.6 A, and the peak resonant voltage is 280-V.

Fig. 14 shows the experimental waveforms with the proposed double-pulse duty cycle modulation under low input voltage. With d_b, the resonant current is charged. After that, the resonant current decreases to zero with $d_{\rm SR}$. Similar to nominal input voltage conditions, the voltage waveform across the primary winding of the transformer is rectangular due to a 0.5 duty of the primary side switches. Under 30-W load condition with 32-V input, the d_b is 1.4%, which matches with the voltage conversion ratio analysis. The peak current is 1 A, and the peak resonant voltage is 225 V. The d_b is 3.7% when the input voltage is 32 V and output is 380 V/300 W. The resonant peak current is 3.2 A, and the peak resonant voltage is 300 V.

The implementation of double-pulse duty cycle modulation for both S_5 and S_6 is shown in Fig. 15. At the positive half cycle, d_b of S_6 is applied at the beginning of the switching cycle to charge the resonant inductor and $d_{\rm SR}$ of S_5 is applied to deliver the energy to the load until the resonant current reaches to zero. During the DCM period, the gate signals of S_5 and S_6 are both low to keep the switches OFF. The positive and negative half switching cycles are symmetrical.

With the proposed converter, all input side switches can achieve ZVS turn ON and output side switches can achieve ZCS turn OFF regardless of input voltage or output power. Fig. 15 shows ZCS turn-ON and turn-OFF waveforms of S_5 and S_6. Fig. 16 shows ZVS turn-ON waveforms of S_3 and S_5. v_{gs3} and v_{gs5} are high after that v_{ds3} and v_{ds5} drops to zero. The turn-ON transitions of $S_{1,2,4}$ and S_6 are the same as S_3 and S_5.

The power stage efficiency of the proposed converter is measured for different input voltages and output power levels. The peak efficiency and CEC efficiency under nominal input conditions is 98.9% and 98.72%, respectively, as shown in Fig. 17(a). An example with *P*–*V* curves generated from Chroma Solar



(a)

(b)

Fig. 14. Experimental steady-state waveforms with low input voltage (32 V): gate to source voltage of S_3 v_{gs3}, resonant current i_{Lr}, voltage across primary winding of the transformer v_{BA}, and voltage across resonant capacitor v_{Cr}. (a) Under light load condition (30 W). (b) Under full load condition (300 W).

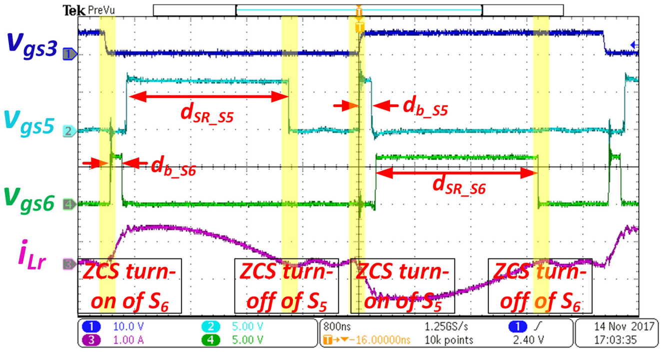
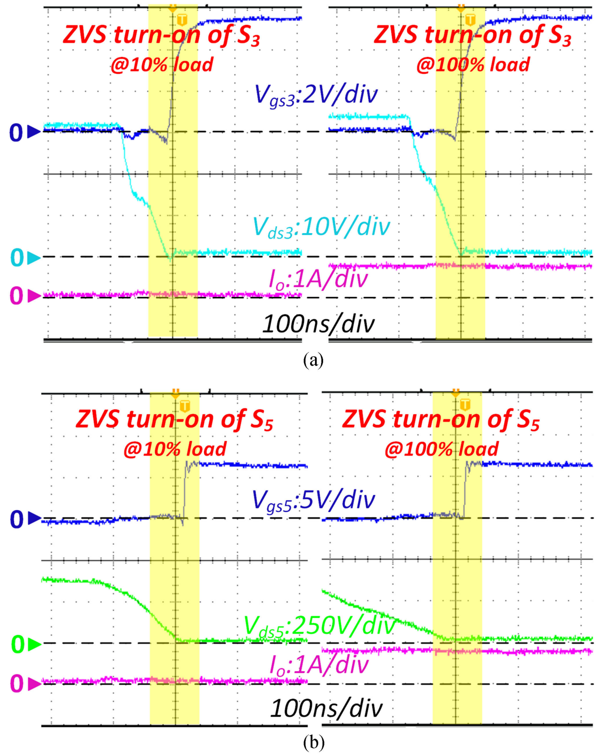


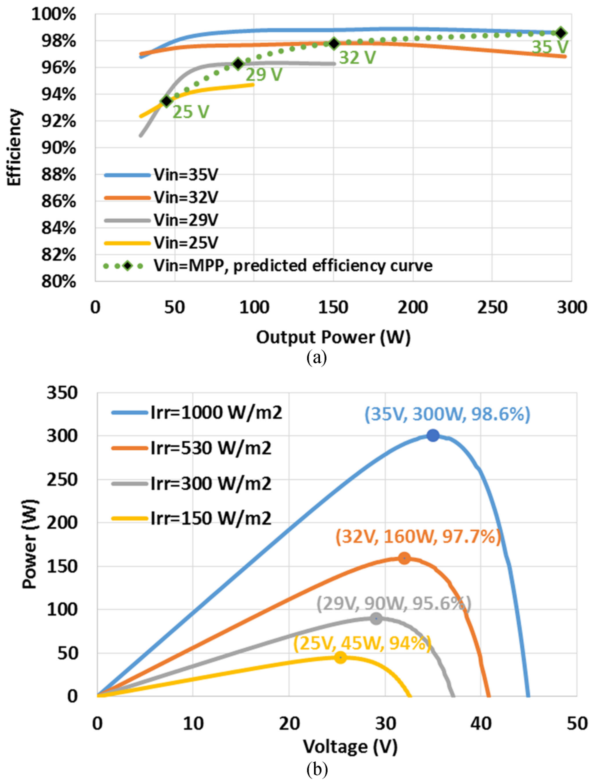
Fig. 15. Experimental waveforms of double-pulse duty: gate to source voltage of S_3 v_{gs3}, gate to source voltage of S_5 v_{gs5}, gate to source voltage of S_6 v_{gs6}, and resonant current i_{Lr}.



(a)

(b)

Fig. 16. Turn-ON transition of input and output side switches with the proposed modulation method: Left is under 30-W load and right is under 300-W load. (a) Turn-ON transition of S_3: gate to source voltage of S_3 v_{gs3}, drain to source voltage of S_3 v_{ds3}, and output current I_o. (b) Turn-ON transition of S_5: gate to source voltage of S_5 v_{gs5}, drain to source voltage of S_5 v_{ds5}, and output current I_o.



(a)

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Fig. 17. Efficiency tesing of the proposed converter. (a) Efficiency curves with different input voltages. (b) MPP Efficiency at different irradiance conditions.

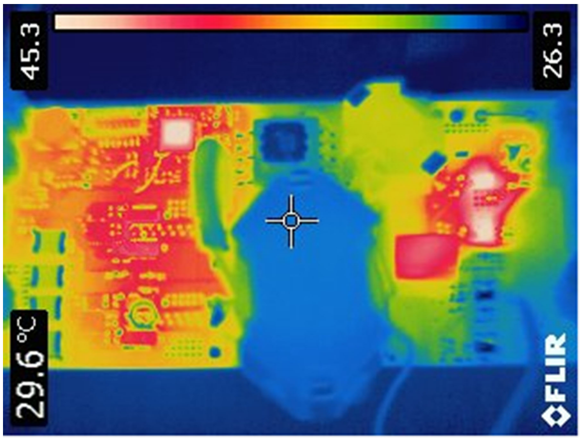
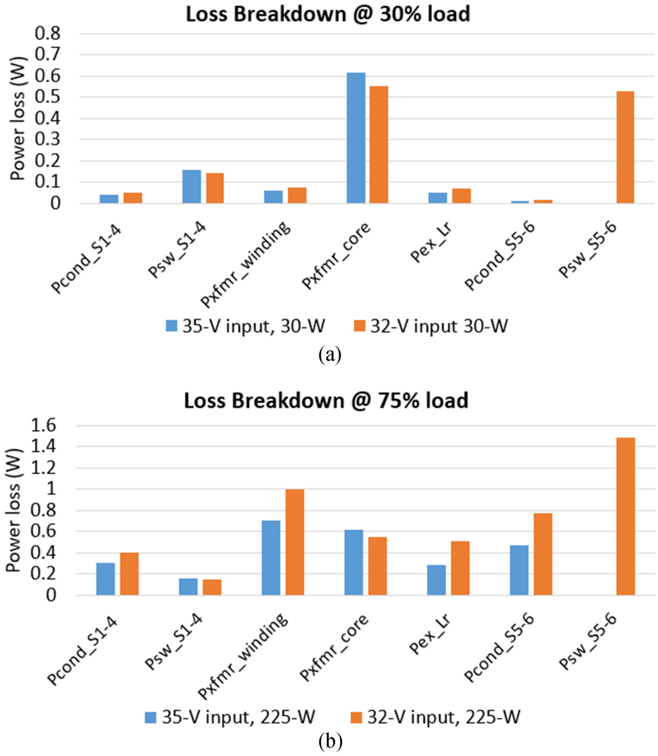


Fig. 18. Thermal testing under nominal input voltage and full load conditions.



(a)

(b)

Fig. 19. Power stage loss breakdown analysis for 35-V and 32-V input conditions. (a) Under 30% load conditions. (b) Under 75% load conditions.

Array Simulator [29] is given in Fig. 17(b) to show the efficiency at maximum power points (MPP) under different irradiance conditions. The nominal irradiance condition is set at 1000 W/m^2, where the MPP is 35 V, 300 W. The efficiency at this point is 98.6%. When irradiance is halved, the MPP moves to 32 kV, 160 W. The efficiency at this point is 97.7%. Based on the different *P–V* curves, the predicted efficiency curve with MPP is marked in Fig. 17(a) with a dashed line. For the majority of time (defined as when irradiance is stronger than 500 W/m^2), the efficiency of the proposed converter is higher than 98%.

Under natural convection cooling, the thermal image is shown in Fig. 18. This testing is under nominal input voltage and full load condition. The hottest spot is on the output side switches, which has a 45 °C or 20 °C temperature rise. The temperature of the input side switches is 32 °C or a 7 °C temperature rise. The transformer core temperature is measured to be only 30 °C. Loss breakdown is calculated at a 75% load condition since its CEC efficiency weight is the highest and is the most important index. The total calculated loss matches with the measured loss. Fig. 19 shows the loss breakdown analysis for different input and output conditions. The main losses are from the magnetic components and ouput side switches under both light and heavy load conditions.

V. CONCLUSION

In this paper, a high-efficiency active-boost-rectifier-based converter is proposed for modular PVs in dc microgrid applications. A novel double-pulse duty cycle modulation scheme is proposed to ensure that the converter not only keeps the benefits of the highly efficient SRC converter, but also achieves a higher voltage gain than the SRC and a wide-range regulation ability without adding additional switches while operating under fixed-frequency condition. The proposed converter has the following distinct features.

1) Compared to the conventional variable frequency *LLC* resonant converter, it has lower circulating energy due to the fixed frequency operation.
2) ZVS and low-current switching of input side switches, and ZCS of output side switches regardless of input voltage or output power.
3) The proposed active-boost-rectifier reduces the number of power devices compared with previous work. With the proposed double-pulse duty cycle modulation, the output side switches not only serve for synchronous rectification but also for the voltage boost function to achieve high voltage gain.

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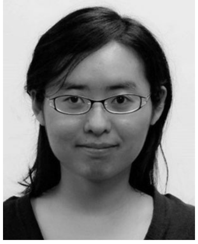

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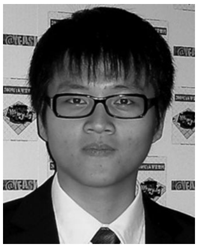

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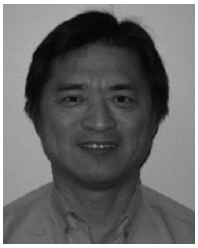

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Dr. Lai was the recipient of the Technical Achievement Award in Lockheed Martin Award Night, 2 Journal Paper Awards, 12 Best Paper Awards from the IEEE sponsored conferences, and the 2016 IEEE IAS Gerald Kliman Innovator Award. He led the student teams to win the top three finalist in Google Little Box Challenge in 2016, Grand Prize Award from International Future Energy Challenge in 2011, and Grand Prize Award from Texas Instruments Engibous Analog Design Competition in 2009. He is the Founding Chairs of the 2001 IEEE IFEC and the 2016 IEEE ACEPT, and General Chairs of IEEE COMPEL-2000, IEEE APEC 2005, IEEE SPEC-2018, and IEEE IFEEC-2019 conferences.