A Current Limiting Strategy With Parallel Virtual Impedance for Three-Phase Three-Leg Inverter Under Asymmetrical Short-Circuit Fault to Improve the Controllable Capability of Fault Currents

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***Abstract*—Voltage-controlled three-phase three-leg inverters are widely applied in various occasions. The inverters are generally switched to the current-controlled mode to limit the fault currents when short-circuit faults happen. Under symmetrical fault, the inverter can be controlled as a symmetrical, three-phase current source. However, the voltage limiting will happen under asymmetrical fault. As a result, the fault phase currents will be distorted and cannot be completely controlled. Considering that the voltage limiting is mainly caused by large load impedance of healthy phase under asymmetrical fault, the voltage limiting is avoided by paralleling the virtual impedance with the output filter capacitor in this paper. As a result, the current limiting loop is not broken and the fault phase currents can be effectively controlled. The implementation of virtual impedance in control system and the influence of virtual impedance on the stability of system are also analyzed in detail in this paper. The theoretical results are validated by experiments.**

***Index Terms*—Asymmetrical short-circuit fault, current limiting control, the virtual impedance, three-phase three-leg (TPTL) inverter.**

I. Introduction

BEING capable of providing the high-quality voltage, voltage controlled three-phase inverters have been widely applied in various occasions [1]–[4], such as household appliances, traction devices, medical equipment, industrial applications, microgrid, etc. In practical operations, the inverters probably experience the short-circuit fault or other abnormal conditions [5], [6]. Generally, when short-circuit fault occurs, the switching devices may be damaged due to the large fault currents.

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system can be equivalent to three independent single-phase systems. Obviously, the similar fault behaviors for three-phase combined inverter (with three independent output transformers for three phases) can be also obtained. However, different from the three-phase four-leg inverter and three-phase combined inverter, the three phases of three-phase three-leg (TPTL) inverter are not completely independent, considering the inherent constraint that the sum of three-phase inductor currents is always zero due to no neutral line. Therefore, for TPTL inverter, the goal that the fault phases work in CCM while the healthy phases still continue to work in VCM cannot be achieved under asymmetrical fault. Three phases of TPTL inverter will all have to work in CCM under asymmetrical fault. In this situation, the output voltage of healthy phase will be very large as the magnitude of the current limiting references (usually two to three times of the magnitude of rated current) is very high and the load impedance of healthy phase is also large. Therefore, the voltage limiter could be triggered if the amplitude of voltage vector exceeds the maximal voltage limiting determined by the dc-link voltage. As a result, the current limiting control loop will be broken and the fault phase currents cannot be completely controlled.

In [16] and [17], an extra maximum RMS output current limiting loop except normal dual loop control is designed to limit the fault current. Although the voltage limiting can be avoided, the instantaneous control for each phase current cannot be achieved as only the maximum RMS current among three-phase output currents is controlled. Besides, the fault response is slow. In order to simultaneously protect the semiconductor devices and ensure the reliable action of the protection devices under asymmetrical fault, it is expected that the fault currents are completely controlled. In [20], from changing current limiting references point of view, the current limiting method based on the improved current limiting references is proposed to avoid the voltage limiting. The current limiting references of three phases are asymmetrical, e.g., the amplitude of current limiting reference of healthy phase is designed to be zero to avoid the voltage limiting, while the magnitudes of current limiting references of the fault phases still keep two to three times of the magnitude of rated current. Under this method, the voltage limiting does not occur and the short-circuit currents can be completely controlled. However, this method needs to identify the types of faults and extract the fault phases. On the one hand, it takes some time to correctly identify the fault phases resulting in the slow fault response. On the other hand, the algorithms of identifying the fault types and extracting the fault phases are also complicated.

Physically, the voltage limiting is mainly caused by the large current limiting reference and the large load impedance of healthy phase when adopting the current limiting method based on instantaneous inner current loop under asymmetrical fault. In this paper, the voltage limiting is avoided by reducing the load impedance by means of paralleling the virtual impedance with the output filter capacitors. As a result, the current limiting loop is not broken and the fault phase currents can be effectively controlled. In addition, the proposed strategy does not need to identify the fault phases and healthy phases, thus, simplifying the design of control system and achieving the fast response.

The rest of the paper is organized as follows. The mechanism of the voltage limiting under asymmetrical fault is briefly analyzed in Section II. In Section III, the basic principle of the proposed current limiting strategy with the virtual impedance is presented. The implementation of virtual impedance in control system and the influence of virtual impedance on the stability of system are given in Section IV. In addition, the influence of the proposed strategy on actual short-circuit currents are analyzed in Section V. In Section VI, the experimental results are provided to verify the effectiveness of the proposed method. Section VII concludes this paper.

II. Mechanism of Voltage Limiting Under Asymmetrical Fault

Fig. 1 shows the structure of TPTL inverter. u_a, u_b, and u_c are arm voltages of phase *a*, *b*, and *c*, respectively. The *LC* filter consists of an inverter-sider inductor *L* and a filter capacitor *C*. B_j represents the circuit breaker in *j*th branch. Fig. 2 shows the dual loop control diagram for three-phase inverter. The dual loop consisting of outer voltage loop and inner current loop is widely adopted and can be implemented in stationary $\alpha\beta$ reference frame (x $= \alpha, \beta$), stationary abc reference frame (x $=$ a, b, c), and synchronous reference frame (x $=$ d, q). G_v(s) and G_c(s) represent the voltage controller and current controller, respectively. The inner current loop can automatically limit the fault currents in the case of short-circuit fault by placing a current limiter in the current control channel. In addition, the voltage limiter is also generally designed to limit the maximum output voltage [21]–[23]. If (1) holds true, the voltage limiter will be triggered (i.e., the amplitude of voltage vector is located outside the maximum circle of the hexagon)

$$|u_r| \geq V_{\text{limit}} \tag{1}$$

where $V_{\text{limit}} = V_{\text{dc}}/\sqrt{3}$ represents the amplitude of voltage vector located at the maximal circle of the hexagon in vector diagram. u_r represents the voltage vector, and $|u_r|$ represents its magnitude with $|u_r| = \sqrt{u_{rd}^2 + u_{rq}^2}$ in synchronous reference frame,$|u_r| = \sqrt{u_{r\alpha}^2 + u_{r\beta}^2}$ in stationary α-β frame, and $|u_r| = \frac{\sqrt{2}}{3}\sqrt{u_{rab}^2 + u_{rbc}^2 + u_{rca}^2}$ in stationary *a*-*b*-*c* frame.

When a symmetrical short-circuit fault occurs, the output voltage of the inverter is approaching zero. According to Fig. 2, the output of voltage control will be saturated, and the inverter is switched from VCM to CCM. In this case, (1) does not hold true and the current loop can work well. The three-phase inverter will behave as symmetrical current sources considering that the current limiting references in different frames are generally given as (2a)–(2c)

$$\begin{cases} i_{Ld\_\text{limit}}^* = I_{L\_\text{limit}} \\ i_{Lq\_\text{limit}}^* = 0 \end{cases} \tag{2a}$$

$$\begin{cases} i_{L\alpha\_\text{limit}}^* = I_{L\_\text{limit}} \cos(\omega t - \varphi_\alpha) \\ i_{L\beta\_\text{limit}}^* = I_{L\_\text{limit}} \sin(\omega t - \varphi_\alpha) \end{cases} \tag{2b}$$

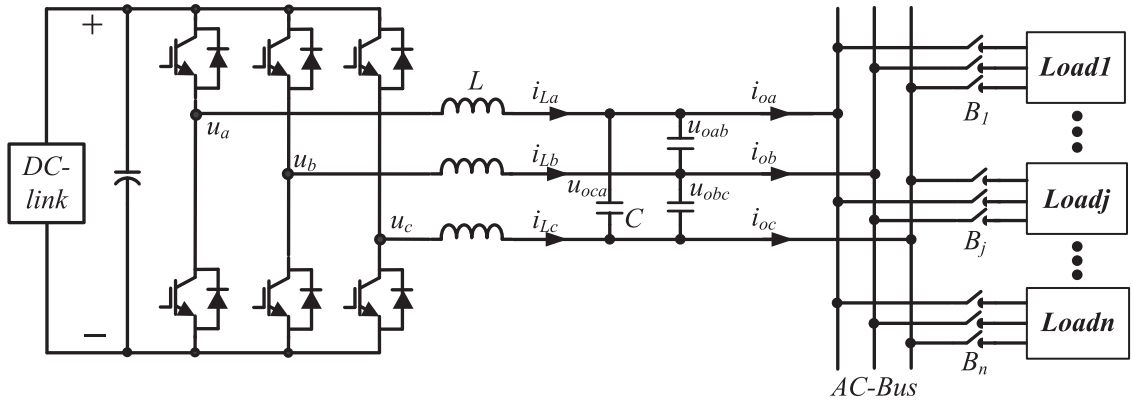

Fig. 1. Configuration of TPTL inverter.

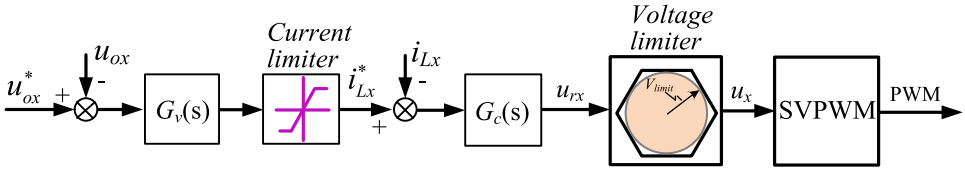

Fig. 2. Control diagram including outer voltage loop and inner current loop.

$$\begin{cases} i^*_{La\_\text{limit}} = I_{L\_\text{limit}} \cos(\omega t - \varphi_a) \\ i^*_{Lb\_\text{limit}} = I_{L\_\text{limit}} \cos(\omega t - \varphi_a - 120^\circ) \\ i^*_{Lc\_\text{limit}} = I_{L\_\text{limit}} \cos(\omega t - \varphi_a + 120^\circ) \end{cases} \tag{2c}$$

where I_{L_limit} represents the magnitude of the current limiting references, and is generally set to two to three times of I_{LM} (I_{LM} is defined as the magnitude of the rated current)., $I_{L\_\text{limit}} = 2{\cdot}I_{LM}$ is chosen in this paper.

However, when the inverter experiences an asymmetrical fault, the different fault characteristics will occur [14], [15], [20]. Assuming that a short-circuit fault happens between phases b and c, Fig. 3 shows the equivalent circuit of TPTL inverter feeding delta-connected equivalent loads or star-connected equivalent loads, where u_a, u_b, and u_c represent the equivalent arm voltages of inverter. Z_f represents the short-circuit impedance.

According to Fig. 3, $u_{oab} \approx (Z_{ca}Z_{ab}i_{La})/(Z_{ab}+Z_{ca})$, $u_{obc} \approx 0, u_{oca} \approx -u_{oab}$. Suppose the voltage limiter is not triggered, meanwhile, neglecting the switching action of the inverter and the inductor voltage, then $u_{rab} \approx u_{oab}, u_{rbc} \approx u_{obc}$, and $u_{rca} \approx u_{oca}$. Based on aforementioned analysis, $|u_r|$ under asymmetrical fault can be also expressed as $|u_r| = \frac{\sqrt{2}}{3}\sqrt{u^2_{\text{r}ab} + u^2_{rbc} + u^2_{rca}} \approx \frac{\sqrt{2}}{3}\sqrt{u^2_{oab} + u^2_{obc} + u^2_{oca}} = \frac{2}{3}|\frac{Z_{ab}Z_{ca}i_{La}}{Z_{ab}+Z_{ca}}|$(neglecting capacitor currents). It can be seen that $|u_r|$ is determined by the inductor current of healthy phase and post-fault load impendences under asymmetrical fault. If the voltage limiter is not triggered, the inductor current of phase a will be equal to the current limiting reference of phase a, i.e., $i_{La} = i^*_{La\_\text{limit}} = I_{L\_\text{limit}} \cos(\omega t - \varphi_a)$ ($I_{L\_\text{limit}} = 2I_{LM}$). Meanwhile, for the sake of convenient analysis, suppose $Z_{ab} = Z_{ca} = Z_L$, then (3) can be obtained as

$$|u_r| \approx \frac{2}{3}\left|\frac{Z_{ab}Z_{ca}i_{La}}{Z_{ab}+Z_{ca}}\right| = \frac{1}{3}|Z_{\text{L}}I_{L\_\text{limit}}| = \frac{2}{3}|Z_{\text{L}}|\,I_{LM}. \tag{3}$$

The voltage limiter will be triggered if (4) holds true

$$|u_r| \approx \frac{2}{3}|Z_{\text{L}}|\,I_{LM} \geq V_{\text{limit}}. \tag{4}$$

Equation (4) can be also expressed as

$$|Z_{\text{n}}|/(2m_n|Z_{\text{L}}|) \leq 1 \tag{5}$$

where m_n represents the rated modulation ratio and $m_n = |Z_n|I_{LM}/(3V_{\text{limit}})$. m_n is typically in the range of $[0.7, 0.9]$ for inverter. Z_n is rated delta-connected load impedance. $|Z_n|I_{LM}/3$ is equal to the amplitude of the nominal phase voltage. Z_n/Z_L represents the overload ratio. $(Z_n/Z_L) \to 0$ represents no load and $(Z_n/Z_L) = 1$ represents rated load.

Based on (5), Fig. 4 can be obtained [20]. Fig. 4 shows the relationship among the voltage limiting, Z_n/Z_L and m_n under asymmetrical fault. It can be seen that the voltage limiting will happen under most cases. Particularly, when the post-fault load is between no load [i.e., $(Z_n/Z_L) \to 0$] and rated load (i.e., $Z_L = Z_n$), the voltage limiting will appear under asymmetrical fault.

According to the previous analysis, when the current limiting control based on the symmetrical references [as shown in (2a)–(2c)] is implemented, the voltage limiting will happen under asymmetrical fault. As a result, the current limiting loop is broken and the fault currents cannot be completely controlled.

This is unacceptable for the inverter, considering that the uncontrolled fault currents may cause overcurrents for the switching devices, and the reliable actions of the breakers installed in the load branches are also greatly influenced.

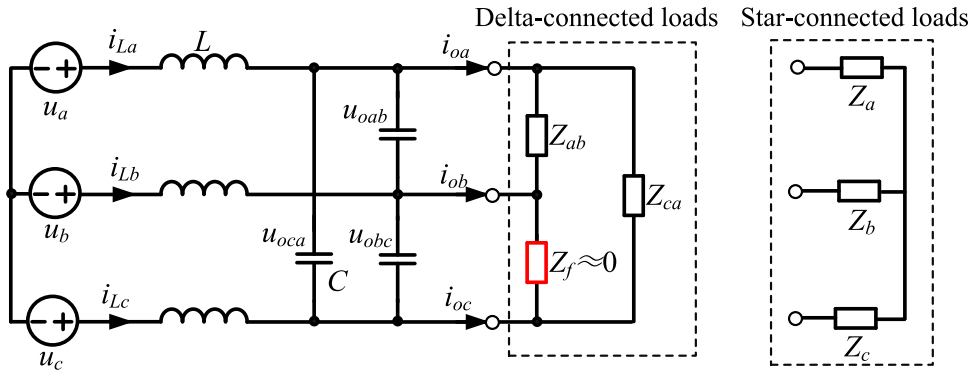

Fig. 3. Equivalent circuit under short-circuit fault between phase *b* and *c*.

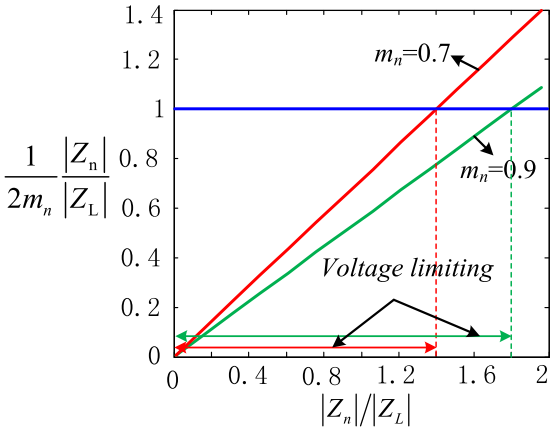

Fig. 4. Relationship among the voltage limiting, Z_n/Z_L and m_n under asymmetrical fault.

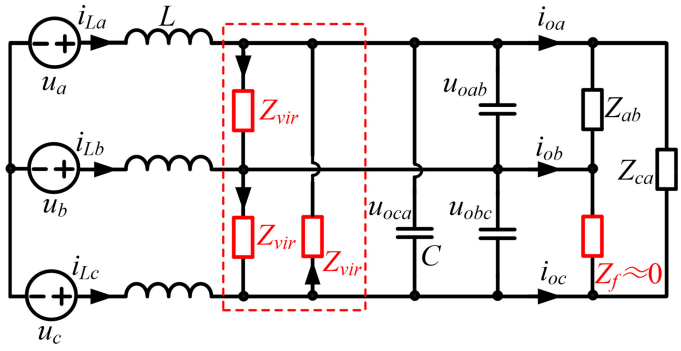

Fig. 5. Equivalent circuit with virtual impedance in parallel with the output filter capacitor.

III. Basic Principle of Proposed Current Limiting Strategy

In order to limit the fault currents and ensure the reliable action of the breakers, the fault currents are expected to be completely controlled. According to the aforementioned analysis, the voltage limiting under asymmetrical fault should be first avoided. Assuming that an asymmetrical fault between phase *b* and *c* occurs, based on the analysis in Section II, the output voltage limiting will not happen if (6) holds true

$$|u_r| \approx \frac{2}{3}\left|\frac{Z_{ab}Z_{ca}i_{La}}{Z_{ab}+Z_{ca}}\right| < V_{\text{limit}}. \tag{6}$$

If $i_{La}=0$, the voltage limiting will not happen under any load. In this situation, the current limiting references can be expressed as [20]

$$\begin{cases} i^*_{La\_\text{limit}} = 0 \\ i^*_{Lb\_\text{limit}} = I_{L\_\text{limit}}\cos(\omega t-\varphi_i) \\ i^*_{Lc\_\text{limit}} = -I_{L\_\text{limit}}\cos(\omega t-\varphi_i). \end{cases} \tag{7}$$

However, this control strategy [20] requires that the different current limiting references should be designed for different types of short-circuit faults, e.g., $i^*_{Lb\_\text{limit}}=0$ for the asymmetrical short-circuit fault between phase *a* and *c*, and $i^*_{Lc\_\text{limit}}=0$ for the asymmetrical short-circuit fault between phase *a* and *b*. Table II in the Appendix gives the detailed current limiting references under different types of short-circuit faults. In order to implement this control strategy, the fault types and fault phases should be identified first, and then the corresponding current limiting references can be obtained. Although this control strategy can avoid the voltage limiting by altering the current limiting references, the algorithm of identifying the fault types is not only complex but also time consuming.

From (6), the voltage limiting can also be avoided if the equivalent load impedances are reduced while the current limiting references are set based on (2a)–(2c). Based on the idea, the current limiting strategy with virtual impedance in parallel with the output filter capacitor is proposed in this paper to avoid the voltage limiting, and at the same time achieving the controlled fault currents under asymmetric short-circuit faults.

Taking the short-circuit fault between phases *b* and *c* as an example, as shown in Fig. 5, the equivalent load impedances can be reduced by the virtual impedances in parallel with the filter capacitors and the load impedances. Equation (6) can be rewritten as (8) considering the effect of the parallel virtual impedance. If (8) holds true, the voltage limiting can be avoided

$$|u_r| \approx \frac{2}{3}\left|\frac{Z'_{ca}Z'_{ab}i_{La}}{Z'_{ab}+Z'_{ca}}\right| = \frac{2}{3}\left|(Z'_{ca}//Z'_{ab})\,i_{La}\right| < V_{\text{limit}} \tag{8}$$

where $i_{La}=i^*_{La\_\text{limit}}=I_{L\_\text{limit}}\cos\omega t$. $Z'_{ab}=Z_{\text{vir}}//Z_c//Z_{\text{ab}}$ and $Z'_{ca}=Z_{\text{vir}}//Z_c//Z_{\text{ca}}$ ($Z_c=1/sC$ represents the impedance of output filter capacitor), are the equivalent load

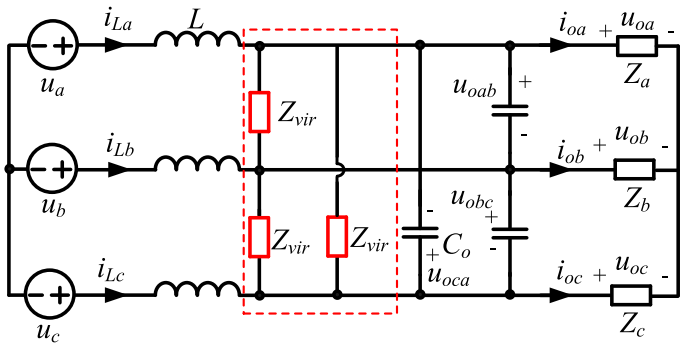

Fig. 6. Equivalent circuit of inverter under parallel virtual impedance.

impedances between phase *a* and *b*, and between phase *c* and *a*, respectively.

In order to avoid the voltage limiting, (8) should hold true for the TPTL inverter feeding any loads. Considering that the equivalent load impedances Z'_{ab} and Z'_{ca} will get the maximum under no load ($Z_{\rm ab} \to \infty, Z_{\rm ca} \to \infty$), the voltage limiting of the TPTL inverter can be avoided under any load condition with the designed virtual impedance if the voltage limiting can be avoided under no load. Under no load, $Z'_{ab} = Z'_{ca} = Z_{\rm vir}//Z_c$. Although the parallel virtual impedance can be composed of inductors, capacitors, and resistors, the pure resistive virtual impedance is chosen to simplify the design in this paper. Then, (8) can be further simplified as $|{\rm Z_{vir}}//Z_c| < \frac{3V_{\rm limit}}{|i_{La}|} = \frac{3V_{\rm limit}}{I_{L\_{\rm limit}}} = \frac{|Z_n|}{2m_n}$(considering that $I_{L\_{\rm limit}} = 2{\cdot}I_{LM}$ and $m_n = |Z_n|I_{LM}/(3V_{\rm limit})$, $m_n = 0.7$–0.9). The upper limit of $Z_{\rm vir}$ can be obtained according to this inequality.

From the aforementioned analysis, the proposed method can effectively avoid the voltage limiting under asymmetrical faults. As long as the voltage limiting does not occur, the current control loop will not be broken, thus providing a possibility for complete control of the fault current. As shown in Fig. 5, if the parallel virtual impedances are smaller than the upper limit, the voltage limiting can be avoided when an asymmetrical fault occurs between any two phases. Therefore, the proposed method does not need to identify the fault phases, which greatly simplifies the design of control system. In Section IV, the implementation of virtual impedance by the control system and the influence of virtual impedance on the system stability will be discussed.

IV. Implement of Virtual Impedance and Stability Analysis

A. Model and Implementation of the Virtual Impedance

In order to implement the parallel virtual impedance by the control under short-circuit fault, the TPTL inverter should be first modeled, and then the controller can be designed. For the sake of simplifying the plant, the star-connected load is adopted, with the impedances denoted as Z_a, Z_b, and Z_c, as shown in Fig. 6.

Based on Fig. 6, applying Kirchhoff's voltage law, [(9a)–(9c)] can be obtained as follows:

$$-u_a + L\frac{di_{La}}{dt} + u_{oa} - u_{ob} - L\frac{di_{Lb}}{dt} + u_b = 0 \tag{9a}$$

$$-u_b + L\frac{di_{Lb}}{dt} + u_{ob} - u_{oc} - L\frac{di_{Lc}}{dt} + u_c = 0 \tag{9b}$$

$$-u_c + L\frac{di_{Lc}}{dt} + u_{oc} - u_{oa} - L\frac{di_{La}}{dt} + u_a = 0. \tag{9c}$$

Applying (9a)–(9c) and $i_{La} + i_{Lb} + i_{Lc} = 0$, one can get

$$3L\frac{di_{La}}{dt} = 2u_a - u_b - u_c + u_{ob} + u_{oc} - 2u_{oa}. \tag{10}$$

Equation (10) can be further simplified as

$$L\frac{di_{La}}{dt} = u_a - u_z + \frac{u_{ob} + u_{oc} - 2u_{oa}}{3} \tag{11}$$

where $\mathrm{u}_z = (u_a + u_b + u_c)/3$.

Similarly, applying (9b)-(9a), and (9c)-(9b), one can get

$$L\frac{di_{Lb}}{dt} = u_b - u_z + \frac{u_{oa} + u_{oc} - 2u_{ob}}{3} \tag{12}$$

$$L\frac{di_{Lc}}{dt} = u_c - u_z + \frac{u_{ob} + u_{oa} - 2u_{oc}}{3}. \tag{13}$$

Furthermore, according to Fig. 6, the load phase voltages can be expressed as

$$\begin{cases} u_{oa} = \left(i_{La} - \frac{u_{oab} - u_{oca}}{Z_{\rm vir}} - C\frac{d(u_{oab} - u_{oca})}{dt}\right) Z_a \\ u_{\rm ob} = \left(i_{Lb} - \frac{u_{obc} - u_{oab}}{Z_{\rm vir}} - C\frac{d(u_{obc} - u_{oab})}{dt}\right) Z_b \\ u_{oc} = \left(i_{La} - \frac{u_{oca} - u_{oab}}{Z_{\rm vir}} - C\frac{d(u_{oca} - u_{oab})}{dt}\right) Z_c. \end{cases} \tag{14}$$

According to (11)–(14), the plant model and current control diagram of the TPTL inverter can be obtained, as shown in Fig. 7.

In Fig. 7, $G_2(s)$ represents the transfer function of the inductor, i.e., $G_2(s) = 1/sL$. $G_c(s)$ represents the transfer function of the current limiting controller in *s*-domain. The feedforward of $(u_{oab} - u_{oca})/3 + u_z$ is introduced in the controller to decouple the coupling terms in the plant, achieving the simplification of the control design. Obviously, the parallel virtual impedance as shown in Fig. 7 cannot be implemented by the controller. In order to implement the parallel virtual impedance in the control system, the control diagram shown in Fig. 7 needs to be further transformed. Taking Fig. 7(a) as an example, moving the connection node of the virtual impedance part, i.e., $(u_{obc} - u_{oca})/Z_{\rm vir}$, from the output of G_2(s) to the input of G_c(s), Fig. 7(a) can be further transformed into Fig. 8(a), where, $G_{i\_{\rm open}}(s)$ is the open loop transfer function of current control loop and can be expressed by $G_c(s)G_2(s)$. The open loop gain within the control bandwidth of current loop is far greater than 1, i.e., $|G_{i\_{\rm open}}(s)| >> 1$. Hence, Fig. 8(a) can be further simplified to Fig. 8(b) considering $(1 + G_{i\_{\rm open}}(s))/G_{i\_{\rm open}}(s) \approx 1$.

It can be seen from Fig. 8(b) that the parallel virtual impedance can be implemented by changing the current limiting references. The new current limiting reference for phase *a* can expressed as $i^*_{La\_{\rm limit\_vir}} = i^*_{La\_{\rm limit}} - (u_{oab} - u_{oca})/Z_{\rm vir}$. Similarly, the current limiting references of phase *b* and *c* can

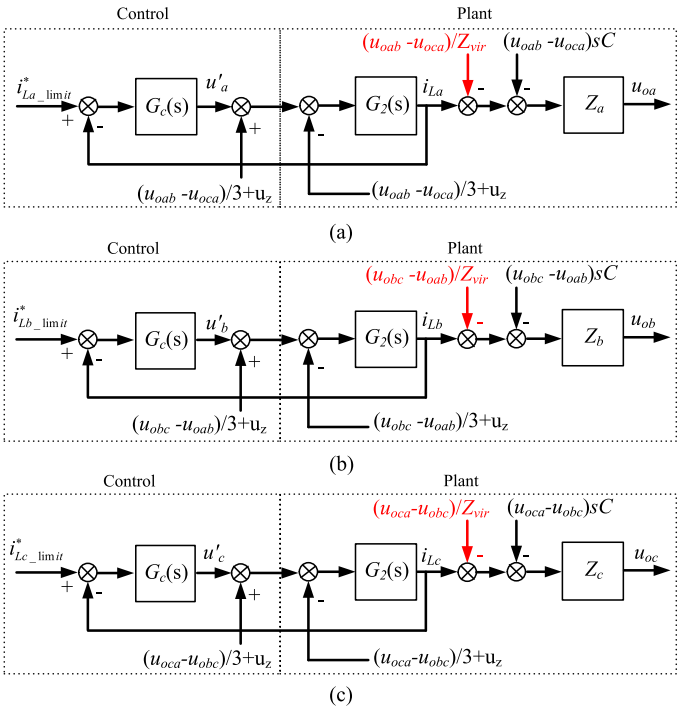

Fig. 7. Equivalent current control diagram of TPTL inverter with parallel virtual impedance. (a) The plant and control of the inductor current of phase a control. (b) The plant and control of the inductor current of phase b control. (c) The plant and control of the inductor current of phase c.

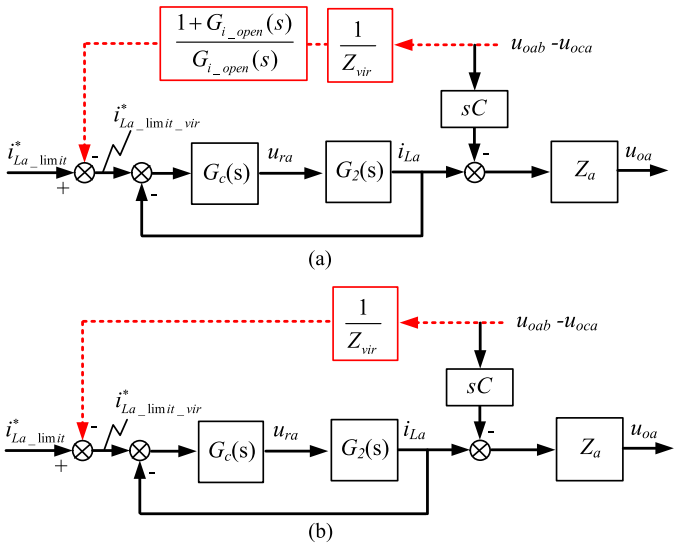

Fig. 8. Equivalent transformation of the parallel virtual impedance.

be also obtained under the parallel virtual impedance and are given in (15)

$$\begin{cases} i^*_{La\_limit\_vir} = i^*_{La\_limit} - (u_{oab} - u_{oca})/Z_{vir} \\ i^*_{Lb\_limit\_vir} = i^*_{Lb\_limit} - (u_{obc} - u_{oab})/Z_{vir} \\ i^*_{Lc\_limit\_vir} = i^*_{Lc\_limit} - (u_{oca} - u_{obc})/Z_{vir} \end{cases} \tag{15}$$

where $i^*_{La\_limit}$, $i^*_{Lb\_limit}$, and $i^*_{Lc\_limit}$ are the symmetrical three-phase current limiting references given by (2a)–(2c).

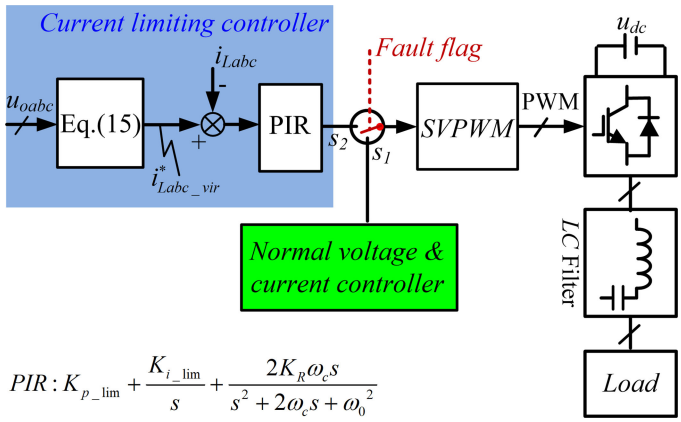

Fig. 9. Control diagram of the proposed method.

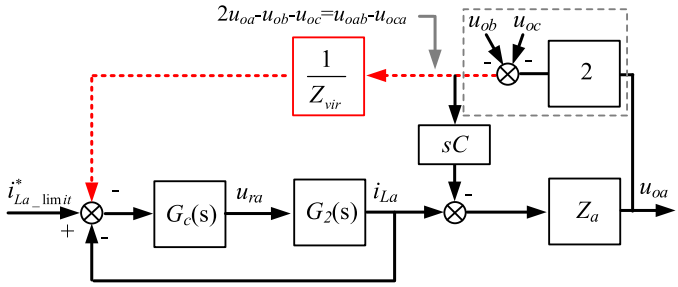

Fig. 10. Equivalent control diagram with parallel virtual impedance for phase a of TPTL inverter working in CCM.

Where, the line voltages u_{oab}, u_{obc}, and u_{oca} of the TPTL inverter are generally detected by the voltage sensors. Therefore, (15) can be easily obtained.

Fig. 9 shows the overall control diagram of the TPTL inverter with the proposed current limiting strategy. In normal state, the dual loop controller works, and the TPTL inverter is switched to the proposed current limiting control when a fault happens. The proportional integral plus resonant controller is adopted in the current limiting control to achieve the precise control of the fault currents.

B. Influence of the Proposed Current Limiting Control on System Stability

It can be seen from Fig. 8(b) that the feedforward of $(u_{oab} - u_{oca})$ with the gain of $1/Z_{\rm vir}$ is aimed at realizing the parallel virtual impedance by control, which may affect the stability of the current control loop of phase a. In Section III, the upper limit of the parallel virtual impedance determined in accordance with avoiding the voltage limiting has been presented. This section will determine the lower limit of the parallel virtual impedance from the system stability perspective.

Considering that the output phase voltages u_{oa}, u_{ob}, and u_{oc} are independent of each other, it is reasonable to treat u_{ob} and u_{oc} as external disturbances while analyzing the current control loop of phase a. Based on this consideration, Fig. 8(b) is further transformed into Fig. 10 considering that $u_{oab} - u_{oca} = 2u_{oa} - u_{ob} - u_{oc}$. For the stability analysis of the closed loop given

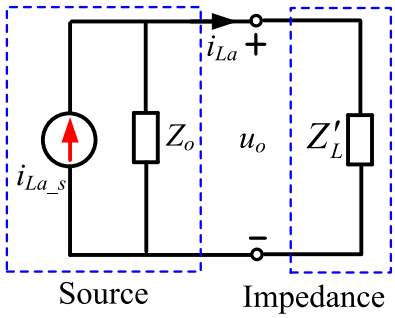

Fig. 11. Norton equivalent circuit of phase a for TPTL inverter working in CCM.

in Fig. 10, there are many approaches, such as the root locus [24], [25], frequency-domain technique, and impedance-based approach [26]–[28]. The impedance-based approach is adopted in this paper.

In order to apply the impedance-based approach, the Norton equivalent circuit consisting of an ideal current source (i_{La_s}) in parallel with an equivalent output impendence (Z_o), should be first obtained, as shown in Fig. 11, where Z'_L represents the equivalent load impedance. Then, the stability of the current control loop with parallel virtual impedance can be easily analyzed according to the relationship between Z_o and Z'_L. Therefore, the range of the parallel virtual impedance can be determined according to the stability of the current control loop.

According to Fig. 10, the expression of i_{La} can be derived in (16) by assuming $u_{ob} = 0$ and $u_{oc} = 0$

$$i_{La} = \frac{G_{i\_\text{open}}}{1 + G_{i\_\text{open}}} i^*_{La\_\text{limit}} - \frac{G_{i\_\text{open}}}{(1 + G_{i\_\text{open}})\, Z_{\text{vir}}} 2u_{oa}. \quad (16)$$

Therefore, $i_{La\_s} = \frac{G_{i\_\text{open}}}{1+G_{i\_\text{open}}} i^*_{L\_\text{limit}} \approx i^*_{L\_\text{limit}}$, and the equivalent output impedance (Z_o) of the TPTL inverter can be expressed as

$$Z_o = \frac{1 + G_{i\_\text{open}}}{2G_{i\_\text{open}}} Z_{\text{vir}}. \quad (17)$$

The equivalent load impedance Z'_L of Fig. 11 can also be obtained according to Fig. 10 as follows:

$$Z'_L = Z_a // \frac{1}{2sC} = \frac{Z_a}{2sCZ_a + 1}. \quad (18)$$

Particularly, the load only includes the output filter capacitor under no load, and the load impedance is expressed as $Z'_L = 1/(2sC)$.

By means of the impedance-based stability criterion, the following two conditions must be satisfied to ensure the stability [28].

1) The current-controlled inverter itself should be stable in the case of $Z'_L(s) = 0$.
2) The impedance ratio $Z'_L(s)/Z_o(s)$ satisfies the Nyquist criterion.

The first condition is easily satisfied by regulating the controller parameters of the current control loop. The second condition can be elaborated as follows. If $Z'_L(s)$ and $Z_o(s)$ does not intersect at any frequency, the system is always stable. If $Z'_L(s)$ and $Z_o(s)$ intersects at f_{cross}, the system will be stable if the phase difference between $Z_o(s)$ and $Z'_L(s)$ is less than 180°at f_{cross}, otherwise, the system will be unstable.

The purely resistive virtual impedance is chosen in the paper.

Based on (17) and Table I, the bode plots of the output impedance Z_o under different values of Z_{vir} is shown in Fig. 12. The bode plots of the load impedance $Z'_L(s)$ under different load impedances corresponding to no-load condition, half-load condition, and rated-load condition, are also given in Fig. 12. As observed from Fig. 12, two rules can be made: First, when Z'_L is fixed, the smaller Z_{vir} is, the easier unstable the system is. Second, when Z_{vir} is fixed, the larger Z'_L is, the easier unstable the system is. Therefore, if the system is stable for $Z_a = \infty$ (no-load condition), the system will be also stable under other load condition for the specified Z_{vir}. It can be seen from Fig. 12 that when $Z_{\text{vir}} = 46\ \Omega$ and $Z_a = \infty$, the phase difference between $Z_o(s)$ and $Z'_L(s)$ at f_{cross} is close to 180°, which means that current control loop is critical stable for $Z_{\text{vir}} = 46\ \Omega$. Thus, $Z_{\text{vir}} > 46\ \Omega$ should be satisfied to ensure the stability of the TPTL inverter working in CCM. On the other hand, according to the requirement of avoiding the voltage limiting, $Z_{\text{vir}} \le \frac{|Z_n|}{2m_n} = \frac{3V_{\text{limit}}}{I_{\text{limit}}} = 66.2\ \Omega$. Therefore, $46\ \Omega < Z_{\text{vir}} \le 66.2\ \Omega$. Finally, $Z_{\text{vir}} = 66.2\ \Omega$ is chosen to consider increasing the stability margin of the current control loop.

Based on the aforementioned analysis, it is concluded that two criteria have to be considered to select the parallel virtual impedance: avoiding the voltage limiting and ensuring the stability of current control loop. The upper limit of the parallel virtual impedance can be obtained by avoiding the voltage limiting in Section III, and the lower limit of the parallel virtual impedance can be obtained by ensuring the stability of current control loop in Section IV-B.

V. Analysis of Output Short-Circuit Currents Under the Proposed Strategy

According to the previous analysis, the voltage limiting can be avoided by the proposed parallel virtual impedance. However, due to the partial current sharing by the proposed parallel virtual impedance as shown in Fig. 5, the maximum short-circuit currents may vary. As is known to all, if the inverter can output sufficiently large currents in case of short-circuit fault, the fault branch can be reliably cleared by the circuit breaker in a short time, which is beneficial to improve the power quality of other normal loads. Therefore, this section will give the evaluation of the influence of parallel virtual impedance on the short-circuit currents.

For the asymmetrical short-circuit fault between phase b and c, the output currents i_{ob}, and i_{oc}, will be approximately equal to the current limiting references while ignoring the currents flowing through the filter capacitors, i.e.,

$$\begin{cases} i_{ob} \approx i^*_{Lb\_\text{limit\_}vir} = i^*_{Lb\_\text{limit}} - \frac{u_{obc} - u_{oab}}{Z_{\text{vir}}} = i^*_{Lb\_\text{limit}} \\ \qquad\qquad + \frac{Z'_{ca} Z'_{ab} i^*_{La\_\text{limit}}}{Z_{\text{vir}}(Z'_{ab} + Z'_{ca})} \\ i_{oc} \approx i^*_{Lc\_\text{limit\_}vir} = i^*_{Lc\_\text{limit}} - \frac{u_{oca} - u_{obc}}{Z_{\text{vir}}} = i^*_{Lc\_\text{limit}} \\ \qquad\qquad + \frac{Z'_{ca} Z'_{ab} i^*_{La\_\text{limit}}}{Z_{\text{vir}}(Z'_{ab} + Z'_{ca})} \end{cases} \quad (19)$$

TABLE I
PARAMETERS OF PROTOTYPE

Parameter	Value	Parameter	Value
DC-link voltage: u_{dc}	650 V	Filter capacitor: C	3.3 μF
Rated line-line voltage (RMS): V_n	380 V	Fundamental frequency: f_o	50 Hz
Rated power: S_o	4 kVA	Switching frequency: f_{sw}	10 kHz
Rated current (RMS): I_N	6 A	The PI parameters of outer voltage loop	$K_{p\text{-}v}$=6.44, $K_{i\text{-}v}$=820
Filter inductor: L	2.7 mH	The parameters of the current limiting controller (PIR)	$K_{p\text{-}lim}$=14, $K_{i\text{-}lim}$=937.5 K_R=300, ω_c =6 $rad \cdot s^{-1}$

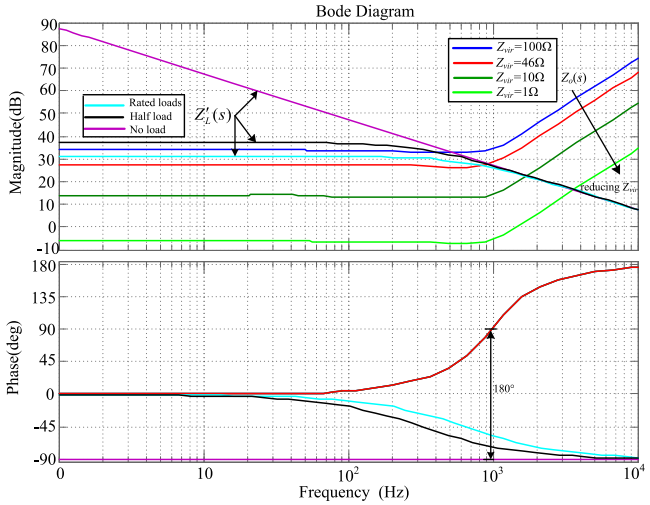

Fig. 12. Bode plots of the equivalent output impedance $Z_o(s)$ and equivalent load impedance $Z'_L(s)$ of the TPTL inverter.

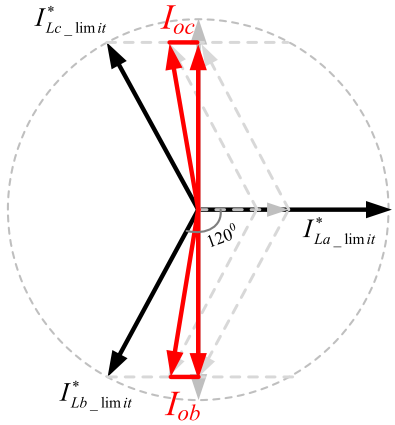

Fig. 13. Phasor diagram of actual currents of faults phases.

where $i^*_{La\_limit}$, $i^*_{Lb\_limit}$, and $i^*_{Lc\_limit}$ are given in (2), $Z'_{ab} = Z_{vir}//Z_{ab}$, $Z'_{ca} = Z_{vir}//Z_{ca}$(ignoring the filter capacitors). For the short-circuit fault between phase b and c, $u_{obc} \approx 0$, $u_{oab} \approx -u_{oca} \approx (Z'_{ca}Z'_{ab}i^*_{La\_limit})/(Z'_{ab} + Z'_{ca})$.

From (19), if $\frac{Z'_{ca}Z'_{ab}}{Z_{vir}(Z'_{ab}+Z'_{ca})}$ becomes smaller, the magnitude of the output short-circuit currents will vary in a smaller range. Due to

$$\frac{Z'_{ca}Z'_{ab}}{Z'_{ab}+Z'_{ca}} = Z'_{ca}//Z'_{ab} = \frac{Z_{vir}}{2}//(Z_{ab}//Z_{ca}).$$

Hence, $\frac{Z'_{ca}Z'_{ab}}{Z_{vir}(Z'_{ab}+Z'_{ca})} = \frac{(Z_{ab}//Z_{ca})}{Z_{vir}+2(Z_{ab}//Z_{ca})}$. Therefore, the larger Z_{vir} is, the smaller $\frac{Z'_{ca}Z'_{ab}}{Z_{vir}(Z'_{ab}+Z'_{ca})}$ is. According to the analysis in Section IV-B, the parallel virtual impedance is set to its upper limit, which is also helpful to reduce the influence of the parallel virtual impedance on the output short-circuit currents.

On the other hand, when the load impedances vary between no load and rated load, $(Z_{ab}\,//\,Z_{ca})$ will be maximal under no-load condition and be minimal under rated-load condition. Therefore, the following results can be obtained.

1) Under no-load condition, $\frac{Z'_{ca}Z'_{ab}i^*_{La\_limit}}{Z_{vir}(Z'_{ab}+Z'_{ca})} = \frac{(Z_{vir}//Z_{vir})i^*_{La\_limit}}{Z_{vir}} = \frac{i^*_{La\_limit}}{2}$.

2) Under rated-load condition, $\frac{Z'_{ca}Z'_{ab}i^*_{La\_limit}}{Z'_{ab}+Z'_{ca}} = \frac{(Z_{ab}//Z_{ca})i^*_{La\_limit}}{Z_{vir}+2(Z_{ab}//Z_{ca})} = \frac{Z_n i^*_{La\_limit}}{2(Z_{vir}+Z_n)} = \frac{Z_n i^*_{La\_limit}}{2(\frac{Z_n}{2m_n}+Z_n)}$, where $m_n = 0.9$, $\frac{Z'_{ca}Z'_{ab}i^*_{La\_limit}}{Z'_{ab}+Z'_{ca}} = 0.321 \cdot i^*_{La\_limit}$.

According to (19), the phasor diagram of output short-circuit currents of faults phases can be obtained, as shown in Fig. 13, where $I^*_{La\_limit}$, $I^*_{Lb\_limit}$, and $I^*_{Lc\_limit}$ are defined as the phasors of $i^*_{La\_limit}$, $i^*_{Lb\_limit}$, and $i^*_{Lc\_limit}$, respectively. I_{ob} and I_{oc} represent the phasors of i_{ob} and i_{oc}, respectively. From Fig. 13, the magnitudes of actual currents of faults phases will vary between 0.884 and $\sqrt{3}/2$(0.866) times of the magnitude of current limiting references when the load impedances of healthy phase vary in the range from no-load condition to rated-load condition. Therefore, the magnitudes of output short-circuit currents of faults phases only vary in a very small range and are almost not affected by the load impedances of the healthy phases, which is beneficial for the reliable fault clearing of the faulty load branch by the circuit breakers.

VI. EXPERIMENTAL VERIFICATION

A rated 4-kW TPTL inverter prototype is established to verify the proposed current limiting strategy under short-circuit fault. The test setup is shown in Fig. 14 (a) and its schematic diagram is shown in Fig. 14 (b). The short-circuit fault between phase b and c is achieved by closing the switch directly connected between

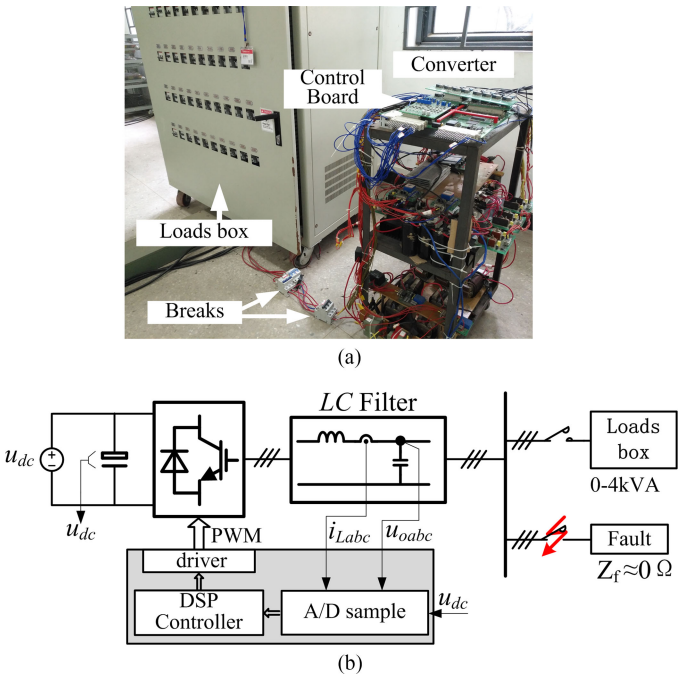

Fig. 14. (a) Test setup. (b) Overview of test setup.

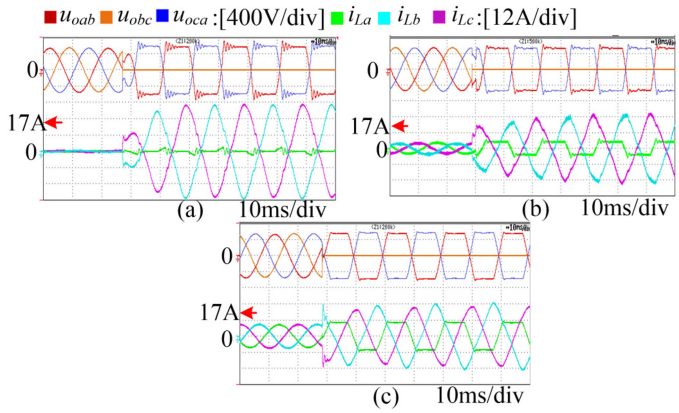

Fig. 15. Experimental results for short-circuit fault between phase b and c when the current limiting strategy based on the inner current loop is adopted. (a) No-load condition before fault occurs. (b) Half-load condition before fault occurs. (c) Rated-load condition before fault occurs.

phase b and c. The parameters of the test setup are listed in Table I. The magnitude of the current limiting references, I_{L_limit}, is set to 17 A (two times of the magnitude of rated current).

A. Current-Limiting Method Based on the Inner Current Loop Without Virtual Impedance

The experimental results shown in Fig. 15 corresponds to traditional current limiting for the short-circuit fault between phase b and c of the TPTL inverter, in which the current limiting is achieved by the inner current loop in the synchronous d-q frame. Three cases are shown when the TPTL inverter works under no-load condition, half-load condition, and rated-load condition before the faults occur, as shown in Fig. 15(a)–(c). From Fig. 15, the post-fault voltages u_{oab} and u_{oca} are flat-topping

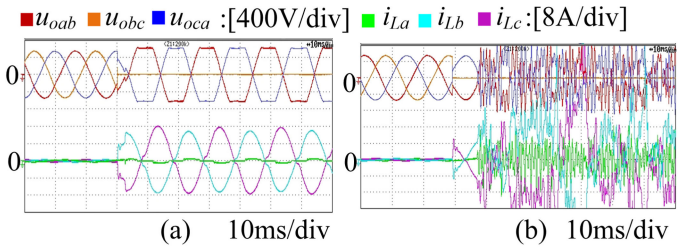

Fig. 16. Experimental results of the proposed current limiting strategy when the asymmetrical short-circuit fault occurs between phase b and c under no-load condition. (a) With $Z_{\text{vir}} = 100\ \Omega$. (b) With $Z_{\text{vir}} = 10\ \Omega$.

as the voltage limiting occurs under asymmetrical fault. Meanwhile, the currents of faulty phases, i_{Lb} and i_{Lc}, are distorted. In Fig. 15(a), the magnitudes of fundamental components of post-fault currents of phase b and c are 29.1 and 29.4 A, respectively, which are much larger than the magnitude of the current limiting reference (17 A). From Fig. 15(b) and (c), the magnitudes of post-fault currents of phase b and c are also larger than the magnitude of current limiting reference. It can be seen that when the current limiting strategy without parallel virtual impedance is adopted, the currents of faulty phases are not fully controlled when asymmetrical short-circuit fault occurs. Moreover, the amplitudes of the fundamental component of faulty phase currents depend on the pre-fault load impedances. Under this current limiting strategy, the semiconductor switches are relatively prone to be damaged by the overcurrent due to the non-fully control of the short-circuit currents. At the same time, the non-fully control of the short-circuit currents will also make the rated current setting of the circuit breakers installed in load branches difficult.

B. Proposed Current Limiting Strategy

Figs. 16 and 17 show the experimental results under the proposed current limiting strategy when short-circuit fault occurs between phase b and c. For comprehensively verifying the proposed current limiting strategy, the experiments are carried out with different values of Z_{vir}. When $Z_{\text{vir}} = 100\ \Omega$, it is seen from Fig. 16(a) that the voltage limiting still exists, which is in consistent with the analysis in Section IV-B. However, when $Z_{\text{vir}} = 10\ \Omega$, it can be observed from Fig. 16(b) the system become unstable, which is also in consistent with the analysis in Section IV-B. Furthermore, the experimental results with $Z_{\text{vir}} = 66.2\ \Omega$ (the recommended value of Z_{vir} in Section IV-B) are shown in Fig. 17. Meanwhile, three cases are respectively carried out when the TPTL inverter operates under no-load condition, half-load condition, and rated-load condition before the asymmetrical short-circuit fault between phase b and c occurs, respectively. It can be observed that the voltage limiting does not occur when asymmetrical fault occurs between phase b and c, as shown in Fig. 17(a)–(c). Besides, the waveforms of the faulty phase currents, i_{Lb} and i_{Lc}, are approximately sinusoidal. Moreover, the magnitudes of the fault phase currents are almost constant and vary only in a small range, i.e., [14.72 A, 15.03 A] (corresponding to $[0.866 I_{L\_\text{limit}}, 0.884 I_{L\_\text{limit}}]$) while the loads change from the no-load condition to

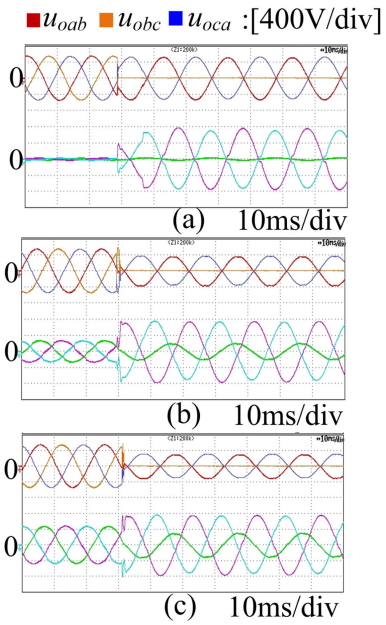

Fig. 17. Experimental results of the proposed current limiting strategy when asymmetrical short-circuit fault occurs between phase b and c with $Z_{vir} = 66.2\ \Omega$. (a) Under no-load condition. (b) Under half-load condition. (c) Under rated-load condition.

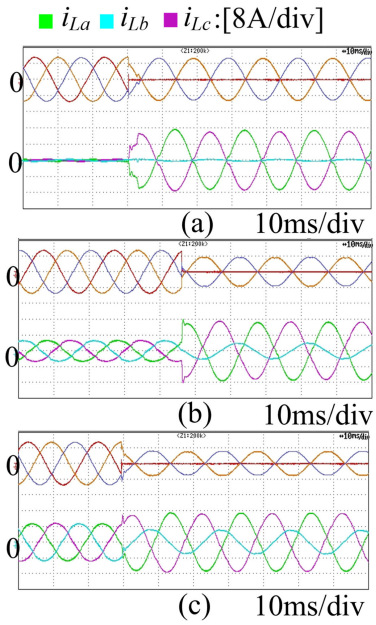

Fig. 18. Experimental results of the proposed current limiting strategy when asymmetrical short-circuit fault occurs between phase a and b with $Z_{vir} = 66.2\ \Omega$. (a) Under no-load condition. (b) Under half-load condition. (c) Under rated-load condition.

rated-load condition, which is in consistent with the analysis in Section V. Under short-circuit fault, the output voltages depend on the inductor currents and load impedance. Therefore, when the load impedance become small (from no load to half load and to rated load), the amplitudes of the u_{oab} and u_{oca} become smaller after fault as shown in Fig. 17(b) and (c).

In order to comprehensively verify the proposed current limiting strategy, the experimental results under asymmetrical short-circuit fault occurs between phase a and b, are also given, as shown in Fig. 18. It can be observed from Fig. 18 that the same conclusions can be obtained, comparing with short-circuit fault that occurs between phase b and c.

It can be seen from the experimental results that the proposed current limiting strategy can effectively limit the short-circuit currents under asymmetrical faults, and at the same time, the theoretical analysis is also in consistent with the experimental results.

VII. Conclusion

TPTL inverter is widely applied in various occasions. The inverters are usually switched to CCM from VCM to limit the fault currents when short-circuit faults happen. However, the voltage limiting may occur under asymmetrical fault. As a result, the currents are distorted and not completely controlled. In the paper, the current limiting strategy with the virtual impedance in parallel with the output filter capacitor is proposed. On the one hand, the voltage limiting can be avoided under symmetrical fault. On the other hand, the magnitudes of currents of faults phases can be effectively controlled and only vary in a very small range. Therefore, the proposed current limiting strategy is beneficial for the setting and reliable action of the protection devices. In addition, this proposed method does not need to identify the fault phase and healthy phase, and is easily implemented. The experimental results validate the effectiveness of the proposed current limiting strategy.

TABLE II
Fault Types and Current Limiting References

Current limiting references	three phase fault	$\begin{cases} i^*_{La\_limit} = I_{L\_limit}\cos(\omega t - \varphi_a) \\ i^*_{Lb\_limit} = I_{L\_limit}\cos(\omega t - \varphi_a - 120°) \\ i^*_{Lc\_limit} = I_{L\_limit}\cos(\omega t - \varphi_a + 120°) \end{cases}$
	phase-phase fault	
	phase a to phase b fault	$\begin{cases} i^*_{La\_limit} = 0 \\ i^*_{Lb\_limit} = I_{L\_limit}\cos(\omega t - \varphi_i) \\ i^*_{Lc\_limit} = -I_{L\_limit}\cos(\omega t - \varphi_i) \end{cases}$
	phase b to phase c fault	$\begin{cases} i^*_{La\_limit} = I_{L\_limit}\cos(\omega t - \varphi_i) \\ i^*_{Lb\_limit} = -I_{L\_limit}\cos(\omega t - \varphi_i) \\ i^*_{Lc\_limit} = 0 \end{cases}$
	phase c to phase a fault	$\begin{cases} i^*_{La\_limit} = I_{L\_limit}\cos(\omega t - \varphi_i) \\ i^*_{Lb\_limit} = 0 \\ i^*_{Lc\_limit} = -I_{L\_limit}\cos(\omega t - \varphi_i) \end{cases}$

Appendix

Table II gives the current limiting references for the control strategy proposed in [20] under different types of short-circuit faults. From Table II, there are four types of current limiting references due to four types of short-circuit faults.

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