Stability Issue of Cascaded Systems With Consideration of Switching Ripple Interaction

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***Abstract*—Impedance-based criteria are often used for assessing the stability of cascaded converter systems. In this paper, it is pointed out that the switching ripple interaction (SRI) between the source converter and the load converter in a cascaded system would change the gain of the pulsewidth modulation of the source converter, causing the cut-off frequency and the phase margin of the source converter to change accordingly. Thus, even if a cascaded system is shown to be stable under an impedance-based criterion, it can, in fact, be unstable due to the SRI. This paper proposes an adaptive modulation sample-and-hold method for eliminating the effect of the SRI. A 48 V–12 V–5 V cascaded system consisting of two buck converters is tested for verification.**

***Index Terms*—Adaptive, cascaded system, sample-and-hold, stability issue, switching ripple interaction (SRI).**

I. Introduction

DUE to high efficiency, high power density, and high reliability, dc distributed power systems (DPSs) have been widely applied in power generation and delivery applications, including renewable energy generation systems [1]–[3], aircraft with increased utilization of electric power (commonly called more electric aircraft) [4], electric vehicles [5], and so on. In a dc DPS, cascade connection is the main connection style, as shown in Fig. 1, where the front-end converter is called the source converter, and the downstream converter is called the load converter.

Despite the stable operation of the source converter and load converter when working individually, the cascaded system constructed may still be unstable [6]. To assess the stability of a cascaded system, we may directly analyze the whole system treating it as a single converter system. However, since the cascaded system is usually a high-order system, such direct analysis is relatively complex and does not provide much physical insight. Middlebrook [7] first proposed the impedance-based analysis method for stability assessment of cascaded systems. Essentially, the ratio of the output impedance of the source converter Z_{o_s} and the input impedance of the load converter Z_{in_l}, i.e., Z_{o_s}/Z_{in_l}, can be equivalently identified as the minor loop gain of the cascaded system. It has been shown that the cascaded system is stable if both the source converter and load converter are stable individually, and meanwhile, Z_{o_s}/Z_{in_l} meets the Nyquist criterion. This is commonly referred to as Middlebrook impedance-based stability criterion, which has been widely applied in the design of input filters for switching-mode power supplies [8]–[10] and other voltage-source cascaded systems [11]–[13]. For current-source systems, such as the grid-connected inverter, the minor loop gain becomes Z_{in_l}/Z_{o_s} [14], [15]. To assess the stability of more complicated DPSs containing an assembly of voltage-source, current-source converters and bi-directional converters, a generalized stability criterion for a dc DPS is proposed, where all the subsystems are classified by their terminal properties [16]. Based on these criteria, a number of control schemes based on shaping the input and output impedances of the subsystems have been presented to improve the system stability [17]–[22].

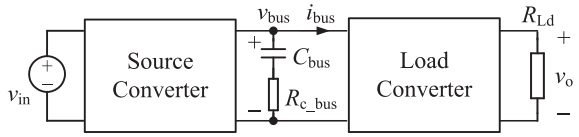

Fig. 1. Typical structure of the cascaded system.

It should be noted that, in assessing the stability of a DPS, the precondition involving the use of the criteria is that all the subsystems should be stable when operating individually. The source converter and load converter are often assumed to have no interactions when assessing the stability of the individual subsystems. However, the switching ripple components of the cascaded subsystems would interact via the intermediate bus port. To be specific, the load current of the source converter is determined by the input current of the load converter. Hence, the load current of the source converter contains not only the dc component but also the switching ripple of the load converter. Similarly, the input voltage of the load converter is determined by the output voltage of the source converter, and it contains not only the dc component but also the switching ripple of the source

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converter. This interaction would affect the performance of the cascaded system under some circumstances. One of the most well-known problems is the beat frequency oscillation in cascaded systems, where the oscillation frequency is determined by the difference between the switching frequencies of the source converter and load converter [23]–[25]. In this paper, an unstable phenomenon caused by the switching ripple interaction (SRI) in cascaded systems is discovered and analyzed. This phenomenon exists regardless of whether the switching frequencies are the same or not. It is found that the SRI would increase the switching ripple of the subsystems, which would further affect their stability. In other words, although both the source converter and load converter are designed to be stable individually, they may still be unstable when cascaded together, and eventually, the whole system would become unstable even if Z_{o_s}/Z_{in_l} meets the Nyquist criterion. Therefore, to evaluate the stability of the cascaded system more accurately, the subsystems have to be stable under the influence of the SRI.

Average models are widely adopted in analyzing the stability of the source converter and load converter [26]–[28]. However, two assumptions are made when applying average models [29], namely, 1) the perturbation signal frequency is far below the switching frequency, and 2) the ripple amplitudes of the state variables and the modulation signal of the pulsewidth modulator are much lower than their dc respective components. Nevertheless, it is shown, in this paper, that the small switching ripple assumption may not be valid in the source converter or load converter when the SRI is considered, thereby invalidating the average models. In fact, the instability caused by the SRI is a fast-scale instability. So, in order to accurately analyze the stability of the subsystems, more accurate models are needed [30].

In the presence of the SRI, the source and load converters are coupled, leading to the instability of the cascaded system as well as increased analytical complexity. This is not desirable for the modular design of the dc DPS. For this reason, this paper proposes a method for suppressing the SRI of the subsystems so as to improve the stability of the cascaded system and to simplify the analysis of the cascaded system.

This paper is organized as follows. In Section II, the influence of the SRI on the source and load converters is investigated. Then, in Section III, the stability of the cascaded system with consideration of the SRI is analyzed by using the extended-frequency-range small-signal model of dc–dc converters [30]. In Section IV, an adaptive modulation sample-and-hold method is proposed to eliminate the SRI. To verify the theoretical analysis and the effectiveness of the proposed solution, experimental test of a 48 V–12 V–5 V cascaded system prototype consisting of two buck converters is provided in Section V. Finally, Section VI concludes this paper.

II. Switching Ripple Interaction in a Cascaded System

The circuit schematic diagrams of the source converter and the load converter are shown in Fig. 2. As shown in Fig. 2(a), the output voltage of the source converter is the intermediate bus voltage of the cascaded system v_{bus} and the load current is the intermediate bus current i_{bus}. This intermediate bus current

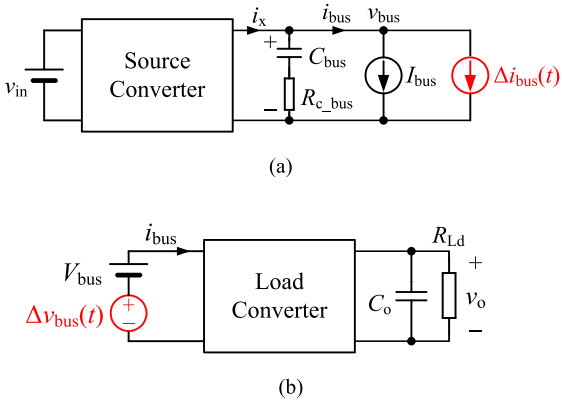

Fig. 2. Circuit schematic diagrams of subsystems in the cascaded system. (a) Source converter. (b) Load converter.

TABLE I
Parameters of the Source Converter

Parameters	Symbols	Values	Parameters	Symbols	Values
Input votlage	V_{in}	48 V	Output capacitance	C_{bus}	200 μF
Output voltage	V_{bus}	12 V	ESR	R_{c_bus}	10 mΩ
Output power	P_{o_s}	50 W	Amplitude of carrier	V_{m_s}	1.45 V
Switching frequency	f_{s_s}	100 kHz	Voltage feedback factor	H_{v_s}	0.12
Inductance	L_s	108 μH			

comprises a dc component I_{bus} and an ac component $\Delta i_{bus}(t)$ caused by the switching ripple of the load converter. As illustrated in Fig. 2(b), the input voltage of the load converter is the intermediate bus voltage of the cascaded system v_{bus}, which comprises a dc component V_{bus} and an ac component $\Delta v_{bus}(t)$ caused by the switching ripple of the source converter. In Fig. 2, it can be seen that the switching ripples from the source and load converters will interact at the intermediate bus port, resulting in the SRI of the source and load converters. Usually, the stability of the source converter and load converter is analyzed without considering the SRI, i.e., with $\Delta v_{bus}(t)$ and $\Delta i_{bus}(t)$ discarded.

As seen in Fig. 2(a), the input current of the load converter is the origin of $\Delta i_{bus}(t)$ in the source converter. When $\Delta i_{bus}(t)$ flows through the output filter capacitor of the source converter C_{bus}, the switching ripple in v_{bus} will change. If the input current of the load converter is continuous, as in the case of a boost converter, Δi_{bus} is smaller than I_{bus}. Therefore, the impact on the switching ripple of v_{bus} is small. However, if the input current of the load converter is discontinuous, as in the case of buck and buck–boost converters, Δi_{bus} is quite large, and may even exceed the value of I_{bus}. The impact on the switching ripple of v_{bus} is large. After the switching ripple component of v_{bus} passes through the feedback compensation circuit of the source converter, it will further affect the switching ripple component in the modulation signal of the source converter.

A buck converter is adopted as the source converter in the cascaded system, and the main parameters are given in Table I.

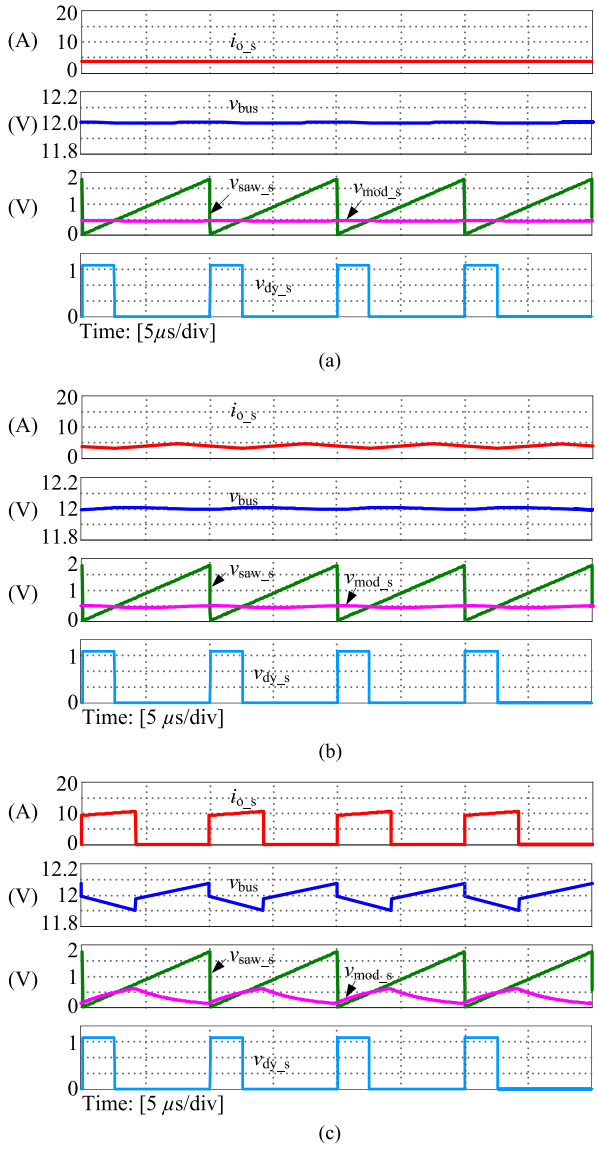

Fig. 3. Key waveforms of the source converter. (a) Operating independently. (b) After cascading with the load converter having a continuous input current load converter. (c) After cascading with the load converter having a discontinuous input current converter.

The transfer function of the voltage regulator of the source converter is designed as

$$G_{c\_s0}(s) = \frac{12\,430\left(1+\frac{s}{9000}\right)\left(1+\frac{s}{11\,000}\right)}{s\left(1+\frac{s}{314\,000}\right)\left(1+\frac{s}{450\,000}\right)}. \quad (1)$$

Fig. 3 shows the simulated key waveforms of the source converter under three conditions, namely, operating independently, cascaded with a continuous input current load converter, and cascaded with a discontinuous input current load converter. As seen in Fig. 3(a), when operating independently, the output current of the source converter i_{o_s} is exactly the dc component I_{bus}, and the switching ripple of v_{bus} is very small. Thus, the corresponding switching ripple of the modulation signal v_{mod_s} is quite small compared to the peak-to-peak value of the carrier signal, and it can be neglected. As seen in Fig. 3(b), when the load converter has continuous input current, i_{o_s} contains the switching ripple of the input current of the load converter, resulting in a small increase of the ripple amplitude in v_{bus} and v_{mod_s}. As seen in Fig. 3(c), when the load converter has a discontinuous input current, the switching ripple in i_{o_s} increases sharply, resulting in a significant increase of the ripple amplitude in v_{bus} and v_{mod_s}. Therefore, the switching ripple of v_{mod_s} is no longer negligible compared with that of the carrier.

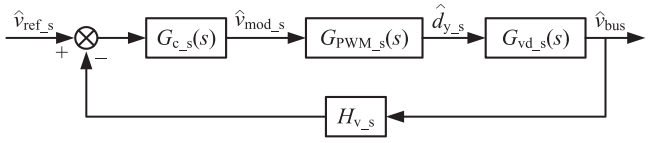

Fig. 4. Control block diagram of the source converter.

Similarly, the switching ripple of the source converter will be imposed on the input voltage of the load converter, resulting in a switching ripple Δv_{bus}, which causes the output voltage of the load converter v_o to fluctuate. However, since Δv_{bus} is usually much less than V_{bus}, and will mostly be filtered by the inherent inductor and capacitor of the load converter before reaching v_o, it can, therefore, be ignored. Thus, it suffices to consider the effect of the SRI on the source converter.

III. Effect of the Switching Ripple Interaction on the Cascaded System

A. Modeling and Analysis of the SRI and Stability of Cascaded Systems

Due to the existence of the SRI, the source converter in the cascaded system can be regarded as a voltage mode controlled system with a pulse load, which is a unique phenomenon in the cascaded system. The pulse load is part of the source converter and should be considered while modeling the converter.

As analyzed in Section II, the switching ripple amplitude of the modulation signal v_{mod_s} may be comparable to that of the carrier signal due to the SRI. Thus, the validity of the average model is questionable here, since it is applicable only when the ripple amplitude of the modulation signal is much smaller than the carrier signal. The extended-frequency-range small-signal model of dc–dc converters is proposed in [30], which is derived only with the small-signal assumption and takes the sideband effect and aliasing effect caused by the switching ripple components into account. This small-signal model is accurate up to the switching frequency and very effective in predicting a variety of instability issues, even if the ripple amplitude of v_{mod_s} is comparable to that of the carrier signal. So, this small-signal model is adopted here to describe the cascaded system with the SRI. Fig. 4 shows the control block diagram of the source converter based on the extended-frequency-range small-signal model, where $G_{c\_s}(s)$ is the transfer function of the voltage regulator, $G_{vd\_s}(s)$ is the transfer function of duty-cycle-to-output-voltage, H_{v_s} is the sense gain of the output voltage, and G_{PWM_s} is the transfer function of the pulsewidth modulation (PWM)

modulator. The expression of $G_{\text{PWM\_s}}$ is [30]

$$G_{\text{PWM\_s}}(s) = \frac{1}{V_{\text{m\_s}} - T_{\text{s\_s}} V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}}) + \sum_{k\neq 0}^{+\infty}_{k=-\infty} H_{\text{v\_s}} G_{\text{c\_s}}(s + jk\omega_{\text{s\_s}}) G_{\text{vd\_s}}(s + jk\omega_{\text{s\_s}})} \tag{2}$$

where $D_{\text{y\_s}}$ is the steady-state duty cycle of the source converter, $T_{\text{s\_s}}$ is the switching period of the source converter, $\omega_{\text{s\_s}}$ is the angular frequency of the carrier, and $V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}})$ is the slope of the steady-state modulation signal $V_{\text{mod\_s}}(t)$ at $D_{\text{y\_s}} T_{\text{s\_s}}$. The infinite series $\sum_{k\neq 0}^{+\infty}_{k=-\infty} H_{\text{v\_s}} G_{\text{c\_s}}(s + jk\omega_{\text{s\_s}}) G_{\text{vd\_s}}(s + jk\omega_{\text{s\_s}})$ describes the sideband effect and aliasing effect on $G_{\text{PWM\_s}}(s)$. This is equivalent to introducing poles to the loop, resulting in a phase delay of $G_{\text{PWM\_s}}(s)$ [30].

According to Fig. 4 and (2), the complete loop gain expression of the source converter with the SRI is derived as

$$T_{\text{v\_s}}(s) = \frac{H_{\text{v\_s}} G_{\text{c\_s}}(s) G_{\text{vd\_s}}(s)}{V_{\text{m\_s}} - T_{\text{s}} V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}}) + \sum_{k\neq 0}^{+\infty}_{k=-\infty} H_{\text{v\_s}} G_{\text{c\_s}}(s + jk\omega_{\text{s\_s}}) G_{\text{vd\_s}}(s + jk\omega_{\text{s\_s}})}. \tag{3}$$

Due to the SRI, $V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}})$ is affected by Δi_{bus} (the quantitative relationship between Δi_{bus} and $V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}})$ is derived in the Appendix), and $V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}})$ increases with the magnitude of Δi_{bus}, as shown in Fig. 3. Specifically, if $V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}}) > 0, V_{\text{m\_s}} - T_{\text{s\_s}} V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}})$ becomes smaller. Hence, according to (3), the magnitude of the loop gain will increase, and also the effect of infinite series arises, and the phase delay will be more obvious [30], leading to a smaller phase margin and hence a less stable or unstable system.

$G_{\text{vd\_s}}(s)$ of the source converter (a buck converter with parameters listed in Table I) is given by [26]

$$G_{\text{vd\_s}}(s) = \frac{V_{\text{in}}(1 + sC_{\text{bus}} R_{\text{c\_bus}})}{s^2 L_{\text{s}} C_{\text{bus}} + sC_{\text{bus}} R_{\text{c\_bus}} + 1}. \tag{4}$$

Setting the cut-off frequency of the independently operated source converter $f_{\text{c\_s}}$ as 5.5 kHz and the phase margin PM_{s} as 45°, the voltage regulator $G_{c\,s}(s)$ can be designed with a type-III network, expressed as

$$G_{\text{c\_s}}(s) = \frac{19\,057\left(1 + \frac{s}{9690}\right)\left(1 + \frac{s}{11\,000}\right)}{s\left(1 + \frac{s}{333\,330}\right)\left(1 + \frac{s}{426\,360}\right)}. \tag{5}$$

As discussed in Section II, the effect of the SRI is most obvious when the input current of the load converter is discontinuous. Therefore, a buck converter is adopted as the load converter with the parameters given in Table II in order to investigate the effect of the SRI on the stability of the cascaded system.

Fig. 5 shows the Bode plots of the source converter loop gain $T_{\text{vs}}(s)$ before and after considering the SRI. As seen, the cut-off frequency and phase margin are consistent with the design indicators without considering the SRI, and therefore, the source converter is stable when operated independently. However, $f_{\text{c\_s}}$ becomes 57 kHz and PM_{s} becomes $-60°$ when the

TABLE II
PARAMETERS OF THE LOAD CONVERTER

Parameters	Symbols	Values	Parameters	Symbols	Values
Input voltage	V_{bus}	12 V	Output capacitance	C_{o}	120 μF
Output voltage	V_{o}	5 V	ESR	$R_{\text{c\_l}}$	5 mΩ
Output power	$P_{\text{o\_l}}$	50 W	Amplitude of carrier	$V_{\text{m\_l}}$	1.45 V
Switching frequency	$f_{\text{s\_l}}$	100 kHz	Voltage feedback factor	$H_{\text{v\_l}}$	0.12
Inductance	L_{l}	22 μH			

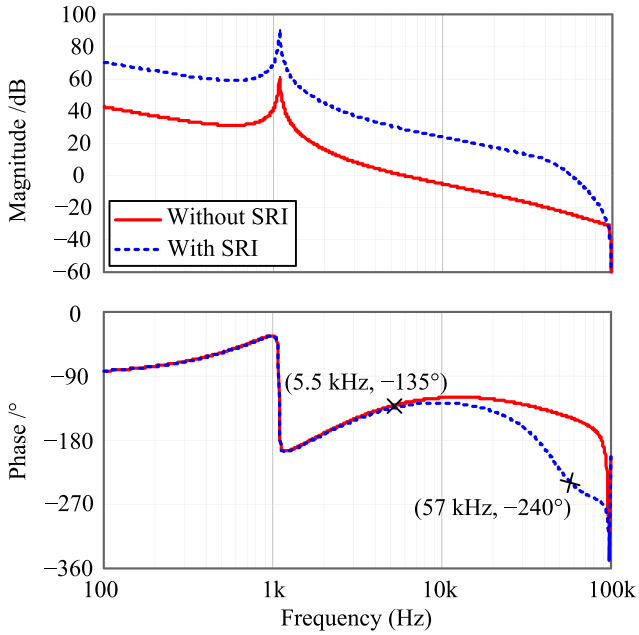

Fig. 5. Bode diagrams of the source converter loop gain with and without the switching ripple interaction.

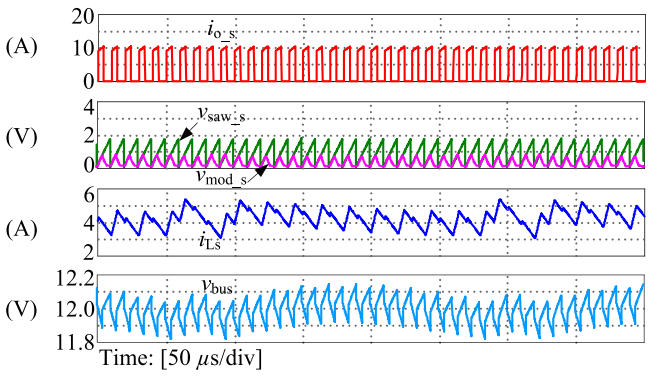

Fig. 6. Key waveforms of the source converter with the switching ripple interaction when the controller is $G_{\text{c\_s}}(s)$.

SRI is taken into account, indicating that the converter is no longer stable. The simulated waveforms of the source converter after considering the SRI are shown in Fig. 6. It can be observed that both the inductor current i_{Ls} and the output voltage v_{bus} oscillate. Compared with i_{Ls}, the oscillation amplitude of v_{bus}

is weak. This is because the high-frequency oscillation in i_{Ls} is well attenuated when it flows through the large bus capacitor, leading to a low amplitude oscillation in v_{bus}. It should be noted that if the pulse load current in $i_{\text{o\_s}}$ is regarded as a noise, the low amplitude oscillation in v_{bus} might be similar even though the system is stable. The stability should be distinguished from the noise. In our understanding, only Period-1 operation represents the stability of the converter and is the desired operation when developing a power supply, while other operating regimes, such as Hopf bifurcation, border collision, period-n operation ($n = 2, 4, 8, \ldots$) are all unstable even if the oscillation is very weak. Essentially speaking, the stability can ultimately be determined by the loop gain as long as it is accurate enough. From the Bode plot of the loop gain, the phase margin corresponding to any unstable operation is below zero (assume there is no right-half-plane pole in the loop gain). Considering the phase margin is $-60°$ here, the source converter with the SRI is indeed unstable although the amplitude of the oscillation is weak.

Based on the analysis mentioned above, it is interesting to see that even if the source converter is stable when assessed separately, it might, in fact, be unstable due to the SRI. This clearly implies possible errors in stability assessment of the cascaded system. The voltage regulator of the load converter $G_{\text{c\_l}}(s)$ is designed as

$$G_{\text{c\_l}}(s) = \frac{24\,873\left(1+\frac{s}{10\,000}\right)\left(1+\frac{s}{15000}\right)}{s\left(1+\frac{s}{180\,000}\right)\left(1+\frac{s}{200\,000}\right)}. \tag{6}$$

The expression of the loop gain of the load converter $T_{\text{v\_l}}(s)$ is obtained as

$$T_{\text{v\_l}}(s) = \frac{H_{\text{v\_l}}G_{\text{vr\_l}}(s)G_{\text{vd\_l}}(s)}{V_{\text{m\_l}} - T_{\text{s\_l}}V'_{\text{mod\_l}}(D_{\text{y\_l}}T_{\text{s\_l}}) + \sum_{\substack{k=-\infty \\ k\neq 0}}^{+\infty} H_{\text{v\_l}}G_{\text{vr\_l}}(s+jk\omega_{\text{s\_l}})G_{\text{vd\_l}}(s+jk\omega_{\text{s\_l}})}. \tag{7}$$

Fig. 7 shows the Bode diagrams of $T_{\text{v\_l}}(s)$, showing that the cut-off frequency and the phase margin satisfy the design objectives. Fig. 8 shows the key waveforms of the load converter when operated separately, which is stable as designed.

Fig. 9 shows the simulated waveforms of the whole cascaded system, which are apparently unstable. This again shows that even though the source converter is found stable when operated independently, the effect of the SRI may render it unstable, leading to oscillation of the whole system. In other words, before applying the Middlebrook criterion to assess the stability of a cascaded system, we have to make sure that both the source converter and load converter are stable in the presence of the SRI.

B. Discussion of Effects of Parameters on the SRI

According to the aforementioned analysis, the effect of the SRI is determined by $V'_{\text{mod\_s}}(D_{\text{y\_s}}T_{\text{s\_s}})$, which is determined by Δi_{bus}. For a cascaded system where the input current of the load converter is continuous, Δi_{bus} is unaffected by the load condition, whereas in the case of the discontinuous input current, Δi_{bus} is closely related to the load condition, and the lighter the load, the smaller the Δi_{bus}, and thus, the stability of the system is improved. Fig. 10 shows the Bode diagrams of $T_{\text{v\_s}}(s)$ at

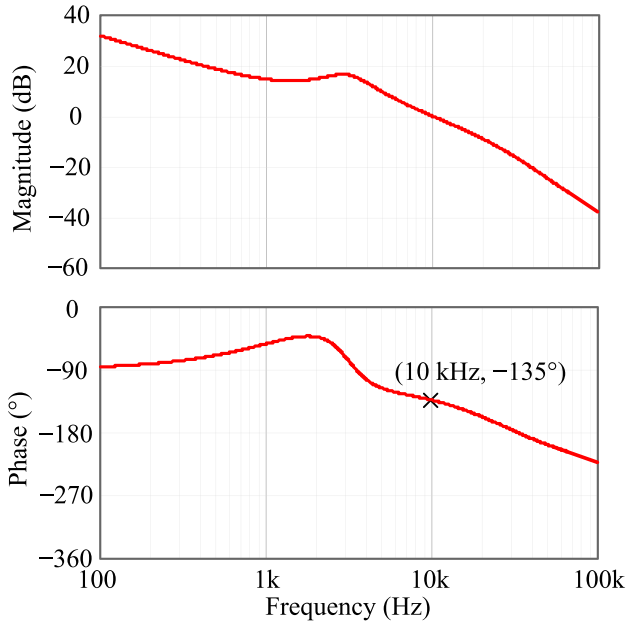

Fig. 7. Bode diagrams of the load converter loop gain.

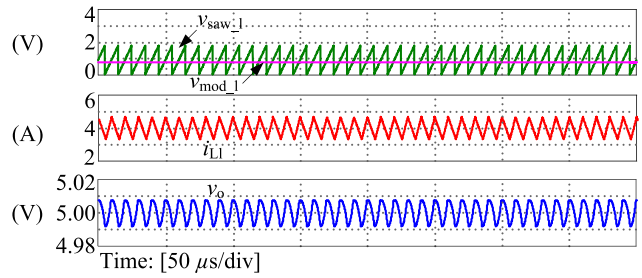

Fig. 8. Key waveforms of the load converter with $G_{\text{c\_l}}(s)$.

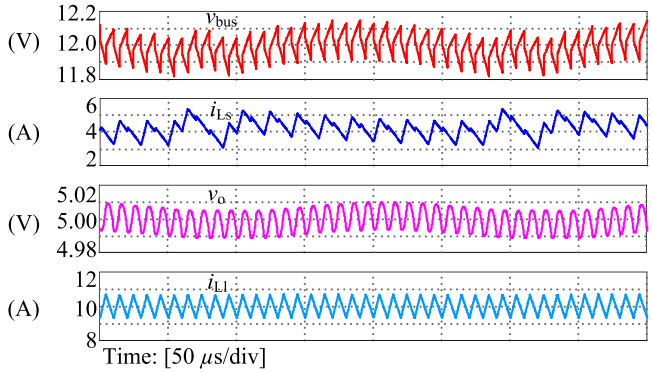

Fig. 9. Simulated waveforms of the cascaded system when the voltage regulators of the source and load converter are $G_{\text{c\_s}}(s)$ and $G_{\text{c\_l}}(s)$, respectively.

20% load and full load conditions. As seen, the phase margin increases and the stability is improved as the load becomes lighter.

Besides, since the impedance of the bus capacitor in the frequency domain decreases monotonically, the higher the switching frequency, the smaller the switching ripple in the bus voltage. Consequently, the stability of the system is improved. Fig. 11

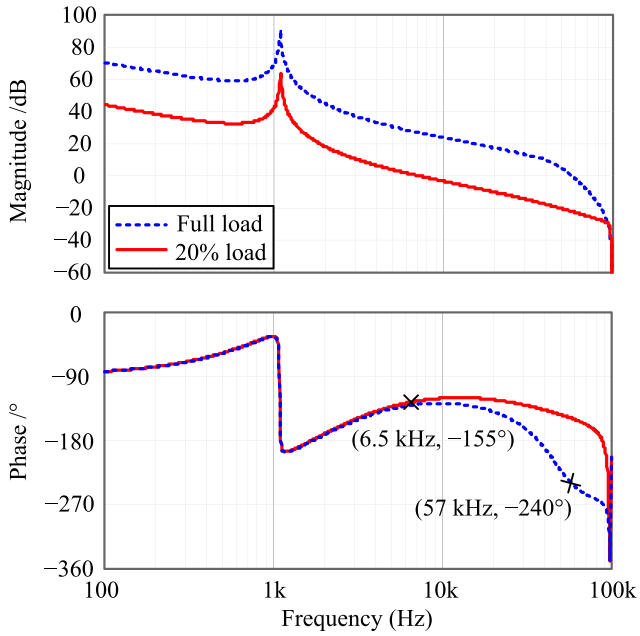

Fig. 10. Bode diagrams of the source converter loop gain with the SRI at different load conditions.

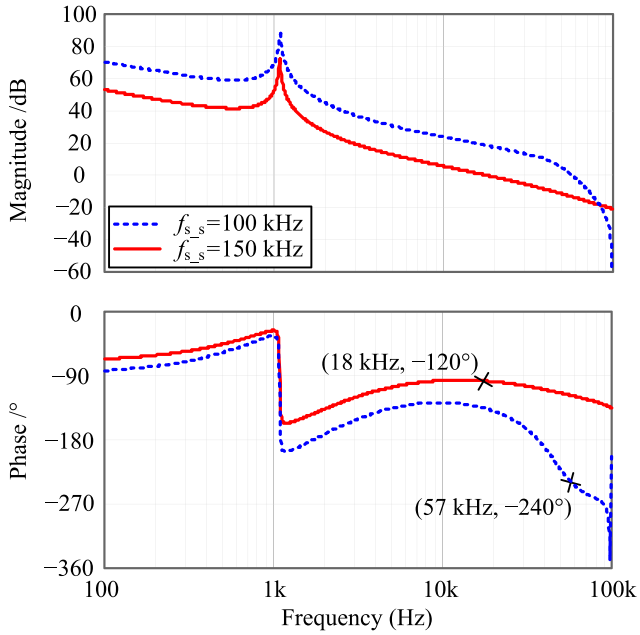

Fig. 11. Bode diagrams of the source converter loop gain with the SRI at different switching frequencies.

shows the Bode plots of $T_{v\_s}(s)$ with the switching frequency being 100 and 150 kHz, from which, it can be seen that the phase margin increases and the stability is improved as the switching frequency increases.

C. Comparison With the Middlebrook Criterion

The Middlebrook criterion is widely applied in stability judgment of cascaded systems. It has been shown that if both the source and the load converter are stable individually, the cascaded system is stable on the condition that the

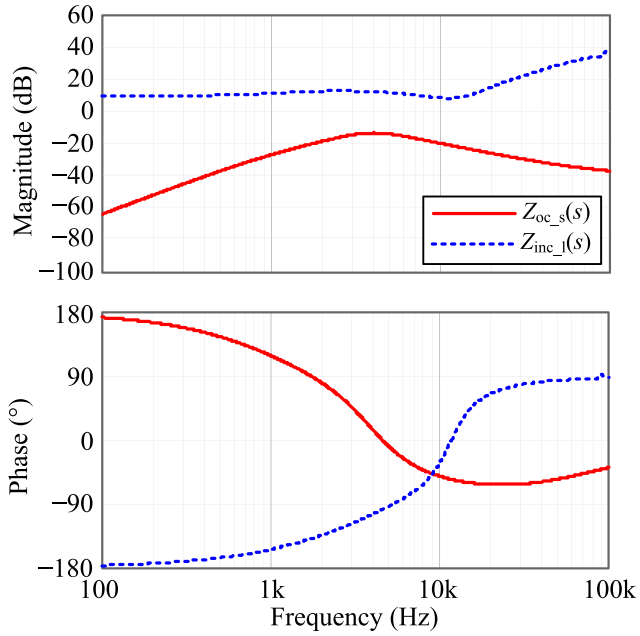

Fig. 12. Bode diagrams of $Z_{oc\_s}(s)$ and $Z_{inc\_l}(s)$ of the cascaded system.

ratio of the source converter's closed-loop output impedance $Z_{oc\_s}(s)$ and the load converter's closed-loop input impedance $Z_{inc\_l}(s)$, $Z_{oc\_s}(s)/Z_{inc\_l}(s)$, meets the Nyquist stability criterion. In the aforementioned cascaded system, the open-loop output impedance of the source converter is expressed as [31]

$$Z_{o\_s}(s) = \frac{sL_s + s^2 L_s C_s R_{c\_s}}{L_s C_s s^2 + R_{c\_s} C_s s + 1}. \tag{8}$$

The open-loop input impedance of the load converter is expressed as

$$Z_{in\_l}(s) = \frac{R_{Ld}}{D_{y\_l}^2} \frac{L_l C_{o\_l} s^2 + \left(R_{c\_l} C_{o\_l} + \frac{L_l}{R_{Ld}}\right) s + 1}{1 + R_{Ld} C_{o\_l} s}. \tag{9}$$

The closed-loop output impedances of the source converter and input impedance of the load converter are, respectively, expressed as

$$Z_{oc\_s}(s) = \frac{Z_{o\_s}(s)}{1 + T_{v\_s}(s)} \tag{10}$$

$$Z_{inc\_l}(s) = \frac{1}{-\frac{D_{y\_l}^2}{R_{Ld}} \frac{T_{v\_l}(s)}{1+T_{v\_l}(s)} + \frac{1}{Z_{in\_l}(s)} \frac{1}{1+T_{v\_l}(s)}}. \tag{11}$$

Fig. 12 shows the Bode plots of $Z_{oc\_s}(s)$ and $Z_{inc\_l}(s)$, where it is observed that $Z_{oc\_s}(s)$ does not intersect $Z_{inc\_l}(s)$ in the entire frequency range, meaning that the cascaded system should be stable according to the Middlebrook criterion. This is inconsistent with the simulated results. As a conclusion, to assess the stability of a cascaded system correctly, the effect of the SRI has to be considered before applying the Middlebrook criterion directly.

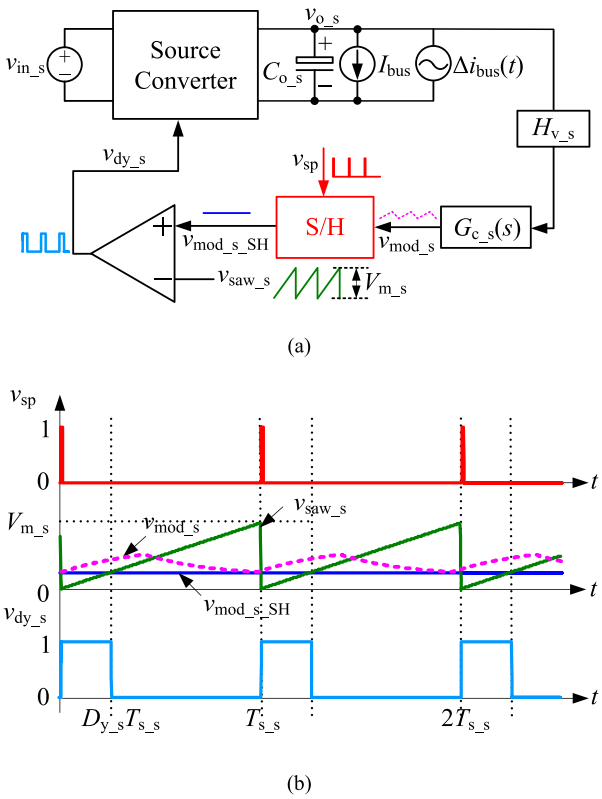

Fig. 13. Control scheme diagram and key waveforms of the modulation signal sample-and-hold method. (a) Control scheme diagram. (b) Key waveforms.

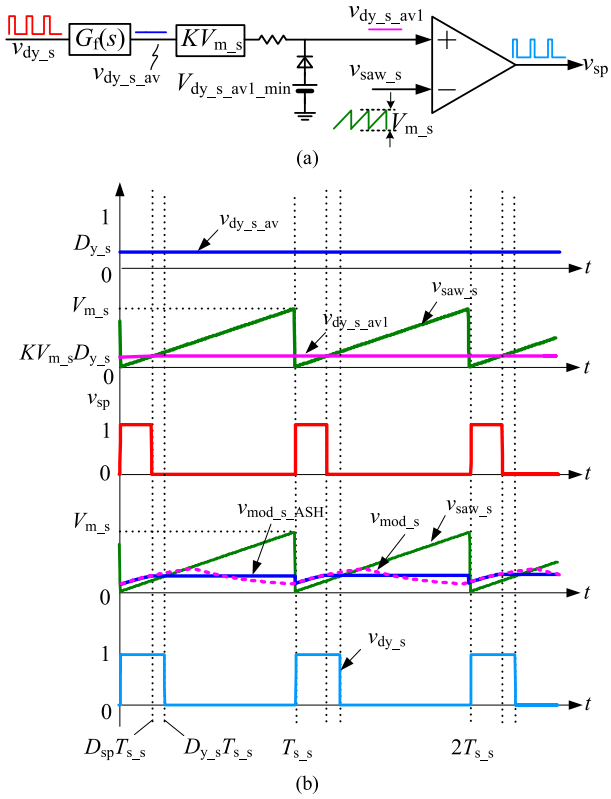

Fig. 14. Adaptive sampling pulse regulation strategy. (a) Control scheme diagram. (b) Key waveforms.

IV. Adaptive Modulation Signal Sample-and-Hold Method to Eliminate the SRI

The SRI is a kind of coupling effect between the source converter and the load converter, which greatly complicates the analysis and design of the source converter. It is, thus, necessary to decouple the source and load converters in order to eliminate the impact of the SRI. Lowering the cut-off frequency of the source converter is a simple and effective method to attenuate the switching ripple of the modulation signal. However, this method degrades the dynamic performance of the source converter and increases the output impedance of the source converter, resulting in significant loading effect in the cascaded system, which can lead to instability of the cascaded system. For this purpose, this paper presents an adaptive modulation signal sample-and-hold method for eliminating the SRI between the source converter and the load converter.

According to (3), if $V'_{\text{mod\,s}}(D_{\text{ys}}T_{\text{s\_s}})$ stays zero, then the model of the PWM modulator will be independent of Δi_{bus}, and the influence of the SRI can be completely suppressed. This can be implemented by introducing a sample-and-hold circuit at the output of the voltage regulator. After sampled and held by the zero-order holder, the new modulation signal is flat and contains no switching ripple. The duty cycle is generated by the new modulation signal intersecting the carrier wave. This method is called the modulation signal sample-and-hold method. Fig. 13 shows the control scheme diagram and key waveforms of the modulation signal sample-and-hold method, where v_{sp} is the sampling pulse with the sampling time set at the beginning of every switching period, $v_{\text{mod\_s\_SH}}$ is the new modulation signal, that is flat as analyzed, and obviously $V_{\text{mod\,s\_SH}}(D_{\text{ys}}T_{\text{s\_s}})$ is zero.

$v_{\text{mod\_s}}(t)$ is sampled at $nT_{\text{s\_s}}$ $(n = 0, 1, 2, \ldots)$, and then remains unchanged until intersecting the carrier wave at $nT_{\text{s\_s}} + D_{\text{y\_s}}T_{\text{s\_s}}$. Therefore, the modulation signal sample-and-hold method would introduce a delay of $D_{\text{y\_s}}T_{\text{s\_s}}$ [32], which will reduce the phase margin of the source converter, jeopardizing its stability. To eliminate the delay, the sampling pulses should be set at $nT_{\text{s\_s}} + D_{\text{y\_s}}T_{\text{s\_s}}$. For this reason, we propose an adaptive modulation signal sample-and-hold method, where the sampling pulse moves adaptively with the value of the duty cycle. The adaptive regulation circuit of the sampling pulse and the corresponding key waveforms are illustrated in Fig. 14. The operating principle is as follows. First, the duty-cycle signal $v_{\text{dy\_s}}$ is filtered by a low-pass filter, generating an average value of the duty-cycle signal, i.e., $v_{\text{dy\_s\_av}} = D_{\text{y\_s}}$. Magnifying $v_{\text{dy\_s\_av}}$ by the factor of $KV_{\text{m\_s}}$, we have $v_{\text{dy\_s\_av1}} = KV_{\text{m\_s}}D_{\text{y\_s}}$, which is then compared with the carrier wave of the source converter to generate the sampling pulse v_{sp}. Considering the amplitude of the carrier wave is $V_{\text{m\_s}}$, the pulsewidth of v_{sp}, denoted as D_{sp}, equals to $KD_{\text{y\_s}}$. When $K = 1$, D_{sp} is exactly the same as $D_{\text{y\_s}}$. In this case, since the sample-and-hold circuit keeps sampling when v_{sp} is at a high level, the final result held is the value of $v_{\text{mod\_s}}$ at $nT_{\text{s\_s}} + D_{\text{y\_s}}T_{\text{s\_s}}$, i.e., the sampling pulse is adaptively adjusted to the interaction instant. The real modulation signal after adaptive sampling and holding is named $v_{\text{mod\_s\_ASH}}$. In practice, to guarantee the slope of $v_{\text{mod\_s\_ASH}}$ at $nT_{\text{s\_s}} + D_{\text{y\_s}}T_{\text{s\_s}}$ is zero, the sampling time should be set

slightly earlier to $nT_{\text{s\_s}} + D_{\text{y\_s}}T_{\text{s\_s}}$, i.e., $K < 1$, and $D_{\text{sp}} < D_{\text{y\_s}}$, as shown in Fig. 14(b). In Fig. 14(b), it is found that $v_{\text{mod\_s\_ASH}}$ is exactly the same as $v_{\text{mod\_s}}$ before $nT_{\text{s\_s}} + D_{\text{sp}}T_{\text{s\_s}}$, but becomes flat when approaching $nT_{\text{s\_s}} + D_{\text{sp}}T_{\text{s\_s}}$, and remains unchanged until the next switching period. Therefore, this method not only completely suppresses the SRI but also eliminates the $D_{\text{y\_s}}T_{\text{s\_s}}$ delay. Besides, in order to guarantee that sampling and holding can be realized every switching period in all circumstances, $V_{\text{dy\_s\_av1\_min}}$ is introduced as the lower limit of $v_{\text{dy\_s\_av1}}$ to restrict the minimum pulsewidth of v_{sp}, as shown in Fig. 14(a).

In the adaptive sample-and-hold modulation method, $v_{\text{dy\_s}}$ is filtered, magnified, and modulated to generate v_{sp}, and v_{sp} is the control signal of the sample-and-hold circuit to generate $v_{\text{dy\_s}}$. In this process, a new closed loop is introduced into the original source converter. The following is to derive the loop gain with the consideration of the new loop.

In every switching period, the modulation signal $v_{\text{mod\_s\_ASH}}$ intersects with the carrier signal $v_{\text{saw\_s}}$ once. The intersection instant in the *n*th cycle is $(n-1)T_{\text{s}} + d_{\text{y\_s}}T_{\text{s}}$. At the intersection instant, $v_{\text{mod\_s\_ASH}}$ is equal to $v_{\text{saw\_s}}$, i.e.,

$$\begin{aligned} &v_{\text{mod\_s\_ASH}}[(n-1)T_{\text{s\_s}} + d_{\text{y\_s}}T_{\text{s\_s}}] \\ &\quad = v_{\text{saw\_s}}[(n-1)T_{\text{s\_s}} + d_{\text{y\_s}}T_{\text{s\_s}}]. \end{aligned} \tag{12}$$

In Fig. 14(b), $v_{\text{mod\_s\_ASH}}$ at the intersection instant is the same as $v_{\text{mod\_s}}$ at the sampling instant. Since the sampling instant is $(n-1)T_{\text{s\_s}} + d_{\text{sp}}T_{\text{s\_s}}$, we have

$$\begin{aligned} &v_{\text{mod\_s\_ASH}}[(n-1)T_{\text{s\_s}} + d_{\text{y\_s}}T_{\text{s\_s}}] \\ &\quad = v_{\text{mod\_s}}[(n-1)T_{\text{s\_s}} + d_{\text{sp}}T_{\text{s\_s}}]. \end{aligned} \tag{13}$$

Substituting (13) into (12) leads to

$$\begin{aligned} &v_{\text{mod\_s}}[(n-1)T_{\text{s\_s}} + d_{\text{sp}}T_{\text{s\_s}}] \\ &\quad = v_{\text{saw\_s}}[(n-1)T_{\text{s\_s}} + d_{\text{y\_s}}T_{\text{s\_s}}]. \end{aligned} \tag{14}$$

Imposing the small-signal perturbation into the system, the variables in (14) are composed of a steady-state part and a small-signal signal, i.e.,

$$v_{\text{mod\_s}}(t) = v_{\text{mod\_s}}(t) + \hat{v}_{\text{mod\_s}}(t) \tag{15a}$$

$$d_{\text{y\_s}} = D_{\text{y\_s}} + \hat{d}_{\text{y\_s}} \tag{15b}$$

$$d_{\text{sp}} = D_{\text{sp}} + \hat{d}_{\text{sp}}. \tag{15c}$$

Substitution of (15) into (14) leads to

$$\begin{aligned} &v_{\text{mod\_s}}[(n-1)T_{\text{s\_s}} + (D_{\text{sp}} + \hat{d}_{\text{sp}})T_{\text{s\_s}}] \\ &+ \hat{v}_{\text{mod\_s}}[(n-1)T_{\text{s\_s}} + (D_{\text{sp}} + \hat{d}_{\text{sp}})T_{\text{s\_s}}] \\ &= v_{\text{saw\_s}}[(n-1)T_{\text{s\_s}} + (D_{\text{y\_s}} + \hat{d}_{\text{y\_s}})T_{\text{s\_s}}]. \end{aligned} \tag{16}$$

By applying the Taylor series expansion to (16) and ignoring the high-order terms, (16) becomes

$$\begin{aligned} &v_{\text{mod\_s}}[(n-1+D_{\text{sp}})T_{\text{s\_s}}] + V'_{\text{mod\_s}}(D_{\text{sp}}T_{\text{s\_s}})\hat{d}_{\text{sp}}T_{\text{s\_s}} \\ &+ \hat{v}_{\text{mod\_s}}[(n-1+D_{\text{sp}})T_{\text{s\_s}}] \\ &= v_{\text{saw\_s}}[(n-1+D_{\text{y\_s}})T_{\text{s\_s}}] + \frac{V_{\text{m\_s}}}{T_{\text{s\_s}}}\hat{d}_{\text{y\_s}}T_{\text{s\_s}} \end{aligned} \tag{17}$$

where $V_{\text{mod\_s}}(D_{\text{sp}}T_{\text{s\_s}})$ is the gradient of $V_{\text{mod\_s}}(t)$ at $(n-1+D_{\text{sp}})T_{\text{s\_s}}$.

Eliminating the quiescent values on both sides of (17), the small-signal equation is obtained as

$$\begin{aligned} &V'_{\text{mod\_s}}(D_{\text{sp}}T_{\text{s\_s}})\hat{d}_{\text{sp}}T_{\text{s\_s}} + \hat{v}_{\text{mod\_s}}[(n-1+D_{\text{sp}})T_{\text{s\_s}}] \\ &= V_{\text{m\_s}}\hat{d}_{\text{y\_s}}. \end{aligned} \tag{18}$$

Considering d_{sp} is the periodical averaging of v_{sp}, $\hat{d}_{\text{sp}}$ can be replaced by $\hat{v}_{\text{sp}}$. Similarly, $\hat{d}_{\text{y\_s}}$ can be replaced by $\hat{v}_{\text{dy\_s}}$.

Based on (18), an approximate relationship in the s-domain among v_{sp}, $v_{\text{dy\_s}}$, and $v_{\text{mod\_s}}$ can be obtained as

$$V'_{\text{mod\_s}}(D_{\text{sp}}T_{\text{s\_s}})T_{\text{s\_s}}\hat{v}_{\text{sp}}(s) + \hat{v}_{\text{mod\_s}}(s) = V_{\text{m\_s}}\hat{v}_{\text{dy\_s}}(s). \tag{19}$$

In addition, assuming ω_{p} is the corner angular frequency of the first-order low-pass filter $G_{\text{f}}(s)$, we have

$$G_{\text{f}}(s) = \frac{\omega_{\text{p}}}{s + \omega_{\text{p}}}. \tag{20}$$

Since $v_{\text{dy\_s}}$ is filtered by $G_{\text{f}}(s)$ and magnified by $KV_{\text{m\_s}}$, and is then compared with the carrier wave to obtain v_{sp}, another small-signal relationship between $v_{\text{dy\_s}}$ and v_{sp} in the s-domain is

$$\hat{v}_{\text{sp}}(s) = \hat{v}_{\text{dy\_s}}(s)K\frac{\omega_{\text{p}}}{s + \omega_{\text{p}}}. \tag{21}$$

Substitution of (21) into (19), the transfer function from $v_{\text{mod\_s}}$ to $v_{\text{dy\_s}}$ with the consideration of the new loop is finally derived as

$$\frac{\hat{v}_{\text{dy\_s}}(s)}{\hat{v}_{\text{mod\_s}}(s)} = \frac{1}{V_{\text{m\_s}} - V'_{\text{mod\_s}}(D_{\text{sp}}T_{\text{s\_s}})T_{\text{s\_s}}K\frac{\omega_{\text{p}}}{s+\omega_{\text{p}}}}. \tag{22}$$

Based on (22) and the extended-frequency-range small-signal model in [30], the closed-loop transfer function $G_{\text{PWM\_s}}(s)$ of the PWM modulator in (2) becomes

$$G_{\text{PWM\_s}}(s) = \frac{\frac{V_{\text{m\_s}}}{V_{\text{m\_s}} - V'_{\text{mod\_s}}(D_{\text{sp}}T_{\text{s\_s}})T_{\text{s\_s}}K\frac{\omega_{\text{p}}}{s+\omega_{\text{p}}}}}{\frac{1}{V_{\text{m\_s}} + \sum_{\substack{k=-\infty \\ k\neq 0}}^{+\infty} H_{\text{v\_s}}G_{\text{c\_s}}(s+jk\omega_{\text{s\_s}})G_{\text{vd\_s}}(s+jk\omega_{\text{s\_s}})}}. \tag{23}$$

Then, the loop gain of the source converter is obtained as

$$T_{\text{v\_s\_ASH}}(s) = \frac{\frac{V_{\text{m\_s}}}{V_{\text{m\_s}} - V'_{\text{mod\_s}}(D_{\text{sp}}T_{\text{s\_s}})T_{\text{s\_s}}K\frac{\omega_{\text{p}}}{s+\omega_{\text{p}}}}}{\frac{H_{\text{v\_s}}G_{\text{c\_s}}(s)G_{\text{vd\_s}}(s)}{V_{\text{m\_s}} + \sum_{\substack{k=-\infty \\ k\neq 0}}^{+\infty} H_{\text{v\_s}}G_{\text{c\_s}}(s+jk\omega_{\text{s\_s}})G_{\text{vd\_s}}(s+jk\omega_{\text{s\_s}})}}. \tag{24}$$

As seen from (24), the corner frequency of the filter has an effect on the loop gain of the source converter. However, since ω_{p} is set far below $\omega_{\text{s\_s}}$, this effect is limited only to low frequencies. At frequencies much higher than ω_{p}, this effect is little. Thus, the loop gain at high frequencies could be approximated to

$$T_{\text{v\_s\_ASH}}(s) \approx \frac{H_{\text{v\_s}}G_{\text{c\_s}}(s)G_{\text{vd\_s}}(s)}{V_{\text{m\_s}} + \sum_{\substack{k=-\infty \\ k\neq 0}}^{+\infty} H_{\text{v\_s}}G_{\text{c\_s}}(s+jk\omega_{\text{s\_s}})G_{\text{vd\_s}}(s+jk\omega_{\text{s\_s}})}. \tag{25}$$

As seen from (25), the switching ripple of the modulation signal would not affect the loop anymore.

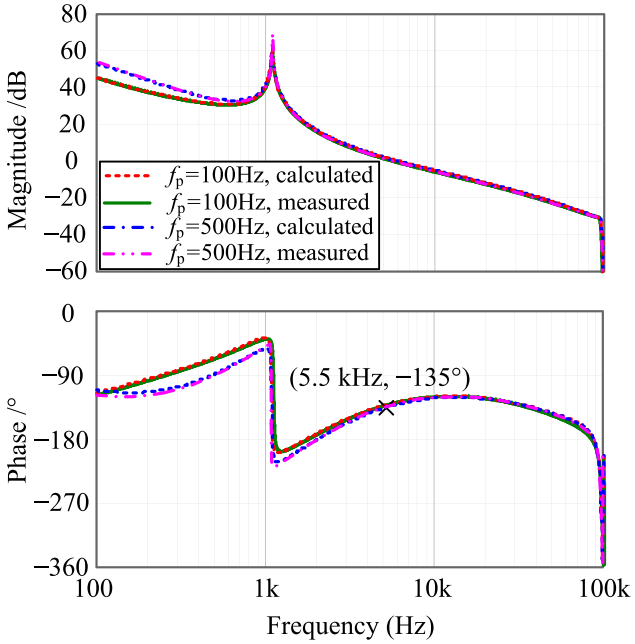

Fig. 15. Calculated and measured Bode diagrams of the source converter loop gain with the adaptive modulation signal sample-and-hold method.

Fig. 15 shows the calculated and measured Bode diagrams of $T_{v\_s\_ASH}(s)$ when the corner frequency of $G_f(s)$, f_p, is 100 and 500 Hz ($K = 0.7$ for both cases), respectively. Here, the measured results are obtained by Simplis software. As seen, the calculated loop gains in both cases coincide very well with the measurements, confirming the correctness of the model.

Obviously, it can be found in Fig. 15 that the loop gain is affected by the new loop introduced by the proposed method at low frequencies. At high frequencies, nevertheless, the loop gains in both cases are almost identical, leading to the same cutoff frequencies or phase margins. The phase margins are 45° in both cases, revealing the stability of the source converter and the cascaded system, which verifies the validity of the proposed method.

Figs. 16 and 17 show the transient simulation waveforms of the cascaded system controlled by the adaptive modulation signal sample-and-hold method in response to load step and input voltage step. In the transient process, the duty cycle varies from cycle to cycle and may reach zero. Therefore, the pulsewidth of the sampling pulse might be larger than the duty cycle in some switching periods. In this case, the modulation signal is not sampled and held before intersecting the carrier wave, and the control scheme becomes ineffective. After a short transient, the system reaches a new steady state, and the modulation signal is again sampled and held before intersecting the carrier wave adaptive to guarantee the stability of the system.

It should be noted that the proposed control method is implemented in the analog form. Since digital control ICs are inexpensive, highly versatile, and contain built-in zero-order holders, the SRI can be easily eliminated with digital control.

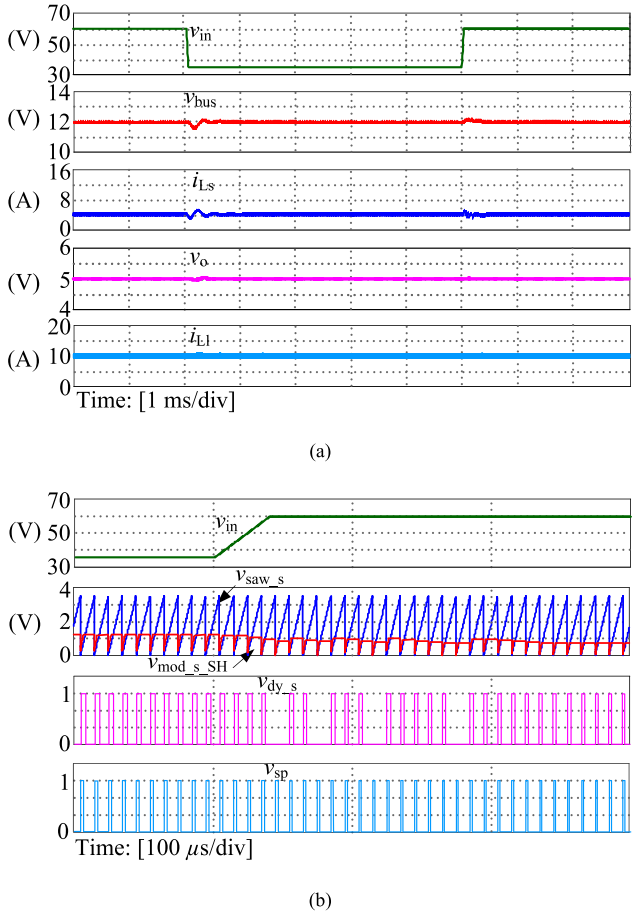

Fig. 16. Simulated transient waveforms of the cascaded system when the input voltage steps between 36 and 60 V. (a) Main circuit waveform. (b) Control circuit waveform of the source converter.

However, digital control will introduce an additional computational delay, which is equal to the switching period T_{s_s}. Thus, the total delay time reaches $(1 + D_{y\_s})T_{s\_s}$. This leads to a significant phase lag of the source converter, which narrows the bandwidth significantly. In contrast, analog control is free from the computational delay, and the $D_{y\_s}T_{s\_s}$ delay is also eliminated by the proposed control scheme, guaranteeing sufficient bandwidth of the closed-loop system.

V. Experimental Verification

To verify the effectiveness of the theoretical analysis, experimental measurements are taken from a cascaded system comprising two buck converters. Their circuit parameters are given in Tables I and II.

Fig. 18(a) and (b) shows the experimental waveforms of the separately (independently) operated source converter and load converter with voltage regulator transfer functions $G_{c\_s}(s)$ and $G_{c\_l}(s)$, respectively, revealing that both the source converter and load converter are stable on their own.

Fig. 19 shows the experimental waveforms of the cascaded system at different load conditions. As seen, the system is stable at 20% load but oscillates at full load. Fig. 20 shows that the

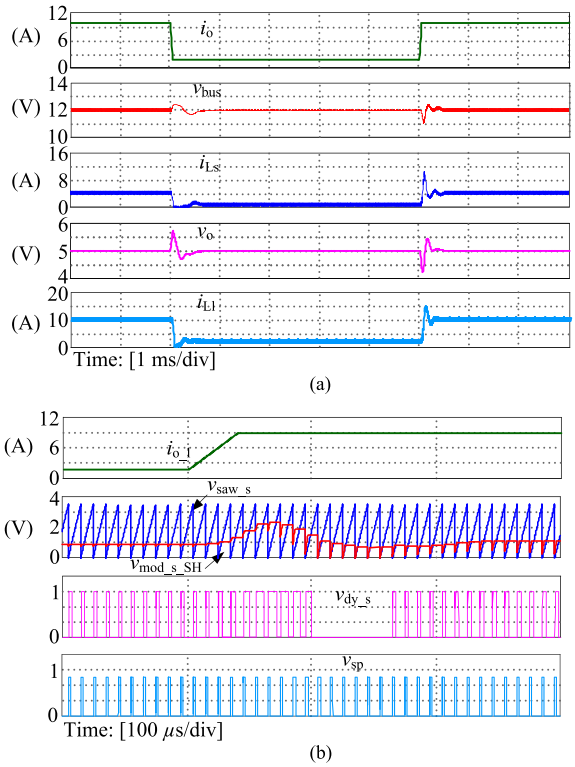

Fig. 17. Simulated transient waveforms of the cascaded system when the load steps between full load and 20% load. (a) Main circuit waveform. (b) Control circuit waveform of the source converter.

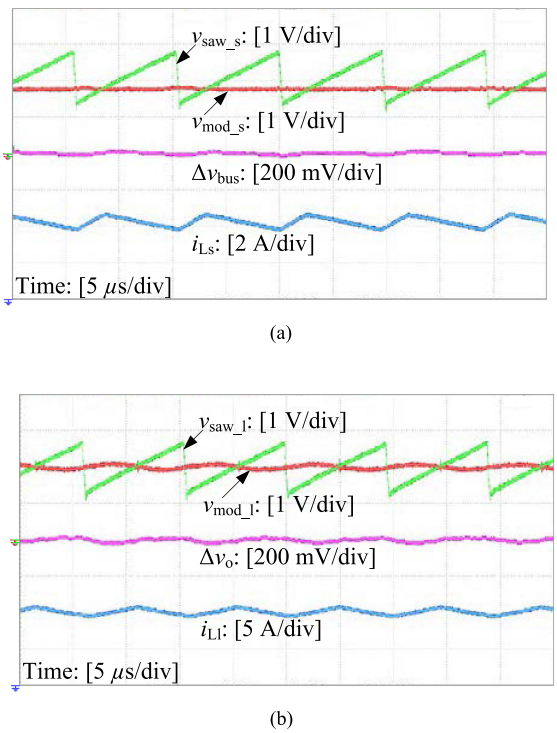

Fig. 18. Experimental waveforms of the source converter and load converter when operating independently. (a) Source converter. (b) Load converter.

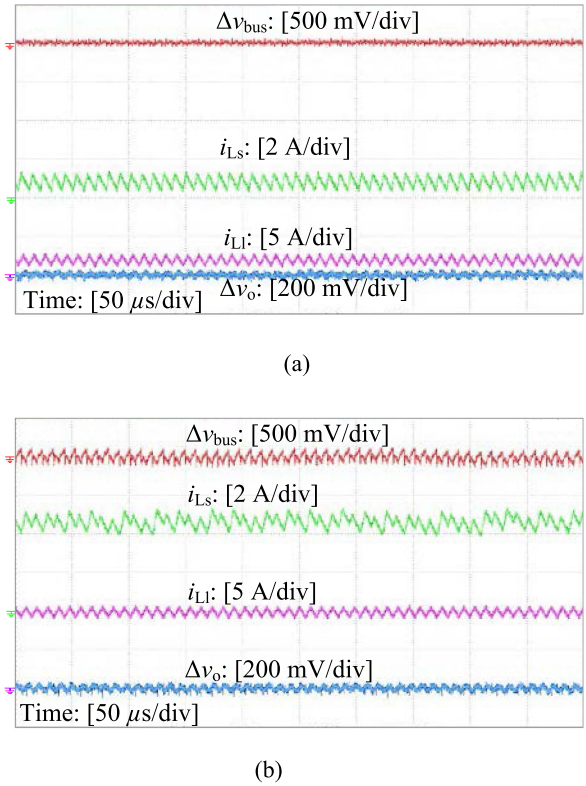

Fig. 19. Experimental waveforms of the cascaded system at (a) 20% load and (b) full load.

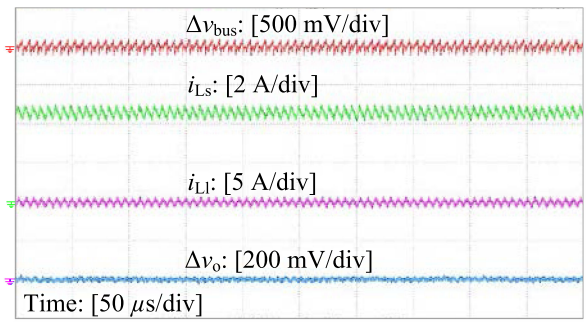

Fig. 20. Experimental waveforms of the cascaded system when the switching frequency is 150 kHz.

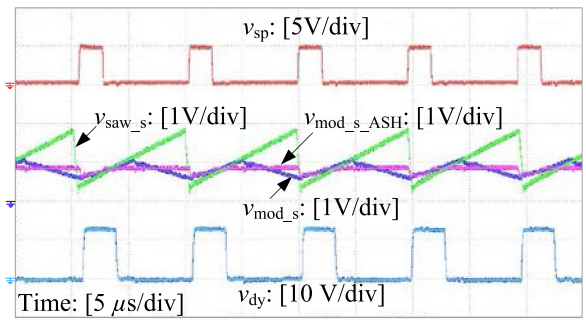

Fig. 21. Pulsewidth modulation process of the source converter with the adaptive modulation sample-and-hold method.

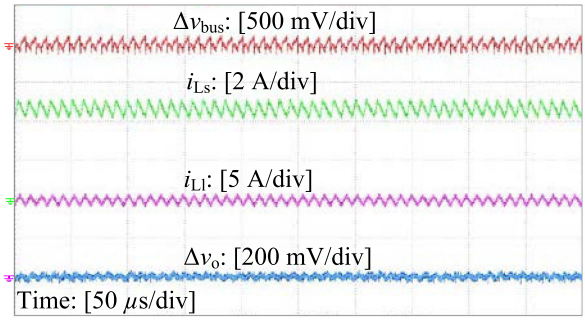

Fig. 22. Experimental waveforms of the cascaded system with the adaptive modulation signal sample-and-hold method.

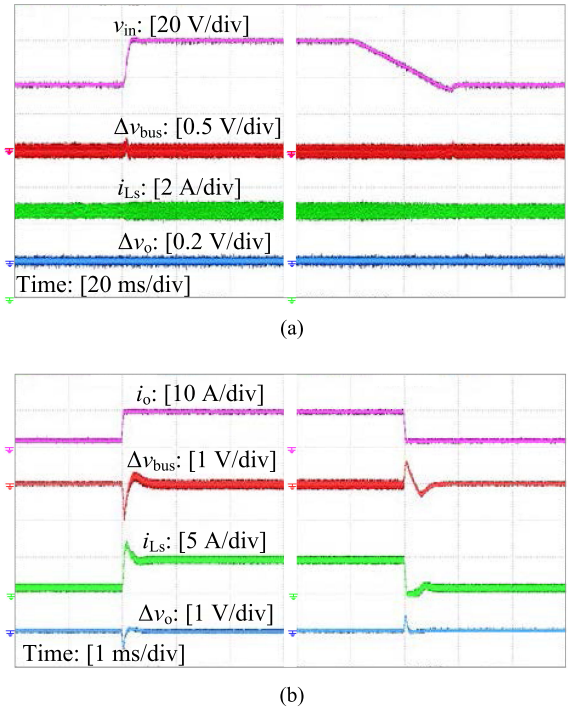

Fig. 23. Experimental waveforms of the cascaded system with the adaptive modulation signal sample-and-hold method. (a) Input voltage step between 36 and 60 V. (b) Load step between 20% load and full load.

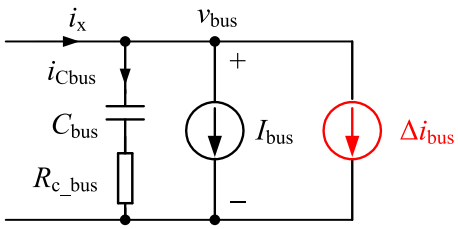

Fig. 24. Output circuit of the source converter after considering the switching ripple interaction.

system remains stable when the switching frequency changes from 100 to 150 kHz. All the results agree well with the analysis.

Fig. 21 shows the regulation process of the duty cycle of the source converter with the adaptive modulation signal sample-and-hold method. As seen, the sampling pulse is slightly narrower than that of the duty cycle, and at the falling edge of $v_{\rm sp}, v_{\rm mod\_s}$ is sampled and held, leading to $v_{\rm mod\_s\_ASH}$, the slope of which is kept at zero after sampling and holding.

The duty-cycle driving signal is produced when $v_{\rm mod\_s\_ASH}$ intersects the carrier wave. Fig. 22 shows the experimental waveforms of the cascaded system after using the adaptive modulation signal sample-and-hold method. It can be seen that the cascaded system remains stable, verifying the effectiveness of the proposed method.

Fig. 23(a) and (b) shows the transient waveforms with the proposed control scheme. In Fig. 23(a), the input voltage step changes between 36 and 60 V. In Fig. 23(b), the load step changes between full load and 20% load. It shows that the cascaded system stays stable in the transient, confirming the validity of the control scheme.

VI. Conclusion

This paper analyzes the SRI between the source converter and the load converter at the intermediate bus port in a cascaded system of converters and points out that the SRI will change the stability of the source converter. Therefore, even if the source converter is well designed on its own, it might be unstable due to the SRI, leading to instability of the cascaded system. The SRI is a coupling phenomenon, which increases the complexity of the stability assessment of the cascaded system. So, this paper proposes the adaptive modulation signal sample-and-hold method for eliminating the SRI. With this method, the stability of the cascaded system is improved, and the judgment of stability is much simpler. Finally, a prototype of a 48 V–12 V–5 V cascaded system comprising two buck converters is fabricated and tested in the laboratory, verifying the theoretical analysis and the validity of the proposed SRI suppression method.

Appendix

In this Appendix, the relationship between $V_{\rm mod\_s}$ $(D_{\rm y\_s}T_{\rm s\_s})$ and $\Delta i_{\rm bus}(t)$ is derived. According to Fig. 2(a), the output circuit of any dc–dc converter is illustrated in Fig. 24, where $i_{\rm x}(t)$ is the current flowing into the bus, $\Delta i_{\rm x}(t)$ is the ac component of $i_{\rm x}(t)$, $i_{C\,\rm bus}(t)$ is the capacitor current, and $v_{\rm bus}(t)$ is the bus voltage.

For the convenience of illustration, the switching frequencies of the source converter and load converter are assumed to be the same. Hence, $\Delta i_{\rm x}(t), \Delta i_{\rm bus}(t)$ are the periodical signals with $T_{\rm s\_s}$ being the switching period, which can be expressed as the Fourier series

$$\Delta i_{\rm x}(t) = \sum_{\substack{k=-\infty,\\ k\neq 0}}^{\infty} \Delta I_{\rm x\_k} e^{jk\omega_{\rm s\_s}t} \tag{A1a}$$

$$\Delta i_{\rm bus}(t) = \sum_{\substack{k=-\infty,\\ k\neq 0}}^{\infty} \Delta I_{\rm bus\_k} e^{jk\omega_{\rm s\_s}t} \tag{A1b}$$

where $\omega_{\rm s\_s} = 2\pi/T_{\rm s\_s}$, and $\Delta I_{\rm x\_k}$ and $\Delta I_{\rm bus\_k}$ are the Fourier coefficients of the kth-order harmonics of $\Delta i_{\rm x}(t)$ and $\Delta i_{\rm bus}(t)$,

respectively, expressed as

$$\Delta I_{\text{x\_k}} = \frac{1}{T_{\text{s\_s}}} \int_0^{T_{\text{s\_s}}} \Delta i_{\text{x}}(t) e^{-jk\omega_{\text{s\_s}}t} dt \tag{A2a}$$

$$\Delta I_{\text{bus\_k}} = \frac{1}{T_{\text{s\_s}}} \int_0^{T_{\text{s\_s}}} \Delta i_{\text{bus}}(t) e^{-jk\omega_{\text{s\_s}}t} dt. \tag{A2b}$$

Therefore, the capacitor current $i_{C\text{bus}}(t)$ is

$$\begin{aligned} i_{\text{Cbus}}(t) &= \Delta i_{\text{x}}(t) - \Delta i_{\text{bus}}(t) \\ &= \sum_{\substack{k=-\infty, \\ k\neq 0}}^{\infty} \Delta I_{\text{x\_k}} e^{jk\omega_{\text{s\_s}}t} - \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} \Delta I_{\text{bus\_k}} e^{jk\omega_{\text{s\_s}}t} \\ &= \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} \left(\Delta I_{\text{x\_k}} - \Delta I_{\text{bus\_k}}\right) e^{jk\omega_{\text{s\_s}}t}. \end{aligned} \tag{A3}$$

According to (A3) and Fig. 24, the ac component of the bus voltage $\Delta v_{\text{bus}}(t)$ is obtained as

$$\begin{aligned} &\Delta v_{\text{bus}}(t) \\ &= \sum_{\substack{k=-\infty, \\ k\neq 0}}^{\infty} \left(\frac{1}{jk\omega_{\text{s\_s}} C_{\text{bus}}} + R_{\text{c\_bus}}\right) \left(\Delta I_{\text{x\_k}} - \Delta I_{\text{bus\_k}}\right) e^{jk\omega_{\text{s\_s}}t}. \end{aligned} \tag{A4}$$

According to Fig. 4, after $\Delta v_{\text{bus}}(t)$ being fed back and compensated, the ac component of the modulation signal $\Delta v_{\text{mod\_s}}$ is derived as

$$\begin{aligned} \Delta v_{\text{mod\_s}}(t) = -\sum_{\substack{k=-\infty, \\ k\neq 0}}^{\infty} \Big[&\left(\tfrac{1}{jk\omega_{\text{s\_s}} C_{\text{bus}}} + R_{\text{c\_bus}}\right) \cdot \\ &\left(\Delta I_{\text{x\_k}} - \Delta I_{\text{bus\_k}}\right) H_{\text{v\_s}} G_{\text{c\_s}}(jk\omega_{\text{s\_s}}) e^{jk\omega_{\text{s\_s}}t} \Big]. \end{aligned} \tag{A5}$$

Upon differentiating the modulation signal, we have

$$\begin{aligned} \Delta v'_{\text{mod\_s}}(t) = -\sum_{\substack{k=-\infty, \\ k\neq 0}}^{\infty} \Big[&\left(\tfrac{1}{C_{\text{bus}}} + jk\omega_{\text{s\_s}} R_{\text{c\_bus}}\right) \cdot \\ &\left(\Delta I_{\text{x\_k}} - \Delta I_{\text{bus\_k}}\right) H_{\text{v\_s}} G_{\text{c\_s}}(jk\omega_{\text{s\_s}}) e^{jk\omega_{\text{s\_s}}t} \Big]. \end{aligned} \tag{A6}$$

Letting $t = D_{\text{y\_s}} T_{\text{s\_s}}$, the slope of $\Delta v_{\text{mod\_s}}$ at $D_{\text{y\_s}} T_{\text{s\_s}}$ is

$$\begin{aligned} &V'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}}) = \Delta v'_{\text{mod\_s}}(D_{\text{y\_s}} T_{\text{s\_s}}) \\ &= -\sum_{\substack{k=-\infty, \\ k\neq 0}}^{\infty} \Big[\left(\tfrac{1}{C_{\text{bus}}} + jk\omega_{\text{s\_s}} R_{\text{c\_bus}}\right) \cdot \\ &\left(\Delta I_{\text{x\_k}} - \Delta I_{\text{bus\_k}}\right) H_{\text{v\_s}} G_{\text{c\_s}}(jk\omega_{\text{s\_s}}) e^{j2k\pi D_{\text{y\_s}}} \Big]. \end{aligned} \tag{A7}$$

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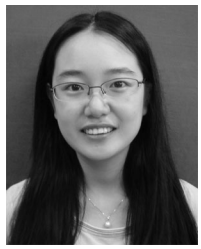

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