Second Harmonic Current Reduction in Front-End DC−DC Converter for Two-Stage Single-Phase Photovoltaic Grid-Connected Inverter

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***Abstract*—The instantaneous output power of the two-stage single-phase grid-connected photovoltaic (PV) inverter pulsates at twice the line frequency ($2f_o$), generating second harmonic current (SHC) in the front-end dc–dc converter and PV panel, which will affect the maximum power point tracking operation and deteriorate the overall conversion efficiency. The generating mechanism of the SHC is analyzed in this paper and it is pointed that in order to eliminate the SHC in the front-end dc–dc converter and PV panel, the voltage loop gain of the front-end dc–dc converter should be high enough at $2f_o$. Since there is a $-180°$ phase abrupt at the resonant frequency of the input side filter capacitor and the inductor, the system may be unstable. To cope with this problem, the inductor current feedback active-damping scheme (ADS) is adopted. For further improving the loop gain at $2f_o$, proportional–integral–resonant regulator with ADS (PIR + ADS) is proposed in this paper. Besides, a step-by-step closed-loop parameters design method is presented. Finally, a 3-kW two-stage single-phase grid-connected PV inverter has been fabricated and tested, and the experimental results verify the feasibility of the proposed control schemes.**

***Index Terms*—Active-damping, proportional–integral–resonant (PIR) regulator, second harmonic current (SHC), two-stage single-phase inverter.**

I. Introduction

With the increasing concerns on energy crisis and environmental issues, renewable energies, such as solar and wind energy, have gained a great interest for their clean and sustainable features. Photovoltaic (PV) grid-connected inverter plays an important role in the distributed power generation systems, which transfers the dc power generated from the PV panel into the power grid. Generally, the PV grid-connected inverters can be classified into single-stage and two-stage types. Compared with the single-stage ones, the two-stage PV grid-connected inverters, which are composed of a front-end dc–dc

Manuscript received June 23, 2018; revised September 17, 2018; accepted October 16, 2018. Date of publication October 22, 2018; date of current version May 2, 2019. This work was supported by the National Natural Science Foundation of China for Distinguished Young Scholars under Award 51525701. Recommended for publication by Associate Editor H. S. Krishnamoorthy. *(Corresponding author: Xinbo Ruan.)*

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front-end dc–dc converter regulates the intermediate dc bus voltage, various methods of reducing the SHC in the front-end dc–dc converter have been proposed. In [10], an inner inductor current loop is added to effectively suppress the SHC in the front-end dc–dc converter. However, the dynamic performance is deteriorated. In [11] and [12], the load current feedforward scheme with notch filter is proposed, which not only eliminates the SHC in the front-end dc–dc converter, but also improves the dynamic performance.

For the cases where the front-end dc–dc converter aims for realizing MPPT, its input voltage or input current, instead of the intermediate dc bus voltage, is regulated, and the control objective is totally different. Therefore, the above-mentioned methods of reducing the SHC are not suitable for the front-end dc–dc converter with MPPT operation. In [13], a bidirectional converter is employed to be connected in parallel with the intermediated bus to buffer the ripple power. However, this will make the system complicated and result in extra power loss. Basically, we can also increase the output impedance of the front-end dc–dc converter with proper control strategy to force the SHC to flow through the intermediate dc bus capacitor, leaving the front-end dc–dc converter free from the SHC. In [14]–[16], the duty cycle compensation method is proposed, which eliminates the disturbance generated by the SHC on the duty cycle of the front-end dc–dc converter. In [17] and [18], a resonant controller is introduced to increase the loop gain at $2f_{\rm o}$ to reduce the SHC in the PV panel. In [19], the feedforward compensation for current control of the boost converter scheme is adopted, and the SHC in the front-end boost converter is drastically restrained.

The original objective of this paper is to propose the approach for reducing the SHC in the front-end dc–dc converter and PV panel from the viewpoint of impedance when the front-end dc–dc converter works at MPPT. Considering that the output voltage of the PV panel is low in the low- and medium-power PV systems, the boost converter is selected as the front-end dc–dc converter in this paper.

The rest of this paper is organized as follows. In Section II, the SHC generating mechanism is analyzed. In Section III, the basic method of reducing the SHC is given, and it is pointed out that, for reducing the SHC in the front-end boost converter, the input voltage loop gain should be high enough at $2f_{\rm o}$. In Section IV, the inductor current feedback active-damping scheme (ADS) is proposed to damp the resonant peak resulted by the input filter capacitor and the boost inductor, aiming to achieve high-voltage loop bandwidth with adequate phase margin (PM). With the ADS, the proportional–integral (PI) regulator is adopted, and a step-by-step design method of the closed-loop parameters and the active-damping resistor is given. Furthermore, the proportional–integral–resonant (PIR) regulator plus inductor current feedback ADS is proposed for further increasing the voltage loop gain at $2f_{\rm o}$, which not only effectively reduces the SHC in the front-end dc–dc converter and PV panel, but also improves the load transient response. In Section V, a 3-kW two-stage single-phase grid-connected PV inverter is fabricated and tested in the laboratory to verify the theoretical analysis and the proposed approaches. Finally, Section VI concludes this paper.

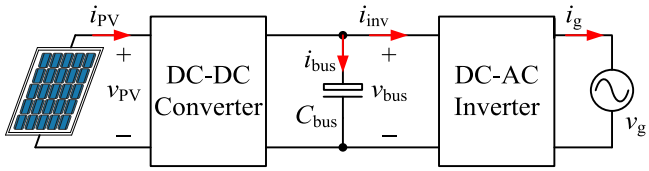


Fig. 1. Configuration of a two-stage single-phase PV grid-connected inverter.

II. Generating Mechanism of the SHC

The configuration of a two-stage single-phase PV grid-connected inverter is shown in Fig. 1, where $C_{\rm bus}$ is the intermediate dc bus capacitor and $v_{\rm g}$ is the power grid voltage. In order to fully utilize the solar energy, the front-end dc–dc converter is operated at MPPT mode for extracting the maximum power from the PV panel. The intermediate dc bus voltage is regulated by the downstream dc–ac inverter.

Without loss of generality, $v_{\rm g}$ is supposed to be ideally sinusoidal waveform and can be expressed as

$$v_{\rm g}(t) = V_{\rm m}\sin\omega_{\rm o}t \tag{1}$$

where $V_{\rm m}$ is the amplitude of $v_{\rm g}$, $\omega_{\rm o} = 2\pi f_{\rm o}$ is the angular frequency of $v_{\rm g}$, and $f_{\rm o}$ is the frequency of $v_{\rm g}$.

The power factor of the downstream dc–ac inverter is assumed to be unity, and the current injected into the power grid can be expressed as

$$i_{\rm g}(t) = I_{\rm m}\sin\omega_{\rm o}t \tag{2}$$

where $I_{\rm m}$ is the amplitude of the current injected into the power grid.

According to (1) and (2), the instantaneous output power of the downstream dc–ac inverter can be derived as

$$\begin{aligned} p_{\rm o}(t) &= v_{\rm g}(t)i_{\rm g}(t) = V_{\rm m}I_{\rm m}\sin^2\omega_{\rm o}t \\ &= \frac{1}{2}V_{\rm m}I_{\rm m} - \frac{1}{2}V_{\rm m}I_{\rm m}\cos(2\omega_{\rm o}t). \end{aligned} \tag{3}$$

Assuming the conversion efficiency is 100%, the instantaneous input power of the downstream dc–ac inverter is equal to its instantaneous output power. Generally, the intermediate dc bus capacitor $C_{\rm bus}$ is large enough and its voltage ripple can be neglected. So, the intermediate dc bus voltage can be regarded as a dc voltage $V_{\rm bus}$. As a result, when ignoring the switching-frequency harmonic components, the input current of the downstream dc–ac inverter can be expressed as

$$i_{\rm inv}(t) = \frac{p_{\rm o}(t)}{V_{\rm bus}} = \frac{V_{\rm m}I_{\rm m}}{2V_{\rm bus}} - \frac{V_{\rm m}I_{\rm m}}{2V_{\rm bus}}\cos\left(2\omega_{\rm ot}\right). \tag{4}$$

Equation (4) indicates that the input current of the downstream dc–ac inverter is composed by a dc component and an ac component pulsating at twice the line frequency, which is called the SHC. As the SHC will propagate to the front-end boost converter and the PV panel, the output power of the PV panel will oscillate around the maximum power point (MPP), which will reduce the utilization efficiency of the power generated by the PV panel. Therefore, it is necessary to make the input current of the front-end boost converter free of the SHC.

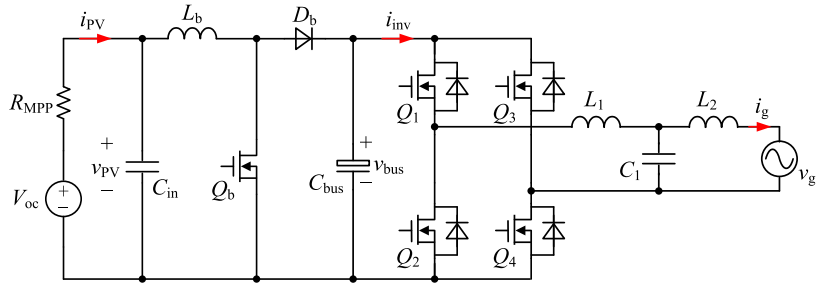


Fig. 2. Main circuit of the two-stage single-phase PV grid-connected inverter.

III. Basic Methods of Reducing the SHC

According to the Thevenin theory, when the PV panel steadily operates at the MPP, it can be represented by an open-circuit voltage source V_{oc} in series with a resistor R_{MPP}. Fig. 2 shows the main circuit of the two-stage single-phase PV grid-connected inverter, where the front-end dc–dc converter adopts the boost converter, consisting of power switch Q_b, diode D_b, and inductor L_b; the downstream dc–ac inverter employs a full-bridge inverter, composed by power switches Q_1-Q_4 and their anti-parallel diodes, and the LCL filter is formed by the filter inductors L_1, L_2 and filter capacitor C_1; C_{in} is the input filter capacitor, and C_{bus} is the intermediate dc bus capacitor.

Since the PV panel exhibits nonlinear $I-V$ characteristic, R_{MPP} presents the dynamic characteristic of a negative resistor [20], which can be expressed as

$$R_{MPP} = \frac{\hat{v}_{MPP}}{\hat{i}_{MPP}} \tag{5}$$

where $\hat{v}_{MPP}$ and $\hat{i}_{MPP}$ denote the small-signal variations of the output voltage and output current of the PV panel around the MPP, respectively. Noted that the reference directions of the output voltage and output current of the PV panel are opposite, as shown in Fig. 2; R_{MPP} is a positive resistor for representing the dynamic characteristic in this paper.

The small-signal ac circuit model of the PV panel can be modeled as R_{MPP}. With the state-space averaging method, the small-signal ac circuit model of the front-end boost converter is given in Fig. 3 [21], where D_y is the duty cycle of the power switch, and $D'_y = 1 - D_y$.

A. SHC Flowing Through the Front-End Boost Converter

According to Fig. 3, $G_{io\text{-}inv}(s)$, the transfer function from $i_{inv}(s)$ to $i_o(s)$, can be derived as

$$G_{io\text{-}inv}(s) = \frac{i_o(s)}{i_{inv}(s)} = \frac{Z_{Cbus}(s)//Z_{o\_c}(s)}{Z_{o\_c}(s)} = \frac{1}{\frac{Z_{o\_c}(s)}{Z_{Cbus}(s)}+1} \tag{6}$$

where $i_{inv}(s)$ is the input current of the downstream dc–ac inverter, $i_o(s)$ is the output current of the front-end boost converter, $Z_{o\_c}(s)$ is the closed-loop output impedance of the front-end boost converter, which excludes C_{bus}, and $Z_{Cbus}(s) = 1/(sC_{bus})$.

According to (6), in order to reduce the SHC flowing into the front-end boost converter, it is necessary to reduce $|Z_{Cbus}(j2\omega_o)|$ and/or increase $|Z_{o\_c}(j2\omega_o)|$. Thus, the SHC will be forced to flow through C_{bus}.

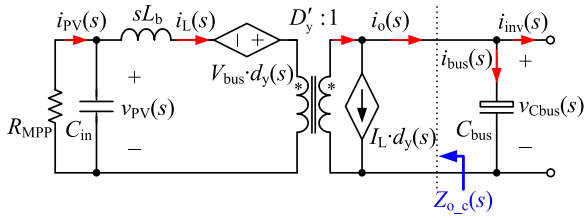


Fig. 3. Small-signal ac circuit model of the front-end boost converter.

In this paper, the perturbation and observation (P&O) MPPT algorithm is employed, and the input voltage of the front-end boost converter is regulated to enforce this. If the voltage step of the MPPT algorithm is small, the MPPT tracking speed is slow, whereas if the voltage step of the MPPT is too large, the output power of the PV panel will oscillate around the MPP [22]. Therefore, there is a tradeoff in selecting the voltage step, and $\Delta v_{pv} = 0.5\% v_{pv}$ is chosen here.

According to Fig. 3 and the above analysis, Fig. 4 gives the control block diagram of the front-end boost converter, where $G_v(s)$ is the voltage regulator; $G_d(s) = e^{-1.5T_s s}$ represents the $1.5T_s$ delay introduced by the digital control, including the computation delay of T_s and the pulsewidth modulation (PWM) delay of $0.5T_s$, and T_s is the sampling period; H_v is the input voltage sensor gain; $K_{PWM} = 1/V_m$ is the gain of the PWM modulator, where V_m is the amplitude of the triangular carrier; and $v_{ref}(s)$ is the voltage reference given by the MPPT algorithm. As the P&O frequency of MPPT is much lower than the voltage-loop crossover frequency f_c, the corresponding influence is ignored when analyzing the voltage control loop.

According to Fig. 4, we obtain

$$i_L(s) = \left[d_y(s)V_{bus} - D'_y v_{bus}(s) + v_{PV}(s)\right]\frac{1}{sL_b} \tag{7}$$

$$v_{PV}(s) = -\frac{R_{MPP}}{1+sC_{in}R_{MPP}} i_L(s) = -Z_{MPP}(s) i_L(s) \tag{8}$$

where

$$Z_{MPP}(s) = \frac{R_{MPP}}{1+sC_{in}R_{MPP}}. \tag{9}$$

Substitution of (8) into (7) yields

$$i_L(s) = \frac{1}{sL_b + Z_{MPP}(s)}\left(d_y(s)V_{bus} - D'_y v_{bus}(s)\right). \tag{10}$$

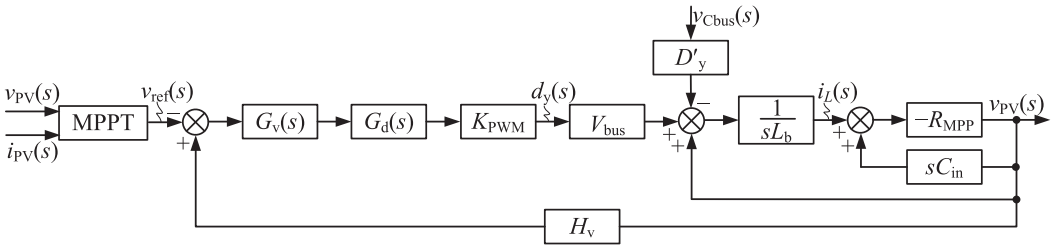


Fig. 4. Control block diagram of the front-end boost converter operating at MPPT.

According to Fig. 3, we obtain

$$i_{\rm o}(s) = D'_{\rm y} i_{\rm L}(s) - I_{\rm L} d_{\rm y}(s) \tag{11}$$

where $I_{\rm L}$ is the average current of the boost inductor.

According to (10) and (11), by setting $d_{\rm y}(s)$ at zero, the open-loop output impedance of the front-end boost converter can be derived as

$$Z_{\rm o\_o}(s) = -\frac{v_{\rm bus}(s)}{i_{\rm o}(s)}\bigg|_{d_{\rm y}(s)=0} = -\frac{sL_{\rm b} + Z_{\rm MPP}(s)}{D'^2_{\rm y}}. \tag{12}$$

Note that $C_{\rm bus}$ is also excluded in $Z_{\rm o\_o}(s)$.

In order to derive the closed-loop output impedance of the front-end boost converter, $Z_{\rm o\_c}(s)$, $v_{\rm ref}(s)$ is set to zero. Thus, according to Fig. 4, we obtain

$$d_{\rm y}(s) = v_{\rm PV}(s) H_{\rm v} G_{\rm v}(s) G_{\rm d}(s) K_{\rm PWM}. \tag{13}$$

According to (7), (8), (10)–(13), $Z_{\rm o\_c}(s)$, excluding $C_{\rm bus}$, can be derived as

$$\begin{aligned} Z_{\rm o\_c}(s) &= -\frac{v_{\rm bus}(s)}{i_{\rm o}(s)} \\ &= -\frac{sL_{\rm b} + Z_{\rm MPP}(s)\left(H_{\rm v}G_{\rm v}(s)G_{\rm d}(s)K_{\rm PWM}V_{\rm bus} + 1\right)}{D'_{\rm y}\left(D'_{\rm y} + Z_{\rm MPP}(s) I_{\rm L} H_{\rm v} G_{\rm v}(s) G_{\rm d}(s) K_{\rm PWM}\right)} \\ &= \frac{1}{\frac{1}{Z_{\rm o\_o}(s)} \cdot \frac{1}{1+T_{\rm v}(s)} - \frac{1}{R_{\rm N}} \cdot \frac{T_{\rm v}(s)}{1+T_{\rm v}(s)}} \end{aligned} \tag{14}$$

where $T_{\rm v}(s)$ is the compensated voltage loop gain, expressed as

$$T_{\rm v}(s) = \frac{H_{\rm v} G_{\rm v}(s) G_{\rm d}(s) K_{\rm PWM} V_{\rm bus}}{s^2 L_{\rm b} C_{\rm in} + s\frac{L_{\rm b}}{R_{\rm MPP}} + 1} \tag{15}$$

and $R_{\rm N}$ is expressed as

$$R_{\rm N} = \frac{V_{\rm bus}}{D'_{\rm y} I_{\rm L}} = \frac{V^2_{\rm bus}}{V_{\rm PV} I_{\rm L}} = \frac{V^2_{\rm bus}}{P_{\rm MPP}} \tag{16}$$

where $P_{\rm MPP}$ is the maximum output power of the PV panel.

According to (12) and (16), we obtain

$$\begin{aligned} \left|\frac{Z_{\rm o\_o}(s)}{R_{\rm N}}\right| &= \left|\left(sL_{\rm b} + Z_{\rm MPP}(s)\right)\frac{P_{\rm MPP}}{D'^2_{\rm y} V^2_{\rm bus}}\right| \\ &= \left|\left(sL_{\rm b} + Z_{\rm MPP}(s)\right)\frac{P_{\rm MPP}}{V^2_{\rm PV}}\right| = \left|\frac{sL_{\rm b} + Z_{\rm MPP}(s)}{R_{\rm MPP}}\right|. \end{aligned} \tag{17}$$

As seen in Fig. 2, $C_{\rm in}$ is used to filter the switching-frequency current ripple in the boost inductor, and its impedance is far larger than $R_{\rm MPP}$ at $2f_{\rm o}$. Thus, $Z_{\rm MPP}$ can be approximated to $R_{\rm MPP}(s)$, and (17) can be rewritten as

$$\left|\frac{Z_{\rm o\_o}(s)}{R_{\rm N}}\right| \approx \left|\frac{sL_{\rm b}}{R_{\rm MPP}} + 1\right| > 1. \tag{18}$$

At the frequencies far lower than the crossover frequency of the voltage loop, $f_{\rm c}$, the compensated voltage loop gain $|T_{\rm v}(s)|$ is far larger than 1. So, according to (14) and (18), $Z_{\rm o\_c}(s)$ can be approximated to

$$Z_{\rm o\_c}(s) \approx -R_{\rm N}. \tag{19}$$

Equation (19) implies that, when the compensated voltage loop gain $|T_{\rm v}(s)|$ at $2f_{\rm o}$ is far larger than 1, the closed-loop output impedance of the front-end boost converter can be approximated to a negative resistor.

Substitution of (19) into (6) yields

$$G_{\rm io\text{-}inv}(s) = \frac{i_{\rm o}(s)}{i_{\rm inv}(s)} = \frac{1}{1 - sC_{\rm bus}R_{\rm N}}. \tag{20}$$

It can be known from (20) that increasing $C_{\rm bus}$ could reduce the SHC in the front-end boost converter.

B. SHC in the PV Panel

According to (8), (11), and (13), the transfer function $G_{\rm iL\text{-}io}(s)$, from $i_{\rm o}(s)$ to $i_{\rm L}(s)$, can be derived as

$$G_{\rm iL-io}(s) = \frac{i_{\rm L}(s)}{i_{\rm o}(s)} = \frac{1}{D'_{\rm y} + I_{\rm L} H_{\rm v} G_{\rm v}(s) G_{\rm d}(s) K_{\rm PWM} Z_{\rm MPP}(s)}. \tag{21}$$

Combining (15) and (21), we obtain

$$G_{\rm iL-io}(s) = \frac{i_{\rm L}(s)}{i_{\rm o}(s)} = \frac{1}{D'_{\rm y} + T_{\rm v}(s)\frac{I_{\rm L}}{V_{\rm bus}}\left(sL_{\rm b} + Z_{\rm MPP}(s)\right)}. \tag{22}$$

Considering $V_{\rm bus} = V_{\rm PV}/D'_{\rm y}$ and $R_{\rm MPP} = V_{\rm PV}/I_{\rm L}$, we have $I_{\rm L}/V_{\rm bus} = D'_{\rm y}/R_{\rm MPP}$. Thus, (22) can be rewritten as

$$G_{\rm iL\text{-}io}(s) = \frac{i_{\rm L}(s)}{i_{\rm o}(s)} = \frac{1}{D'_{\rm y}\left[1 + T_{\rm v}(s)\frac{1}{R_{\rm MPP}}\left(sL_{\rm b} + Z_{\rm MPP}(s)\right)\right]}. \tag{23}$$

It can be known from (23) that increasing the voltage loop gain $T_{\rm v}(s)$ at $2f_{\rm o}$ could help reduce and even eliminate the SHC in the PV panel.

C. Reducing the SHC in the Front-End Boost Converter and PV Panel

According to (20), in order to reduce the SHC in the front-end boost converter, it is required that

$$|G_{\text{io-inv}}(j2\omega_{\text{o}})| = \left|\frac{i_{\text{o}}(j2\omega_{\text{o}})}{i_{\text{inv}}(j2\omega_{\text{o}})}\right| = \frac{1}{|1-j2\omega_{\text{o}}C_{\text{bus}}R_{\text{N}}|} = \frac{1}{\sqrt{1+(2\omega_{\text{o}}C_{\text{bus}}R_{\text{N}})^2}} \le a_1 \tag{24}$$

where a_1 is SHC suppression requirement in the front-end boost converter.

From (24), the required C_{bus} is obtained as

$$C_{\text{bus}} \ge \frac{1}{2\cdot 2\pi f_{\text{o}}R_{\text{N}}}\sqrt{\frac{1}{a_1^2}-1}. \tag{25}$$

Here, $a_1 = 2.5\%$ is selected, and f_{o} is 50 Hz. Meanwhile, V_{bus} is regulated at 380 V by the downstream dc–ac inverter, and the maximum power of the PV panel in the prototype is 3 kW. With these parameters, according to (16) and (25), we have $C_{\text{bus}} \ge 1322.2\,\mu$F. Here, three 470 μF/450 V electrolytic capacitors connected in parallel are used to constitute C_{bus}.

As mentioned above, Z_{MPP} can be approximated to $R_{\text{MPP}}(s)$ at $2f_{\text{o}}$. Thus, according to (23), we obtain

$$G_{\text{iL-io}}(j2\omega_{\text{o}}) = \frac{i_{\text{L}}(j2\omega_{\text{o}})}{i_{\text{o}}(j2\omega_{\text{o}})} \approx \frac{1}{D'_{\text{y}}\left[1+T_{\text{v}}(j2\omega_{\text{o}})\left(\frac{j2\omega_{\text{o}}L_{\text{b}}}{R_{\text{MPP}}}+1\right)\right]}. \tag{26}$$

Here, the SHC in i_{o} is limited to 2.5% of that in the input current of the downstream dc–ac inverter. Thus, according to (26), the SHC in the PV panel can be easily limited to 2.5% since $|T_{\text{v}}(j2\omega_{\text{o}})|$ is far larger than 1 when $2f_{\text{o}}$ is far lower than f_{c}.

In conclusion, if the crossover frequency of the voltage loop, f_{c}, is far higher than $2f_{\text{o}}$, and C_{bus} is designed to satisfy (25), the SHC in the front-end boost converter and PV panel will be limited to the desired value. So, the input capacitor C_{in} is employed to mainly bypass the harmonics at the switching frequency and its multiples in the input current.

IV. Control Schemes for Reducing the SHC

A. Proportional-Integral Regulator plus Inductor Current Feedback ADS (PI + ADS)

According to (15) and letting $G_{\text{v}}(s) = 1$, the Bode diagram of the uncompensated voltage loop gain at the MPP, $T_{\text{v\_u}}(s)$, is depicted, as shown in Fig. 5 with the solid lines. Note that all the Bode diagrams in this paper are depicted with the parameters listed in Table II given in Section V. As shown in Fig. 5, there is a resonant peak in the magnitude–frequency curve of $T_{\text{v\_u}}(s)$, which is caused by the resonance between the input filter capacitor C_{in} and the boost inductor L_{b}, and a $-180°$ phase drop occurs around the resonant frequency f_{r}. As seen in Fig. 3, R_{MPP} is connected in parallel with C_{in}, and it could damp the resonant peak, which can also be found in (15). However, even if the PV panel is free of partial shading, R_{MPP} has limited effects on resonance damping. Fig. 5 also gives the Bode diagram of $T_{\text{v\_u}}(s)$ when the PV panel gets shaded, as shown with the dashed lines. Here, R_{MPP} is intentionally set as infinity for the worst case. As shown, a $-180°$ phase jump occurs at f_{r}.

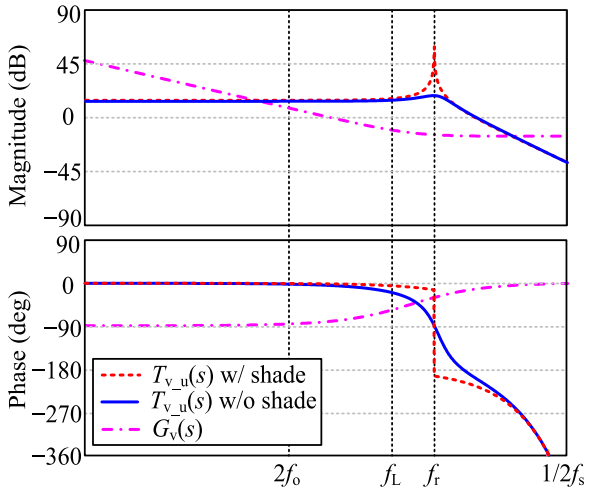


Fig. 5. Bode diagrams of uncompensated voltage loop gain and the voltage regulator.

Since the PI compensator is simple and could track the dc reference without error, it is adopted as the voltage regulator $G_{\text{v}}(s)$, expressed as

$$G_{\text{v}}(s) = K_{\text{p}} + \frac{K_{\text{i}}}{s} \tag{27}$$

where K_{p} is proportional gain and K_{i} is the integral gain. The corner frequency f_{L} is expressed as

$$f_{\text{L}} = \frac{K_{\text{i}}}{2\pi K_{\text{p}}}. \tag{28}$$

According to (27), Fig. 5 shows the Bode diagram of $G_{\text{v}}(s)$ with the dash-dot lines. As seen, at the frequencies around the corner frequency, f_{L}, the slope of the magnitude changes from $-$ 20 to 0 dB/dec, and the phase of the PI regulator increases from $-90°$ to $0°$. In order to avoid the reduction of the PM caused by PI regulator, f_{L} is set lower than f_{c}. Thus, we have $|G_{\text{v}}(j2\pi f_{\text{c}})| \approx K_{\text{p}}$. According to the discussions in Section III, in order to increase the magnitude of loop gain at $2f_{\text{o}}$ to restrain the SHC in the front-end boost converter and improve the dynamic performance of the system, the crossover frequency f_{c} of the voltage loop is usually set to be higher than f_{r}. Since there are a $-180°$ phase jump at f_{r} and a negative phase shift caused by $G_{\text{v}}(s)$, the phase of $T_{\text{v}}(s)$ will definitely cross $-180°$ at f_{r}, and thus the system is unstable.

In order to ensure the system stability, the resonant peak should be properly damped, and a damping resistor *r* could be introduced in series with the boost inductor. Thus, based on Fig. 4, the control block diagram with the damping resistor is given in Fig. 6. By moving the feedback node of the inductor current to the output of the voltage compensator and modifying the corresponding feedback function, the control block diagram

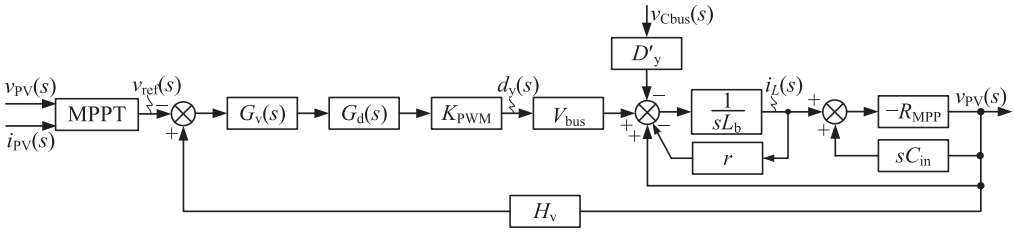


Fig. 6. Control block diagram with a resistor introduced in series with the boost inductor.

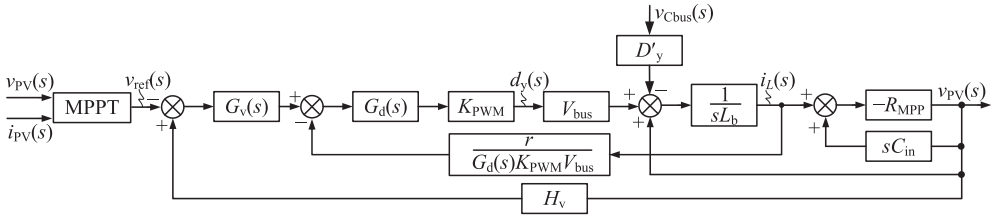


Fig. 7. Active-damping solution equivalent to a resistor in series with the boost inductor.

shown in Fig. 6 can be equivalently transformed into that shown in Fig. 7. As seen, the damping resistor *r* can be realized by the feedback of the inductor current, which is an ADS, and thus the power loss in a passive resistor is avoided.

As seen from Fig. 7, the feedback function of the boost inductor current includes $1/G_{\rm d}(s)$, which is a prediction component with unity gain and cannot be realized physically. So, $1/G_{\rm d}(s)$ is replaced by 1 in practice, and the feedback function of the boost inductor current is approximated to $r/(K_{\rm PWM}V_{\rm bus})$. Thus, the actual damping component is $rG_{\rm d}(s)$ instead of *r*. By replacing $sL_{\rm b}$ with $sL_{\rm b}+rG_{\rm d}(s)$ in (15), the voltage loop gain with the ADS can be obtained as

$$T_{\rm v\_PI+ADS}(s)=\frac{H_{\rm v}G_{\rm v}(s)G_{\rm d}(s)K_{\rm PWM}V_{\rm bus}}{sC_{\rm in}\left(sL_{\rm b}+rG_{\rm d}(s)\right)+\frac{sL_{\rm b}+rG_{\rm d}(s)}{R_{\rm MPP}}+1}$$
$$=\frac{H_{\rm v}G_{\rm v}(s)G_{\rm d}(s)K_{\rm PWM}V_{\rm bus}}{s^2L_{\rm b}C_{\rm in}+s\left(rG_{\rm d}(s)C_{\rm in}+\frac{L_{\rm b}}{R_{\rm MPP}}\right)+\left(1+\frac{rG_{\rm d}(s)}{R_{\rm MPP}}\right)}. \quad (29)$$

1) Effects of Digital Control Delay on Damping Performance

As mentioned in Section III-A, $G_{\rm d}(s)=e^{-1.5T_{\rm s}s}$. So, we obtain

$$G_{\rm d}(j2\pi f)=\cos(3\pi f/f_{\rm s})-j\sin(3\pi f/f_{\rm s}) \quad (30)$$

where $f_{\rm s}=1/T_{\rm s}=1/T_{s1}$ is the switching frequency of the boost converter.

As mentioned above, the actual damping component is $rG_{\rm d}(s)$. So, according to (30), we obtain

$$rG_{\rm d}(j2\pi f)=R_{\rm eq}+jX_{\rm eq} \quad (31)$$

where

$$R_{\rm eq}=r\cos(3\pi f/f_{\rm s}),\ X_{\rm eq}=-r\sin(3\pi f/f_{\rm s}). \quad (32)$$

This means that the active damping with the inductor current feedback is equivalent to a virtual resistor $R_{\rm eq}$ and a virtual reactor $X_{\rm eq}$ connected in series with the boost inductor. The $R_{\rm eq}$ could damp the resonance, and the $X_{\rm eq}$ will change the resonance frequency.

As seen in (32), both $R_{\rm eq}$ and $X_{\rm eq}$ are frequency dependent. When $f<f_{\rm s}/3$, $X_{\rm eq}$ behaves as a capacitor, which is connected in series with the boost inductor, yielding a higher actual resonance frequency $f'_{\rm r}$, whereas when $f_{\rm s}/3<f<f_{\rm s}/2$, $X_{\rm eq}$ behaves as an inductor, yielding a lower actual resonance frequency $f'_{\rm r}$. Meanwhile, when $f<f_{\rm s}/6$, $R_{\rm eq}$ is a positive resistor, whereas when $f>f_{\rm s}/6$, $R_{\rm eq}$ is a negative resistor. As the actual resonance frequency is $f'_{\rm r}$, instead of $f_{\rm r}$, $R_{\rm eq}$ will be essential for the resonance damping at $f'_{\rm r}$. When $f'_{\rm r}>f_{\rm s}/6$, $R_{\rm eq}$ is a negative resistor at $f'_{\rm r}$. Thus, a pair of open-loop unstable poles is introduced, which will deteriorate the system stability [23]. Specially, when $f'_{\rm r}=f_{\rm s}/6$, $R_{\rm eq}=0$, which has no contribution to the resonance damping, so the magnitude plot shows an infinite resonance gain and a $-180°$ phase jump occurs at $f'_{\rm r}$. Thus, $f'_{\rm r}<f_{\rm s}/6$ is set here for ensuring that $R_{\rm eq}$ is a positive resistor.

According to (29) and letting $G_{\rm v}(s)=1$, as the phase plot of $T_{\rm v}(s)/G_{\rm d}(s)$ at the frequencies higher than $f'_{\rm r}$ crosses over $-90°$ and the negative phase shift caused by $G_{\rm d}(s)$ at $f_{\rm s}/6$ is $-90°$, the phase plot of the uncompensated loop gain will cross over $-180°$ at $f<f_{\rm s}/6$ with the inductor current feedback active damping. Thus, $f_{\rm c}$ should be set to be lower than $f_{\rm s}/6$. Furthermore, to improve the dynamic performance of the system, $f_{\rm c}$ is usually set higher than $f'_{\rm r}$. So, $f'_{\rm r}<f_{\rm c}<f_{\rm s}/6$ is set here.

2) Step-by-Step Design Method of the Closed-Loop Parameters and the Active Damping Resistor

Based on the above considerations, a step-by-step design method of the closed-loop parameters and the active damping resistor *r* is presented to obtain a satisfactory region of *r* and $f_{\rm c}$, which is illustrated as follows.

By substituting (27) and (30) into (29), the voltage loop gain with ADS can be expressed as (33) shown at the bottom of the next page.

Since $f_{\rm L}$ is sufficiently lower than $f_{\rm c}$, we have $\sqrt{1+(f_{\rm L}/f_{\rm c})^2}\approx 1$. Furthermore, as the magnitude of the loop gain at $f_{\rm c}$ is unity, according to (33), we obtain (34) shown at the bottom of the next page. By solving (34), we obtain (35) shown at the bottom of the next page.

According to (29), the relationship between r and f'_{r} can be derived as

$$r=\frac{\left(2\pi f'_{\mathrm{r}}\right)^2 L_{\mathrm{b}}C_{\mathrm{in}}-1}{2\pi f'_{\mathrm{r}}C_{\mathrm{in}}\sin\left(3\pi\frac{f'_{\mathrm{r}}}{f_{\mathrm{s}}}\right)+\frac{1}{R_{\mathrm{MPP}}}\cos\left(3\pi\frac{f'_{\mathrm{r}}}{f_{\mathrm{s}}}\right)}. \tag{36}$$

Note that, according to (32), a larger r leads to a larger $|X_{\mathrm{eq}}|$, which means that the actual resonant frequency f'_{r} will be higher when $f'_{\mathrm{r}}<f_{\mathrm{s}}/3$. So r should be constrained by f_{c} to guarantee $f'_{\mathrm{r}}<f_{\mathrm{c}}\le f_{\mathrm{s}}/6$.

Due to $2f_{\mathrm{o}}<<f_{\mathrm{s}}$, the influence of the digital control delay can be negligible at $2f_{\mathrm{o}}$; thus, we have $G_{\mathrm{d}}(j4\pi f_{\mathrm{o}})\approx 1$. So, according to (33), the magnitude of $T_{\mathrm{v\_PI+ADS}}(s)$ at $2f_{\mathrm{o}}$ can be expressed as

$$|T_{\mathrm{v\_ADS}}(j2\pi\cdot 2f_{\mathrm{o}})|\approx\frac{H_{\mathrm{v}}K_{\mathrm{PWM}}V_{\mathrm{bus}}K_{\mathrm{p}}\sqrt{1+\left(\frac{f_{\mathrm{L}}}{2f_{\mathrm{o}}}\right)^2}}{\sqrt{\begin{array}{l}\left(1-4\pi^2(2f_{\mathrm{o}})^2L_{\mathrm{b}}C_{\mathrm{in}}+\frac{r}{R_{\mathrm{MPP}}}\right)^2\\+4\pi^2(2f_{\mathrm{o}})^2\left(rC_{\mathrm{in}}+\frac{L_{\mathrm{b}}}{R_{\mathrm{MPP}}}\right)^2\end{array}}}. \tag{37}$$

By substituting (35) into (37) and manipulating, we obtain (38) shown at the bottom of this page.

The PM of the compensated loop gain is expressed as

$$\mathrm{PM}=180^\circ+\angle T_{\mathrm{v\_PI+ADS}}(j2\pi f_{\mathrm{c}}). \tag{39}$$

Substitution of (33) into (39) yields (40) shown at the bottom of the next page.

3) Design Example

A 3-kW two-stage single-phase PV grid-connected inverter is taken as an example to verify the effectiveness of the closed-loop parameters design method. The key parameters of the PV panel under normal and shaded conditions and the parameters of the prototype are listed in Tables I and II, respectively.

The design requirements of the compensated loop gain are listed as follows.

1) $|T_{\mathrm{v\_PI+ADS}}(j4\pi f_{\mathrm{o}})|\ge 20\,\mathrm{dB}$ is set to ensure the closed-loop output impedance of the front-end boost converter can be approximated to a negative resistor.
2) The phase margin PM $\ge 30^\circ$ is set to confirm a good dynamic performance and robustness of the system.

Substituting (38) into (40), the curves constrained by PM $\ge 30^\circ$ and $|T_{\mathrm{v\_PI+ADS}}(j4\pi f_{\mathrm{o}})|\ge 20\,\mathrm{dB}$ under different R_{MPP} are depicted, as shown in Fig. 8 with the dashed lines, and the satisfactory region of r and f_{c} is above the curves. It can be seen that the satisfactory region of r and f_{c} is shrunk with the

$$T_{\mathrm{v\_PI+ADS}}(j2\pi f)=\frac{H_{\mathrm{v}}K_{\mathrm{P}}K_{\mathrm{PWM}}V_{\mathrm{bus}}\left(1-jf_{\mathrm{L}}/f\right)\left[\cos\left(3\pi f/f_{\mathrm{s}}\right)-j\sin\left(3\pi f/f_{\mathrm{s}}\right)\right]}{\left\{\begin{array}{l}\left[1-4\pi^2f^2L_{\mathrm{b}}C_{\mathrm{in}}+2\pi fC_{\mathrm{in}}r\sin\left(3\pi f/f_{\mathrm{s}}\right)+\frac{r}{R_{\mathrm{MPP}}}\cos\left(3\pi f/f_{\mathrm{s}}\right)\right]\\+j\left[2\pi fC_{\mathrm{in}}r\cos\left(3\pi f/f_{\mathrm{s}}\right)+\frac{2\pi fL_{\mathrm{b}}}{R_{\mathrm{MPP}}}-\frac{r}{R_{\mathrm{MPP}}}\sin\left(3\pi f/f_{\mathrm{s}}\right)\right]\end{array}\right\}} \tag{33}$$

$$|T_{\mathrm{v\_PI+ADS}}(j2\pi f_{\mathrm{c}})|\approx\frac{H_{\mathrm{v}}K_{\mathrm{p}}K_{\mathrm{PWM}}V_{\mathrm{bus}}}{\sqrt{\begin{array}{l}\left[1-4\pi^2f_{\mathrm{c}}^2L_{\mathrm{b}}C_{\mathrm{in}}+2\pi f_{\mathrm{c}}C_{\mathrm{in}}r\sin\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)+\frac{r}{R_{\mathrm{MPP}}}\cos\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)\right]^2\\+\left[2\pi f_{\mathrm{c}}C_{\mathrm{in}}r\cos\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)+\frac{2\pi f_{\mathrm{c}}L_{\mathrm{b}}}{R_{\mathrm{MPP}}}-\frac{r}{R_{\mathrm{MPP}}}\sin\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)\right]^2\end{array}}}=1 \tag{34}$$

$$K_{\mathrm{p}}=\frac{1}{H_{\mathrm{v}}K_{\mathrm{PWM}}V_{\mathrm{bus}}}\sqrt{\begin{array}{l}\left[1-4\pi^2f_{\mathrm{c}}^2L_{\mathrm{b}}C_{\mathrm{in}}+2\pi f_{\mathrm{c}}C_{\mathrm{in}}r\sin\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)+\frac{r}{R_{\mathrm{MPP}}}\cos\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)\right]^2\\+\left[2\pi f_{\mathrm{c}}C_{\mathrm{in}}r\cos\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)+\frac{2\pi f_{\mathrm{c}}L_{\mathrm{b}}}{R_{\mathrm{MPP}}}-\frac{r}{R_{\mathrm{MPP}}}\sin\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)\right]^2\end{array}} \tag{35}$$

$$f_{\mathrm{L}}=2f_{\mathrm{o}}\sqrt{\frac{|T_{\mathrm{v\_ADS}}(j2\pi\cdot 2f_{\mathrm{o}})|^2\left[\left(1-4\pi^2(2f_{\mathrm{o}})^2L_{\mathrm{b}}C_{\mathrm{in}}+\frac{r}{R_{\mathrm{MPP}}}\right)^2+4\pi^2(2f_{\mathrm{o}})^2\left(rC_{\mathrm{in}}+\frac{L_{\mathrm{b}}}{R_{\mathrm{MPP}}}\right)^2\right]}{\left\{\begin{array}{l}\left[\begin{array}{l}1-4\pi^2f_{\mathrm{c}}^2L_{\mathrm{b}}C_{\mathrm{in}}+2\pi f_{\mathrm{c}}C_{\mathrm{in}}r\sin\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)\\+\frac{r}{R_{\mathrm{MPP}}}\cos\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)\end{array}\right]^2+\left[\begin{array}{l}2\pi f_{\mathrm{c}}C_{\mathrm{in}}r\cos\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)+\frac{2\pi f_{\mathrm{c}}L_{\mathrm{b}}}{R_{\mathrm{MPP}}}\\-\frac{r}{R_{\mathrm{MPP}}}\sin\left(3\pi f_{\mathrm{c}}/f_{\mathrm{s}}\right)\end{array}\right]^2\end{array}\right\}}-1} \tag{38}$$

TABLE I
PARAMETERS OF PV PANEL

Normal Condition			Shaded Condition		
Parameter	Symbol	Value	Parameter	Symbol	Value
Open-circuit voltage	V_{oc}	225.1 V	Open-circuit voltage	V_{c_oc}	225.1 V
Short-circuit current	I_{sc}	20.6 A	Short-circuit current	I_{c_sc}	11.4 A
Voltage at MPP	V_{MPP}	168.4 V	Voltage at MPP	V_{c_MPP}	165.8 V
Current at MPP	I_{MPP}	17.87 A	Current at MPP	I_{c_MPP}	10.1 A
Power output at MPP	P_{MPP}	3000 W	Power output at MPP	P_{c_MPP}	1672 W

TABLE II
PARAMETERS OF THE PROTOTYPE

	Parameter	Symbol	Value
Boost converter	Inductor	L_b	200 μH
	Input side filter capacitor	C_{in}	20 μF
	Bus capacitor	C_{bus}	1410 μF
	Switching frequency	f_{s1}	100 kHz
	MPPT frequency	f_{MPPT}	10 Hz
	MPPT voltage step	Δv_{pv}	0.9 V
Inverter	Inverter-side inductor	L_1	1.6 mH
	Grid–side inductor	L_2	400 μH
	Filter capacitor	C_2	4.7 μF
	Switching frequency	f_{s2}	10 kHz

increase of R_{MPP}. It is because that, according to Fig. 5, R_{MPP} increases when the PV panel is partially shaded, and R_{MPP} has limited effects on resonance damping. Thus, in order to ensure the effects on resonance damping, the damping resistor r should be increased.

Substituting the parameters in Table II into (36), the curves constrained by $f_r' < f_c$ are depicted, as shown in Fig. 8 with the solid lines, and the satisfactory region of r and f_c is under the curves.

According to Fig. 8, it is easy to pick out a group of closed-loop parameters to ensure the compensated system to meet the design requirements. Here, $r = 4\,\Omega$ and $f_c = 4$ kHz are chosen, corresponding to point A. Substituting $L_b = 200\,\mu$H, $C_{in} = 20\,\mu$F, $r = 4\,\Omega$, $f_c = 4$ kHz, and $f_s = 100$ kHz into (35) and (38), respectively, it can be calculated that $K_p = 0.38$ and $f_L = 2$ kHz. Thus, according to (28), we have $K_i = 4800$. With the designed parameters, the Bode diagram of $T_{v\_PI+ADS}(s)$ is depicted, as shown in Fig. 9 with the solid lines. As seen, $|T_{v\_PI+ADS}(j2\omega_o)| = 29$ dB, and the crossover frequency is 4 kHz.

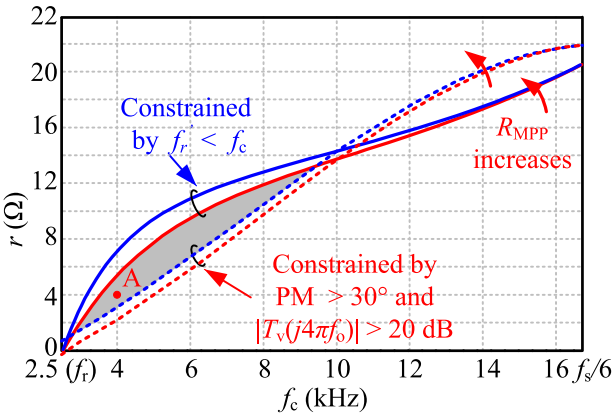


Fig. 8. Satisfactory region of r and f_c constrained by PM and $|T_v(j4\pi f_o)| \geq 20$ dB.

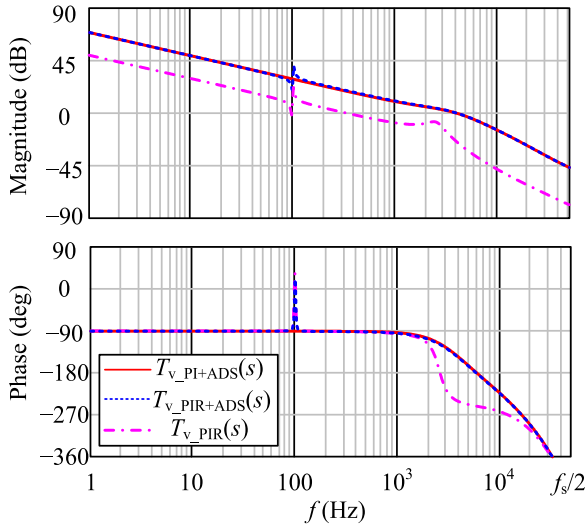


Fig. 9. Bode diagram of the voltage loop gain at MPP.

B. PIR Regulator Plus ADS (PIR + ADS)

In order to further increase the magnitude of loop gain at $2f_o$, a resonant component with the characteristic frequency of $2f_o$ can be incorporated into the voltage regulator, leading to a PIR regulator, expressed as

$$G_{PIR}(s) = K_p + \frac{K_i}{s} + \frac{K_r \omega_i s}{s^2 + 2\omega_i s + \omega_r^2} \tag{41}$$

where K_r is the resonant coefficient, $\omega_r = 2\omega_o$, and ω_i is the bandwidth of the resonant part concerning -3 dB cutoff frequency to reduce the sensitivity of the regulator to variations at the fundamental frequency.

In the PV power generation systems, the fundamental frequency of the grid fluctuates between 49.5 and 50.2 Hz, and the corresponding maximum frequency fluctuation is 0.5 Hz [24]. Therefore, the corresponding maximum variations of the

$$\mathrm{PM} = 180^\circ - \frac{3\pi f_c}{f_s} - \arctan\frac{f_L}{f_c} - \arctan\frac{2\pi f_c C_{in} r\cos(3\pi f_c/f_s) + \frac{2\pi f_c L_b}{R_{MPP}} - \frac{r}{R_{MPP}}\sin(3\pi f_c/f_s)}{1 - 4\pi^2 f_c^2 L_b C_{in} + 2\pi f_c C_{in} r\sin(3\pi f_c/f_s) + \frac{r}{R_{MPP}}\cos(3\pi f_c/f_s)} \tag{40}$$

frequency of the SHC is 1 Hz, and ω_i is set to be $2\pi\Delta f$, where $\Delta f = 1$ Hz.

According to (29) and (41), considering $G_d(j4\pi f_o) \approx 1$, the magnitude of $T_{v\_PIR+ADS}(s)$ at $2f_o$ can be expressed as (42) shown at the bottom of this page.

The design requirements of the compensated loop gain with PIR + ADS are listed as follows.

1) The magnitude of $T_{v\_PIR+ADS}(s)$ at $2f_o$ is larger than 40 dB to further restrain the SHC in the output current of PV panel.
2) The phase margin PM $\geq 30°$ to confirm a good dynamic performance.

In order to meet the above requirement, substituting $r = 4\,\Omega$, $K_p = 0.38$, $K_i = 4800$, which are obtained with the PI + ADS, and the parameters listed in Table II into (42), $K_r = 50$ is calculated. With the calculated parameters, the Bode diagram of $T_{v\_PIR+ADS}(s)$ is depicted, as shown in Fig. 9 with the dashed lines, which is almost the same as that with PI+ADS, except around $2f_o$. Here, $|T_{v\_PIR+ADS}(j2\omega_o)| = 40$ dB, higher than $|T_{v\_PI+ADS}(j2\omega_o)| = 29$ dB.

C. PIR Regulator Without ADS

For the purpose of comparison, the voltage regulator adopting the PIR regulator without ADS is discussed here. According to the design method presented in [25], $K_p = 0.01$ and $K_i = 400$ are obtained. Meanwhile, according to the method for designing the resonant component in the PIR regulator given in Section IV-B, $K_r = 5$ is obtained to ensure the magnitude of the compensated loop gain $T_{v\_PIR}(s) \geq 20$ dB at $2f_o$. With the parameters above, the Bode diagram of $T_{v\_PIR}(s)$ when the PV panel works at MPP is depicted, as shown in Fig. 9 with the dash-dot lines. As seen, $|T_{v\_PIR}(j2f_o)| = 23$ dB, $f_c = 380$ Hz, and PM $= 88°$.

As seen in Fig. 9, all the approaches of PI + ADS, PIR + ADS, and PIR have a higher magnitude at $2f_o$, implying strong ability of suppressing the SHC. However, since the ADS is not incorporated, the crossover frequency of $T_{v\_PIR}(s)$ is far lower than that of $T_{v\_PI+ADS}(s)$ and $T_{v\_PIR+ADS}(s)$ for ensuring the system stability; the dynamic performance of the front-end boost converter with PIR is not as good as that of with PI + ADS and PIR + ADS.

D. PV Panel Operation Point Sensitivity Analysis of the Proposed Control Scheme

According to (16) and (19), if the loop gain at $2f_o$ is far larger than 1, the closed-loop output impedance of the front-end boost converter at $2f_o$ can be approximated to a negative resistor, i.e., $Z_{o\_c}(j2\omega_o) = -V_{bus}^2/P_{MPP}$. Hence, $|Z_{o\_c}(j2\omega_o)|$ increases as the maximum power extracting from the PV panel decreases. This implies that, when the maximum power extracting from the PV panel decreases, the SHC in the front-end boost converter will be reduced.

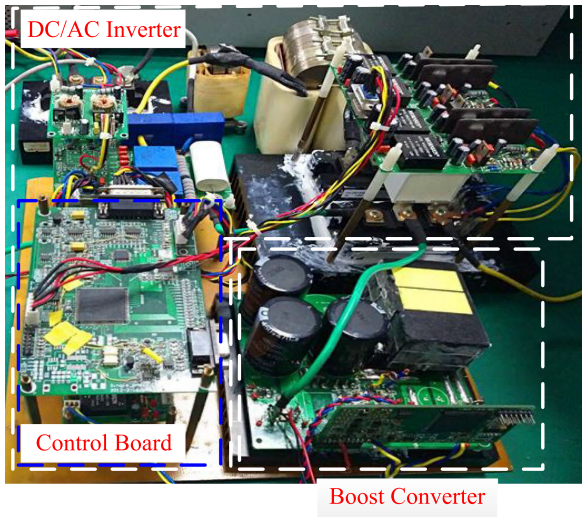


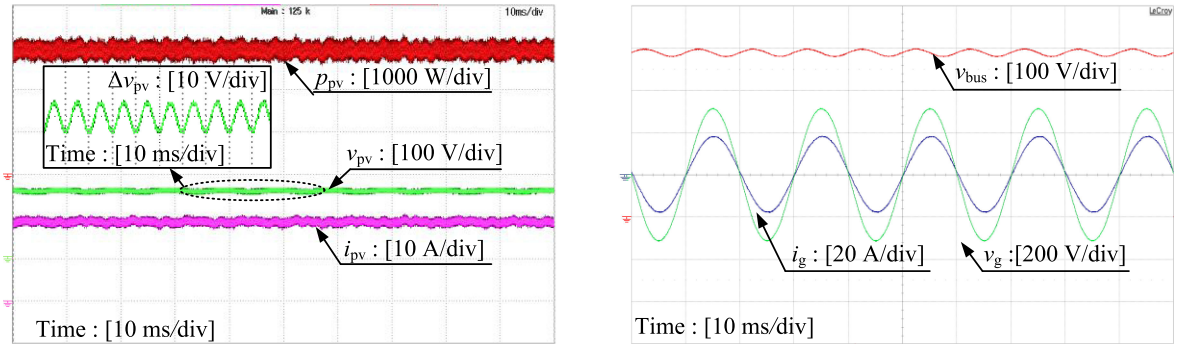
Fig. 10. Photograph of the experimental prototypes.

V. Experimental Results

In order to verify the effectiveness of the theoretical analysis and the proposed control schemes with PI + ADS and PIR + ADS, a 3-kW two-stage single-phase PV grid-connected inverter prototype, as shown in Fig. 10, is built and tested. The MPPT controller and active damping are implemented by a DSP (TMS320F2812). The key parameters of the PV panel under normal and shaded conditions, and the parameters of the prototype are listed in Tables I and II, respectively. A PV simulator Chroma 62000H–600S is adopted to imitate the PV panel here.

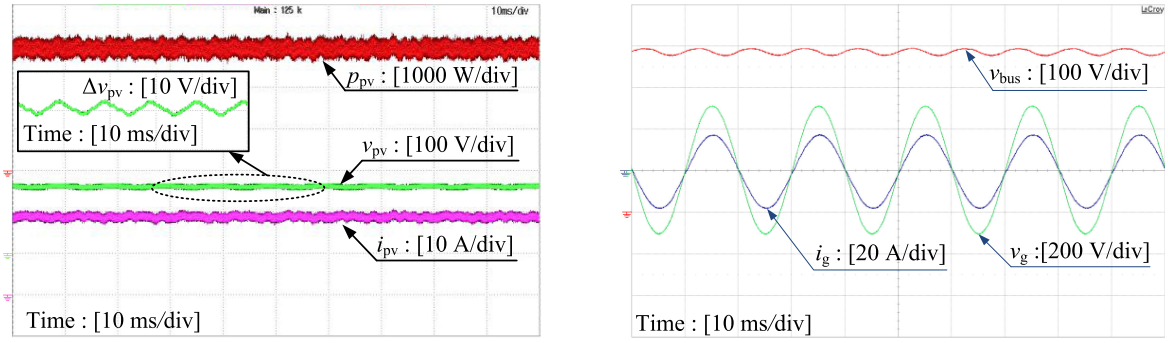
The control of the downstream dc–ac inverter includes two loops, namely, the outer intermediate bus voltage loop and the inner loop. The outer dc bus voltage loop regulates the dc bus voltage and generates the current reference for the current injected into the grid. When the SHC is bypassed by C_{bus}, there will be second harmonic voltage ripple in the dc bus voltage, leading to undesired third harmonic current in the grid current. In order to suppress the harmonic distortion of the injected grid current, the crossover frequency of the outer intermediate bus voltage loop gain should be designed far lower than $2f_o$ [26]. The LCL filter is used since it features good attenuation of the switching frequency harmonics compared with the L filter, and the filter capacitor current feedback active-clamping scheme is

$$|T_{v\_PI\ R+ADS}(j2\pi\cdot 2f_o)| \approx \frac{H_v K_{PWM} V_{bus}\sqrt{\left\{K_p + \frac{2K_r(4\pi f_o\omega_i)^2}{\left[\omega_r^2-(4\pi f_o)^2\right]^2+(8\pi f_o\omega_i)^2}\right\}^2 + \left\{\left(\frac{K_i}{2\pi f_o}\right)^2 - \frac{4\pi f_o K_r\omega_i\left[\omega_r^2-(4\pi f_o)^2\right]}{\left[\omega_r^2-(4\pi f_o)^2\right]^2+(8\pi f_o\omega_i)^2}\right\}^2}}{\sqrt{\left(1-4\pi^2(2f_o)^2 L_b C_{in}+\frac{r}{R_{MPP}}\right)^2 + 4\pi^2(2f_o)^2\left(rC_{in}+\frac{L_b}{R_{MPP}}\right)^2}} \quad (42)$$



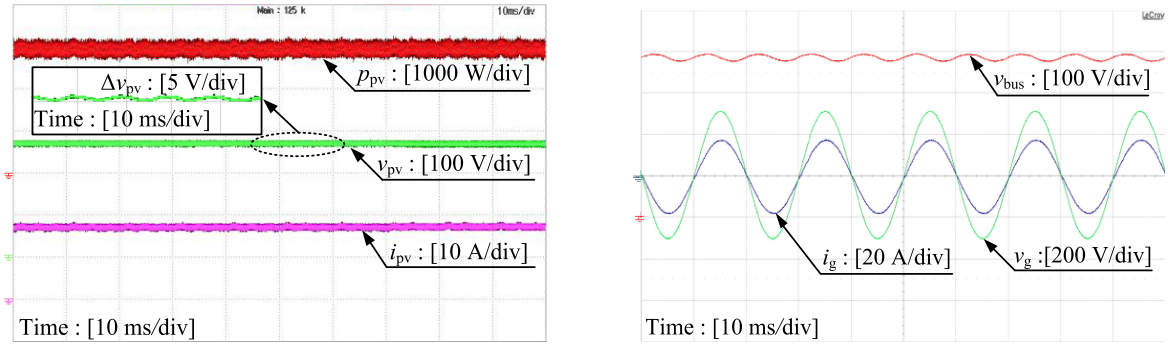
(a) (b)

Fig. 11. Steady-state waveforms with PIR. (a) Voltage, current, and output power of the PV panel. (b) Intermediate bus voltage, power grid voltage, and current injecting into the power grid.



(a) (b)

Fig. 12. Steady-state waveforms with PI + ADS. (a) Voltage, current, and output power of the PV panel. (b) Intermediate bus voltage, power grid voltage, and current injecting into the power grid.



(a) (b)

Fig. 13. Steady-state waveforms with PIR + ADS. (a) Voltage, current, and output power of the PV panel. (b) Intermediate bus voltage, power grid voltage, and current injecting into the power grid.

adopted for damping the resonance of the LCL filter to ensure the stability of the downstream dc–ac inverter [25].

Figs. 11–13 show the steady-state waveforms with PIR, PI + ADS, and PIR + ADS schemes when the PV panel operates at MPP, respectively. As seen from Fig. 11, with the PIR scheme, the SHC in the PV panel is about 2.4% and the peak-to-peak value of the PV panel output voltage is about 4 V. As seen from Fig. 12, when the PI + ADS scheme is adopted, the SHC in the PV panel is about 2.37% and the peak-to-peak value of the PV panel output voltage is about 4 V. For the PIR + ADS scheme, it can be seen from Fig. 13 that the SHC in the PV panel is about 0.74% and the peak-to-peak value of the PV panel output voltage is about 1.25 V. Obviously, compared with the PIR and PI + ADS schemes, the PIR + ADS scheme has the strongest ability of suppressing the SHC in the PV panel.

Fig. 14 shows the dynamic waveforms of the voltage, current, and output power of the PV panel with three control schemes when the PV panel power step changes between 50% and 100% rated power. As seen from Fig. 14(a), with the PIR scheme, the PV panel voltage overshoot is about 12 V and the settling time is

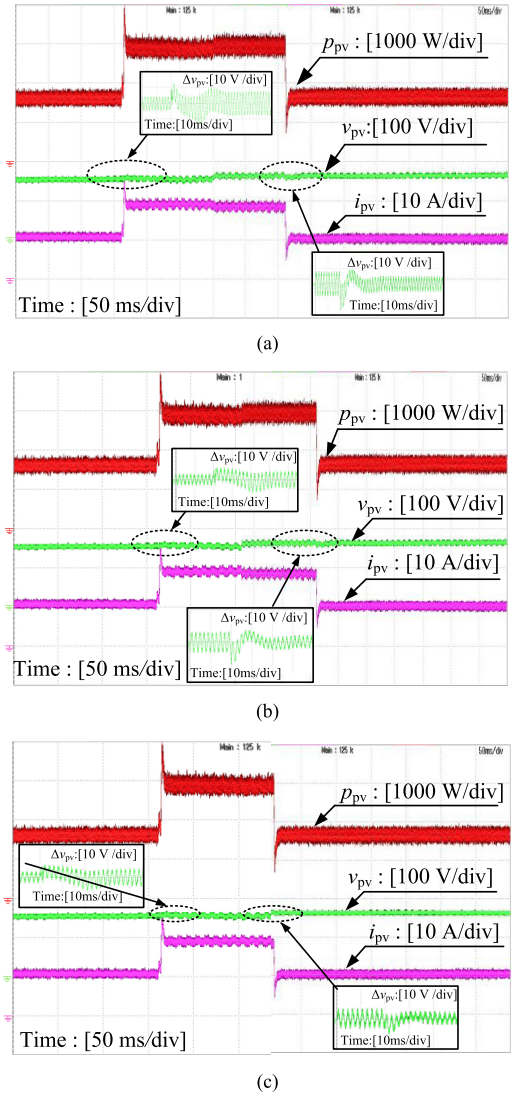


Fig. 14. Dynamic waveforms when the PV panel power step changes between 50% and 100% rated power. (a) PIR. (b) PI + ADS. (c) PIR + ADS.

about 40 ms, whereas the PV panel voltage undershoot is about 13 V and the settling time is 38 ms. As seen from Fig. 14(b), with the PI + ADS scheme, the PV panel voltage overshoot is about 4.5 V and the settling time is about 30 ms, whereas the PV panel voltage undershoot is about 4.8 V and the settling time is about 30 ms. As seen from Fig. 14(c), with the PIR + ADS scheme, the PV panel voltage overshoot is about 4.5 V and the settling time is about 30 ms, whereas the PV panel voltage undershoot is about 4.5 V and the settling time is about 28 ms.

Table III summarizes the performance comparison of these control schemes in terms of the SHC proportion in the current of the PV panel and voltage fluctuation of the PV panel when the PV panel power step changes between 50% and 100% rated power. As seen, the SHC in the PV panel is very small with three control schemes, and the PIR + ADS has the strongest ability of suppressing the SHC in the PV panel since it has the highest magnitude of the loop gain at $2f_o$. Meanwhile, the PI + ADS and PIR + ADS have better dynamic performance than the PIR scheme because they have a higher crossover frequency of the voltage loop gain. In a word, among the three control schemes, the PIR + ADS has the strongest ability of suppressing the SHC in the PV panel and has the best dynamic performance when the PV panel power step changes.

TABLE III
PERFORMANCE COMPARISON OF DIFFERENT CONTROL SCHEMES

Control Scheme	Steady Performance	Dynamic Performance	
	SHC proportion in the PV panel	Undershoot / Settling time	Overshoot / Settling time
PIR	2.4 %	12 V / 40 ms	13 V / 38 ms
PI+ADS	2.37 %	4.8 V /30 ms	4.5 V / 30 ms
PIR+ADS	0.74 %	4.5 V / 30 ms	4.5 V / 28ms

VI. CONCLUSION

The pulsating power at twice the line frequency of a two-stage single-phase PV grid-connected inverter results in the SHC in the PV panel, leading to the PV panel output power oscillation and reduced energy harvesting efficiency. From the viewpoint of impedance, the generating mechanism of the SHC is analyzed, indicating that increasing the voltage loop gain of the front-end dc–dc converter at $2f_o$ could reduce and even eliminate the SHC in the PV panel. To satisfy this requirement, PI regulator plus inductor current feedback ADS (PI + ADS) is employed for achieving high-voltage loop bandwidth. A step-by-step closed-loop parameters design method, which considers the requirements of the PM, loop gain, and SHC reduction, is presented for achieving an optimized design without trial and error. For possibly increasing the loop gain at $2f_o$, PIR regulator with ADS (PIR + ADS) is further employed, enabling the PV panel and the front-end dc–dc converter free of SHC. Finally, a 3-kW two-stage single-phase PV grid-connected inverter is fabricated and tested in the laboratory. The experimental results demonstrate that increasing the voltage loop gain at $2f_o$ could help reduce and even eliminate the SHC in the PV panel.

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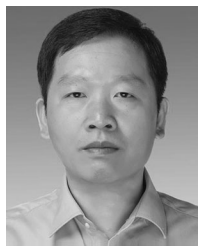

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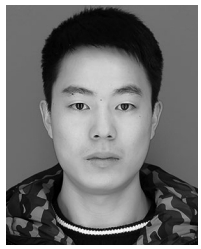

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