Reconsideration of Loop Gain and Its Measurement in DC–DC Converters

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***Abstract*—Two measurement schemes, namely, the modulation signal perturbation scheme and the pulse perturbation scheme, have been used for evaluating the loop gain of dc–dc converters. However, the two measured loop gains do not give consistent results due to the use of different forms of the injected small perturbation signal, and the difference in the two schemes cannot be distinguished by the usual averaged model. In this paper, the two loop gain measurement schemes are analyzed based on an extended-frequency-range small-signal model. Expressions of the loop gain are derived and their use in stability assessment and derivation of closed loop transfer functions is demonstrated. A sample-and-hold scheme is proposed as a simple alternative implementation of the pulse perturbation scheme. Finally, experimental prototypes of buck, boost, and buck–boost converters are tested for verification of the analytical results and the effectiveness of the sample-and-hold scheme.**

***Index Terms*—Extended-frequency-range small-signal model, loop gain, modulation signal perturbation scheme, pulse perturbation scheme, sample-and-hold.**

NOMENCLATURE

$\mathbf{A}_1, \mathbf{B}_1, \mathbf{C}_1$	State matrices and the output matrix when the switch is ON.
$\mathbf{A}_2, \mathbf{B}_2, \mathbf{C}_2$	State matrices and the output matrix when the switch is OFF.
$A(s)$	Polynomial of all the zeros in $T_0(s)$.
$B(s)$	Polynomial of all the poles in $T_0(s)$.

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v_{mod}	Modulation signal.
v_{mod1}	Sum of v_{mod} and $v_{\sin}$.
$v_{\text{mod\_}t}$, $v_{\text{mod\_}r}$	Forward and returned signals of the modulation signal perturbation scheme.
v_o	Output voltage.
$v_{\text{pul\_dy\_}c}$	Constant pulse by pulse compensation circuit.
$v_{\text{pul\_dy\_}p}$	Small-signal perturbation of duty cycle.
$v_{\text{pul\_dy\_}o}$	Duty cycle modulated by v_{mod}.
$v_{\text{pul\_dy\_}r}$, $v_{\text{pul\_dy\_}t}$	Forward and returned signals in the pulse perturbation scheme.
v_{pulse}	Pulse at the falling edge of $v_{\text{pul\_dy\_}o}$.
$v_{\text{pul\_dy\_}r1}$	Duty cycle modulated by v_{mod1}.
v_{ref}	Reference of the output voltage.
v_{saw}	Triangle carrier wave.
$v_{\text{sh\_}r}$, $v_{\text{sh\_}t}$	Forward and returned signals in the sample-and-hold scheme.
$v_{\sin}$	Small-signal sinusoidal perturbation.
$v_{\sin\text{\_mod}}$	Sum of $v_{\sin}$ and V_{bias}.
v_{sp}	Sampling pulse.
$\hat{x}$	Small-signal component of a variable x.
$\hat{x}[j(\omega + k\omega_s)]$	$\omega + k\omega_{\text{s}}$ component in $\hat{x}$.
$\mathbf{x}(t)$	State variables matrix.
Z_{mod}, Z_{pul}	Number of RHP zeros in $1 + T_{\text{mod}}$, $1 + T_{\text{pul}}$.
$Z_{\text{oc}}(j\omega)$	Closed-loop output impedance.
$Z_{o\_k}(j\omega)$	Open-loop output impedance.
ω_s	Switching angular frequency.

I. Introduction

FOR any closed-loop controlled system, the loop gain provides essential information for controller design and stability assessment [1]–[4]. Although the loop gain can be computed based on the model of the regulator and the power stage, the nonideality of the devices or the limited accuracy of the model may introduce significant error to the calculated loop gain. Therefore, it is necessary to measure the loop gain in order to correct the regulator design. Several measurement-correction iterations may be required until the final regulator design can be adopted [5]. The basic scheme of loop gain measurement is to inject a small-signal perturbation at a node of the feedback path with a network analyzer, and then obtain both the forward and returned signals at the injection point with voltage probes, which are sent to the Ref port and the Test port of the network analyzer, respectively. The signals are then processed by a built-in intermediate frequency filter of the network analyzer to extract the components at the frequency of the injected signal. The loop gain is thus determined by the ratio of the returned signal and forward signal at the injected signal frequency [6]–[10].

For dc–dc converters, it has been found that different perturbation injection points might lead to different measurement results of the loop gain [11]–[13]. Up to now, classified by the perturbation injection points, there are two loop gain measurement schemes for dc–dc converter systems, namely, the modulation signal perturbation scheme [14], [15] and the pulse perturbation scheme [16]. In the modulation signal perturbation scheme, a small-signal sinusoidal perturbation signal is injected into an analog signal node in the feedback path, such as the modulation signal node or the output voltage node. In the pulse perturbation scheme, however, a narrow pulse perturbation is directly injected into the duty cycle, and the loop gain is the ratio of the returned and forward duty cycles at the perturbation frequency. Compared with the modulation signal perturbation scheme, the pulse perturbation scheme is less frequently adopted. The pulse perturbation scheme is first proposed and used in multiloop systems [16], [17]. For a multiloop control system, the loop gain is not uniquely defined. For example, in a two-loop controlled converter consisting of a voltage loop and a current loop, perturbation can be injected into the loop through the voltage feedback path, the current feedback path or the duty cycle, which correspond to three different loop gain results. The three loop gains are found to be equivalent in stability judgment, which is explained in the Appendix. However, the one by duty-cycle perturbation or by the pulse perturbation scheme has no right-half-plane (RHP) poles, and is thus more convenient for stability assessment. Besides, in digital control systems, the discrete-time loop gain that best reveals the discretization process cannot be directly measured by the modulation signal scheme, but can be readily obtained by the pulse perturbation scheme [18], [19].

Moreover, in the experiment, it is observed that for a simple analog controlled voltage-mode converter, the modulation signal perturbation scheme also gives a different result from that by the pulse perturbation scheme. The difference in the two measurement schemes, being indistinguishable by the commonly used averaged model, has not been clearly understood. This motivates us to have a reconsideration of loop gain and its measurement schemes in dc–dc converters.

For dc–dc converters, pulsewidth modulation (PWM) is the key operation in the control circuits, and it is usually regarded as a linear operation and analyzed by an averaged model [20]–[23]. However, PWM operation generates sideband frequency components around the switching frequency and its multiples [24]–[29], which have a profound impact on the loop gain. The extended-frequency-range small-signal model for dc–dc converters has been proposed in [30], which takes into account all the sideband frequency components and greatly improves the accuracy of the mathematical model. This extended-frequency-range small-signal model will be adopted in this paper for analyzing the measurement of loop gains using the modulation signal perturbation scheme and pulse perturbation scheme.

Moreover, the implementation of the pulse perturbation scheme presented in [16] is relatively complicated since it involves the use of a pulse perturbation circuit and a pulse compensation circuit. In order to simplify the implementation, this paper proposes a novel measurement scheme with a sample-and-hold circuit, which gives results as accurate as the pulse perturbation scheme, but is simpler.

This paper is organized as follows. The operating principles of the aforementioned two loop gain measurement schemes are analyzed based on the extended-frequency-range small-signal model, and the expressions of the loop gains are derived in Section II. The applications of the two measured loop gains in stability assessment and closed-loop transfer function derivation

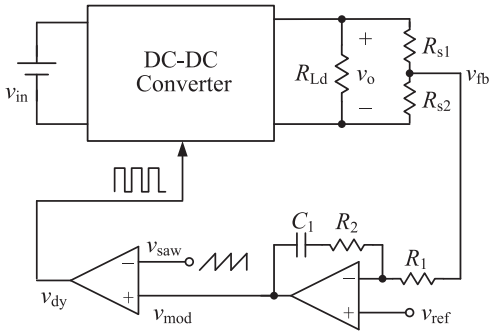


Fig. 1. Circuit diagram of closed-loop controlled of dc–dc converter.

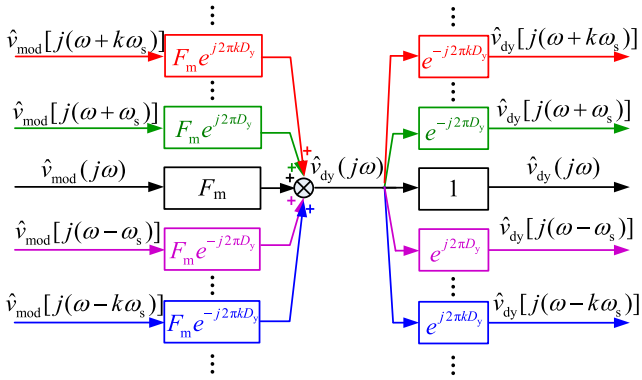


Fig. 2. Extended-frequency-range small-signal model of PWM modulator.

are demonstrated in Section III. To simplify the implementation of the pulse perturbation scheme, a sample-and-hold scheme is proposed in Section IV. In Section V, experimental prototypes of buck, boost, and buck–boost converters are used for verification of the analytical results and the accuracy of the proposed measurement scheme. Section VI concludes this paper.

II. Basic Principle of the Loop Gain Measurement Schemes

A. Extended-Frequency-Range Small-Signal Model of DC–DC Converters

Fig. 1 gives the circuit diagram of a closed-loop controlled dc–dc converter, which is composed of the power stage, the output voltage sense circuit, the voltage regulator and the PWM modulator.

The model of the PWM modulator in dc–dc converters is usually regarded as a constant, which equals to $1/V_m$, in the averaged model, where V_m is the amplitude of the saw-tooth carrier wave. However, the PWM modulator is essentially a natural sampling system [25], which generates sideband frequency components around the switching frequency and its multiples. If the perturbation frequency of the modulation signal is ω, the resulting duty cycle contains both the perturbation-frequency component and the sideband frequency components. The sideband frequencies are $\omega + k\omega_s$ $(k = \pm1, \pm2, \ldots)$, where ω_s is the switching frequency. Thus, the output voltage will contain all these frequency components through the power stage. In the closed-loop control, all the frequency components in the output voltage are fed back to the PWM modulator, contributing to additional perturbation-frequency component and sideband frequency components in the modulation signal. After sampled again by the PWM modulator, aliasing among different frequency components will occur. Considering this, the extended-frequency-range small-signal model of the PWM modulator was proposed in [30], as shown in Fig. 2, where F_m is the gain magnitude of the PWM modulator, D_y is the steady-state duty cycle, $\hat{v}_{\rm mod}[j(\omega + k\omega_s)]$ and $\hat{v}_{\rm dy}[j(\omega + k\omega_s)]$ are the components at $\omega + k\omega_s$ in the modulation signal and the duty-cycle signal, respectively.

With the model in Fig. 2, the extended-frequency-range small-signal model of dc–dc converters are given in Fig. 3 [30], where $G_{\rm vd}([j(\omega + k\omega_s)]$ is the duty-cycle-to-output-voltage transfer function at $\omega + k\omega_s$, $G_{\rm vr}[j(\omega + k\omega_s)]$ is the transfer function of the voltage regulator at $\omega + k\omega_s$, H_v is the output voltage sensor gain. The shadow blocks in Fig. 3 represent the perturbation injection points for different loop gain measuremnt schemes, which will be discussed later.

For the three basic dc–dc converters, i.e., buck, boost, and buck–boost converters, the piecewise linear state equations and output equation are expressed as

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_j\mathbf{x}(t) + \mathbf{B}_j v_{\rm in}(t) \tag{1a}$$

$$v_o(t) = \mathbf{C}_j\mathbf{x}(t) \tag{1b}$$

where $\mathbf{x}(t)$ is the state variable matrix, $\mathbf{A}_j$, $\mathbf{B}_j$, and $\mathbf{C}_j$ are the coefficient matrices, j is 1 and 2 for on-time interval and off-time interval, respectively. According to [31], the accurate duty-cycle-to-output-voltage transfer function is

$$\begin{aligned} &G_{\rm vd}(j\omega) \\ &= \left\{\begin{matrix} \mathbf{C_1}(j\omega\mathbf{I} - \mathbf{A_1})^{-1}[\mathbf{I} - e^{-j\omega D_y T_s}\mathbf{\Phi_1}]e^{-j\omega(1-D_y)T_s}\mathbf{\Phi_2} \\ + \mathbf{C_2}(j\omega\mathbf{I} - \mathbf{A_2})^{-1}[\mathbf{I} - e^{-j\omega(1-D_y)T_s}\mathbf{\Phi_2}] \end{matrix}\right\} \\ &(\mathbf{I} - e^{-j\omega T_s}\mathbf{\Phi_1}\mathbf{\Phi_2})^{-1}\mathbf{\Psi} + (\mathbf{C_1} - \mathbf{C_2})\mathbf{X}(D_yT_s) \end{aligned} \tag{2}$$

where

$$\begin{aligned} &\mathbf{\Phi_1} = e^{\mathbf{A_1}D_yT_s},\ \mathbf{\Phi_2} = e^{\mathbf{A_2}(1-D_y)T_s} \\ &\mathbf{\Psi} = (\mathbf{A_1} - \mathbf{A_2})\mathbf{X}(D_yT_s) + (\mathbf{B_1} - \mathbf{B_2})V_{\rm in} \\ &\mathbf{X}(D_yT_s) = (\mathbf{I} - \mathbf{\Phi_1}\mathbf{\Phi_2})^{-1} \\ &\cdot\left[\mathbf{\Phi_1}\mathbf{A_2}^{-1}(e^{\mathbf{A_2}(1-D_y)T_s} - \mathbf{I})\mathbf{B_2} + \mathbf{A_1}^{-1}(e^{\mathbf{A_1}D_yT_s} - \mathbf{I})\mathbf{B_1}\right]V_{\rm in}. \end{aligned} \tag{3}$$

For better accuracy, the switching ripple in the modualtion signal has been taken into account when calculating F_m in [30]; thus, explicitly incorporating the effect of the slope of the steady-state modulation signal on F_m. This effect is similar to the slope compensation in peak current control. Fig. 4 provides the key waveforms of the modulation process, where $V'_{\rm mod}(D_yT_s)$ is the slope of the modulation signal in the steady state. Based on the derivation in [30], the corresponding gain amplitude of the

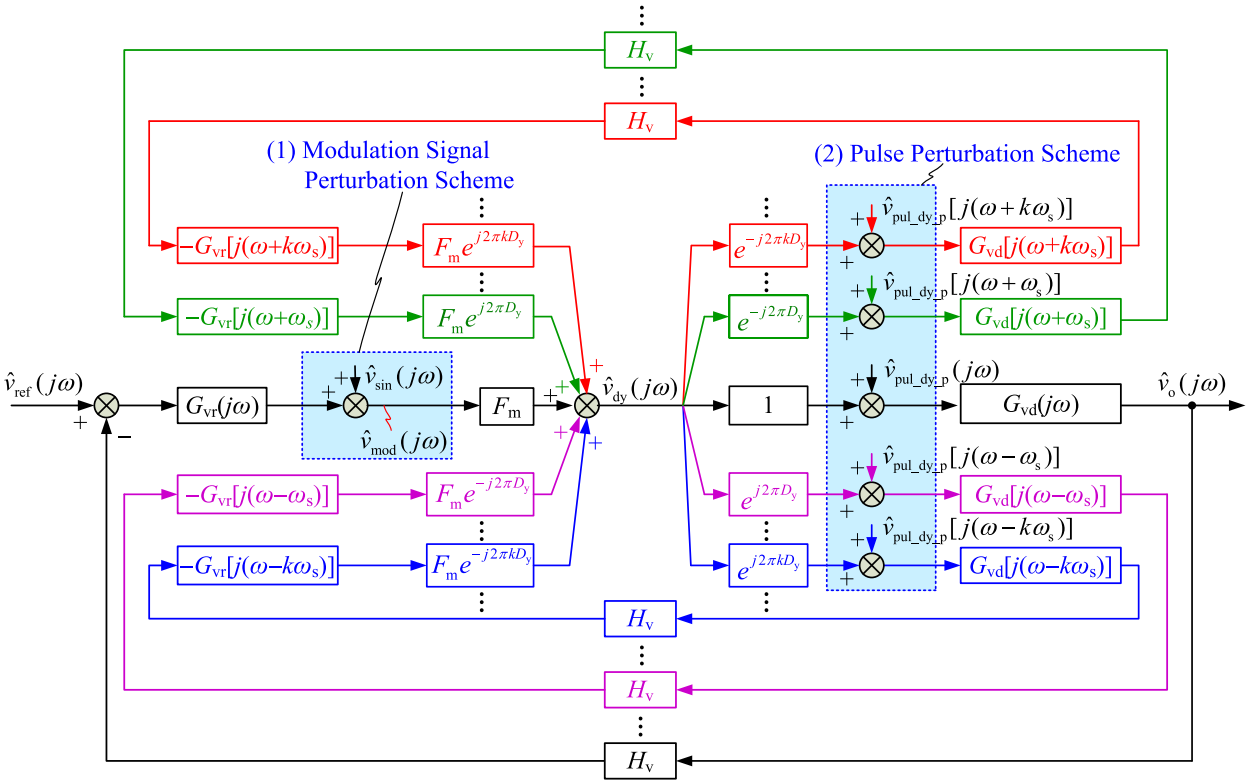


Fig. 3. Control block diagram of the extended-frequency-range small-signal model of dc–dc converters with the modulation signal perturbation scheme and the pulse perturbation scheme.

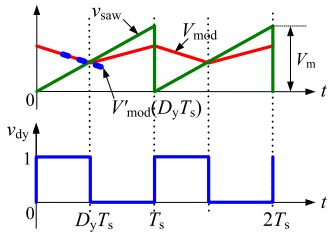


Fig. 4 Key waveforms of the PWM process.

PWM modulator is given by

$$F_m = \frac{1}{V_m - V'_{\text{mod}}(D_y T_s)}. \tag{4}$$

The PI regualtor is adopted as the voltage regulator here, expressed as

$$G_{\text{vr}}(s) = K_p + \frac{K_i}{s}. \tag{5}$$

If the corner frequency of the PI regulator is far below the switching frequency, the respective expression of F_m for the buck, boost, and buck–boost converters are obtained as

$$F_{m\_\text{bu}} = \frac{1}{V_m + \frac{(1-D_y)K_p H_v V_{\text{in}} T_s}{LC}(R_c C + 0.5 D_y T_s)} \tag{6a}$$

$$F_{m\_\text{bst}} = \frac{1}{V_m - \frac{K_p H_v V_{\text{in}} T_s}{(1-D_y)R_{\text{Ld}} C}} \tag{6b}$$

$$F_{m\_\text{bb}} = \frac{1}{V_m - \frac{D_y K_p H_v V_{\text{in}} T_s}{(1-D_y)R_{\text{Ld}} C}} \tag{6c}$$

where V_{in} is the input voltage, L is the inductor, C is the output capacitor, R_c is the equivalent series resistance (ESR) of the output capacitor, and R_{Ld} is the load resistor.

As seen in Fig. 3, each frequency component forms an independent loop of its own at the node of $\hat{v}_{\text{dy}}(j\omega)$. In dc–dc converters, the essential control objective is to regulate the output voltage $v_o(j\omega)$ to track its reference $v_{\text{ref}}(j\omega)$. The sideband components have an effect on the tracking ability via aliasing. To see this clearly, the infinite loops constructed by the sideband frequency components can be simplified. From Fig. 3, the transfer function from $\hat{v}_{\text{mod}}(j\omega)$ to $\hat{v}_{\text{dy}}(j\omega)$ can be derived as

$$G_{\text{PWM}}(j\omega) = \frac{\hat{v}_{\text{dy}}(j\omega)}{\hat{v}_{\text{mod}}(j\omega)} = \frac{F_m}{1 + \sum_{\substack{k=-\infty \\ k\neq 0}}^{+\infty} T_0[j(\omega + k\omega_s)]} \tag{7}$$

where $T_0[j(\omega + k\omega_s)]$ represents the loop gain of sideband component at $\omega + k\omega_s$ expressed as

$$T_0[j(\omega + k\omega_s)] = G_{\text{vr}}[j(\omega + k\omega_s)] F_m G_{\text{vd}}[j(\omega + k\omega_s)] H_v. \tag{8}$$

Obviously, $G_{\text{PWM}}(j\omega)$ is no longer a constant as would be described by the averaged model, but is related to $T_0[j(\omega + k\omega_s)]$.

Using (7), Fig. 3 can be simplified as Fig. 5, from which the complete loop gain expression of the extended-frequency- range

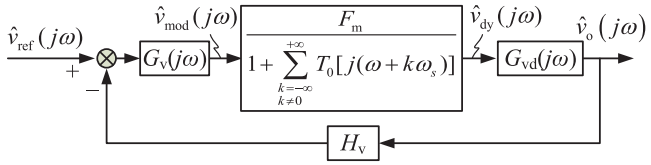


Fig. 5. Simplified control block diagram of the extended-frequency-range small-signal model of dc–dc converters.

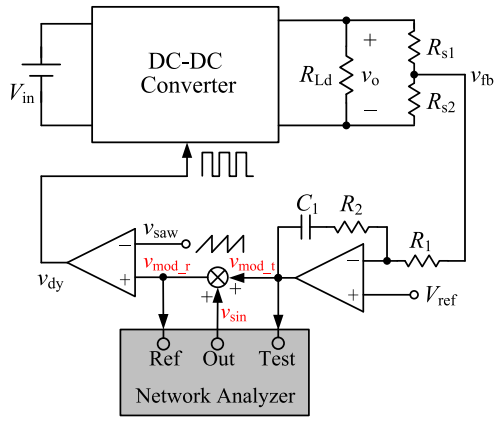


Fig. 6. Modulation signal perturbation scheme.

small-signal model is derived as

$$T(j\omega)=\frac{T_0(j\omega)}{1+\sum_{\substack{k=-\infty\\k\neq0}}^{+\infty}T_0[j(\omega+k\omega_s)]}. \tag{9}$$

B. Modulation Signal Perturbation Scheme

Fig. 6 shows the schematic diagram of the modulation signal perturbation scheme. The Out port of the network analyzer generates a sinusoidal perturbation signal $v_{\sin}$. For the safety of the network analyzer, a transformer is usually connected to the Out port to isolate the network analyzer from the converter in practice, but is omitted here for convenience of illustration. $v_{\sin}$ is imposed into the output of the voltage regulator, giving the forward and returned modulation signals through the feedback loop, namely, v_{mod_r} and v_{mod_t}, which are then sent to the Ref and Test ports of the network analyzer, respectively. By plotting the Bode diagram of $-$Test/Ref, the loop gain is obtained.

The control block diagram of the extended-frequency-range small-signal model of dc–dc converter with the modulation signal perturbation scheme is given in Fig. 3. The modulation signal perturbation scheme is equivelant to injecting $\hat{v}_{\sin}(j\omega)$ into the node $\hat{v}_{\mathrm{mod}}(j\omega)$ in Fig. 5. Obviously, the injected perturbation signal has no effect on the loop of the sideband frequencies. Thus, the measured loop gain by the modulation signal perturbation scheme is consistent with the real one, i.e.,

$$T_{\mathrm{mod}}(j\omega)=T(j\omega)=\frac{T_0(j\omega)}{1+\sum_{\substack{k=-\infty\\k\neq0}}^{+\infty}T_0[j(\omega+k\omega_s)]}. \tag{10}$$

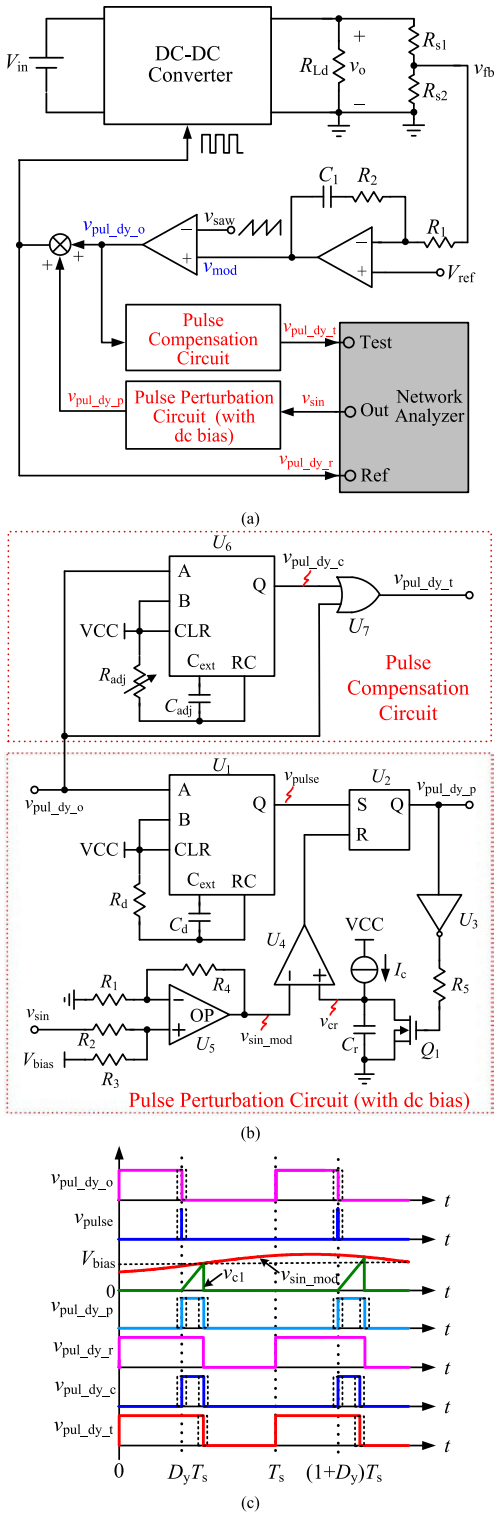


Fig. 7. Pulse perturbation scheme. (a) Schematic diagram. (b) Pulse perturbation circuit and pulse compensation circuit. (c) Key operating waveforms.

C. Pulse Perturbation Scheme

Fig. 7(a) illustrates the schematic diagram of the pulse perturbation scheme. The network analyzer sends a sinusoidal signal $v_{\sin}$ to the pulse perturbation circuit. In the pulse perturbation circuit, a dc bias voltage is first imposed on $v_{\sin}$, and then

a narrow pulse perturbation signal $v_{\text{pul\_dy\_}p}$ is generated. The pulsewidth of $v_{\text{pul\_dy\_}p}$ is modulated by $v_{\sin}$. After that, $v_{\text{pul\_dy\_}p}$ is added to the original duty cycle $v_{\text{pul\_dy\_}o}$ at its falling-edge, giving $v_{\text{pul\_dy\_}r}$. In the meanwhile, $v_{\text{pul\_dy\_}o}$ is sent to the pulse compensation circuit to compensate a constant pulsewidth, generating $v_{\text{pul\_dy\_}t}$. The forward and returned duty cycles, $v_{\text{pul\_dy\_}r}$ and $v_{\text{pul\_dy\_}t}$, are sent to the Ref and Test ports of the network analyzer, respectively. By plotting the Bode diagram of $-$Test/Ref, the loop gain is obtained.

The detailed implementation of the pulse perturbation circuit and the pulse compensation circuit is shown in Fig. 7(b), and the key waveforms are given in Fig. 7(c). As seen, when the monostable trigger U_1 detects the falling edge of $v_{\text{pul\_dy\_}o}$, a narrow pulse signal v_{pulse} is generated, whose pulsewidth is determined by R_d and C_d. Then, v_{pulse} is sent to the S port of the RS trigger U_2, setting $v_{\text{pul\_dy\_}p}$ to a high level. The inverter U_3 outputs a low level signal to turn OFF the transistor Q_1. Subsequently, the constant current source I_c starts charging the capacitor C_r from zero. As soon as the voltage of v_{cr} reaches the sinusoidal modulated voltage with a dc bias, $v_{\sin\_\text{mod}}$ ($v_{\sin\_\text{mod}} = v_{\sin} + V_{\text{bias}}$, where V_{bias} is the dc bias), the comparator U_4 would output a high level signal, and it is sent to R port of U_2, toggling $v_{\text{pul\_dy\_}p}$ from high to low. Then, the output of inverter U_2 would turn ON Q_1, discharging C_r to zero sharply. Thus, the pulsewidth of $v_{\text{pul\_dy\_}o}$ is sinusoidally modulated cycle by cycle.

The dc bias in $v_{\sin\_\text{mod}}$ would result in an additional constant pulsewidth in $v_{\text{pul\_dy\_}p}$, leading to a constant pulsewidth difference between $v_{\text{pul\_dy\_}o}$ and $v_{\text{pul\_dy\_}r}$. Therefore, $v_{\text{pul\_dy\_}o}$ should be compensated as shown in the pulse compensation circuit in Fig. 7(b). The monostable trigger U_6 detects the falling edge of $v_{\text{pul\_dy\_}o}$, and outputs a pulse signal $v_{\text{pul\_dy\_}c}$, whose pulsewidth can be adjusted by R_{adj} and C_{adj} to reach the same pulsewidth of $v_{\text{pul\_dy\_}p}$. By sending $v_{\text{pul\_dy\_}c}$ and $v_{\text{pul\_dy\_}o}$ into the OR gate, U_7, $v_{\text{pul\_dy\_}t}$ is obtained. Finally, $v_{\text{pul\_dy\_}r}$ and $v_{\text{pul\_dy\_}t}$ are send to Ref port and Test port of the network analyzer, respectively, to give the loop gain result of T_{pul}.

As shown in Fig. 7, the pulsewidth of the perturbation signal is modulated by $v_{\sin}$. According to the frequency characteristic of the PWM modulator, the small-signal components in the duty cycle include not only the perturbation frequency ω, but also the sideband frequencies $\omega + k\omega_{\text{s}}$ ($k = \pm1, \pm2, \pm3, \ldots$), expressed as [30]

$$\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)] = \hat{v}_{\text{pul\_dy\_}p}(j\omega)e^{-j2\pi kD_y}. \tag{11}$$

As seen in (11), the sideband frequency component $\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)]$ has the same amplitude as the perturbation signal $\hat{v}_{\text{pul\_dy\_}p}(j\omega)$, but the initial phase of $\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)]$ has a lagging phase of $2\pi kD_y$ with respect to $\hat{v}_{\text{pul\_dy\_}p}(j\omega)$. The control block diagram of the extended-frequency-range small-signal model of dc–dc converter with the pulse perturbation scheme is also given in Fig. 3. Obviously, infinite frequency components, i.e., $\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)]$ ($k = 0, \pm1, \pm2, \ldots$) are injected into the feedback loop in the pulse perturbation scheme, which is found to be different from the modulation signal perturbation scheme.

Referring to Fig. 3, all the injected signals in the pulse perturbation scheme, $\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)]$ ($k = 0, \pm1, \pm2, \ldots$), will have an effect on $\hat{v}_{\text{pul\_dy\_}t}(j\omega)$. Using Mason's gain formula, the closed-loop transfer function of any frequency component $\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)]$ to $\hat{v}_{\text{pul\_dy\_}t}(j\omega)$ can be derived as

$$\begin{aligned}\hat{v}_{\text{pul\_dy\_}t\_k}(j\omega) &= \hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)]\cdot \\ &\frac{-G_{\text{vd}}[j(\omega + k\omega_s)]G_{\text{vr}}[j(\omega + k\omega_s)]H_v F_m e^{j2\pi kD_y}}{1 + \sum_{m=-\infty}^{+\infty} T_0[j(\omega + m\omega_s)]} \\ &= \frac{-T_0[j(\omega + k\omega_s)]e^{j2\pi kD_y}}{1 + \sum_{m=-\infty}^{+\infty} T_0[j(\omega + m\omega_s)]}\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)].\end{aligned} \tag{12}$$

Taking all the frequency components into consideration, $\hat{v}_{\text{pul\_dy\_}t}(j\omega)$ is the sum of (12) for k ranging from $-\infty$ to $+\infty$ on the basis of superposition theorem, i.e.,

$$\begin{aligned}\hat{v}_{\text{pul\_dy\_}t}(j\omega) &= \sum_{k=-\infty}^{+\infty} \hat{v}_{\text{pul\_dy\_}t\_k}(j\omega) \\ &= \frac{-\sum_{k=-\infty}^{+\infty} T_0[j(\omega + k\omega_s)]e^{j2\pi kD_y}\hat{v}_{\text{pul\_dy\_}p}[j(\omega + k\omega_s)]}{1 + \sum_{k=-\infty}^{+\infty} T_0\,[j(\omega + k\omega_s)]}.\end{aligned} \tag{13}$$

Substitution of (11) into (13) yields

$$\hat{v}_{\text{pul\_dy\_}t}(j\omega) = \frac{-\sum_{k=-\infty}^{+\infty} T_0[j(\omega + k\omega_s)]}{1 + \sum_{k=-\infty}^{+\infty} T_0[j(\omega + k\omega_s)]}\hat{v}_{\text{pul\_dy\_}p}(j\omega) \tag{14}$$

$\hat{v}_{\text{pul\_dy\_}r}(j\omega)$ is the sum of $\hat{v}_{\text{pul\_dy\_}p}(j\omega)$ and $\hat{v}_{\text{pul\_dy\_}t}(j\omega)$; thus,

$$\begin{aligned}\hat{v}_{\text{pul\_dy\_}r}(j\omega) &= \hat{v}_{\text{pul\_dy\_}p}(j\omega) + \hat{v}_{\text{pul\_dy\_}t}(j\omega) \\ &= \frac{1}{1 + \sum_{k=-\infty}^{+\infty} T_0[j(\omega + k\omega_s)]}\hat{v}_{\text{pul\_dy\_}p}(j\omega).\end{aligned} \tag{15}$$

Combining (14) and (15), the measured loop gain by the pulse perturbation scheme can be expressed as

$$T_{\text{pul}}(j\omega) = -\frac{\hat{v}_{\text{pul\_dy\_}t}(j\omega)}{\hat{v}_{\text{pul\_dy\_}r}(j\omega)} = \sum_{k=-\infty}^{+\infty} T_0[j(\omega + k\omega_s)]. \tag{16}$$

III. Applications of the Measured Loop Gains in Stability Assessment and Closed-Loop Transfer Function Derivation

A. Stability Assessments Using $T_{mod}(s)$ and $T_{pul}(s)$

It can be seen from (10) and (16) that the measured loop gain $T_{\text{pul}}(j\omega)$ deviates from $T_{\text{mod}}(j\omega)$, and the relationship between T_{mod} and T_{pul} is found to be

$$T_{\text{mod}}\,(s) = \frac{T_0(s)}{1 + T_{\text{pul}}(s) - T_0(s)}. \tag{17}$$

Therefore, we have

$$1 + T_{\text{mod}}\,(s) = \frac{1 + T_{\text{pul}}(s)}{1 + T_{\text{pul}}(s) - T_0(s)}. \tag{18}$$

For the closed-loop systems, if $1 + T(s)$ has no RHP zero, i.e., $Z = 0$, the system is considered stable. As seen in (8),

$T_0(s)$ has no RHP pole. Thus, it can be found from (18) that $1+T_{\text{mod}}(s)$ and $1+T_{\text{pul}}(s)$ have the same number of RHP zeros, i.e., $Z_{\text{mod}}=Z_{\text{pul}}$. In other words, T_{mod} is as effective as T_{pul} for estimating the stability of the converters. According to the Nyquist stability criterion, Z is calculated as follows. Supposing P is the number of the open-loop RHP poles, R is the number of times the phase-frequency Bode plot of $T(s)$ crosses the phase line (s) $n\times 180^\circ$ $(n=\pm1,\pm3,\pm5,\ldots)$ when the magnitude of the loop gain is above 0 dB, we have $Z=P-R$. It should be pointed out that $R=2(N_+-N_-)$, where N_+ and N_- are the numbers of positive crossing and negative crossing, respectively, which can be found easily from the Bode plot.

In the following, the stability estimation with the measured loop gains T_{mod} and T_{pul} will be discussed. Rewriting $T_0(s)$, we have

$$T_0(s)=G_{\text{vd}}(s)F_mH_vG_{\text{vr}}(s)\triangleq\frac{A(s)}{B(s)} \tag{19}$$

where $A(s)$ is the polynomial of all the zeros in $T_0(s)$ and $B(s)$ is the polynomial of all the poles in $T_0(s)$. Substitution of (19) into (16) leads to

$$\begin{aligned}T_{\text{pul}}(s)&=\sum_{k=-\infty}^{\infty}\frac{A(s+jk\omega_s)}{B(s+jk\omega_s)}\\&=\frac{\sum_{k=-\infty}^{\infty}\left[A(s+jk\omega_s)\prod\limits_{\substack{m=-\infty,\\ m\neq k}}^{\infty}B(s+jm\omega_s)\right]}{\prod\limits_{k=-\infty}^{\infty}B(s+jk\omega_s)}.\end{aligned} \tag{20}$$

Since there is no RHP pole in $G_{\text{vd}}(s)$ and $G_{\text{vr}}(s)$, $B(s)$ would not have a RHP zero, nor does $\prod\limits_{k=-\infty}^{\infty}B(s+jk\omega_s)$ in (20). This means that T_{pul} has no RHP pole, i.e., $P_{\text{pul}}=0$. Thus, the Nyquist stability criterion can be simplified as follows. If the Bode plot of T_{pul} does not cross the phase line (s) $n\times180^\circ$ $(n=\pm1,\pm3,\pm5,\ldots)$, i.e., $R_{\text{pul}}=0$, the system is stable. That is to say, the stability estimation of the converter requires inspecting only the Bode plot of T_{pul}.

Substitution of (19) into (10) yields (21) as shown at the bottom of this page.

As seen from (21), the denominator of T_{mod} is related to both $A(s)$ and $B(s)$. Therefore, the number of the RHP poles in T_{mod} might not be zero, especially in the boost converter and the buck–boost converter, where $G_{\text{vd}}(s)$ usually contains RHP zeros, increasing the possibility of having RHP poles in T_{mod}. Thus, the assessment of the stability of the converters with T_{mod} requires not only the Bode plot of T_{mod}, but also the number of its RHP poles. However, from (21), it is difficult to know the RHP poles in T_{mod}. Therefore, T_{mod} cannot estimate the stability of the converters easily in the case of $P_{\text{mod}}\neq0$ and $R_{\text{mod}}\neq0$.

Since T_{mod} is the actual loop gain for the analysis and design, it is often expected to assess the stability by T_{mod}. To achieve this goal, P_{mod} has to be figured out in a simple way. On the grounds that $1+T_{\text{mod}}(s)$ and $1+T_{\text{pul}}(s)$ have the same number of RHP zeros, i.e., $Z_{\text{mod}}=Z_{\text{pul}}$, we have

$$P_{\text{mod}}-R_{\text{mod}}=P_{\text{pul}}-R_{\text{pul}}. \tag{22}$$

It has been illustrated above that $P_{\text{pul}}=0$; thus, (22) can be simplified as

$$P_{\text{mod}}=R_{\text{mod}}-R_{\text{pul}}. \tag{23}$$

It means that P_{mod} can be determined by the difference between R_{mod} and R_{pul}, which can be read from the Bode plots readily. As a conclusion, the stability can be judged by T_{mod} with the assistance of T_{pul} for computing P_{mod}.

B. Closed-Loop Transfer Function Derivation Using $T_{mod}(s)$ and $T_{pul}(s)$

For a closed-loop controlled converter, there are mainly three closed-loop transfer functions that describe the dynamic performance, namely, the reference-to-output transfer function, the audiosusceptibility, and the output impedance. The reference-to-output transfer function indicates the ability of tracking a reference voltage, the audiosusceptibility represents the transfer function from the input voltage to the output voltage, and the closed-loop output impedance represents the transfer function from the load current to the output voltage. The shaded blocks in Fig. 8 illustrate the control function with reference perturbation and input voltage perturbation. The load current perturbation is similar to the input voltage perturbation, and is omitted in the block diagram.

From Fig. 8, the closed-loop transfer function from the reference $\hat{v}_{\text{ref}}(j\omega)$ to the output voltage $\hat{v}_o(j\omega)$ is

$$\hat{v}_o(j\omega)=\frac{1}{H_v}\frac{T_{\text{mod}}(j\omega)}{1+T_{\text{mod}}(j\omega)}\hat{v}_{\text{ref}}(j\omega). \tag{24}$$

Based on (17), we have

$$\frac{T_{\text{mod}}(j\omega)}{1+T_{\text{mod}}(j\omega)}=\frac{T_0(j\omega)}{1+T_{\text{pul}}(j\omega)}. \tag{25}$$

Therefore, (24) can be rewritten as

$$\hat{v}_o(j\omega)=\frac{1}{H_v}\frac{T_0(j\omega)}{1+T_{\text{pul}}(j\omega)}\hat{v}_{\text{ref}}(j\omega). \tag{26}$$

$$T_{\text{mod}}(s)=\frac{\frac{A(s)}{B(s)}}{1+\sum_{\substack{k=-\infty,\\ k\neq0}}^{\infty}\frac{A(s+jk\omega_s)}{B(s+jk\omega_s)}}=\frac{A(s)\prod_{\substack{m=-\infty,\\ m\neq0}}^{\infty}B(s+jm\omega_s)}{\prod\limits_{m=-\infty}^{\infty}B(s+jm\omega_s)+\sum_{\substack{k=-\infty,\\ k\neq0}}^{\infty}\left[A(s+jk\omega_s)\prod\limits_{\substack{m=-\infty,\\ m\neq k}}^{\infty}B(s+jm\omega_s)\right]} \tag{21}$$

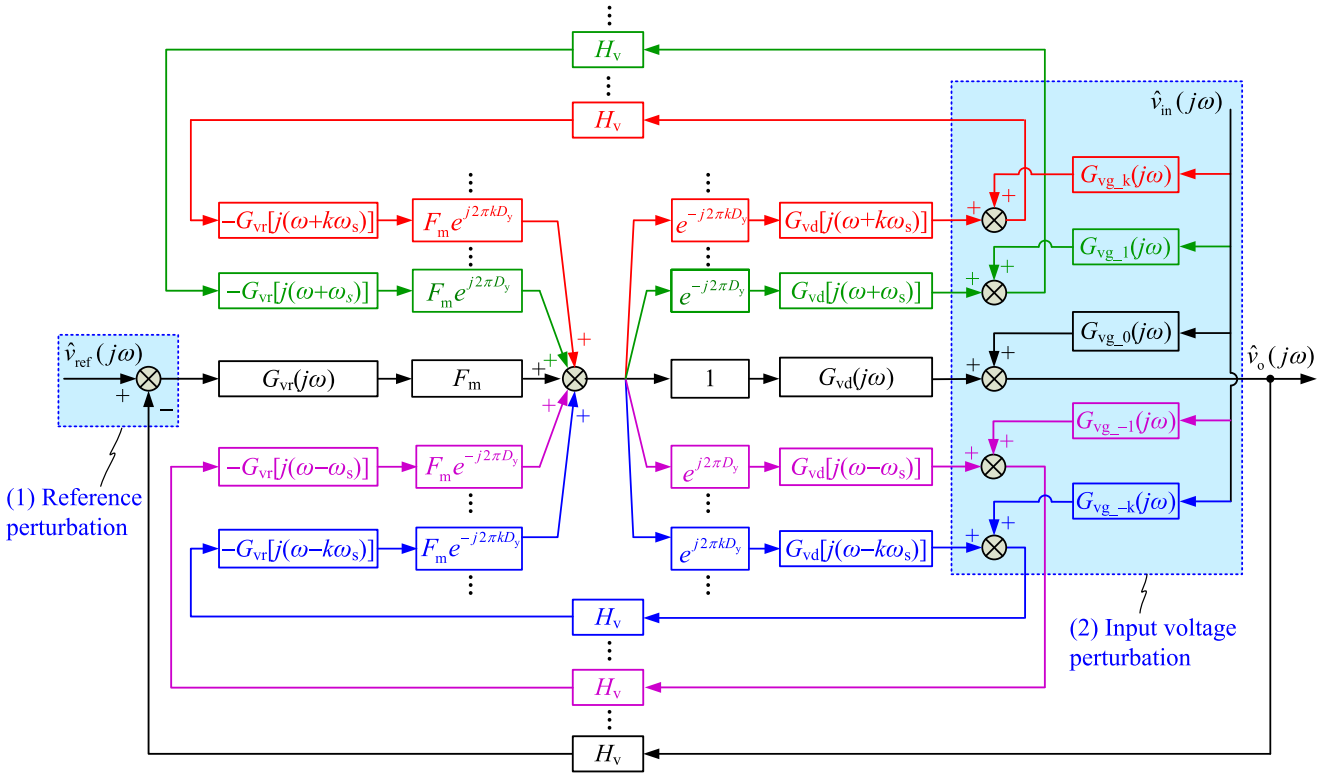


Fig. 8. Control block diagram of the extended-frequency-range small-signal model of dc–dc converters with reference and input votlage perturbations.

From (24), we can see that the tracking ability of the converter can be fully described by $T_{\rm mod}(j\omega)$. The larger the magnitude of $T_{\rm mod}(j\omega)$, the better the tracking ability.

From (26), $T_{\rm pul}(j\omega)$ can also reflect the tracking ability, but it requires the information of $T_0(j\omega)$. Thus, $T_{\rm mod}(j\omega)$ is more convenient in analyzing the tracking ability of a dc–dc converter. Note that if the sideband components are negligible, we have

$$T_{\rm mod}\,(j\omega) = T_{\rm pul}(j\omega) = T_0(j\omega). \tag{27}$$

Then, the reference-to-output transfer function becomes the widely used average model, i.e.,

$$\hat{v}_o\,(j\omega) = \frac{1}{H_v}\frac{T_0\,(j\omega)}{1+T_0\,(j\omega)}\hat{v}_{\rm ref}(j\omega). \tag{28}$$

Regarding the input voltage, we observe from Fig. 8 that for a single-frequency perturbation of the input voltage $\hat{v}_{\rm in}(j\omega)$, the output voltage response contains sideband components even under open-loop operation. Here, we define $G_{\rm vg\_k}(j\omega)\,(k=0,\pm1,\pm2,\ldots)$ as the open-loop transfer function from $\hat{v}_{\rm in}(j\omega)$ to the $\omega+k\omega_s$ components even under open-loop operation. Here, we define $G_{\rm vg\_k}(j\omega)\,(k=0,\pm1,\pm2,\ldots)$ as the open-loop transfer function from $\hat{v}_{\rm in}(j\omega)$ to the $\omega+k\omega_{\rm s}$ component in the output voltage $\hat{v}_o[j(\omega+k\omega_s)]$, i.e.,

$$G_{{\rm vg}\_k}(j\omega) \triangleq \frac{\hat{v}_o[j(\omega+k\omega_s)]}{\hat{v}_{\rm in}(j\omega)} \tag{29}$$

which gives the open-loop audiosusceptibility. According to Fig. 8, using Mason's gain formula, the closed-loop audio-susceptibility $G_{\rm vgc}(j\omega)$ can be obtained as

$$G_{\rm vgc}(j\omega) = \frac{\hat{v}_o(j\omega)}{\hat{v}_{\rm in}(j\omega)} = \frac{G_{\rm vg\_0}(j\omega)}{1+T_{\rm mod}\,(j\omega)} - \sum_{\substack{k=-\infty\\k\neq0}}^{k=+\infty}\frac{T_{\rm mod}\,[j(\omega+k\omega_s)]}{1+T_{\rm mod}\,[j(\omega+k\omega_s)]}\frac{G_{\rm vd}(j\omega)e^{j2\pi kD_y}}{G_{\rm vd}[j(\omega+k\omega_s)]}G_{{\rm vg}\_k}(j\omega). \tag{30}$$

Based on (25), $G_{\rm vgc}(j\omega)$ can also be expressed in terms of $T_{\rm pul}(j\omega)$ as

$$G_{\rm vgc}(j\omega) = \frac{1+T_{\rm pul}(j\omega)-T_0(j\omega)}{1+T_{\rm pul}(j\omega)}G_{\rm vg\_0}(j\omega) - \sum_{\substack{k=-\infty\\k\neq0}}^{k=+\infty}\frac{T_0[j(\omega+k\omega_s)]}{1+T_{\rm pul}(j\omega)}\frac{G_{\rm vd}(j\omega)e^{j2\pi kD_y}}{G_{\rm vd}[j(\omega+k\omega_s)]}G_{{\rm vg}\_k}(j\omega). \tag{31}$$

Similarly, the open-loop output impedance can be found. Also, define $Z_{\rm o\_k}(j\omega)\,(k=0,\pm1,\pm2,\ldots)$ as

$$Z_{\rm o\_k}(j\omega) \triangleq -\frac{\hat{v}_o[j(\omega+k\omega_s)]}{\hat{i}_o(j\omega)} \tag{32}$$

where $\hat{i}_o(j\omega)$ is the output current perturbation. The closed-loop output impedance $Z_{\rm oc}(j\omega)$ can be found as

$$Z_{\rm oc}(j\omega) = -\frac{\hat{v}_o(j\omega)}{\hat{i}_o(j\omega)} = \frac{Z_{o\_0}(j\omega)}{1+T_{\rm mod}\,(j\omega)} - \sum_{\substack{k=-\infty \\ k\neq 0}}^{k=+\infty} \frac{T_{\rm mod}\,[j(\omega+k\omega_s)]}{1+T_{\rm mod}\,[j(\omega+k\omega_s)]} \frac{G_{\rm vd}(j\omega)e^{j2\pi kD_y}}{G_{\rm vd}[j(\omega+k\omega_s)]} Z_{\rm o\_k}(j\omega). \tag{33}$$

$Z_{\rm oc}(j\omega)$ can also be expressed in terms of $T_{\rm pul}(j\omega)$ as

$$Z_{\rm oc}(j\omega) = \frac{1+T_{\rm pul}(j\omega)-T_0(j\omega)}{1+T_{\rm pul}(j\omega)} Z_{o\_0}(j\omega) - \sum_{\substack{k=-\infty \\ k\neq 0}}^{k=+\infty} \frac{T_0[j(\omega+k\omega_s)]}{1+T_{\rm pul}(j\omega)} \frac{G_{\rm vd}(j\omega)e^{j2\pi kD_y}}{G_{\rm vd}[j(\omega+k\omega_s)]} Z_{\rm o\_k}(j\omega). \tag{34}$$

Accurate expressions of $G_{\rm vg\_0}(j\omega)$ and $Z_{\rm o\_0}(j\omega)$ have been derived from time-varying system theory [32], [33], and the expressions of $G_{\rm vg\_k}(j\omega)$ and $Z_{\rm o\_k}(j\omega)$ when k is nonzero can also be obtained easily with the same method.

From (30) and (33), we can see that the closed-loop audiosusceptibility and the closed-loop output impedance are solely determined by $T_{\rm mod}(j\omega)$. By increasing the magnitude of $T_{\rm mod}(j\omega)$, $||T_{\rm mod}(j\omega)||$, and decreasing $||T_{\rm mod}[j(\omega+k\omega_{\rm s})]||\,(k\neq 0)$ at the same time, the magnitudes of $G_{\rm vgc}(j\omega)$ and $Z_{\rm oc}(j\omega)$ can be reduced. In other words, to suppress the effect of the input voltage or load current perturbation on the output voltage, we need to increase the bandwidth while reducing the magnitudes of the loop gain at the sideband frequencies. Since the sideband frequencies are usually above the Nyquist frequency, the loop gain in the high-frequency range would be attenuated significantly, which is consistent with the usual design rules of feedback regulators. From (31) and (33), $T_{\rm pul}(j\omega)$ can give the closed-loop audiosusceptibility and the closed-loop output impedance, but the information of $T_0(j\omega)$ is also required. Thus, $T_{\rm mod}(j\omega)$ is more convenient for analyzing the closed-loop audiosusceptibility and the closed-loop output impedance of a dc–dc converter. Again, if the sideband components are negligible, (27) holds true, the model simply reduces to the widely used average model, i.e.,

$$G_{\rm vgc}(j\omega) = \frac{G_{\rm vg\_0}(j\omega)}{1+T_0(j\omega)} \tag{35}$$

$$Z_{\rm oc}(j\omega) = \frac{Z_{o\_0}(j\omega)}{1+T_0(j\omega)}. \tag{36}$$

IV. Sample-and-Hold Scheme

A. Deduction Process of the Sample-and-Hold Scheme

According to the analysis above, $T_{\rm pul}$ is more convenient for stability judgment than $T_{\rm mod}$. However, as seen from Fig. 7, the implementation of the pulse perturbation scheme is relatively complex. Thus, an improved pulse perturbation scheme, which is called sample-and-hold scheme, will be proposed below as an alternative implementation scheme for simplifying the circuits. As observed from Fig. 7(a), $v_{\rm pul\_dy\_t}$ is generated by $v_{\rm mod}$ passing through the PWM modulator and the pulse compensation circuit, which can be equivalently realized by introducing an extra identical PWM modulator between $v_{\rm mod}$ and the pulse compensation circuit. In addition, $v_{\rm pul\_dy\_r}$ is the superposition of $v_{\rm pul\_dy\_p}$ and $v_{\rm pul\_dy\_o}$. Considering $v_{\rm pul\_dy\_p}$ and $v_{\rm pul\_dy\_o}$ are generated by $v_{\rm sin}$ and $v_{\rm mod}$, respectively, as an alternative, $v_{\rm sin}$ can be added to $v_{\rm mod}$ first to equivalently obtain $v_{\rm pul\_dy\_r}$. Since $V_{\rm bias}$ in the pulse perturbation scheme provides a fixed narrow pulse, and the pulsewidth of which is identical to the pulse compensation circuit, an extra pulse compensation circuit should be introduced after the PWM modulator in the control loop. With these considerations, the pulse perturbation scheme in Fig. 7(a) can be converted to Fig. 9(a). Furthermore, since a fixed pulse created by the pulse compensation circuits is superimposed on both $v_{\rm pul\_dy\_t}$ and $v_{\rm pul\_dy\_r}$, as shown in Fig. 9(a), the signals preceding the pulse compensation circuits, i.e., $v_{\rm pul\_dy\_o}$ and $v_{\rm pul\_dy\_r1}$, can be collected to acquire the loop gain without affecting the accuracy. Based on this, the pulse compensation circuit after $v_{\rm pul\_dy\_o}$ can be discarded, resulting in Fig. 9(b). By introducing an extra PWM modulator between $v_{\rm mod1}$ and the Ref port, Fig. 9(c) is obtained. Moreover, the two extra PWM modulators acts as a natural sampling switch; thus, they can be replaced with sampling holders if the sampling instant remains unchanged. Since the intersection instant of the PWM modulator locates at $nT_{\rm s}+(D_{\rm y}-D_{\rm c})T_{\rm s}$, where $D_cT_s(D_c \ll 1)$ is the pulsewidth of the pulse compensation circuit, the sampling instant of the sampling holder should also set at $nT_s+(D_y-D_c)T_s$. After sampling and holding, both the ω components in $v_{\rm pul\_dy\_o}$ and $v_{\rm pul\_dy\_r1}$ are multiplied by the transfer function of the sampling holder; hence, the ratio of $\hat{v}_{\rm sh\_t}(j\omega)$ and $\hat{v}_{\rm sh\_r}(j\omega)$ is exactly the same as that of $\hat{v}_{\rm pul\_dy\_t}(j\omega)$ and $\hat{v}_{\rm pul\_dy\_r1}(j\omega)$. Therefore, $T_{\rm pul}(j\omega)$ can still be measured in this way. Since the pulse compensation circuit in Fig. 9(c) provides only a constant pulsewidth, which has no effect on the control loop, and hence can be discarded. Finally, Fig. 9(d) is obtained, which is called the sample-and-hold scheme.

B. Implementation of the Sample-and-Hold Scheme

The detailed schematic diagram and waveforms of the sample-and-hold scheme are given in Fig. 10. When the clock signal of the RS trigger inherent in the PWM modulator $v_{\rm clk}$ arrives, Q_1 is turned ON. Capacitor C_1 is discharged and v_{c1} falls to zero. At this instant, Q_2 is turned OFF, and C_2 starts to get charged, and v_{c2} rises from V_f, the forward voltage drop of the diode D_2. Here, U_1 is a hysteresis comparator. When v_{c2} rises to $V_{\rm dydc}$ (the average value of the driving signal produced from a low-pass filter, ranging from 0 to $V_{\rm cc}$ when the duty cycle varies from 0 and 1), the sampling pulse $v_{\rm sp}$ goes high and turns ON D_1. At this instant, $v_{\rm mod}$ and $v_{\rm mod1}$ are sampled. In the meanwhile, v_{c1} rises to turn ON Q_2, and C_2 is discharged. When v_{c2} falls below, $V_{\rm dydc}$, $v_{\rm sp}$ goes low and D_1 is turned OFF. Afterward, C_1 is discharged slowly through R_2 while maintaining the turn-ON state of Q_2 till the next pulse of $v_{\rm clk}$.

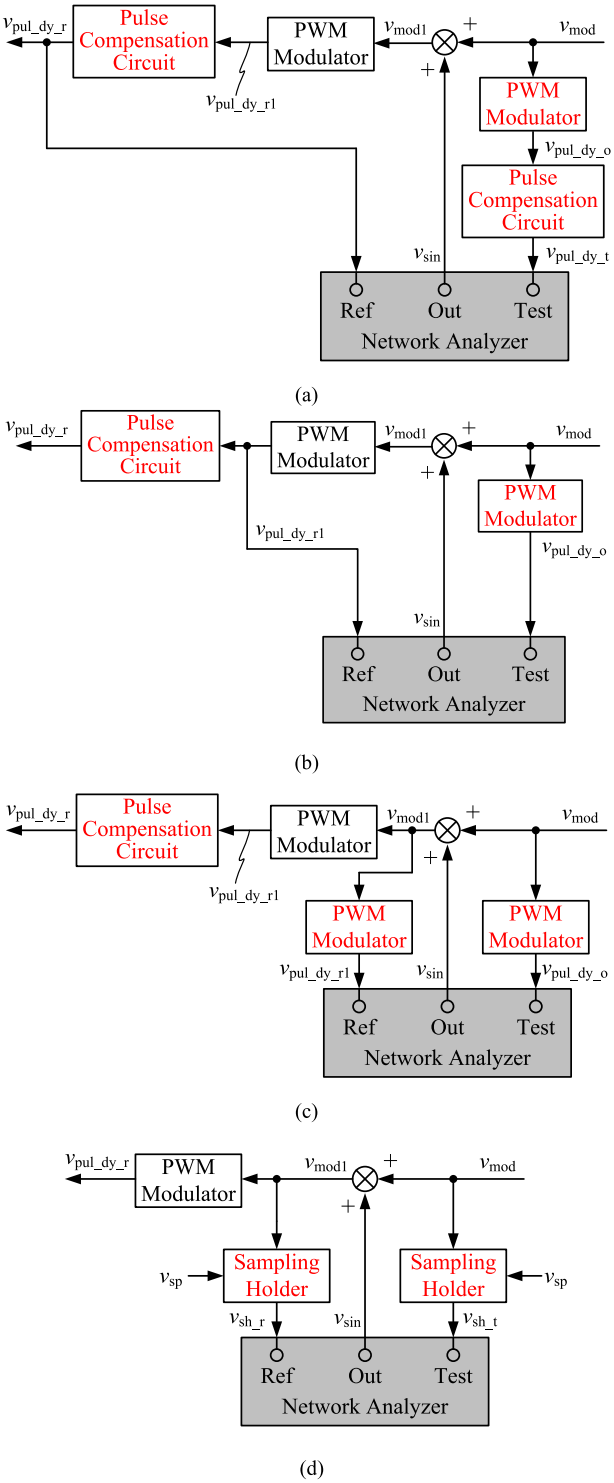


Fig. 9. Equivalent schematic diagrams of sample-and-hold scheme. (a) Equivalent transformation I. (b) Equivalent transformation II. (c) Equivalent transformation III. (d) Equivalent transformation IV.

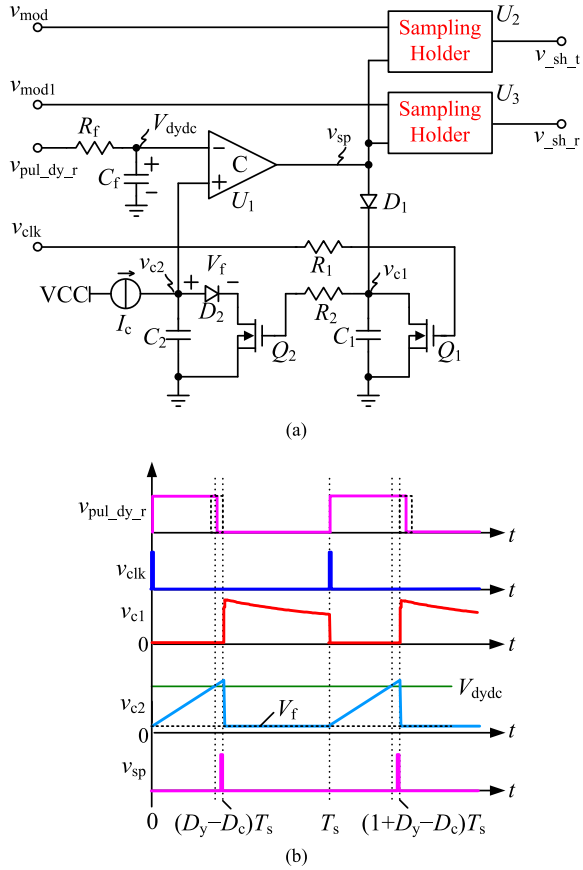


Fig. 10. Sample-and-hold scheme. (a) Detailed schematic diagram. (b) Key waveforms.

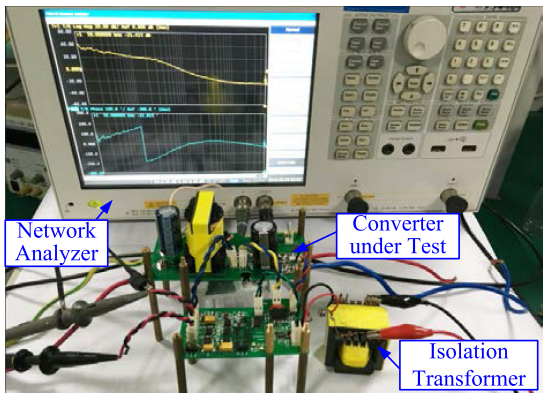


Fig. 11. Photograph of the prototype with various loop gain measurement schemes.

V. Experimental Verification

A. Measurement Verification

To verify the analytical results and the effectiveness of the proposed sample-and-hold scheme, experimental prototypes (buck, boost, and buck–boost converters) are constructed and measured. Fig. 11 shows the photograph of the prototype with various loop gain measurement schemes.

The main circuit parameters of the three converters are given in Tables I to III. The voltage regulators for the three converters are set as

$$G_{\mathrm{vr\_bu}}(s) = 24 + 2800/\mathrm{s} \tag{37}$$

$$G_{\mathrm{vr\_bst}}(s) = 4 + 2000/\mathrm{s} \tag{38}$$

$$G_{\mathrm{vr\_bb}}(s) = 0.5 + 200/\mathrm{s}. \tag{39}$$

TABLE I
PARAMETERS OF THE BUCK CONVERTER

Parameter	Symbol	Value	Parameter	Symbol	Value
Input votlage	V_{in}	48 V	Output capacitor	C	220 μF
Output voltage	V_o	36 V	Capacitor ESR	R_c	0.24 Ω
Output power	P_o	200 W	Peak to peak value	V_m	2.6 V
Switching frequency	f_s	100 kHz	Voltage feedback factor	H_v	0.07
Inductor	L	72 μH			

TABLE II
PARAMETERS OF THE BOOST CONVERTER

Parameter	Symbol	Value	Parameter	Symbol	Value
Input votlage	V_{in}	24 V	Output capacitor	C	680 μF
Output voltage	V_o	48 V	Capacitor ESR	R_c	0.2 Ω
Output power	P_o	200 W	Peak to peak value	V_m	2.6 V
Switching frequency	f_s	100 kHz	Voltage feedback factor	H_v	0.052
Inductor	L	72 μH			

TABLE III
PARAMETERS OF THE BUCK–BOOST CONVERTER

Parameter	Symbol	Value	Parameter	Symbol	Value
Input votlage	V_{in}	36 V	Output capacitor	C	1 mF
Output voltage	V_o	48 V	Capacitor ESR	R_c	0.3 Ω
Output power	P_o	200 W	Peak to peak value	V_m	2.6 V
Switching frequency	f_s	100 kHz	Voltage feedback factor	H_v	0.052
Inductor	L	220 μH			

It should be noted that due to the presence of ESR, the output voltage of boost and buck–boost converters is discontinuous as the switch turns OFF and ON, causing jump discontinuities in the modulation signal at the switching instant. Such a discontinuous modulation signal displays the Gibbs phenomenon, and cannot be accurately described by a Fourier series upon which the extended-frequency-range small-signal model is based even if infinite number of the sideband frequencies is taken into consideration. To eliminate the jump discontinuities in the modulation signal while keeping everything else the same, four first-order low-pass filters with the corner frequency being five times higher than the switching frequencies are incorporated after the PI regulator (only used in calculating T_{mod} and T_{pul}, not in the experiment). This avoids the Gibbs phenomenon and preserves the validity of the loop gain below Nyquist frequency.

The loop gains of the three converters are measured by Agilent E5061B. Figs. 12–14 give the experimental results from the

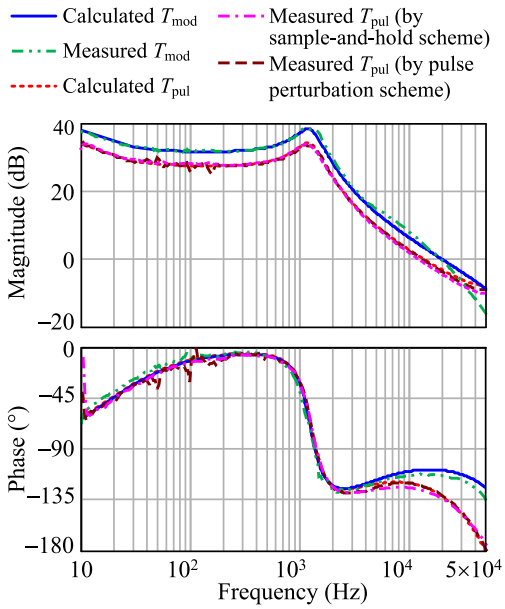


Fig. 12. Measured loop gain of buck converter with different schemes.

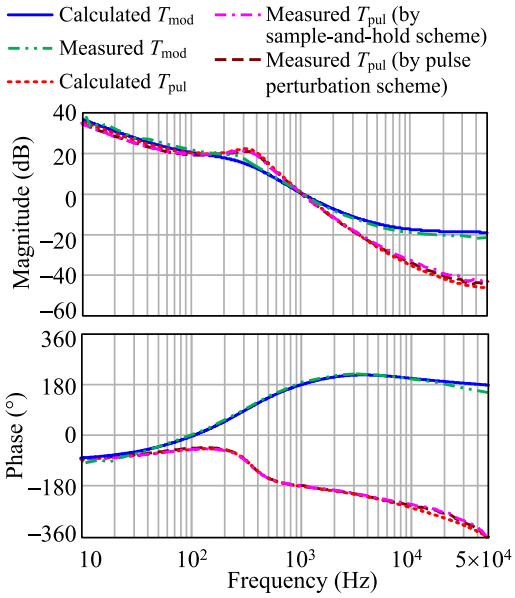


Fig. 13. Measured loop gain of boost converter with different schemes.

modulation signal perturbation scheme, the pulse perturbation scheme, and the sample-and-hold scheme. Also, the calculated loop gains by the modulation signal perturbation scheme and the pulse perturbation scheme are given in these figures. As seen from the results, the measured loop gains are well matched with the calculated ones, and the measured T_{pul} by the sample-and-hold scheme is fully consistent with the pulse perturbation scheme, verifying the effectiveness of the proposed measurement scheme. Besides, the measured T_{mod} is different from the measured T_{pul}, which agrees with the theoretical analysis.

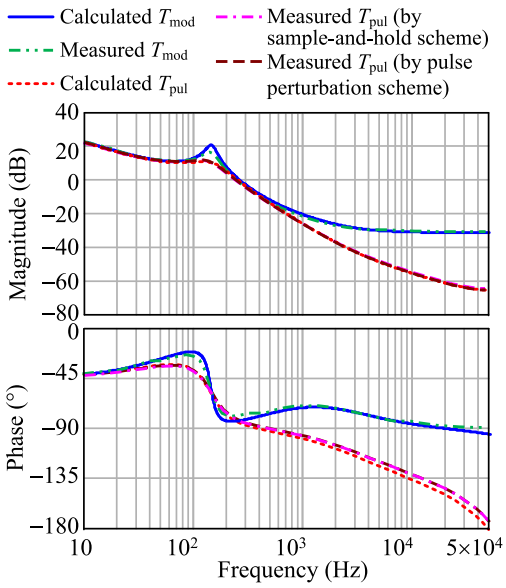


Fig. 14. Measured loop gain of buck–boost converter with different schemes.

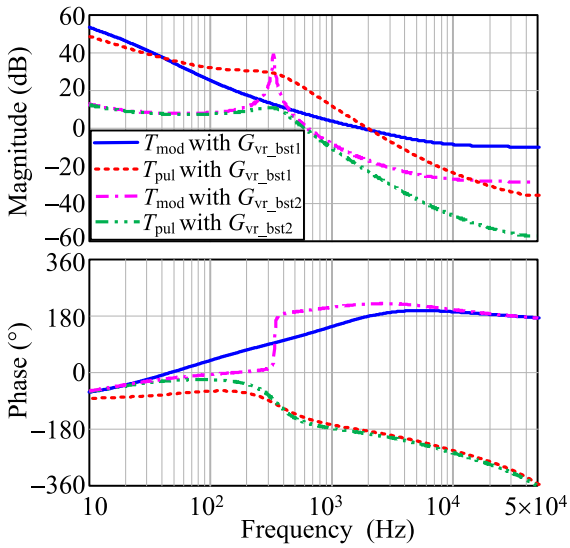


Fig. 15. Bode plot of T_{mod} and T_{pul} for boost converter with $G_{\mathrm{vr\_bst1}}(\mathrm{s})$ and $G_{\mathrm{vr\_bst2}}$ (s).

B. Stability Judgment Verification

The boost converter is taken as an example to verify the previous analysis on stability assessment using the two loop gains. The voltage regulator is intentionally modified to be $G_{\mathrm{vr\_bst1}}(s)$ expressed as

$$G_{\mathrm{vr\_bst1}}(\mathrm{s}) = 16 + 10000/\mathrm{s}. \tag{40}$$

According to (10) and (16), T_{pul} and T_{mod} with $G_{\mathrm{vr\_bst1}}(s)$ are plotted, as shown in Fig. 15. It can be seen that the phase-frequency curve of T_{pul} positively crosses the $-180°$ line for one time before the magnitude drops to 0 dB, i.e., $N_{\mathrm{pul}+} = 0, N_{\mathrm{pul}-} = 1$. Thus, we have $R_{\mathrm{pul}} = 2(N_{\mathrm{pul}+} - N_{\mathrm{pul}-}) = -2$. Since $P_{\mathrm{pul}} = 0$ in all cases, we have $Z_{\mathrm{pul}} = P_{\mathrm{pul}} - R_{\mathrm{pul}} = 2$, and the system can be estimated as unstable by T_{pul}. It can also be found that the magnitude-frequency curve of T_{mod} goes down while the phase-frequency curve goes up around the resonant frequency, which implies that T_{mod} has RHP poles, i.e., $P_{\mathrm{mod}} \neq 0$. However, the phase-frequency curve of T_{mod} does not cross the $n \times 180°$ lines $(n = \pm1, \pm3, \pm5, \ldots)$ before the magnitude declines to 0 dB, i.e., $R_{\mathrm{mod}} = 0$. Thus, we have $Z_{\mathrm{mod}} = P_{\mathrm{mod}} - R_{\mathrm{mod}} \neq 0$, and the system can be judged as unstable by T_{mod}. In this case, both T_{mod} and T_{pul} can determine the stability by themselves.

When the voltage regulator is intentionally designed to be $G_{\mathrm{vr\_bst2}}(s)$, expressed as

$$G_{\mathrm{vr\_bst2}}(s) = 1.2 + 118/\mathrm{s} \tag{41}$$

T_{pul} and T_{mod} with $G_{\mathrm{vr\_bst2}}(s)$ are calculated and plotted, as shown in Fig. 15. As seen, the phase-frequency curve of T_{pul} does not cross the $-180°$ line before the magnitude drops to 0 dB, i.e., $R_{\mathrm{pul}} = 0$. Since $P_{\mathrm{pul}} = 0$, we have $Z_{\mathrm{pul}} = P_{\mathrm{pul}} - R_{\mathrm{pul}} = 0$, and the system can be estimated as stable by T_{pul}. It can also be found from the Bode plot that the phase-frequency curve of T_{mod} crosses the 180° line positively for one time before the magnitude declines to 0 dB, i.e., $N_{\mathrm{mod}+} = 1, N_{\mathrm{mod}-} = 0$. Thus, we have $R_{\mathrm{mod}} = 2(N_{\mathrm{mod}+} - N_{\mathrm{mod}-}) = 2$. Besides, as seen from Fig. 15, the magnitude curve of T_{mod} goes down while the phase curve goes up around the resonant frequency, which implies that T_{mod} has RHP poles, i.e., $P_{\mathrm{mod}} \neq 0$, but the number of RHP poles cannot be accurately read from the Bode plot. According to (23), we can figure out that $P_{\mathrm{mod}} = R_{\mathrm{mod}} - R_{\mathrm{pul}} = 2$, Thus, $Z_{\mathrm{mod}} = 0$, showing that the converter is stable by T_{mod}. In this case, T_{pul} can determine the stability by itself, and T_{mod} can also determine the stability, but it needs the aid of T_{pul} to determine the number of RHP poles first.

Fig. 16(a) and (b) gives the experimental waveforms of the inductor current i_L and the output voltage v_{o} of the boost converter with the voltage regulator being $G_{\mathrm{vr\_bst1}}(s)$ and $G_{\mathrm{vr\_bst2}}(s)$, respectively. Obviously, as seen from Fig. 16(a), the system is unstable as predicted by T_{mod} and T_{pul}, and as seen from Fig. 16(b), the system is stable as predicted by T_{pul}, verifying the effectiveness of the loop gains in stability judgment.

From Fig. 15, we can see that the bandwidth of $T_{\mathrm{mod}}(s)$ with $G_{\mathrm{vr\_bst1}}(s)$ is higher than that with $G_{\mathrm{vr\_bst2}}(s)$. Comparing the Bode plots of $T_{\mathrm{mod}}(s)$ with $G_{\mathrm{vr\_bst1}}(s)$ and $G_{\mathrm{vr\_bst2}}(s)$, it is found that the resonant peak of $T_{\mathrm{mod}}(s)$ is damped when using $G_{\mathrm{vr\_bst1}}(s)$, which is different from the commonly cognition that the voltage regulator has no effect on the resonant peak. This is because in boost and buck–boost converters, G_{vd} has multiple resonant frequencies [31]. To be specific, besides the natural resonant frequency of the low-pass filter f_r, there are other resonant frequencies at $f_r + kf_s$. When ω approaches $2\pi f_{\mathrm{r}}, T_0[j(\omega + k\omega_{\mathrm{s}})]\,(k = \pm1, \pm2, \pm3, \ldots)$ in the denominator of $T_{\mathrm{mod}}(s)$ [see (10)] approaches its own resonant peak, and it damps the resonant peak of $T_{\mathrm{mod}}(s)$. As the bandwidth of the converter becomes higher, this impact turns more distinct.

It should be noted that in practice $T_0(s)$ instead of $T_{\mathrm{mod}}(s)$ or $T_{\mathrm{pul}}(s)$ is widely adopted in regulator design because of its simplicity. However, $T_0(s)$ is accurate only in the frequency range much below the switching frequency, which makes the regulator

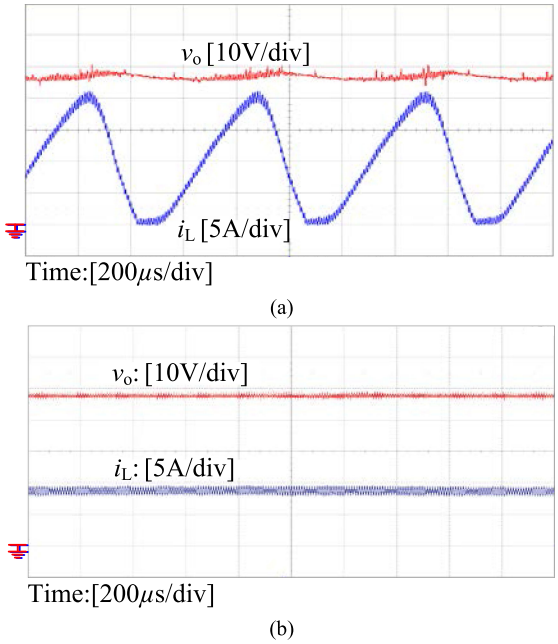


Fig. 16. Experimental waveforms of boost converter with (a) $G_{\text{vr\_bst1}}$ (s) and (b) $G_{\text{vr\_bst2}}$ (s).

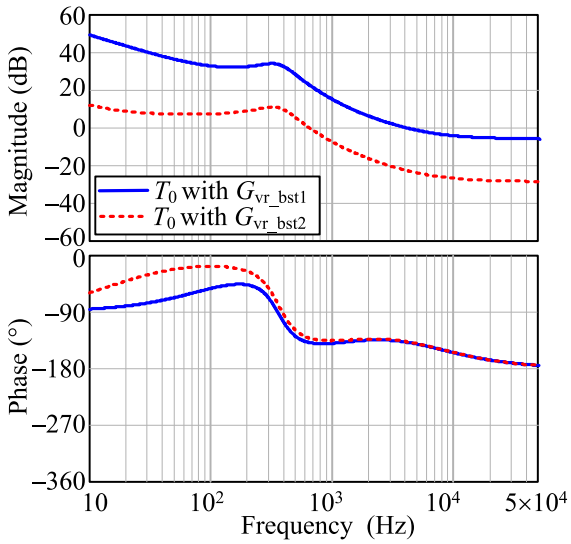


Fig. 17. Bode plot of T_0 for boost converter with $G_{\text{vr\_bst1}}$ (s) and $G_{\text{vr\_bst2}}$ (s).

design based on $T_0(s)$ unrealistic and invalidates the stability assessment result. Even if the converter is designed stable, the phase margin may not be adequate. Taking the boost converter as an example, the Bode diagrams of $T_0(s)$ with the regulator being $G_{\text{vr\_bst1}}$ and $G_{\text{vr\_bst2}}$ are given in Fig. 17. As seen, when the regulator is $G_{\text{vr\_bst1}}$, the phase margin is 42° using $T_0(s)$, but the converter is actually unstable. When the regulator is $G_{\text{vr\_bst2}}$, the phase margin is 45°using $T_0(s)$, which is higher than that using $T_{\text{mod}}(s)$ or $T_{\text{pul}}(s)$ although the stability judgment is correct. By measuring the loop gain, we can obtain precise magnitude and phase information about the closed-loop system, based on which a badly designed regulator can be corrected.

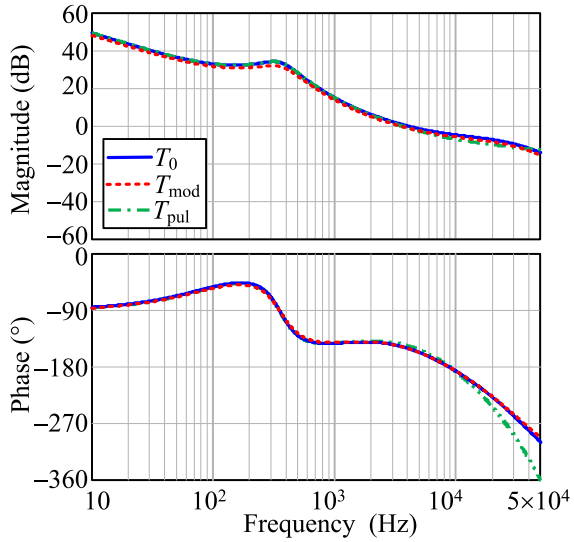


Fig. 18. Bode plots of T_0, T_{mod}, T_{pul} for boost converter with $G_{\text{vr\_bst3}}$ (s).

In the following, we describe the process of correcting the regulator design based on experimental measurement of the loop gain using the boost converter as an example. Comparing the Bode plots of $T_0(s)$ and the measured $T_{\text{pul}}(s)$, it is found the sideband frequency components reduce the phase margin of the converter significantly. Therefore, the stability can be improved by weakening the effect of the sideband frequency components. One simple method is to introduce a low-pass filter to attenuate the magnitude of the loop gain at the sideband frequencies. To ensure an adequate phase margin, the corner frequency of the low-pass filter should be set between the cutoff frequency and the minimum sideband frequency. In this example, the cutoff frequency is 4 kHz using $T_0(s)$, the sideband frequencies are 96 kHz, 104 kHz, etc. Thus, the corner frequency should be set between 4 and 96 kHz. Here, we choose the two first-order low-pass filters with corner frequency being 40 kHz. The low-pass filter is added to both $G_{\text{vr\_bst1}}(s)$ and $G_{\text{vr\_bst2}}(s)$ to correct the regulator design and improve the stability. Taking $G_{\text{vr\_bst2}}(s)$ as an example, it is modified to $G_{\text{vr\_bst3}}(s)$, i.e.,

$$G_{\text{vr\_bst3}}(s) = \frac{16 + 10000/\text{s}}{\left(1 + \frac{\text{s}}{251200}\right)^2}. \tag{42}$$

With $G_{\text{vr\_bst3}}(s)$ as the regulator, T_0, T_{mod}, and T_{pul} are plotted in Fig. 18, where we can see that T_0, T_{mod}, and T_{pul} are nearly identical. The cutoff frequencies are 3.5 kHz by both T_{mod} and T_{pul}, and the phase margins are 32° and 37° by T_{mod} and T_{pul}, respectively, verifying that the stability of the converter has been restored. The corresponding experimental waveforms are given in Fig. 19.

C. Closed-Loop Transfer Functions Verification

The buck converter is taken as an example to verify the closed loop transfer function using the two loop gains. The voltage regulator is still the one given in (37). Fig. 20 gives both the calculated and measured Bode diagrams of the reference to

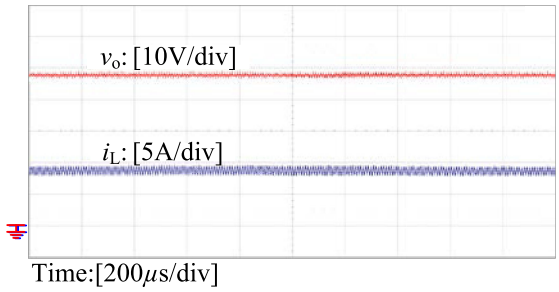


Fig. 19. Experimental waveforms of boost converter with $G_{\text{vr\_bst3}}$ (s).

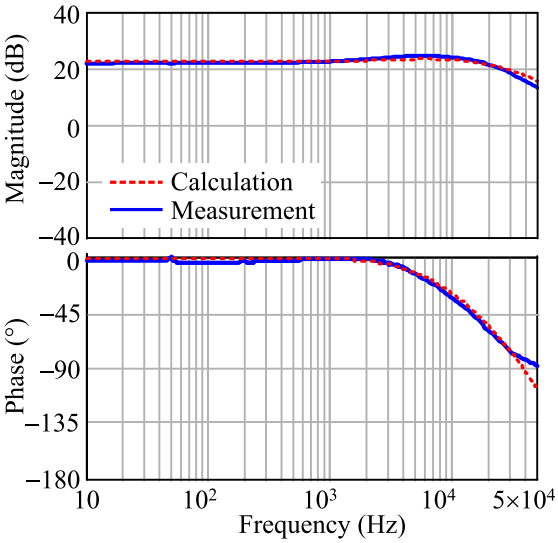


Fig. 20. Measured reference-to-output-voltage transfer function of buck converter.

output voltage transfer function, where we see that the measured result is in good agreement with the calculation.

As for the audiosusceptibility, the expression of $G_{\text{vg\_k}}(j\omega)$ for the buck converter is

$$G_{\text{vg\_0}}(j\omega) = \frac{D_y(1 + j\omega CR_c)}{(j\omega)^2 LC + j\omega\left(\frac{L}{R_{\text{Ld}}} + CR_c\right) + 1} \tag{43a}$$

when $k = 0$ and

$$G_{\text{vg\_}k}(j\omega) = \frac{e^{-j2\pi kD_y} - 1}{-j2\pi k} \cdot \frac{1 + j(\omega + k\omega_s)CR_c}{[j(\omega + k\omega_s)]^2 LC + j(\omega + k\omega_s)\left(\frac{L}{R_{\text{Ld}}} + CR_c\right) + 1} \tag{43b}$$

when $k \neq 0$. With (43), the closed loop audiosusceptibility can be obtained. Fig. 21 gives both the calculated and measured results of the closed loop audiosusceptibility. As seen, the measurement also agrees with the analytical result.

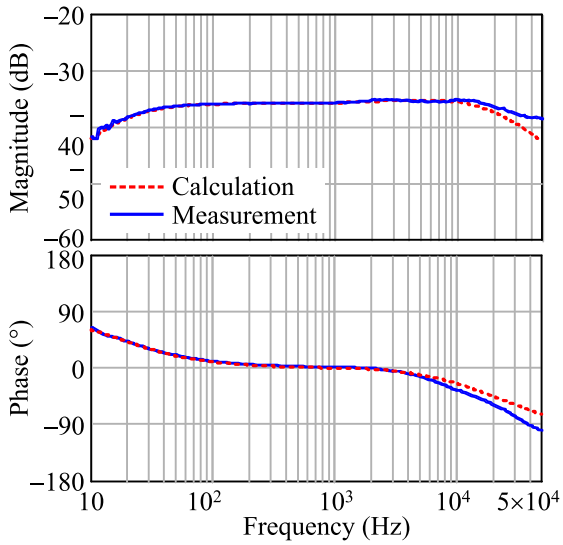


Fig. 21. Measured closed-loop audiosusceptibility of buck converter.

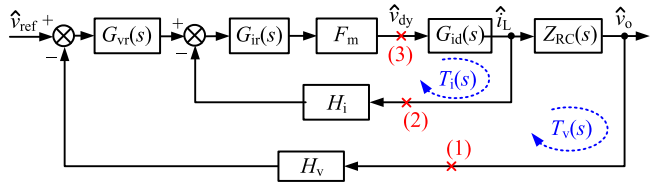


Fig. 22. Control block diagrams of a two-loop controlled converters.

VI. Conclusion

The modulation signal perturbation scheme and the pulse perturbation scheme are two commonly used schemes for measuring the loop gain of closed-loop dc–dc converter systems. However, the results from the two schemes are not fully consistent. Using the extended-frequency-range small-signal model, a quantitative relation can be derived between the loop gains found from the two schemes. The pulse perturbation scheme is a simpler scheme in stability assessment. In this paper, an alternative implementation using a sample-and-hold scheme is proposed, which is simple yet equally effective as the original pulse modulation scheme. Finally, experimental prototypes of buck, boost, and buck–boost converters are studied for the purpose of verifying the analytical results and the effectiveness of the proposed sample-and-hold loop gain measurement schemes.

Appendix

This Appendix explains the equivalence of different loop gains in two-loop controlled systems. Fig. 22 shows the small-signal control block diagram of a two-loop system with the example of average current mode controlled converter, where F_m is the gain magnitude of the PWM modulator, $G_{\text{vd}}(s)$ is the duty-cycle-to-output-voltage transfer function, $G_{\text{vr}}(s)$ is the voltage regulator, H_v is the output voltage sensor gain, $G_{\text{ir}}(s)$ is the current regulator, $G_{\text{id}}(s)$ is the duty-cycle-to-inductor-current transfer function, H_i is the inductor current sensor gain, $Z_{\text{RC}}(s)$ is the inductor-current-to-output-voltage transfer

function, and $G_{\rm vd}(s) = G_{\rm id}(s)Z_{\rm RC}(s)$. T_v(s) and $T_i(s)$ are the loop gains of voltage loop and current loop, respectively, expressed as [16]

$$T_v(s) = G_{\rm vr}(s)G_{\rm ir}(s)F_m G_{\rm id}(s)Z_{\rm RC}(s)H_v \tag{A1}$$

$$T_i(s) = G_{\rm ir}(s)F_m G_{\rm id}(s)H_i. \tag{A2}$$

When measuring the loop gain of the whole system, the perturbation can be injected into the loop through the voltage feedback path, the current feedback path, or the duty cycle, as shown in Fig. 22, which correspond to three different loop gain results expressed as follows, respectively,

$$T_1(s) = \frac{T_v(s)}{1 + T_i(s)} \tag{A3}$$

$$T_2(s) = \frac{T_i(s)}{1 + T_v(s)} \tag{A4}$$

$$T_3(s) = T_v(s) + T_i(s). \tag{A5}$$

For any closed-loop controlled system, if $1 + T(s)$ has no RHP zero, the system is considered stable. From (A3) to (A5), we have

$$1 + T_1(s) = \frac{1 + T_v(s) + T_i(s)}{1 + T_i(s)} \tag{A6}$$

$$1 + T_2(s) = \frac{1 + T_v(s) + T_i(s)}{1 + T_v(s)} \tag{A7}$$

$$1 + T_3(s) = 1 + T_v(s) + T_i(s). \tag{A8}$$

As seen from (A6) to (A8), since $T_v(s)$ and $T_i(s)$ have no RHP poles, the number of RHP zeros of $1 + T_j(s)$ $(j = 1, 2, 3)$ is equal to that of $1 + T_v(s) + T_i(s)$, indicating that the three loop gains are equivalent in stability assessment.

REFERENCES

[1] M. Shirazi, J. Morroni, A. Dolgov, and D. Maksimovic, "Integration of frequency response measurement capabilities in digital controllers for dc-dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2524–2535, Sep. 2008.

[2] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-step controller design for *LCL*-type grid-connected inverter with capacitor current-feedback active-damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239–1253, Mar. 2014.

[3] Y. Sugimoto, T. Sai, K. Watanabe, and M. Abe, "Feedback loop analysis and optimized compensation slope of the current-mode buck dc-dc converter in DCM," *IEEE Trans. Circuits Syst.—I, Reg. Papers*, vol. 62, no. 1, pp. 311–319, Jan. 2015.

[4] T. Roinila, J. Huusari, and M. Vilkko, "On frequency-response measurements of power-electronic systems applying MIMO identification techniques," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5270–5276, Nov. 2013.

[5] R. D. Middlebrook, "Measurement of loop gain in feedback systems," *Int. J. Electron.*, vol. 38, no. 4, pp. 485–512, 1975.

[6] N. Kondrath and M. K. Kazimierczuk, "Margins of stability of inner-current loop of peak current-mode controlled PWM dc–dc converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2009, pp. 1985–1988.

[7] R. Ridley, "Frequency response measurements for switching power supplies," in *Proc. Unitrode Power Supply Des. Semin.*, 1999-00 Series, pp. A1–A12.

[8] X. Liu, J. Jiang, P. K. T. Mok, and W. Ki, "Methods for measuring loop-gain function of high-frequency dc-dc converters," in *Proc. IEEE Asia Pac. Conf. Circuits Syst.*, 2016, pp. 247–249.

[9] J. Morroni, R. Zane, and D. Maksimovic, "An online stability margin monitor for digitally controlled switched-mode power supplies," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2639–2648, Nov. 2009.

[10] T. Roinila, M. Vilkko, and T. Suntio, "Fast loop gain measurement of switched-mode converter using binary signal with specified Fourier amplitude spectrum," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2746–2755, Dec. 2009.

[11] Y. Panov and M. M. Jovanovic, "Loop gain measurement of paralleled dc-dc converters with average-current-sharing control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2942–2948, Nov. 2008.

[12] Y. Jiang, X. Ruan, and C. Xiong, "Study of loop gain measurement of digitally controlled dc/dc converters," in *Proc. IEEE Int. Power Electron. Motion Control Conf.*, 2016, pp. 2806–2812.

[13] R. B. Ridley, B. H. Cho, and F. C. Lee, "Analysis and interpretation of loop gains of multiloop-controlled switching regulators," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 489–498, Oct. 1988.

[14] R. W. Erickson and D. Maksimovic, *Fundamental of Power Eletronics*. Norwell, MA, USA: Kluwer, 2001.

[15] Y. Panov and M. M. Jovanovic, "Small-signal measurement techniques in switching power supplies," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 770–776.

[16] B. H. Cho and F. C. Lee, "Measurement of loop gain with the digital modulator," *IEEE Trans. Power Electron.*, vol. 1, no. 1, pp. 55–62, Jan. 1986.

[17] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, vol. 2, no. 2, pp. 109–124, Apr. 1987.

[18] J. Castello and J. M. Espi, "DSP implementation for measuring the loop gain frequency response of digitally controlled power converters," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4113–4121, Sep. 2012.

[19] F. González-Espín, E. Figueres, G. Garcerá, R. González-Medina, and M. Pascual, "Measurement of the loop gain frequency response of digitally controlled power converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2785–2796, Aug. 2010.

[20] G. W. Wester and R. D. Middlebrook, "Low-frequency characterization of switched dc-dc converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-9, no. 3, pp. 376–385, May 1973.

[21] R. D. Middlebrook, "Small-signal modeling of pulse-width modulated switched-mode power converter," *Proc. IEEE*, vol. 76, no. 4, pp. 343–354, Apr. 1988.

[22] V. Vorperian, "Simplified analysis of PWM converter using model of PWM switch, Part I: Continuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 490–496, May 1990.

[23] V. Vorperian, "Simplified analysis of PWM converter using model of PWM switch, Part II: Discontinuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 497–505, May 1990.

[24] J. Groves, "Small-signal analysis using harmonic balance methods," in *Proc. 22nd Annu. IEEE Power Electron. Spec. Conf.*, 1991, pp. 74–79.

[25] Y. Qiu, M. Xu, K. Yao, J. J. Sun, and F. C. Lee, "Multifrequency small-signal model for buck and multiphase interleaving buck converters," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1185–1192, Sep. 2006.

[26] Y. Wang *et al.* "Multiharmonic small-signal modeling of low-power PWM dc-dc converters,"*ACM Trans. Des. Autom. Electron. Syst.*, vol. 22, no. 4, pp. 68–83, Jun. 2017.

[27] U. Vargas and A. Ramirez, "Reformulating extended harmonic domain models for accurate representation of harmonics dynamics," *IEEE Trans. Power Del.*, vol. 31, no. 6, pp. 2562–2564, Dec. 2016.

[28] S.-F. Hsiao, D. Chen, C.-J. Chen, and H.-S. Nien, "A new multiple-frequency small-signal model for high-bandwidth computer V-core regulator applications," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 733–742, Jan. 2016.

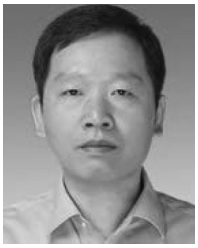
[29] G. Verghese and V. Thottuvelil, "Aliasing effects in PWM power converters," in *Proc. IEEE Power Electron. Spec. Conf.*, 1999, pp. 1043–1049.

[30] X. Li, X. Ruan, M. Sha, and C. K. Tse, "Small-signal models with extended frequency range for dc-dc converters with large modulation ripple amplitude," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8151–8163, Sep. 2018.

[31] R. Tymerski, "Frequency analysis of time-interval -modulated switched networks," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 287–295, Apr. 1991.

[32] R. Tymerski, "Exact input-to-output frequency response of time interval modulated switched networks," in *Proc. IEEE Power Electron. Spec. Conf.*, 1997, pp. 428–434.

[33] R. Tymerski, "Application of the time-varying transfer function for exact small-signal analysis," *IEEE Trans. Power Electron.*, vol. 9, no. 2, pp. 196–205, Apr. 1994.



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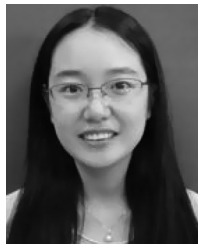

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