P^{3}DCT—Partial-Power Pre-Regulated DC Transformer

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***Abstract*—In this paper, a new approach to regulate the output voltage of a resonant, constant voltage transfer ratio 380 V/48 V isolated dc–dc converter is presented. Rather than applying variable frequency control to the resonant converter, which would result in reactive power processing and a more complicated electromagnetic compatibility filter design, the converter remains in its optimal operating point all time and an additional partial-power (PP) processing auxiliary converter is used to tightly regulate the output voltage. The PP converter, supplied through a tertiary winding of the resonant converter's transformer, regulates the output by adding or subtracting voltage from the dc input and has only a marginal impact on the overall efficiency of the dc–dc converter. The principal of operation is explained in detail including Sankey diagrams to illustrate the power processing of the converter and a feedback control system is proposed to tightly regulate the 48 V output voltage. A hardware demonstrator rated at 1.5 kW is implemented to cope with input voltage variations between 340 and 420 V and experimental results are provided showing that the output voltage can be kept within $\pm 1\%$ of the nominal 48 V even under harsh input voltage and load transients. The realized dc–dc converter with PP pre-regulation features an overall efficiency of 97.7% at rated power and a power density of 8.6 kWdm^{-3} (141w/^{3} in).**

***Index Terms*—Auxiliary converter, dc transformer (DCT), partial-power (PP) converter, pre-regulation, series-resonant *LLC* converter.**

I. Introduction

THE series-resonant *LLC* dc–dc converter is widely accepted in the IT and telecom industry due to several desired features such as high efficiency, low electromagnetic interference, and high power density. The converter is typically employed to step down from 380 V and to supply a 48 V power distribution bus. When operated exactly at the resonance frequency of the *LLC* tank, the voltage transfer ratio becomes

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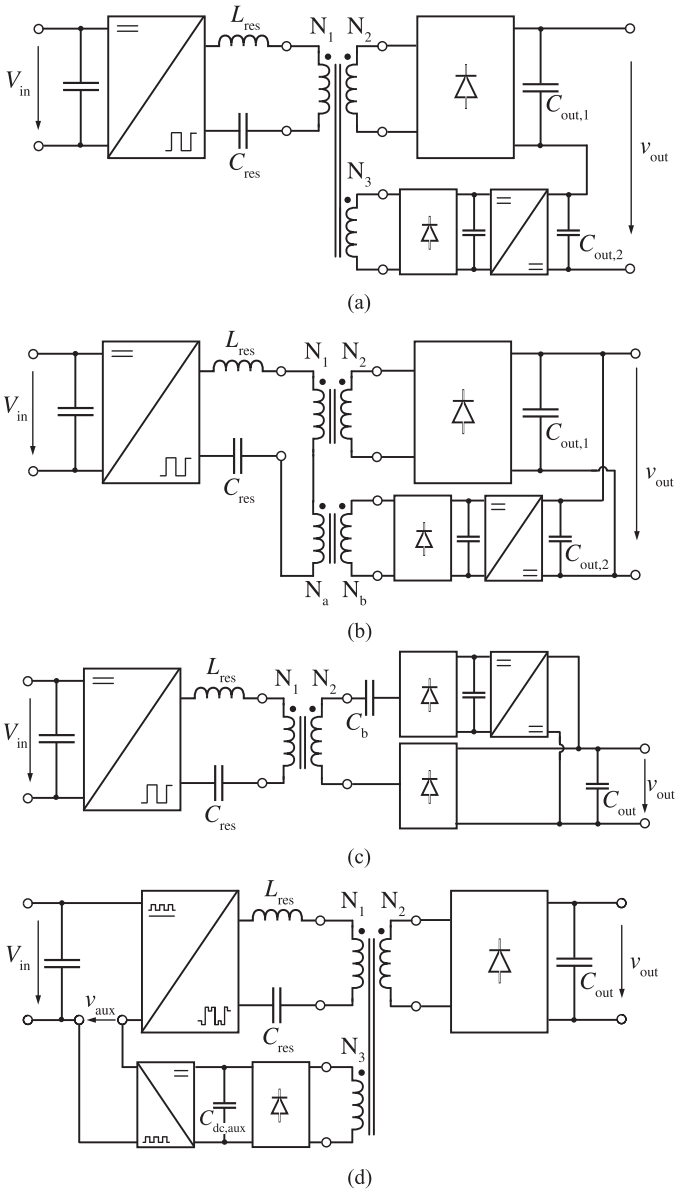

Fig. 1. (a)–(c) Several approaches to provide a regulated output voltage by means of an additional PP converter and (d) the filter-less, PPP³ approach proposed in this paper.

processes around half the rated power of the main converter, the proposed topology constitutes a $1^1/_2$ stage converter rather than an unregulated main converter with PP regulation.

The filter-less, pre-regulation approach proposed in this paper is depicted in Fig. 1(d). Here, the output voltage $V_{\rm out}$ is regulated by adjusting the average voltage applied to the input of the main converter. Omitting additional filter components at the output of the PPC, a pulsewidth modulated voltage is impressed between the negative terminal of the dc input ($V_{\rm in}$) and the main converter. It follows that the square wave voltage applied to the resonant tank of the DCT exhibits a high-frequency superimposed pulsewidth modulator (PWM) pattern, which allows to adjust the average amplitude of the fundamental square wave voltage applied to the *LLC* tank by adopting the modulation index.

TABLE I
DESIGN SPECIFICATION OF THE CONVERTER

Parameter	Value	Description
$V_{\rm in,nom}$	380 V	Nominal DC input voltage
$V_{\rm in,\Delta}$	340 V - 420 V ($\approx \pm 10.0\,\%$)	Input voltage range
$V_{\rm out,nom}$	48 V	Nominal DC output voltage
$V_{\rm out,\Delta}$	± 500 mV ($\approx \pm 1.0\,\%$)	Max. output voltage deviation in steady-state and during transients
$P_{\rm r}$	1.5 kW	Rated power
η^*	98 %	Target efficiency 98 % and max. power density

In the following, the proposed converter topology is presented in detail and the basic theory of operation is discussed (see Section II). Subsequently, in Section III, a control system for the proposed converter is designed. In order to demonstrate the basic concept and verify the claimed performance of the proposed PP pre-control, a hardware demonstrator is implemented as described in detail in Section IV. The implemented 380 V/48 V dc–dc converter is rated at 1.5 kW and has been designed to cope with input voltage variations in the range of 340–420 V. The design specifications are summarized in Table I.

Subsequently, in Section V, experimental results are presented showing the performance of the implemented prototype in steady-state and during transients. Finally, Section VI concludes this paper.

II. PP PRE-REGULATED (P³) DCT

The proposed topology shown in Fig. 2 consist of an unregulated resonant LLC converter and an additional PPC employed to tightly control output voltage $V_{\rm out}$ by pre-regulating the voltage applied to the input of the LLC converter. The full-bridge input stage, $\rm FB_1$, of the *LLC* converter processes the main share of the output power and the resonant tank is dimensioned to feature a resonance frequency typ. in the range of 70–250 kHz in order to achieve a high power density. Since the resonant converter is always operated exactly at the resonance frequency regardless of input voltage and load conditions, a very efficient transfer of real power to the 48 V output is possible because only the reactive power to enable ZVS of full-bridge $\rm FB_1$ must be processed. The stepped-down rectangular ac voltage appearing at the secondary side of the transformer, $v_{\rm T2}$, is then rectified by means of a diode rectifier or a low-voltage MOSFET full-bridge (shown in Fig. 2) for increased conversion efficiency (sync. rectification) and/or bidirectional power flow support. When operated at resonance, the LLC converter is capable of autonomously adapting the current in case of a load step in order to keep the output voltage at

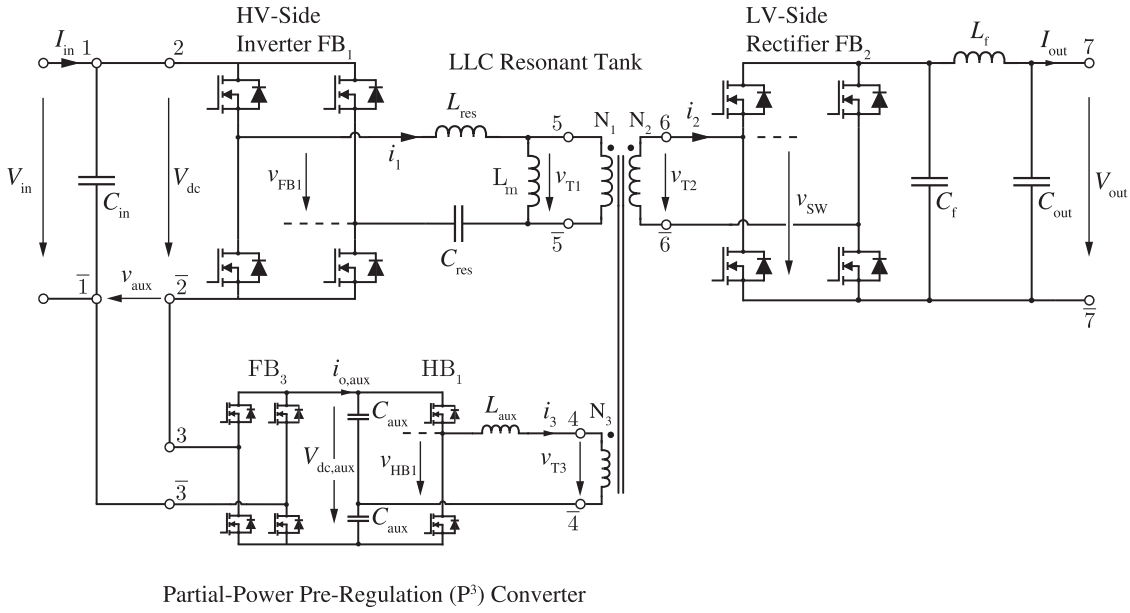

Fig. 2. Schematic of the proposed 380 V/48 V dc–dc converter comprised of a unregulated, resonant LLC converter operating as DCT and an additional PP P^{3}auxiliary converter dedicated to tightly control output voltage V_o.

its nominal value according to the voltage transfer ratio defined by the transformer turns ratio. Thus, the control system of the preregulation converter just has to ensure a proper input voltage level of FB_1 to compensate for ohmic voltage drops and other non-idealities in the main converter in order to keep V_out tightly regulated to the desired 48 V reference value.

A. PP P^3 Auxiliary Converter

As shown in Fig. 2, a PPC with bidirectional power flow and bipolar voltage generation capabilities is proposed. The rectifier-side terminals of the PPC (cf., $4-\overline{4}$) are connected to a tertiary winding of the isolation transformer (N_3) and the output terminals of the inverter (cf., $3-\overline{3}$) are connected between the negative terminal of the input capacitor, C_in, and the negative rail of the full-bridge FB_1 of the main converter. The PP dc-link, $V_\mathrm{dc,aux}$, formed by two stacked capacitors C_aux is supplied from the *LLC* converter transformer through the low-voltage rectifier half-bridge HB_1 operated with the switching frequency of the main converter. For the given input voltage range (cf., Table I), the level of $V_\mathrm{dc,aux}$ is regulated typ. to 50–60 V by adjusting the phase-shift between HB_1 and the leading-leg of full-bridge FB_1 of the main converter. One of the novelties of this approach is that the switched voltage v_aux, generated from PWM of $V_\mathrm{dc,aux}$, is directly impressed between the terminals $\overline{1}-\overline{2}$ (cf., Fig. 2), taking advantage of the transfer characteristic of the *LLC* resonant tank and omitting additional filter elements. The waveforms of a circuit simulation with preliminary system parameters according to Table II are provided in Fig. 3(a) and (b) in order to illustrate the basic operation of the proposed converter system. Given that the switching frequency of FB_3 is a multiple of the resonance frequency (typ. factor 4–10) of the main converter, a rectangular waveform with modulated

TABLE II
PARAMETERS OF THE P^3 DCT CIRCUIT SIMULATION (SEE FIG. 3)

System		P^{3}DCT			
V_in	380 V	C_res	150 nF	C_aux	125 µF
V_out	48 V	C_in	400 µF	$f_\mathrm{s,FB,1}$	120 kHz
$V_\mathrm{dc,aux}$	50 V	C_out	5.4 mF	$f_\mathrm{s,HB,1}$	120 kHz
P_r	1.5 kW	L_res	10 µH	$f_\mathrm{s,FB,3}$	720 kHz
P_aux	60 W	L_m	400 µH	$N_1:N_2:N_3$	14:2:1

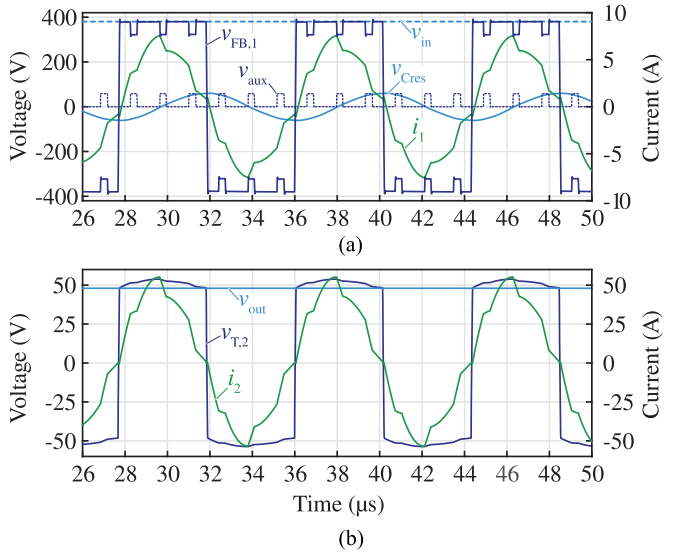

Fig. 3. Switching frequency waveforms of the simulated P^{3}DCT converter operating at rated power (1.5 kW). Primary side related voltage and current waveforms are shown in (a), secondary side related waveforms in (b).

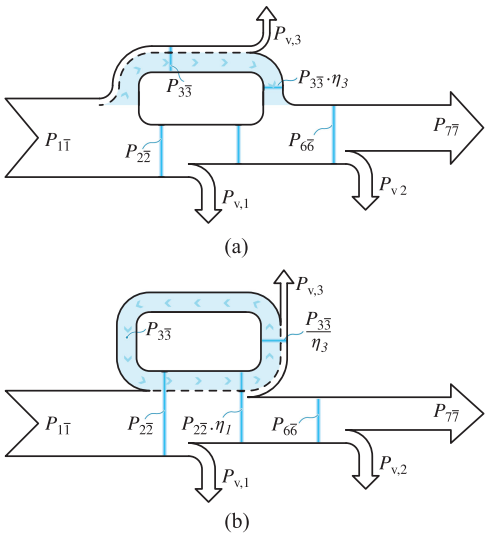

Fig. 4. Sankey diagram of the power flow inside the P³DCT for pre-regulation voltage (a) $\overline{v}_{\mathrm{aux}} > 0$ and (b) $\overline{v}_{\mathrm{aux}} < 0$. The indices denote the power flow through the respective interfaces labeled in Fig. 2. Power loss $P_{\mathrm{v},1}$ and $P_{\mathrm{v},2}$ is caused by the inverter and rectifier stages of the main converter, respectively. $P_{\mathrm{v},3}$ are the losses associated with the processing of the pre-regulation power flow.

amplitude due to the superimposed pulse pattern is applied to the *LLC* tank of the main converter. It follows that the average amplitude of the square wave voltage applied to the resonant tank can be adjusted by means of the modulation index of FB_3, although the switched voltage v_{aux} causes the resonant current i_1 to slightly deviate from it is ideal sinusoidal shape. Choosing a switching frequency multiple of 6 or higher, the total harmonic distortion of i_1 can be kept below $\approx 12\%$ according to circuit simulation.

Given a converter input current $I_{\mathrm{in}} \geq 0$ for unidirectional operation of the main converter, the polarity of the average preregulation voltage, $\overline{v}_{\mathrm{aux}}$, defines the direction of power flow in the PPC as illustrated by the Sankey diagrams in Fig. 4. In case of $\overline{v}_{\mathrm{aux}} > 0$, a fraction of the output power $P_{7\overline{7}}$ (index $7\overline{7}$ denotes the respective power flow interfaces according to the terminal labels in Fig. 2) is actually provided by the PPC as depicted in Fig. 4(a). On the contrary, for $\overline{v}_{\mathrm{aux}} < 0$, power $P_{3\overline{3}}$ circulates within the PPC and the inverter stage of the DCT and does not contribute to the output power $P_{7\overline{7}}$. Consequently, an operation of the P³DCT with $\overline{v}_{\mathrm{aux}} > 0$ is advantageous in terms of efficiency.

B. Power Rating and Efficiency Impairment

The power requirement of the PPC is given by

$$P_{\mathrm{aux}} = \frac{\overline{v}_{\mathrm{aux}}}{V_{\mathrm{in}}} P_{\mathrm{out}} = \frac{V_{\mathrm{in}} - nV_{\mathrm{out}} - \Delta v(i_1)}{V_{\mathrm{in}}} P_{\mathrm{out}} = \left(1 - n\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} - \frac{\Delta v(i_1)}{V_{\mathrm{in}}}\right) P_{\mathrm{out}} \tag{1}$$

where $n = \frac{N_1}{N_2}$ is the primary-to-secondary winding turns-ratio of the isolation transformer and Δv, a function of the resonant current i_1, takes the voltage drop across circuit non-idealities

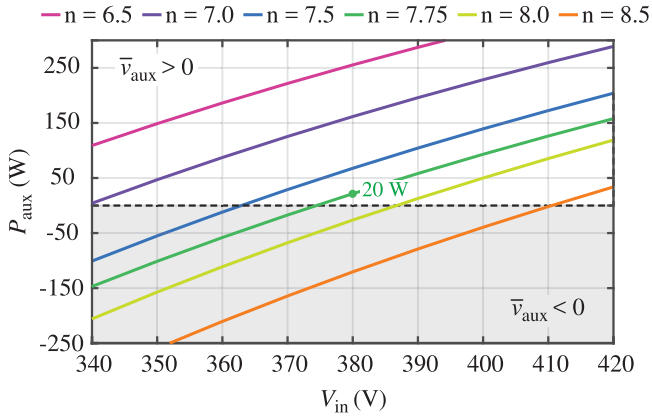

Fig. 5. Power requirement of the PPC as a function of the input voltage V_{in} and the transformer turns ratio, $n = N_1 : N_2$, at 1.5 kW output power.

such as, e.g., transistor on-state or winding resistances into account. Expression (1) is plotted in Fig. 5 with respect to the input voltage, V_{in}, and different transformer turns-ratios. It can be seen that depending on n, unipolar operation is feasible, e.g., $\overline{v}_{\mathrm{aux}} \leq 0$ for $n > 8.75$ considering the given input voltage range, which would allow to further simplify the topology of the PPC (half-bridge instead of FB_3 and diode rectifier instead of HB_1). However, as a consequence of unipolar operation, the total power to be processed by the PPC increases substantially due to the additional bias in $\overline{v}_{\mathrm{aux}}$ at nominal input voltage, which reduces the overall conversion efficiency of the P³DCT although operation with circulating power [cf., Fig. 4(b)] could be completely omitted if $\overline{v}_{\mathrm{aux}}$ remains positive for $n < 7.0$.

For the implemented hardware demonstrator described in detail in Section IV of this paper, a turns-ratio of $n = 7.75$ was chosen (cf., green line in Fig. 5), which results in a maximum power requirement of approximately 150 W. At rated output power and nominal input voltage, $V_{\mathrm{in}} = 380\,\mathrm{V}$, the PPC processes only around 20 W. Thus, the PPC must only be dimensioned for a fraction of the nominal output power processed by the main converter.

A numerical example based on efficiency measurements of the hardware demonstrator presented later in Section V should illustrate the marginal impairment of the overall conversion efficiency due to the PPC. The total conversion efficiency of the P³DCT can be derived from the Sankey diagrams (cf., Fig. 4) and is given by

$$\eta = \begin{cases} \eta_1\eta_2 \cdot (1+k) - \frac{\eta_2}{\eta_{\mathrm{aux}}} \cdot k, & \overline{v}_{\mathrm{aux}} < 0 \\ \eta_1\eta_2 \cdot (1-k) + \eta_2\eta_{\mathrm{aux}} \cdot k, & \overline{v}_{\mathrm{aux}} > 0 \end{cases} \tag{2}$$

wherein η_1 and η_2 denotes the efficiency of the inverter and the rectifier stage, respectively. Accordingly, the efficiency of the main converter is given by $\eta_{\mathrm{m}} = \eta_1\eta_2$. The efficiency of the PPP³ is denoted with η_3 and factor $k = {}^{P_{\mathrm{aux}}}/_{P_1}$ is the ratio between the power processed by the pre-regulator and the DCT. Given the efficiency of the main converter, $\eta_{\mathrm{m}} = 99.25\% \cdot 98.75\% = 98.0\%$, a power ratio $k = {}^{20\,\mathrm{W}}/_{1.5\,\mathrm{kW}} = 0.013$ and an efficiency $\eta_{\mathrm{aux}} = 82\%$ at 20 W of the PPC, then according to (2), $\eta = 97.7\%$ results if $\overline{v}_{\mathrm{aux}} < 0$ and $\eta = 97.8\%$ if $\overline{v}_{\mathrm{aux}} > 0$.

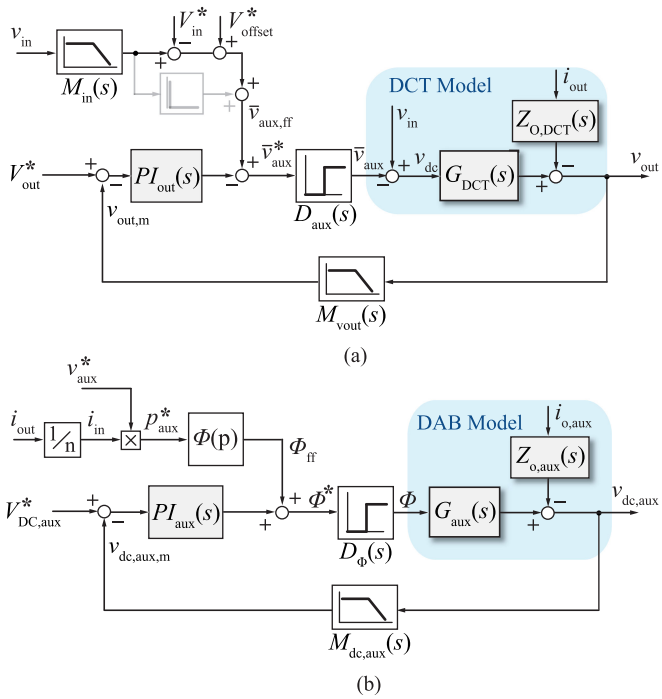

Fig. 6. Schematic of the control system to regulate (a) the output voltage, $v_{\rm out}$, of the main converter and (b) the dc-link voltage of the auxiliary converter, $v_{\rm dc,aux}$.

Hence, the (very) low efficiency (82%) of the PPC reduces the overall conversion efficiency of the converter at rated power only by 0.2%–0.3% at rated power and nominal input voltage.

III. Control System Design

In order to tightly regulate the output voltage to 48 V and reject load and input voltage disturbances, the control system depicted in Fig. 6 is proposed. Two feedback control loops are employed to regulate $v_{\rm out}$ and the PP dc-link voltage $v_{\rm dc,aux}$. As it will become evident from the experimental results presented in Section V, the dc-link of the PPC is sized large enough and/or the bandwidth of the $v_{\rm dc,aux}$ control loop suffices such that coupling between the control loops can be neglected and, for the sake of simplicity, two individual SISO designs are considered in the following.

The proposed small-signal feedback loop of the output voltage is shown in Fig. 6(a). A first-order low-pass filter with 1 kHz corner frequency, $M_{\rm vout}$, is employed to take both analog and digital implemented low-pass filters of the output voltage measurement into consideration. The control error, the difference between reference $V^*_{\rm out}$ and $v_{\rm out,m}$, is passed on to the PI controller

$$\mathrm{PI}_{\rm out}(s) = K_{\rm p,out}\frac{(sT_{\rm i,out}+1)}{s}. \tag{3}$$

Deviations of the input voltage from the nominal $V^*_{\rm in} = 380\,\mathrm{V}$ are directly compensated by means of the feed-forward term, $\overline{v}_{\rm aux,ff}$. The transfer function $M_{\rm in}$ represents a first-order low-pass with 10 kHz corner frequency and captures the phase-delay introduced by the measurement and conditioning of $v_{\rm in}$. A derivative term can be included to better cope with abrupt input voltage changes but was finally not implemented on the digital signal controller (DSC) of the hardware demonstrator. The parameter $V^*_{\rm offset}$, added to the measured input voltage, is used to adjust $\overline{v}^*_{\rm aux}$, such that the nominal input voltage results in the desired 48 V output voltage for a specific transformer turns-ratio. According to the polarity of the auxiliary voltage $\overline{v}_{\rm aux}$ in Fig. 2, $\overline{v}_{\rm aux}$ must be decreased in order to increase the output voltage, which explains why the output of $\mathrm{PI}_{\rm out}$ is subtracted from the feed-forward term, $\overline{v}_{\rm aux,ff}$. The deadtime introduced by the PWM of FB_3 is considered by means of a second-order Padé approximation of the delay $D_{\rm aux}(s) = \mathrm{e}^{-s\frac{T_{\rm s,aux}}{2}}$, where $T_{\rm s,aux}$ is the switching period of FB_3. In order to determine suitable coefficients for the PI controller, a small-signal model of the DCT including the CLC filter (cf., Fig. 2) was derived based on the analysis presented in [1]. The PI controller parameter (3) for a conservative design with 400 Hz bandwidth and 60° phase-margin are listed in Table III.

TABLE III
Controller Parameters

Controller	Parameter	Value
$\mathrm{PI}_{\rm out}$	$K_{\rm p,out}$	17.0×10^{3}
	$T_{\rm i,out}$	2.94×10^{-6}
$\mathrm{PI}_{\rm aux}$	$K_{\rm p,aux}$	1.5
	$T_{\rm i,aux}$	0.02
$\Phi(p)$	m	3.641×10^{-3} (rad/W)
	q	6.9×10^{-2} (rad)

The proposed feedback loop to control the PPC dc-link voltage, $v_{\rm dc,aux}$, is depicted in Fig. 6(b). By means of another PI controller

$$\mathrm{PI}_{\rm aux}(s) = K_{\rm p,aux}\frac{(sT_{\rm i,aux}+1)}{s} \tag{4}$$

the phase-shift Φ between the leading-leg of FB_1 and HB_3 is regulated in order to control the correct power flow at the terminals of the transformer tertiary winding (cf., $4-\overline{4}$ in Fig. 2) such that $v_{\rm dc,aux}$ meets the reference value $V^*_{\rm dc,aux}$. A first-order low-pass filter with 1 kHz corner frequency, $M_{\rm dc,aux}$, is employed to model the measurement and conditioning of the dc-link voltage. The deadtime introduced by the PWM of HB_1 is considered by means of a second-order Padé approximation of the delay $D_\phi(s) = \mathrm{e}^{-s\frac{T_{\rm s}}{2}}$, where $T_{\rm s}$ is the switching period of FB_1. In order to determine proper parameters for $\mathrm{PI}_{\rm out}(s)$, a small-signal model of the PPC rectifier, $G_{\rm aux}(s) = \frac{v_{\rm dc,aux}(s)}{\Phi(s)}$, was derived according to the work in [2] and [3]. The PI controller parameter (4) for a conservative design with 100 Hz bandwidth and 135° phase-margin are listed in Table III. By estimating the power processed by the PPC

$$p^*_{\rm aux} = \overline{v}_{\rm aux}I_{\rm in} \approx \overline{v}^*_{\rm aux}I_{\rm in} = \overline{v}^*_{\rm aux}\frac{I_{\rm out}}{n} \tag{5}$$

a feed-forward phase-shift term, $\Phi^*_{\rm ff}$, is added to the output of controller $\mathrm{PI}_{\rm aux}$. The phase-shift in the range $[-\pi/2, \pi/2]$ as a

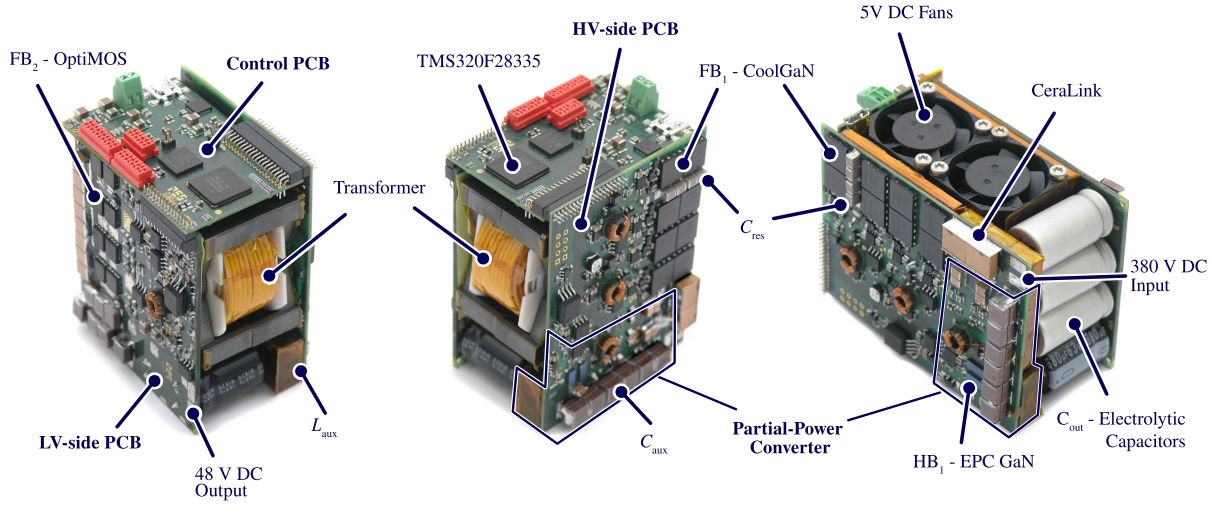

Fig. 7. Pictures of the implemented P³DCT hardware prototype taken from different perspectives.

function of power is given by [3]

$$\Phi(p^*_{\mathrm{aux}}) = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8 f_{\mathrm{s,FB1}} L_{\mathrm{aux}} |p^*_{\mathrm{aux}}|}{(1^1/_2 v_{\mathrm{dc,aux}})(1^{N_3}/_{N_2} v_{\mathrm{out}})}}\right) \cdot \mathrm{sign}(p^*_{\mathrm{aux}}) \tag{6}$$

and is linearized around the nominal operating point ($P_{\mathrm{out}} = 1.5\,\mathrm{kW}$, $P_{\mathrm{aux}} = 20\,\mathrm{W}$) in order to facilitate implementation on the DSC of the hardware prototype

$$\Phi(p^*_{\mathrm{aux}}) \approx m \cdot p^*_{\mathrm{aux}} + q \tag{7}$$

with parameters m and q listed in Table III.

In order to implement the designed controllers on the DSC of the hardware prototype (cf., Section IV), $\mathrm{PI}_{\mathrm{out}}(s)$ and $\mathrm{PI}_{\mathrm{aux}}(s)$ were discretized using the Tustin z-transformation with a sample frequency of $F_{\mathrm{ctrl}} = 25\,\mathrm{kHz}$. In addition, the designed PI controllers were augmented with output limitation and anti-windup capability.

IV. Hardware Prototype

In order to verify the proposed converter topology shown in Fig. 2 and assess the performance of the suggested control system, a hardware prototype was realized as will be described in this section. The implemented 380 V/48 V P³DCT is depicted in Fig. 7. The system is rated for 1.5 kW and exhibits a total volume of 175 cm³, which corresponds to a power density of 8.6 kWdm^{-3} (141 W/in³). Only 10%–15% of the total converter volume is occupied by components related to the PPC. The component parameter values of the realized hardware are listed in Table IV and have been obtained from a comprehensive Pareto design optimization, seeking maximum power density at a minimum target efficiency of around 98%.

As it can be seen from the picture, the converter system is realized by means of two individual power Printed Circuit Boards (PCBs), the first PCB is equipped with power electronic components of the HV-side (380 V) and the PPC and the second PCB with the power electronics of the LV-side (48 V). In addition, a third dedicated digital control and auxiliary supply board is connected to both power PCBs. In order to extract the losses from the power electronics, both power PCBs are attached to the baseplates of a double-sided forced-air cooled heatsink. The implemented cooling system with 25 mm × 25 mm, 5 V dc fans achieves an Rth of around 0.49 KW^{-1} at a volume of roughly 33 cm³, which corresponds to a cooling system performance index ([4]) of roughly 62 WK^{-1} dm^{-3}. The primary-side full-bridge (cf., FB_1) is realized with 600 V, 55 mΩ E-mode GaN from Infineon, whereby two physical transistors are connected in parallel per switch. The employed gate drive employs the LM5114 IC and the MAX13256 full-bridge transformer driver IC for galvanic isolation of the high-side supply voltage and is described in detail in [21].

The secondary-side full-bridge (cf., FB_2) is realized with 60 V, 2.5 mΩ OptiMOS from Infineon, also with two physical transistors per switch, and employs the UCC27211A gate drive IC with bootstrapping supply of the high-side gate voltage. The switching frequency of FB_1 and FB_3 is 100 kHz, which corresponds to the natural frequency of the series resonant tank comprised of L_σ, the stray inductance of the transformer, and C_{res}. The employed three-winding transformer, encompassed by the PCBs and cooled by the air-flow exiting the heatsink, is implemented by means of a PQ 40/40, N97 MnZn ferrite core with custom-machined total height of 30 mm. In order to adjust the magnetizing current to achieve ZVS of FB_1, a total air gap of 200 μm is introduced resulting in a magnetizing inductance of 950 μH. HF-litz wire according to the specifications in Table IV is used to implement the three windings of the transformer, whereby $N_1 = 31$ and $N_2 = 4$ results in a turns ratio of $n = 7.75$ and $N_3 = 2$ results in a turns ratio of $n_{\mathrm{aux}} = 15.5$. The stacked dc-link capacitors of the PPC, C_{aux}, are assembled from 5 × 22 μF, 100 V MLCCs, and $V_{\mathrm{dc,aux}}$ is regulated to 50 V by means of adjusting the phase-shift between $\mathrm{FB}_{1/2}$ and HB_3. An additional discrete inductor, $L_3 = 3.0\,\mu\mathrm{H}$, is added, which results in a linearized power-transfer to

TABLE IV
TECHNICAL DETAILS OF THE IMPLEMENTED P^3 DCT HARDWARE PROTOTYPE

	Component	Parameter	Description	Part Number
Power Semiconductors	FB_1	600 V, 55 mΩ Infineon CoolGaN	HV-side full-bridge, 2 transistors in parallel	BSC028N06NS
	FB_2	60 V, 2.5 mΩ Infineon OptiMOS	LV-side full-bridge, 2 transistors in parallel	
	HB_1	100 V, 3.0 mΩ EPC GaN	Transformer-side half-bridge	EPC2022
	FB_3	100 V, 5.6 mΩ EPC GaN	HV-side full-bridge	EPC2001C
	F_s	100 kHz	Switching frequency of FB_1, FB_2, HB_1	
	$F_{\mathrm{s,aux}}$	600 kHz	Switching frequency of FB_3	
Transformer & Resonant Tank	Core	PQ 40/40, MnZn Ferrite N97	Customized 30 mm height and 100 µm gap	B65883A0000R097
	N_1	31 turns	120 × 71 µm HF-litz wire	
	N_2	4 turns	630 × 71 µm HF-litz wire	
	N_3	2 turns	120 × 71 µm HF-litz wire	
	L_σ	18 µH	Stray inductance of transformer	
	L_m	950 µH	Magnetizing inductance of transformer	
	C_res	4 × 33 nF	630 V C0G MLCC	C3225C0G2J333J250AA
DC Capacitors & Filter Passives	C_in	5 × 2 µF	500 V CeraLink	
	C_aux	5 × 22 µF	100 V X7S MLCC	CKG57NX7S2A226M500JJ
	L_aux	3.0 µH	Coilcraft Power Inductor 43 A I_sat	XAL1580-302
	C_f	14 × 22 µF	100 V X7S MLCC	CKG57NX7S2A226M500JJ
	L_f	150 nH	Inductor 50 A I_sat	FP0906R1-R15-R
	C_out	3 × 560 µF	63 V Electrolytic Capacitor	EGPD630ELL561MK25H
		1 × 680 µF	63 V Electrolytic Capacitor	UHW1J681MHD6TN
Cooling System	l_hs	11 mm	Length of the heatsink	
	w_hs	50 mm	Width of the heatsink	
	h_hs	25 mm	Height of the fins	
	$w_{\mathrm{c,hs}}$	0.7 mm	Space between individual fins	
	b_hs	4 mm	Thickness of the baseplate	
	Fans	5 V DC	Dimension: 25 mm x 25 mm	MC25060V2-000U-A99

phase-shift ratio of $\frac{P_\mathrm{aux}}{\Phi} \approx 4.795\,\mathrm{W}/^\circ$ (cf., (7) and Table III). The PPC is designed to process peak powers up to 150 w in order to cope with the specified input voltage range (340–420 V) up to the rated power of the converter. At nominal dc input voltage, $V_\mathrm{in} = 380\,\mathrm{V}$, and 1.5 kW output power, the PPC processes just 20 w, which corresponds to a phase-shift of roughly 4.2°. The rectifier half-bridge, HB_3, and the inverter full-bridge, FB_3, of the PPC, are implemented using 100 V E-mode GaN HEMT from EPC in combination with Si8274 gate drive IC from Silicon Labs. The switching frequency of the inverter is set to $f_{\mathrm{s,aux}} = 600\,\mathrm{kHz}$, a reasonable tradeoff between the distortion of the LLC converter's sinusoidal current and the occurring switching loss in FB_3. The output filter at the 48 V side of the converter was designed to meet the 100 mV steady-state ripple requirement and confine output voltage deviation during load and input voltage transients to $\pm 500\,\mathrm{mV}$ ($\approx \pm 1\%$ of 48 V). The implemented CLC filter structure (cf., Fig. 2) is comprised of 100 V MLCCs at the output of FB_3, $C_\mathrm{f} = 308\,\mu\mathrm{F}$, a subsequent 150 nH inductor, and an 2.4 mF output capacitance assembled from individual 560 μF, 63 V aluminum electrolytic capacitors.

The developed control system presented in Section III was implemented on a TMS320F28335 DSC from Texas Instruments Delfino series, located on the designated control PCB. The DSC generates the constant 50% duty-cycle gate signals for full-bridge FB_1, FB_2 and the phase-shift adjusted half-bridge

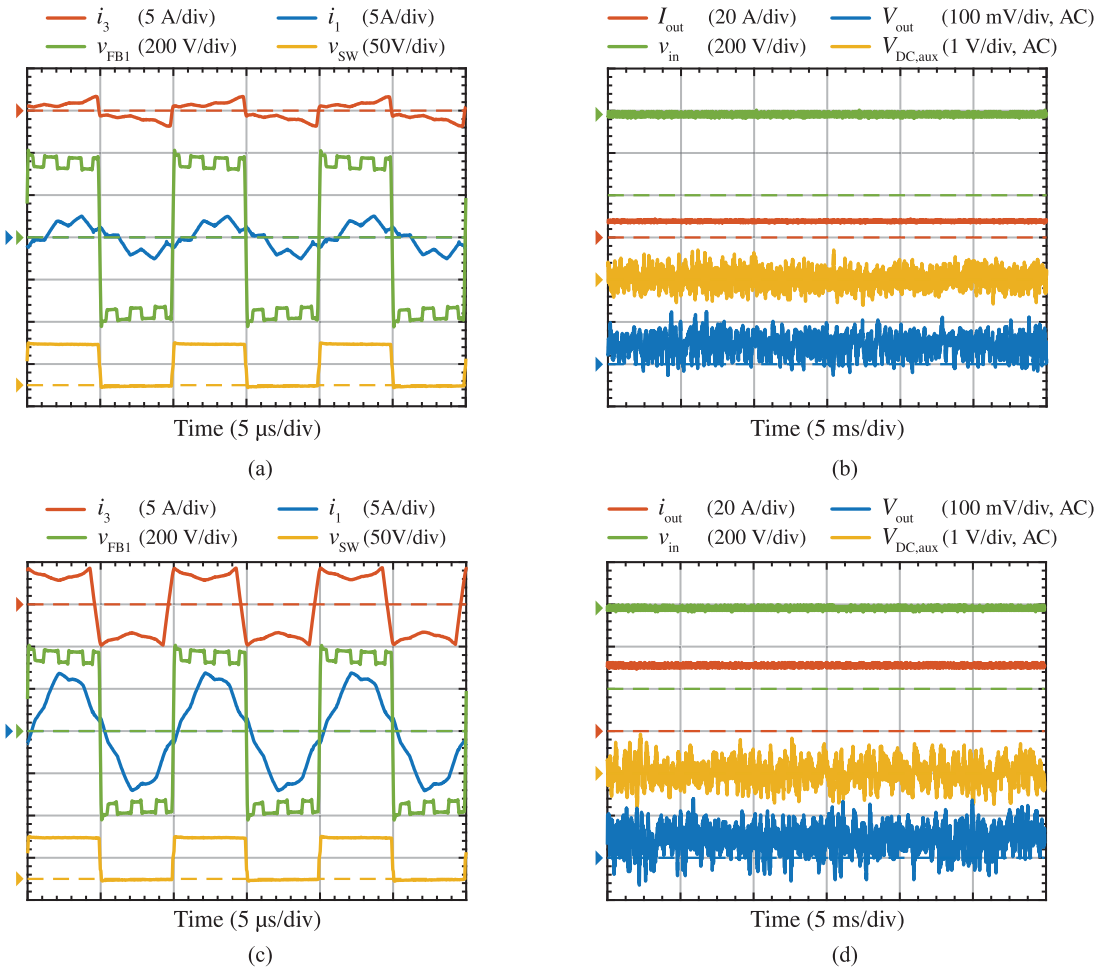

Fig. 8. Measured steady-state waveforms of the P³DCT hardware demonstrator operating at a quarter of the output power, $1^{P_r}/_4 = 350\,\mathrm{W}$, shown in (a) and (b) and at rated output power, $P_r = 1.5\,\mathrm{kW}$, shown in (c) and (d). The waveforms of the HF link are depicted in (a) and (c) and the dc waveforms are shown in (b) and (d). The waveforms are labeled according to the circuit schematic shown in Fig. 2.

HB_3 and the varying duty-cycle gate signals for the inverter full-bridge, FB_3. The control board is supplied by means of a 12 V laboratory voltage source and is equipped with 12 V/5 V dc–dc converters (LMZ21701) to provide auxiliary power to the HV and LV power boards. The ground potential of the control board is connected to the dc-rail of the HV full-bridge FB_1 (cf., terminal $\overline{2}$ in Fig. 2).

The dc input voltage, V_{in}, is measured by means of a differential amplifier with a corner frequency set to 12 kHz employing the AD8615 operational amplifier from Analog Devices. The 48 V output voltage, V_{out}, is measured by means of a differential amplifier with a corner frequency set to 48 kHz employing the AD8615 operational amplifier. Subsequently, the precision isolation amplifier ACPL-C79B from Broadcom is employed to provide galvanic isolation between control board and LV-side. The output current, I_{out}, is measured with the current sensor ACS722 from Allegro featuring a 80 kHz bandwidth. The dc-link voltage of the PPC, $V_{\mathrm{dc,aux}}$, is sensed by means of a differential amplifier with a corner frequency of 30 kHz employing the AD8615 operational amplifier and subsequently the ACPL-C87BT isolation amplifier from Broadcom to provide galvanic isolation between PPC and control board.

V. Experimental Results

In this section, the experimental measurement results of the implemented P³DCT prototype are presented. First, the performance of the converter system under steady-state conditions is presented and subsequently the effectiveness of the proposed topology and control system is confirmed by step response waveforms. The output voltage is tightly regulated to 48 V and the dc-link of the PPC is regulated to 50 V.

A. Steady-State Measurements

The waveforms of the P³DCT operating in steady-state at 350 W output power ($P_r/4$) and 380 V nominal input voltage are shown in Fig. 8(a) and (b) and at 1.5 kW output power in Fig. 8(c) and (d). The high-frequency ac waveforms of the converter are shown in Fig. 8(a) and (b) with a time resolution of 5 μs/division and the dc waveforms are depicted in Fig. 8(c) and (d) with a time resolution of 5 ms/division. The waveforms are labeled according to the circuit schematic shown in Fig. 2. Clearly visible is the superimposed pulse pattern in v_{FB1} and the deviation of current i_1 from its ideal sinusoidal shape, which is more pronounced under light load condition.

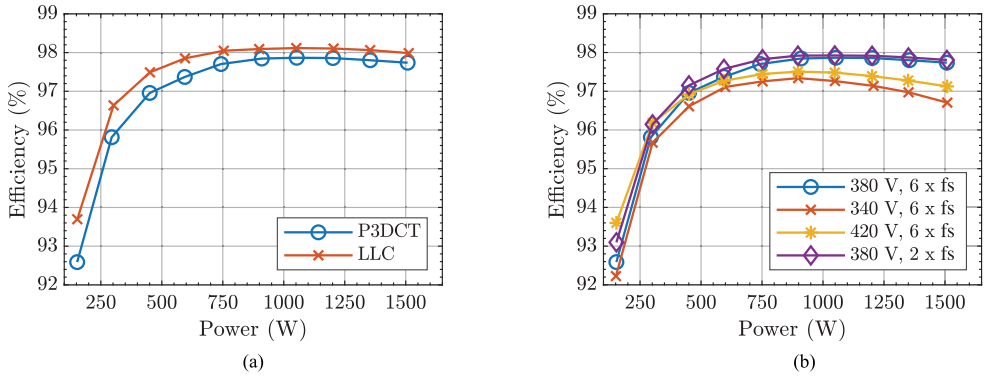

Fig. 9. Efficiency of the P^{3}DCT with respect to output power determined with Yokogawa WT3000 power analyzer. (a) shows the efficiency of the P^{3}DCT for nominal input voltage, $V_{\mathrm{in}} = 380\,\mathrm{V}$, opposed to the efficiency of the unregulated DCT (main converter) without PPC. (b) shows the efficiency of the P^{3}DCT with respect to output power for different input voltages and switching frequencies of FB_3 (cf., Fig. 2).

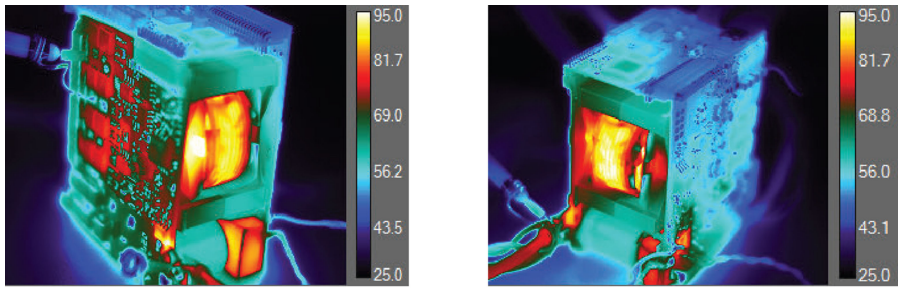

Fig. 10. Steady-state IR image of the P^{3}DCT operating at 1.5 kW output power. The PPC processes 100W in the selected operating point. The low-voltage side of the converter facing the IR camera is shown in (a) and the high-voltage side in (b).

The power processed by the PPC increases from 9 W at 350 W output power to around 20 W at rated output power also indicated by the increased amplitude of i_3. Moreover, the V_{out} voltage ripple requirement of ± 100 mV is met as can be inferred from Fig. 8(b) and (d). The conversion efficiency of the P^{3}DCT was determined with the Yokogawa WT3000 power analyzer and includes the 12 V auxiliary power supply for digital control and gate drive circuitry as well as the 5 V power supply for the employed dc fans. Fig. 9(a) depicts the measured conversion efficiency with respect to output power of the P^{3}DCT (blue line) and the DCT without regulation (red line). The realized P^{3}DCT exhibits an efficiency of 97.7% at 1.5 kW and shows a peak efficiency of 97.9% around 1.0 kW. In comparison, the DCT transformer without regulation (PPC disabled and/or bypassed) reaches 98.0% efficiency at 1.5 kW and a peak efficiency of 98.1% around 1.0 kW. It must be mentioned that, in case of the unregulated DCT, the input voltage V_{in} was slightly adjusted (3% max. deviation from nominal input voltage) to ensure 48 V at the output. It can be concluded that the additional PPC leads to a reduction of efficiency by approximately 0.25% for an output power above 1 kW and to a reduction of 0.3%–1% in the low output power range. At rated output power, the reduction of 0.25% in efficiency corresponds to an additional power loss of roughly 3.75 W caused by the PPC assuming that the loss of the DCT is unchanged. The PPC processes around 20 W at the input terminal (cf., $3 - \overline{3}$ in Fig. 2) in this operating point, which results in an estimated efficiency of approximately 82%.

The efficiency with respect to output power for the minimal and maximal specified input voltages, $V_{\mathrm{in}} = 340\,\mathrm{V}$ and $V_{\mathrm{in}} = 420\,\mathrm{V}$ is depicted in red (cross marker) and in yellow (star marked) in Fig. 9(b), respectively. Since the PPC processes a larger share of the output power if the input voltage deviates from the nominal 380 V, the overall converter efficiency deteriorates as the PPC exhibits a lower efficiency. At 340 and 420 V, the overall efficiency at the rated power drops to 96.7% and 97.13%, respectively. As discussed in Section A, for lower than nominal input voltage, the power processed by the PPC only circulates within the system and is not provided to the output, which explains why the overall efficiency at $V_{\mathrm{in}} = 340\,\mathrm{V}$ is lower compared to $V_{\mathrm{in}} = 420\,\mathrm{V}$. Moreover, the efficiency of the P^{3}DCT with inverter full-bridge FB_3 operating at only 200 kHz (only twice the DCT switching frequency, F_{s}) is depicted in purple (diamond marker). It can be seen that the overall efficiency marginally improves, most notably at light load conditions. The infrared (IR) images in Fig. 10 show the steady-state temperature distribution of the P^{3}DCT operating at 1.5 kW output power with 100 W being processed by the PPC. The captured temperature distribution of the converter with the LV-side and HV-side facing the IR camera is depicted in Fig. 10(a) and (b), respectively, and reveals that permanent operation at rated power can be sustained by the realized hardware. It can be seen that the max. measured surface temperature of 95 °C is attained by the transformer winding. The LV-side power transistors (OptiMOS) and the rectifier of the PPC attain a steady-state temperature of

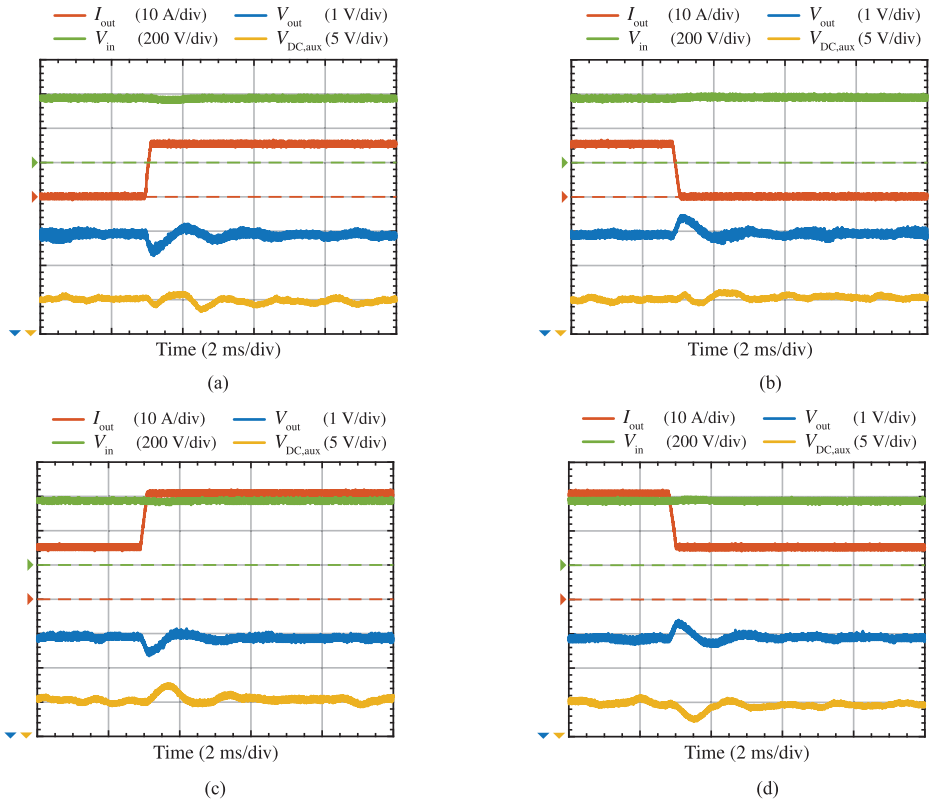

Fig. 11. Measured output voltage V_{out} and PPC dc-link time behavior of the P³DCT hardware demonstrator subject to a stepwise output load change between 0 and 750 W shown in (a) and (b) and between 750 W and 1.5 kW shown in (c) and (d). The waveforms are labeled according to the circuit schematic shown in Fig. 2.

around 80 °C. The HV-side power transistors (CoolGaN) and the inverter of the PPC exhibit a surface temperature in the 60 °C range.

B. Step Response Measurements

In order to assess the performance of the converter with proposed control system, stepwise input voltage and output load variations were applied. The output load was adjusted with a Chroma 63202 electric load and the input voltage steps were applied using a Xantrex XDC 600-10 dc supply. The current and voltage slew-rates of the supplies were set to their maximum supported values for the conducted step response experiments. Fig. 11(a) and (b) depict the output voltage and PPC dc-link voltage of the P³DCT subject to a stepwise change of output load between 0 and 750 W. Likewise, the response to a stepwise change of output load between 750 and 1.5 kW is shown in Fig. 11(c) and (d). It can be seen from the measurements that stepwise load changes up to half the rated power are causing a V_{out} deviation of less than ± 500 mV ($\approx \pm 1\%$ of 48 V), which is eliminated by the control in less than approximately 5 ms. The deviation in dc-link voltage, $V_{\mathrm{dc,aux}}$, remains within ± 3 V and settles within 3 ms. The responses of the P³DCT subject to a 50 V stepwise change in input voltage amplitude between 350 and 400 V are shown in Fig. 12, whereby in Fig. 12(a) and (b), the input voltage steps are performed at 750 W output power and in Fig. 12(c) and (d) at 1.5 kW output power.

It can be seen from the experimental waveforms that the maximum V_{out} deviation resulting from input voltage steps with 50 V magnitude is also around ± 500 mV and settles in less than approximately 8 ms. The deviation in dc-link voltage, $V_{\mathrm{dc,aux}}$, remains within ± 7 V and settles within 8ms. Note that because of the limited current sink capability of the employed dc supply, the input voltage slope is mainly governed by the actual load of the converter, which explains the different slew rates in Fig. 12(c) and (d), and consequently there is an undershoot of roughly 20 V present in V_{in}.

Remark: In order to visualize the basic operation of the P³DCT, this paper is accompanied with additional video content showing the oscilloscope screen with several captured waveforms: Channel C1 (yellow) shows the PPC dc-link voltage $V_{\mathrm{dc,aux}}$; Channel C2 (red) shows the PPC rectifier current i_3; Channel C3 shows output voltage V_{out} (blue); Channel C4 (green) shows the primary full-bridge voltage, v_{FB1}. In **Video A**, the output voltage reference is slowly varied between 43 and 52 V in order to visualize how controller $\mathrm{PI}_{\mathrm{out}}$ adjusts $\overline{v}_{\mathrm{aux}}$; the superimposed pulse-pattern in v_{FB1} changes accordingly. The dc-link voltage controller, $\mathrm{PI}_{\mathrm{aux}}$, adjusts the phase-shift according to the resulting processed power (depends on level of $\overline{v}_{\mathrm{aux}}$), which alters the amplitude of current i_3 to keep $V_{\mathrm{dc,aux}}$ at its reference value. In a similar fashion, **Video B** shows the waveforms of the P³DCT subject to a slow variation of the dc-link reference value between 40 and 60 V, illustrating how the dc-link voltage can be changed while keeping V_{out} tightly

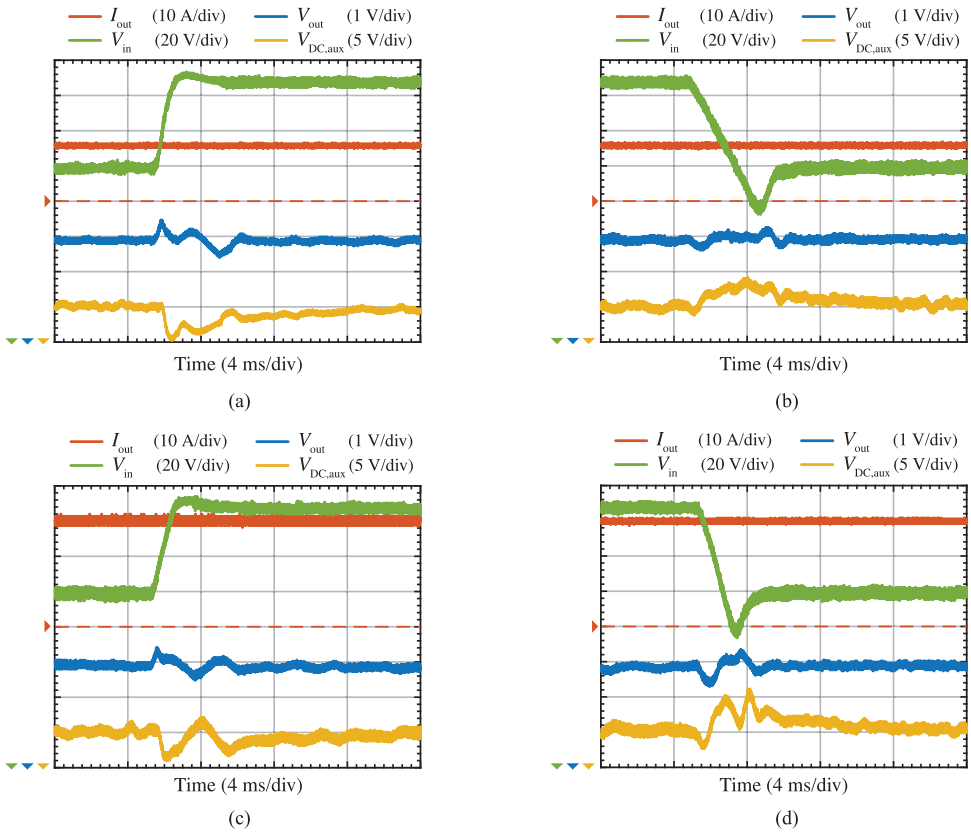

Fig. 12. Measured output voltage V_{out} and PPC dc-link time behavior of the $\mathrm{P}^3\mathrm{DCT}$ hardware demonstrator subject to a stepwise change of the input voltage change V_{in} between 350 and 400 V shown in (a) and (b) for 750 W output power and in (c) and (d) for 1.5 kW output power. The waveforms are labeled according to circuit schematic in Fig. 2.

regulated to the desired 48 V. In **Video C**, the dc input voltage of the P^3DCT, V_{in}, is slowly varied between 340 and 420 V. It can be seen how $\overline{v}_{\mathrm{aux}}$ and thus the superimposed pulse-pattern is adopted by controller $\mathrm{PI}_{\mathrm{out}}$ in order to keep V_{out} at 48 V despite the changing input voltage.

VI. Conclusion

In this paper, a novel approach to realize a high efficiency 380 to 48 V dc–dc converter with output voltage regulation was presented. A main dc–dc converter, implemented by means of an unregulated resonant *LLC* converter operating as DCT, is accompanied by a PPC dedicated to tightly regulate the output voltage by means of adjusting the average input voltage of the main converter. Taking advantage of the transfer characteristic of the DCT, a filter-less implementation of the PPC was proposed where the pulsewidth modulated auxiliary dc-link voltage is superimposed to the dc input voltage of the main converter. Since the PPC processes only a fraction of the rated power, the overall efficiency is only marginally affected. A prototype of the proposed converter rated at 1.5 kW was implemented and specified to cope with input voltage variations between 340 and 420 V. The hardware demonstrator features an overall conversion efficiency of 97.7% at rated power and a power density of 8.6 kWdm^{-3}. The performance of the PP regulator with proposed control system was assessed by means of input voltage and load step responses. A stepwise change of half the rated output power (750 W) and a 50 V stepwise variation of the input voltage are causing an output voltage deviation of less than $\pm 500\,\mathrm{mV}$, which is settled within 8 ms.

Adding output voltage control to an unregulated, series-resonant *LLC* dc–dc converter by means of a PPC adds roughly 10% of volume to the converter while reducing the overall efficiency by 0.3%. The proposed PPC can also be used to mitigate or completely eliminate the double-line frequency dc voltage ripple in single-phase dc–ac converter systems with very tight voltage ripple requirements and/or demanding power density requirements.

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