Optimal Design Method of Interleaved Boost PFC for Improving Efficiency from Switching Frequency, Boost Inductor, and Output Voltage

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***Abstract*—Many research works have been conducted on increasing the efficiency of interleaved boost converters (IBCs) applied for power factor correction (PFC) by using high-performance power electronic devices and soft switching circuits, which are not helpful in reducing the hardware cost and systematic complexity. In this paper, three intrinsic parameters affecting the efficiency of IBC PFC are found and analyzed, including the switching frequency value, boost inductor value, and output voltage value. Based on the findings, considering the limitations of current ripples, power factor, maximum magnetic flux density, and volume of a boost inductor, an optimization design method for high-efficiency IBC PFC is proposed. A 3.3-kW IBC PFC prototype is developed based on Si devices. The experimental result verifies that the proposed method can improve the efficiency of IBC PFC with low-cost low-performance devices in the full-load range.**

***Index Terms*—Boost inductor, high efficiency, interleaved boost converter (IBC), output voltage, power factor correction (PFC), switching frequency.**

NOMENCLATURE

$A_{L,l}$	Inductance coefficient of boost inductor.
$B_{\max,\text{allowed}}$	Allowed maximum magnetic flux density.
$B_{L,\max}$	Maximum magnetic flux density in a grid period.
$B_{L,\max}^{(k)}$	Value of $B_{L,\max}$ in the kth switching period.
C_e	Electromagnetic interference (EMI) capacitor.
C_o	Output capacitor.
D	Thickness of the boost inductor's winding layer.
D_1, D_4	Diodes of the rectifier bridge.
D_5, D_6	Freewheeling diodes.
I_{ac}	RMS value of i_{ac}.
I_{Ce}	RMS value of i_{Ce}.
$I_{Co,\text{hf}}$	High-frequency component of i_{Co}.

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$P_{\text{dio, rev}}$ Reverse recovery loss of the freewheeling diode.
$P_{\text{dri, loss}}$ Driving loss.
$P_{\text{tot, loss}}$ Total loss of an IBC.
P_o Output power.
Q_1, Q_2 MOSFETs.
Q_g Total charge of MOSFET.
Q_{rr} Reverse recovery charge of freewheeling diodes.
R_{bri} Equivalent series resistor (ESR) of the rectifier bridge.
R_{Ce} ESR of the EMI capacitor.
R_c ESR of the capacitor.
$R_{Co,\text{lf}}$ Low-frequency ESR of C_o.
$R_{Co,\text{hf}}$ High-frequency ESR of C_o.
R_{dio} ON-resistor of the freewheeling diode.
$R_{ds,\text{on}}$ ON-resistor of MOSFET.
R_{Le} ESR of the EMI inductor's windings.
$R_{L,\text{ac}}$ AC resistor of the boost inductor's windings.
$R_{L,\text{dc}}$ DC resistor of the boost inductor's windings.
S_1, S_2 Trigger pulses of Q_1 and Q_2.
S_w Cross-sectional area of the winding's conductor.
$T_{\text{mos},j}$ Junction temperature of MOSFET.
T_j Junction temperature of the rectifier bridge.
V_{ac} RMS value of the input voltage.
V_{dri} Driving voltage.
$V_{F,\text{bri}}$ Forward voltage-drop of the rectifier bridge.
$V_{F,\text{dio}}$ Forward voltage-drop of the freewheeling diode.
V_L Volume of the magnetic core.
V_o Output voltage.
ΔT_L Temperature rise of the conductor.
$d_1^{(k)}, d_2^{(k)}$ Duty cycles in the kth switching period.
f_g Frequency of the input voltage.
f_s Switching frequency.
i_{ac} Input current.
i_{Ce} Current flowing though C_e.
i_{Co} Current flowing through C_o.
i_{D5}, i_{D6} Currents flowing through D_5 and D_6.
i_{rect} Current flowing through the rectifier bridge.
i_{L1}, i_{L2} Currents flowing through L_1 and L_2.
$i_{L1,\text{avg}}, i_{L2,\text{avg}}$ Average current of i_{L1} and i_{L2}.
$i_{L1,\text{avg}}^{(k)}$ Peak value of $i_{L1,\text{avg}}$ in the kth switching period.
$i_{L1,peak}^{(k)}$ Peak current of i_{L1} in the kth switching period.
i_{load} Current flowing through R_{load}.
i_{Q1}, i_{Q2} Currents flowing through Q_1 and Q_2.
i_o Output current.
$l_{L,\text{mlt}}$ Mean length per turn of the boost inductor's core.
l_g Gap length of the magnetic core.
m Number of the boost inductor's winding layers.
k Sequence of the switching period.
PF Power factor of the IBC.
$r_{L,\text{per}}$ Average ESR per turn of the boost inductor.
t_g Period of the input voltage.
t_s Switching period.
$t_{\text{mos},f}$ Fall time of MOSFET.
$t_{\text{mos},r}$ Rise time of MOSFET.
$u(t)$ Step function.
v_{ac} Input ac voltage.
α_{20} Temperature coefficient of the conductor.
α_L, β_L, K_L Dimensional parameters of the magnetic core.
$\alpha_{L,\text{rip}}$ Ratio of current ripples of the boost inductor.
$\alpha_{L,\text{rip,allowed}}$ Allowed ratio of current ripples.
σ Conductivity of the boost inductor's windings.
ω_g Angular frequency of v_{ac}.
$\delta(t)$ Impulse function.
δ_c Loss angle of the capacitor.
δ_{skin} Skin depth of windings.
ρ_{20} Resistivity of the conductor at 20 °C.
μ_0 Space permeability.
$\mu_{L,\text{eff}}$ Effective permeability of the boost inductor's core.
η Efficiency of the IBC.
$\eta_{\min,\text{full}}$ Minimum efficiency at full load.
$\Delta i_{L1}^{(k)}$ Current ripple of i_{L1} in the kth switching period.

I. Introduction

THE interleaved boost converter (IBC) is commonly used for power factor correction (PFC) due to its advantages of low current ripples, small filtering volume, and high power density. Power density is a key factor that limits the application of the IBC PFC, which requires only a small volume and is light weight, such as on-board chargers (OBCs), laptop adapters, and aircraft power supply. Heatsink, which is used to transfer the heat generated by power loss to maintain the working temperature of devices within the proper range, occupies a lot of volume in the IBC PFC. Therefore, it is necessary to reduce the heatsink volume by increasing the efficiency. If the efficiency can be increased without additional hardware and software costs, then the total loss and heat can be decreased, the heatsink volume can be reduced, and the power density of the IBC PFC can be increased.

Many research works have been conducted to improve the efficiency of the IBC PFC by modifying the topology to create a soft switching condition for reducing the switching loss. For example, an auxiliary coupled inductor is introduced in [1] to realize the zero-voltage switching turn-ON condition of a MOSFET. An auxiliary device is added in [2] to realize the zero-current switching (ZCS) condition of an IGBT. A snubber cell is introduced in [3] to realize the soft switching condition of all devices. The above-mentioned auxiliary circuits can reduce the switching loss, but they simultaneously increase the complexity and cost of hardware, which are not practical for the industry. To increase the efficiency without adding any extra circuits, some research works aimed at using high-performance power electronic devices have been conducted. As is known to all, wide bandgap (WBG) devices, such as SiC devices and GaN devices, have better material properties compared with traditional Si de-

vices; this allows WBG devices to operate at higher switching speeds, higher voltages, and higher temperatures [4]. Moreover, the ON-resistance of WBG devices is much lower than that of Si devices. They also have a much lower switching loss and conduction loss compared with Si devices. Due to these advantages, all Si devices are replaced by WBG devices in [5] to increase the efficiency of a two-stage 6.6-kW OBC from 94% to 96%. WBG devices can, indeed, increase the efficiency; however, their cost is much higher than that of Si devices, which is an obstacle to commercial applications. It is impossible to completely replace Si devices by WBG devices within a short period due to their high cost, especially in industrial applications.

An IBC consists of an input EMI filter, a rectifier bridge, boost inductors, high-frequency power switches, freewheeling diodes, and an output capacitor. In addition to circuit modification and WBG device utilization, the efficiency and power density of the IBC can be improved by optimizing the components and its intrinsic parameters. To increase the power density, boost inductors are optimized, considering the switching loss, system volume, inductor power loss, working temperature, and electromagnetic noise, in [6] and [7]. Integrated magnetics and coupled inductors are used to reduce the volume of boost inductors in [8] and [9]. In [10], a comprehensive optimization method is used to optimize the operation modes, the EMI filter, and the switching frequency, considering the volume and losses of components, the lifetime of the capacitor, and the cost of the IBC. A proportional switching strategy for reducing current ripples of a dc–dc boost converter is implemented in [11]; however, it is not suitable for PFC application because its input voltage is not a sinusoidal waveform.

To improve the efficiency, a digital adaptive discontinuous current source drive (CSD) circuit for reducing driving and switching losses is proposed in [12], and the experimental result verifies that the efficiency can be increased from 92.5% to 93.2%; however, this method is limited if the power switches are voltage-driven devices. In [13] and [14], an adaptive switching strategy is proposed to increase the efficiency. Based on the work presented in [13], a proportional switching strategy is also used to optimize the efficiency as well as the power density in [15]. The relationship between efficiency and switching frequency can be used to optimize the efficiency of a boost converter [15], [16]. However, the optimization methods in [13]–[16] are suitable only for dc–dc applications and not for PFC because the input voltage and currents flowing through boost inductors are not sinusoidal. Pulse-frequency modulation (PFM) control is used in [17] to improve the efficiency of a boost converter, but it has disadvantages, such as a narrow frequency spectrum, a large output ripple, and a large EMI [18]. In [19], a nonlinear inductor is designed to improve the light-load efficiency of a boost PFC, but the nonlinear inductor is susceptible to temperature and is difficult to design, and there is no experimental confirmation of the idea proposed in [19]. In [20], one winding of coupled saturable inductors is used to reduce the reverse recovery loss of freewheeling diodes, but an extra winding cascaded with a freewheeling diode leads to a complex circuit configuration.

In fact, the efficiency of the IBC PFC is mainly determined by rms currents, switching currents, and the performance of components. The power density of the IBC PFC is mainly affected by the layout of the printed circuit board (PCB) and the volume of the EMI filter, boost inductors, output capacitors, and heatsink. On the one hand, rms currents and switching currents have a direct relationship with current ripples. A large current ripple brings large rms currents and switching currents. For the concerned input voltage and output power, the current ripple is determined by three optimizable parameters, including the switching frequency, the boost inductance, and the output voltage, which means that the efficiency can be optimized from the perspectives of the three above-mentioned intrinsic parameters. On the other hand, for the concerned input voltage and output power, volumes of passive components are determined by the operation frequency and current ripple. Since the current ripple is affected by three intrinsic parameters, the volume of passive components also has a direct relationship with the switching frequency, the boost inductance, and the output voltage, i.e., the switching frequency, the boost inductance, and the output voltage can be used to optimize the efficiency and power density of the IBC PFC.

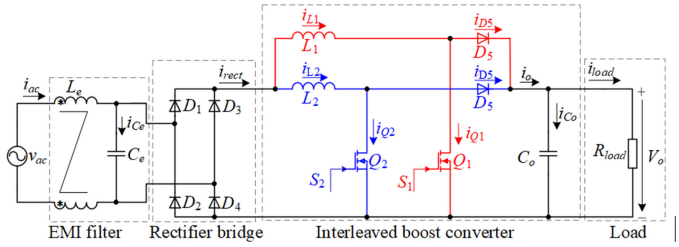


Fig. 1. Topology of a single-phase IBC applied for PFC.

Based on the aforementioned analyses, considering the limitations of current ripples, magnetic flux density, boost inductor volume, and power switches' junction temperature, this paper proposes a comprehensive design method to design a high-efficiency high power density high PF IBC PFC by optimizing the switching frequency, the boost inductor, and the output voltage without adding any extra auxiliary circuits or using high-performance high-cost devices. The efficiency is calculated and analyzed by an iterative method in the time-domain.

II. Interleaved Boost PFC

A. Topology of the IBC

The topology of the IBC is shown in Fig. 1, where the input ac voltage is $v_{\rm ac} = \sqrt{2}V_{\rm ac}\sin(\omega_g t)$, $\omega_g = 2\pi f_g$, and $L_1 = L_2 = L_b$. The output capacitor C_o is used to filter the output current ripple and to stabilize the output voltage. If C_o is large enough, V_o can be seen as a constant value.

The EMI is used to filter the input current ripple. The rectifier bridge converts $v_{\rm ac}$ into a full-wave dc voltage. When Q_1 is turned-ON, $v_{\rm ac}$ is applied on L_1 and i_{L1} rises linearly. When Q_1 is turned-OFF, i_{L1} charges C_o and supplies power to $R_{\rm load}$.

B. Operation Modes of the IBC

The IBC has three operation modes, namely, the continuous conduction mode (CCM), the discontinuous conduction mode

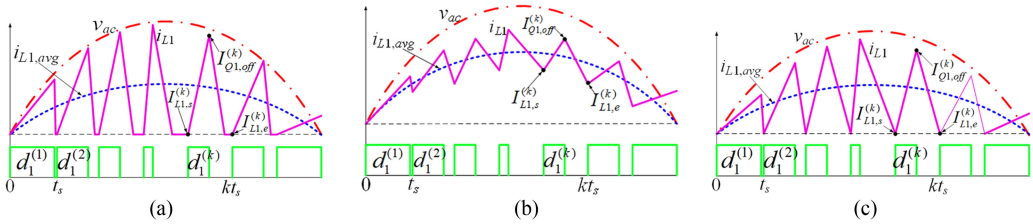


Fig. 2. Waveforms of S_1, i_{L1}, and $v_{\rm ac}$ in (a) DCM, (b) CCM, and (c) BCM.

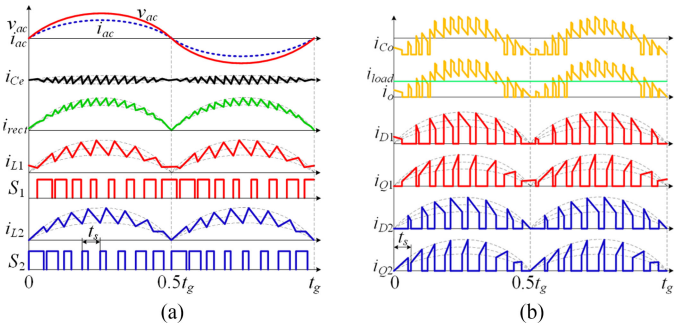


Fig. 3. Waveforms of (a) $v_{\rm ac}, i_{\rm ac}, i_{Ce}, i_{\rm rect}, i_{L1}, S_1, i_{L2}, S_2$, and (b) i_{Co}, $i_{\rm load}, i_o, i_{D1}, i_{Q1}, i_{D2}$, and i_{Q2} in the CCM for the IBC in a grid period.

(DCM), and the boundary conduction mode (BCM). In the DCM and BCM, i_{L1} is zero at the starting point of each switching period, as shown in Fig. 2(a) and (c). On this occasion, Q_1 is the ZCS turn-ON and has no turn-ON loss, and D_5 is the ZCS turn-OFF and has no turn-OFF loss. Therefore, the switching loss in the DCM and BCM is much lower than that in the CCM, and the conduction loss in the DCM and BCM is much higher. However, the current ripple in the DCM and BCM is much larger than in the CCM; the DCM and BCM, therefore, need larger EMI filters.

Irrespective of the mode in which the IBC operates, the conduction loss generally dominates the total loss. Therefore, the efficiency in the CCM is generally higher than in the DCM and BCM. Moreover, the current ripple in the CCM is also much smaller, which can reduce the volume of the EMI filter and the output capacitor.

III. Calculation of Current

Before calculating the loss and efficiency, rms currents and switching currents of the IBC must be preobtained. Assuming that the EMI filter can well smooth $i_{\rm ac}$, and $i_{\rm ac}$ is a pure sinusoidal wave, then all waveforms can be obtained, as shown in Fig. 3.

$i_{\rm ac}$ can be expressed as follows:

$$i_{\rm ac}(t) = \frac{\sqrt{2}P_o}{V_{\rm ac}} \sin(\omega_g t) \tag{1}$$

and $d_1^{(k)}$ is given by

$$d_1^{(k)} = \frac{V_o - v_{\rm ac}(kt_s)}{V_o}. \tag{2}$$

In half a grid period, i_{L1} is given by

$$i_{L1}(t) = \sum_{k=1}^{0.5t_g/t_s} i_{L1,k}(t) \tag{3}$$

$$i_{L1,k}(t) = \begin{cases} I_{L1,s}^{(k)} = I_{L1,e}^{(k-1)}, & t = (k-1)t_s \\ I_{L1,s}^{(k)} + \frac{v_{\rm ac}(t)}{L_b}[t-(k-1)t_s], & (k-1)t_s < t \le (k-1+d_1^{(k)})t_s \\ I_{L1,s}^{(k)} + \frac{v_{\rm ac}(t)}{L_b} d_1^{(k)} t_s & (k-1+d_1^{(k)})t_s < t < kt_s \\ \quad -\frac{V_o}{L_b}[t-(k-1+d_1^{(k)})t_s], & \\ I_{L1,e}^{(k)} = I_{L1,s}^{(k+1)}, & t = kt_s \end{cases} \tag{4}$$

and $I_{Q1,\rm off}^{(k)}$ and $I_{Q1,\rm on}^{(k)}$ are given by

$$\begin{aligned} I_{Q1,\rm off}^{(k)} &= i_{L1}(t)\delta\left[(k-1+d_1^{(k)})t_s\right] \\ &= i_{L1}(t)\delta\left[\left(k-1+\frac{V_o-\sqrt{2}V_{\rm ac}\sin(kt_s)}{V_o}\right)t_s\right] \end{aligned} \tag{5}$$

$$I_{Q1,\rm on}^{(k)} = i_{L1}(t)\delta(kt_s) \tag{6}$$

and i_{Q1} and i_{D5} can be expressed as follows:

$$i_{Q1}(t) = \sum_{k=1}^{0.5t_g/t_s} i_{L1}(t)\left\{u[(k-1)t_s - u[t-(k-1+d_1^{(k)})t_s]\right\} \tag{7}$$

$$i_{D5}(t) = \sum_{k=1}^{0.5t_g/t_s} i_{L1}(t)\left\{u\left[t-\left(k-1+d_1^{(k)}\right)t_s\right] - u(t-kt_s).\right\} \tag{8}$$

There is a difference of 180° between the initial phases of S_1 and S_2. Therefore, i_{L2}, i_{Q2}, and i_{D6} can be expressed as follows:

$$\begin{cases} i_{L2}(t) = i_{L1}(t-0.5t_s) \\ i_{Q2}(t) = i_{Q1}(t-0.5t_s) \\ i_{D6}(t) = i_{D1}(t-0.5t_s). \end{cases} \tag{9}$$

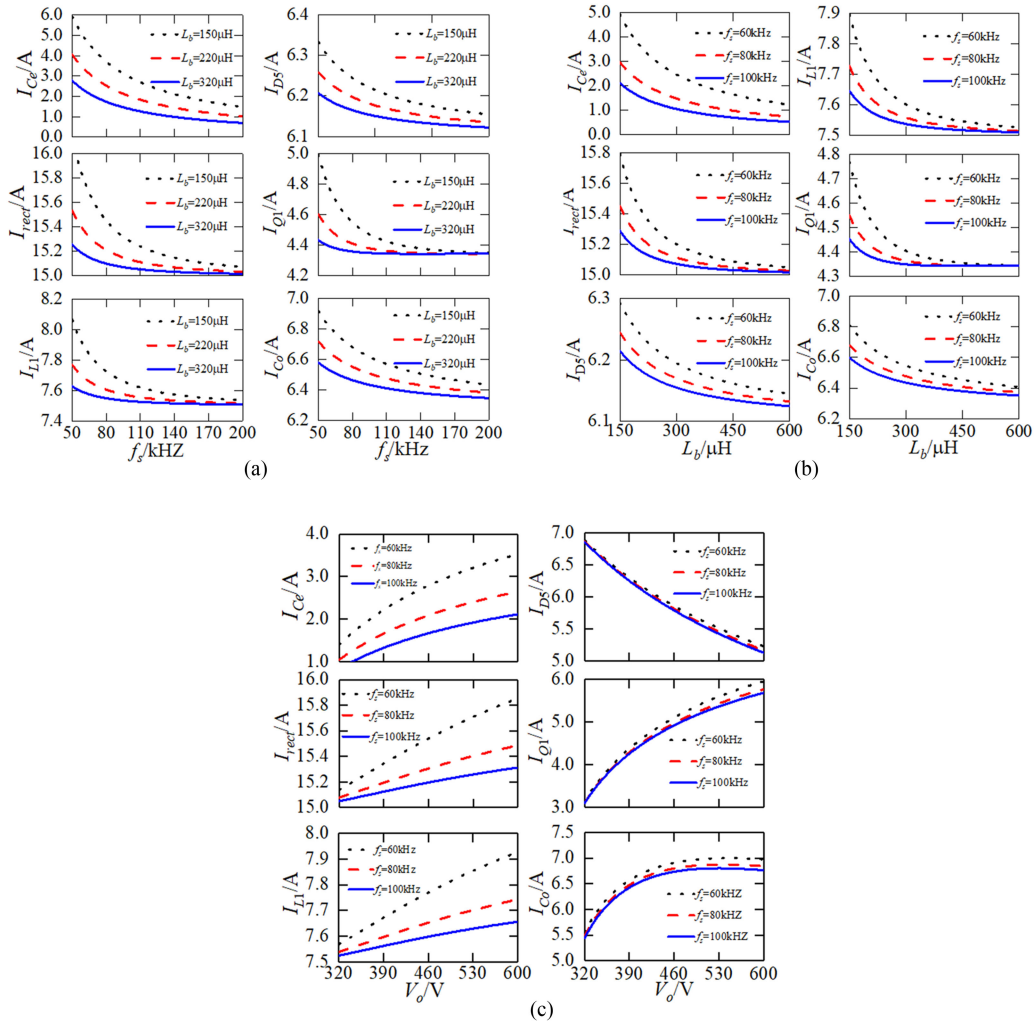


Fig. 4. Curves of (a) I_{Ce} versus f_s, I_{rect} versus f_s, I_{L1} versus f_s, I_{D5} versus f_s, I_{Q1} versus f_s, and I_{Co} versus f_s for $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW at $L_b = 150$, 220, and 320 μH; (b) I_{Ce} versus L_b, I_{rect} versus L_b, I_{D5} versus L_b, I_{L1} versus L_b, I_{Q1} versus L_b, and I_{Co} versus L_b for $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW at $f_s = 60$, 80, and 100 kHz; and (c) I_{Ce} versus V_o, I_{rect} versus V_o, I_{L1} versus V_o, I_{D5} versus V_o, I_{Q1} versus V_o, and I_{co} versus V_o for $V_{\text{ac}} = 220$ V, $L_b = 220\,\mu$H, and $P_o = 3.3$ kW at $f_s = 60$, 80, and 100 kHz.

$i_{\text{rect}}, i_{Ce}, i_{\text{load}}$, and i_{Co} are given by

$$i_{\text{rect}}(t) = |i_{L1}(t) + i_{L2}(t)| \tag{10}$$

$$i_{Ce}(t) = |i_{\text{rect}}(t)| - |i_{\text{ac}}(t)| \tag{11}$$

$$i_{\text{load}} = \frac{P_o}{V_o} \tag{12}$$

$$i_{Co}(t) = i_{D1}(t) + i_{D2}(t) - i_{\text{load}}. \tag{13}$$

$I_{Ce}, I_{L1}, I_{L2}, I_{Q1}, I_{Q2}, I_{D1}, I_{D2}$, and I_{Co} can be obtained by substituting (3), (7)–(11), and (13) into the following:

$$I_{\text{rms}} = \sqrt{\frac{1}{0.5t_g}\int_0^{0.5t_g} i(t)^2\,dt}. \tag{14}$$

$I_{Co,\text{lf}}$ and $I_{Co,\text{hf}}$ can be calculated as follows [21]:

$$I_{Co,\text{lf}} = \frac{P_o}{\sqrt{2}V_o} \tag{15}$$

$$I_{Co,\text{hf}} = \sqrt{I_{Co}^2 - I_{Co,lf}^2}. \tag{16}$$

Based on the aforementioned calculations, all rms currents can be obtained, which can be used to evaluate the conduction loss. Fig. 4 shows the curves of the relationship between rms currents and f_s, L_b, and V_o. As f_s and L_b increase, the current ripple of the IBC decreases. Since rms currents decrease with the decrease of the current ripple, all rms currents decrease with f_s and L_b.

$I_{Ce}, I_{\text{rect}}, I_{Q1}, I_{L1}$, and I_{Co} decrease as V_o increases. However, as V_o increases, I_{D5} decreases. On the one hand, the increase of V_o can increase the average duty cycles of Q_1 and Q_2. A large average duty cycle will increase the current ripple, and a large current ripple results in large rms currents. Therefore, $I_{Ce}, I_{\text{rect}}, I_{L1}, I_{Q1}$, and I_{Co} increase with V_o. The trend of I_{D5}

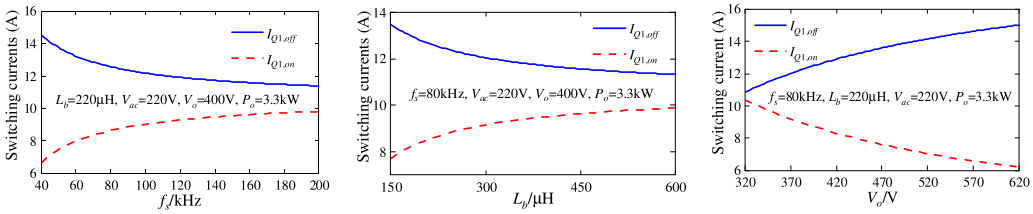


Fig. 5. Curves of (a) $I_{Q1,\text{off}}$ versus f_s and $I_{Q1,\text{on}}$ versus f_s for $L_b = 220\,\mu$H, $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW; (b) $I_{Q1,\text{off}}$ versus L_b and $I_{Q1,\text{on}}$ versus L_b for $f_s = 80$ kHz, $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW; and (c) $I_{Q1,\text{off}}$ versus V_o and $I_{Q1,\text{on}}$ versus V_o for $f_s = 80$ kHz, $L_b = 220\,\mu$H, $V_{\text{ac}} = 220$ V, and $P_o = 3.3$ kW.

TABLE I
AFFECTING PROCESSES OF THREE PARAMETERS ON THE RMS VALUES OF CURRENTS

Parameters	Average duty cycle	Current ripple	I_{Ce}	I_{rect}	I_{L1}	I_{Q1}	I_{D5}	I_{Co}
f_s↑	—	↓	↓	↓	↓	↓	↓	↓
L_b↑	—	↓	↓	↓	↓	↓	↓	↓
V_o↑	↑	↑	↑	↑	↑	↑	↑	
	P_o=2V_oI_{D5} is constant		—	—	—	—	—	↓

versus V_o can be explained from two perspectives. On the one hand, P_o is constant and equal to $2\,V_o \times I_{D5}$. It is no doubt that I_{D5} decreases as V_o increases. The low-frequency component of I_{D5} is determined by V_o. This is the main reason behind I_{D5} versus V_o trend. On the other hand, the increase of V_o increases the average duty cycle of Q_1 and, then, increases the current ripple of i_{L1}. The current ripple of i_{D5} has the same trend as the current ripple of i_{L1}. Then, the current ripple of i_{D5} increases with V_o. This means that the high-frequency component of i_{D5} increases with V_o. However, the high-frequency components of i_{D5} have a smaller effect on I_{D5} compared with the effect of the low-frequency component on I_{D5}. Therefore, I_{D5} decreases with V_o.

To demonstrate how the three parameters affect rms currents, Table I presents the affecting processes of f_s, L_b, and V_o on the I_{Ce}, I_{rect}, I_{L1}, I_{Q1}, I_{D5}, and I_{Co}.

When v_{ac} reaches the peak value, the current ripple and switching currents are maximum, which can be used to evaluate the switching loss. Fig. 5 shows the curves of relationships between switching currents (when $v_{\text{ac}} = \sqrt{2}\,V_{\text{ac}}$) and the three parameters. $I_{Q1,\text{off}}$ decreases with f_s, and $I_{Q1,\text{on}}$ increases with f_s. Since the switching loss is approximately proportional to the product of the switching frequency and switching currents, the switching loss increases with f_s. $I_{Q1,\text{off}}$ decreases with L_b, and $I_{Q1,\text{on}}$ increases with L_b, which mean that the turn-ON loss increases with L_b and the turn-OFF loss decreases with L_b. If L_b is designed to be too large, the turn-ON loss will be equal to the turn-OFF loss, and they will be constant. In this case, further increasing L_b will not help to reduce the switching loss. On the contrary, too large L_b will increase the volume of boost inductors. Therefore, L_b should be well designed. $I_{Q1,\text{off}}$ increases with V_o, and $I_{Q1,\text{on}}$ decreases with V_o, which mean that the turn-OFF loss increases with V_o and the turn-ON loss decreases with V_o.

All rms currents and switching currents are the functions of f_s, L_b, and V_o. As shown in Fig. 4, all rms currents change with f_s, L_b, and V_o. Since the conduction loss has a direct relationship with rms currents, the conduction loss is indirectly determined by f_s, L_b, and V_o. As shown in Fig. 5, switching currents also change with the variations of f_s, L_b, and V_o. Since switching currents have a direct effect on the switching loss, the switching loss is also indirectly determined by f_s, L_b, and V_o. Therefore, f_s, L_b, and V_o affect the total loss and can be used to optimize the efficiency of the IBC PFC.

IV. CALCULATIONS OF LOSS AND EFFICIENCY

In this paper, high-frequency switches are MOSFETs. The total loss of the IBC consists of the EMI loss, the rectifier bridge loss, the boost inductor loss, the MOSFET loss, freewheeling diodes' loss, the output capacitor loss, and other losses. The EMI loss is generated by ESRs of the EMI inductor and the EMI capacitor. Since f_g is low, the switching loss of the rectifier bridge can be ignored. The boost inductor loss includes the copper loss and ferrite loss. The MOSFET loss consists of the conduction loss and the switching loss. The switching loss includes the turn-ON loss and the turn-OFF loss. Freewheeling diodes' loss consists of the conduction loss and the reverse recovery loss. The output capacitor loss is generated by $R_{Co,\text{lf}}$ and $R_{Co,\text{hf}}$. Other losses are generated by the drive circuit, the ESRs of the PCB, the surface mount technology (SMT) components, and so on.

The ESRs of the capacitor and the inductor can be calculated as follows:

$$R_c(f) = \frac{\tan\delta_c}{2\pi f C} \tag{17}$$

$$R_l(L) = \frac{[1+\alpha_{20}(20+\Delta T_l)]\rho_{20} l_{\text{mlt}} N_l}{S_w} = \frac{[1+\alpha_{20}(20+\Delta T_l)]\rho_{20} l_{\text{mlt}}}{S_w}\sqrt{\frac{L}{A_l}} \tag{18}$$

where C and L are the capacitance and inductance, respectively, f and $\tan\delta_c$ are the operation frequency and the loss angle of the capacitor, respectively, $R_c(f)$ and $R_l(L)$ are ESRs of the capacitor and the inductor, respectively, N_l is the turn number, S_w is the cross-sectional area, l_{mlt} is the mean length of the magnetic loop, and A_l is the inductance coefficient.

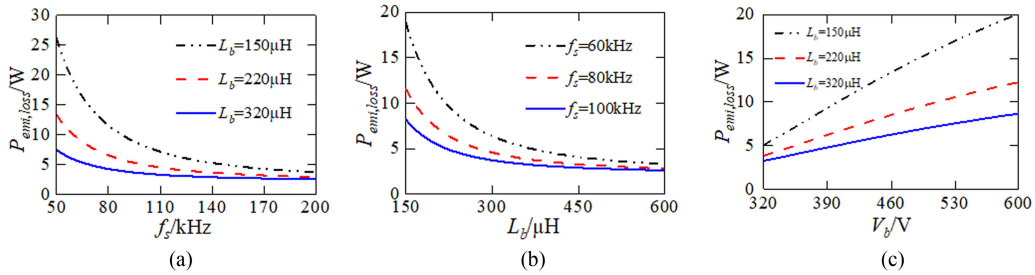


Fig. 6. Curves of the relationship between EMI loss $P_{\text{loss, emi}}$ and (a) f_s for $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW at $L_b = 150$, 220, and 320 μH; (b) L_b for $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW at $f_s = 60$, 80, and 100 kHz; and (c) V_o for $V_{\text{ac}} = 220$ V, $f_s = 80$ kHz, and $P_o = 3.3$ kW at $L_b = 150$, 220, and 320 μH.

TABLE II
MAIN COMPONENTS OF THE IBC

Components	Type
EMI inductor	2×H25/15/13 (AWG #11 wire)
EMI capacitor	1×C4BTHBX4500Z
Rectifier bridge	2×GBU2508
Boost inductor	2×PQ35/35 core (material is DMR44)
MOSFETs	2×IPP65R150CFD
Freewheeling diodes	2×STTH12T06DI
Output capacitors	4×EKMS451VSN470

The main components of the IBC PFC are listed in Table II. Based on the selected components, the total loss and efficiency can be calculated by the proposed method.

A. Loss of EMI

$P_{\text{emi, loss}}(f_s, L_b, V_o)$ can be calculated as follows:

$$P_{\text{emi,loss}}(f_s, L_e) = P_{Ce,\text{loss}}(L_e) + P_{Le,\text{loss}}(f_s) = R_{Le}(L_e)I_{\text{ac}}^2 + R_{Ce}(f_s)I_{Ce}^2. \quad (19)$$

Fig. 6 shows the curves of $P_{\text{emi, loss}}$ versus f_s, $P_{\text{emi, loss}}$ versus L_b, and $P_{\text{emi, loss}}$ versus V_o. As shown in Fig. 6(a) and (b), $P_{\text{emi, loss}}$ decreases as f_s and L_b increase. $P_{\text{emi, loss}}$ increases with V_o. To reduce the EMI loss, f_s and L_b should be as large as possible, and V_o should be as low as possible.

B. Loss of the Rectifier Bridge

$P_{\text{bri, loss}}(f_s, L_b, V_o)$ can be calculated as follows:

$$P_{\text{bri,loss}}(f_s, L_b, V_o) = V_{F,\text{bri}} I_{\text{rect}}(f_s, L_b, V_o) + R_{\text{bri}} I_{\text{rect}}^2(f_s, L_b, V_o). \quad (20)$$

In this paper, the GBU2508 rectifier bridge is selected. Its $V_{F,\text{bri}}$ has a direct relationship with I_{rect} and T_j, as shown in Fig. 7. $V_{F,\text{bri}}$ increases with I_{rect} and decreases with T_j.

Fig. 8 shows $P_{\text{bri, loss}}$ curves. A large f_s and L_b bring a small current ripple to i_{rect}, and the small current ripple of i_{rect} brings a small I_{rect}. Therefore, $P_{\text{bri, loss}}$ decreases with f_s and L_b, as shown in Fig. 8(a) and (b). On the contrary, high V_o leads to a large average duty cycle and current ripple and results in a large I_{rect} and large conduction loss. More precisely, as shown in Fig. 8(c), $P_{\text{bri, loss}}$ increases with V_o.

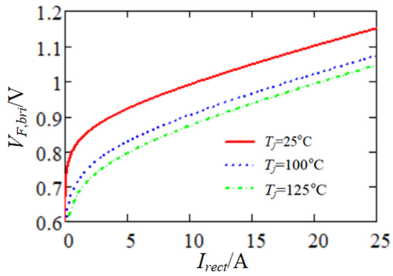


Fig. 7. Curves of the relationship between forward voltage-drop $V_{F,\text{bri}}$ and rms current I_{rect} of GBU2508 rectifier bridge at the junction temperature T_j = 25, 100, and 125 °C.

C. Loss of Boost Inductors

$P_{L,\text{loss}}(f_s, L_b, V_o)$ can be calculated as follows [22]:

$$\begin{cases} P_{L,\text{loss}}(f_s, L_b, V_o) = P_{L,\text{Fe}}(f_s, L_b, V_o) + P_{L,\text{Cu}}(f_s, L_b, V_o) \\ P_{L,\text{Fe}}(f_s, L_b, V_o) = \\ \quad 2K_L V_L f_s^{\alpha_L - 1} f_g \sum_{k=1}^{t_s/t_g} \left[B_{L,\max}^{(k)}(f_s, L_b, V_o) \right]^{\beta_L} \\ P_{L,\text{Cu}}(f_s, L_b, V_o) = P_{L,\text{Cu,dc}}(f_s, L_b, V_o) \\ \quad + P_{L,\text{Cu,dc}}(f_s, L_b, V_o) \\ P_{L,\text{Cu,dc}}(f_s, L_b, V_o) = 2R_L(L_b) I_{L,\text{dc}}^2(f_s, L_b, V_o) \\ P_{L,\text{Cu,ac}}(f_s, L_b, V_o) = 2R_{L,\text{ac}}(f_s, L_b) I_{L,\text{ac}}^2(f_s, L_b, V_o) \\ I_{L,\text{ac}}(f_s, L_b, V_o) = \\ \sqrt{\frac{t_s}{2t_g} \sum_{k=1}^{2t_g/t_s} \left(\frac{\sqrt{2}V_{\text{ac}} \sin(2\pi f_g k t_s)}{2\sqrt{3} L_b f_s} \frac{V_o - \sqrt{2}V_{\text{ac}} \sin(2\pi f_g k t_s)}{V_o} \right)^2} \end{cases} \quad (21)$$

$$B_{L,\max}{}^{(k)}(f_s, L_b, V_o) = \frac{N_L \mu_0 u_{L,\text{eff}} i_{L1,\text{peak}}{}^{(k)}(f_s, L_b, V_o)}{l_{L,\text{mlt}}} = \frac{\mu_0 u_{L,\text{eff}}}{l_{L,\text{mlt}}} \sqrt{\frac{L_b}{A_{L,l}}} \left[i_{L1,\text{avg}}{}^{(k)} + \Delta i_{L1}{}^{(k)} \right] = \frac{\mu_0 u_{L,\text{eff}}}{l_{L,\text{mlt}}} \sqrt{\frac{L_b}{A_{L,l}}} \left[\frac{\sqrt{2}P_o}{2V_{\text{ac}}} \sin(2\pi f_g k t_s) + \frac{t_s}{2} \frac{\sqrt{2}V_{\text{ac}} \sin(2\pi f_g k t_s)}{L_b} \times \frac{V_o - \sqrt{2}V_{\text{ac}} \sin(2\pi f_g k t_s)}{V_o} \right] \quad (22)$$

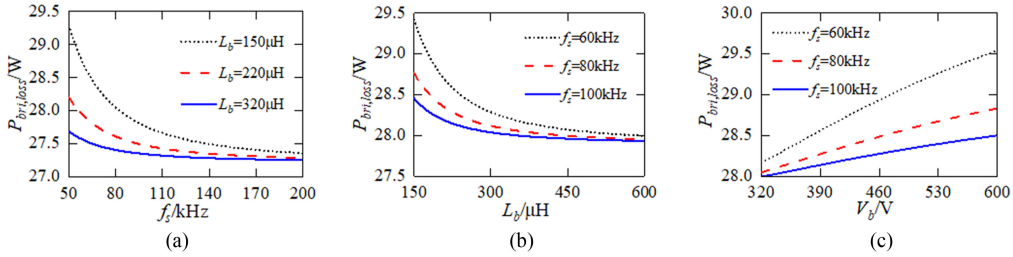


Fig. 8. Curves of the relationship between the rectifier bridge loss $P_{\text{loss, emi}}$ and (a) f_s for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $L_b = 150$, 220, and 320 μH; (b) L_b for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz; and (c) V_o for $V_{\text{ac}} = 220\,\text{V}$, $L_b = 220\,\mu\text{H}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz.

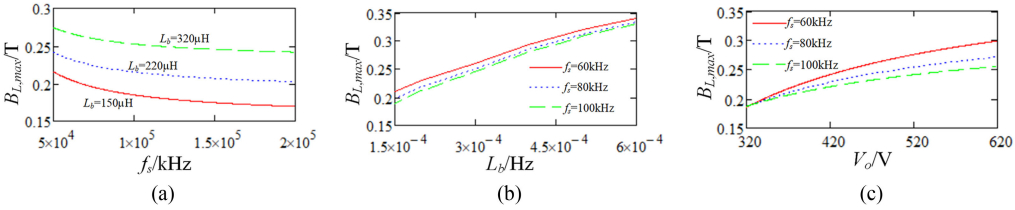


Fig. 9. Curves of the relationship between the maximum magnetic flux density $B_{L,\max}$ at $t = t_g$ and (a) f_s for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $L_b = 150$, 220, and 320 μH; (b) L_b for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz; and (c) V_o for $V_{\text{ac}} = 220\,\text{V}, P_o = 3.3\,\text{kW}$, and $L_b = 220\,\mu\text{H}$ at $f_s = 60$, 80, and 100 kHz.

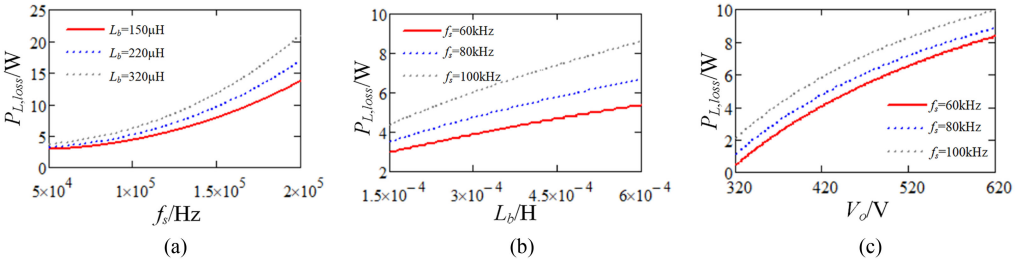


Fig. 10. Curves of the relationship between the boost inductor loss $P_{L,\text{loss}}$ and (a) f_s for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $L_b = 150$, 220, and 320 μH; (b) L_b for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz; and (c) V_o for $V_{\text{ac}} = 220\,\text{V}, P_o = 3.3\,\text{kW}$, and $L_b = 220\ \mu\text{H}$ at $f_s = 60$, 80, and 100 kHz.

$$\begin{cases} R_{L,\text{ac}}(f_s, L_b) = R_{L,\text{dc}}(L_b)\left[X\frac{\sinh(2X)+\sin(2X)}{\cosh(2X)-\cos(2X)} \right. \\ \qquad\qquad \left. + 2X\frac{m^2-1}{3}\frac{\sinh(X)-\sin(X)}{\cosh(X)+\cos(X)}\right] \\ R_{L,\text{dc}}(L_b) = r_{L,\text{per}}\sqrt{\frac{L_b}{A_{L,l}}} \\ X = \frac{D}{\delta_{\text{skin}}} \\ \delta_{\text{skin}} = \frac{1}{\sqrt{\pi\sigma\mu_0 f_s}}. \end{cases} \tag{23}$$

At $t = 0.25t_g$, $B_{L,\max}$ is maximum. Fig. 9 shows $B_{L,\max}$ curves at $t = 0.25t_g$. First, a large f_s brings a small current ripple and a small I_{pk} to i_{L1} because $B_{L,\max}$ is proportional to $N_L \times I_{pk}$; then, $B_{L,\max}$ decreases with f_s, as shown in Fig. 9(a). On the contrary, a large L_b leads to a large turn number N_L and $N_L \times I_{pk}$; then, $B_{L,\max}$ increases with L_b, as shown in Fig. 9(b). A high V_o leads to a large current ripple and I_{pk}, which also results in a large $N_L \times I_{pk}$; therefore, $B_{L,\max}$ increases with V_o, as shown in Fig. 9(c).

Fig. 10 shows $P_{L,\text{loss}}$ curves. $P_{L,\text{loss}}$ increases with f_s, L_b, and V_o. First, $P_{L,\text{Fe}}$ has an exponential relationship with f_s and quickly increases with f_s. If f_s is within a range of large values, $P_{L,\text{Fe}}$ is much larger than $P_{L,\text{Cu}}$. Therefore, for the boost inductors, $P_{L,\text{loss}}$ increases with f_s, as shown in Fig. 10(a). Second, R_L is proportional to L_b. A large L_b results in a large R_L, and a large R_L results in a large $P_{L,\text{Cu}}$. Therefore, $P_{L,\text{loss}}$ increases approximately linearly with L_b, as shown in Fig. 10(b).

Moreover, a large V_o brings large average duty cycles and results in a large I_{L1}, as shown in Fig. 4(c), and a large I_{pk}; then, a large I_{L1} results in a large $P_{L,\text{Cu}}$, and a large I_{pk} results in a large $B_{L,\max}$ and a large $P_{L,\text{Fe}}$; therefore, $P_{L,\text{loss}}$ increases with V_o, as shown in Fig. 10(c).

D. Loss of MOSFET

$P_{\text{mos, loss}}(f_s, L_b, V_o)$ can be estimated as follows [23]–[26]:

$$\begin{aligned} P_{\text{mos,loss}}(f_s, L_b, V_o) &= P_{\text{mos,con}}(f_s, L_b, V_o) \\ &\quad + P_{\text{mos,swi}}(f_s, L_b, V_o) \\ &= 2R_{ds,\text{on}} I_{Q1}^2(f_s, L_b, V_o) + 2f_g V_o \\ &\quad \left[\frac{t_{\text{mos},r}}{2}\sum_{k=1}^{0.5t_g/t_s} I_{Q1,\text{off}}^{(k)}(f_s, L_b, V_o) \right. \\ &\quad \left. + \frac{t_{\text{mos},f}}{2}\sum_{k=1}^{0.5t_g/t_s} I_{Q1,\text{on}}^{(k)}(f_s, L_b, V_o)\right] \end{aligned} \tag{24}$$

$$R_{\text{ds,on}} = 0.063(a + bT_{\text{mos},j}) \tag{25}$$

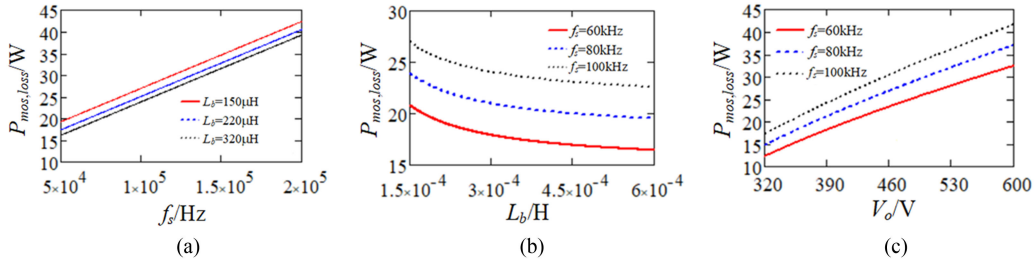


Fig. 11. Curves of the relationship between MOSFET loss $P_{\text{mos, loss}}$ and (a) f_s for $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW at $L_b = 150$, 220, and 320 μH; (b) L_b for $V_{\text{ac}} = 220$ V, $V_o = 400$ V, and $P_o = 3.3$ kW at $f_s = 60$, 80, and 100 kHz; and (c) V_o for $V_{\text{ac}} = 220$ V, $P_o = 3.3$ kW, and $L_b = 220\,\mu$H at $f_s = 60$, 80, and 100 kHz.

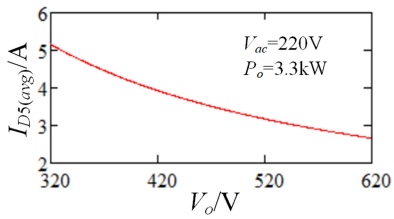


Fig. 12. Curves of $I_{D5(\text{avg})}$ versus V_o for $V_{\text{ac}} = 220$ V and $P_o = 3.3$ kW.

where $t_{\text{mos},f}$ and $t_{\text{mos},r}$ are 5.6 and 7.6 ns, respectively, and a and b are about 8×10^{-4} and 0.0242, respectively.

Fig. 11 shows MOSFET loss curves. First, a large f_s leads to a large $P_{\text{mos, swit}}$; if f_s is in a range of large values, $P_{\text{mos, swit}}$ will dominate $P_{\text{mos, loss}}$; then, $P_{\text{mos, loss}}$ increases with f_s, as shown in Fig. 10(a). Second, on the one hand, a large L_b brings a small $I_{Q1,\text{off}}$ and $I_{Q2,\text{off}}$ and a small switching loss. On the other hand, a large L_b also brings a small current ripple, small rms currents, and a small conduction loss. Therefore, $P_{\text{mos, loss}}$ decreases with L_b, as shown in Fig. 10(b). Finally, a high V_o leads to large average duty cycles and a large current ripple and results in large $I_{Q1}, I_{Q2}, I_{Q1,\text{off}}$, and $I_{Q2,\text{off}}$ and, then, in large $P_{\text{mos, con}}$ and $P_{\text{mos, swit}}$. Therefore, $P_{\text{mos, loss}}$ increases with V_o, as shown in Fig. 10(c).

E. Loss of Freewheeling Diodes

According to the datasheet of STTH12T06DI diode, $P_{\text{dio, con}}(f_s, L_b, V_o)$ should be estimated as follows:

$$P_{\text{dio,con}}(f_s, L_b, V_o) = 2 \times [1.75 I_{D5(\text{avg})}(V_o) + 0.0667 I_{D5}^2(f_s, L_b, V_o) \tag{26}$$

$$I_{D5(\text{avg})}(V_o) = \frac{1}{0.5t_g} \int_0^{0.5t_g} i_{L1,\text{avg}}(t)\,[1 - d(t)]\,dt. \tag{27}$$

$I_{D5(\text{avg})}$ is only determined by V_o, and $I_{D5(\text{avg})}$ decreases with V_o, as shown in Fig. 12.

Fig. 13 shows the curves of $P_{\text{dio, con}}$ versus f_s, $P_{\text{dio,con}}$ versus L_b, and $P_{\text{dio, con}}$ versus V_o. Since I_{D5} and I_{D6} decrease with f_s and L_b, $P_{\text{dio, con}}$ decreases with f_s and L_b, as shown in Fig. 13(a) and (b), and $P_{\text{dio, con}}$ decreases with V_o, as shown in Fig. 13(c).

$P_{\text{dio, rev}}$ is estimated as follows [22]:

$$P_{\text{dio,rev}}(f_s, V_o) = 2 \times Q_{\text{rr}} V_o f_s \tag{28}$$

where Q_{rr} is 30 nC at 100 °C. Fig. 14 shows the curves of $P_{\text{dio, rev}}$ versus f_s and $P_{\text{dio, rev}}$ versus V_o. $P_{\text{dio, rev}}$ linearly increases with f_s and V_o.

$P_{\text{dio, loss}}$ can be calculated as follows:

$$P_{\text{dio,loss}}(f_s, L_b, V_o) = P_{\text{dio,con}}(f_s, L_b, V_o) + P_{\text{dio,rev}}(f_s, L_b, V_o). \tag{29}$$

Fig. 15 shows the curves of $P_{\text{dio, loss}}$ versus f_s, $P_{\text{dio, loss}}$ versus L_b, and $P_{\text{dio, loss}}$ versus V_o. If L_b is large enough, $P_{\text{dio, loss}}$ increases with f_s due to a large reverse recovery loss. If L_b is too small, there is an optimized switching frequency point, as shown in Fig. 15(a), where $dP_{\text{dio, loss}}/df_s = 0$. Since increasing L_b can decrease the current ripple, I_{D5} and I_{D6} decrease with L_b; thus $P_{\text{dio, loss}}$ decreases with L_b, as shown in Fig. 15(b). As for the trend of $P_{\text{dio, loss}}$ versus V_o, because P_o is constant and equal to $2 \times I_{D5(\text{avg})} V_o$, I_{D5} almost linearly decreases with V_o, and $P_{\text{dio, loss}}$ is dominated by the product of $V_{F,\text{dio}}$ and $I_{D5(\text{avg})}$. Therefore, $P_{\text{dio, loss}}$ decreases with V_o.

F. Loss of Output Capacitors

$P_{Co,\text{loss}}$ can be obtained by [23]

$$P_{Co,\text{loss}}(f_s, L_b, V_o) = R_{Co,\text{hf}}(f_s) I_{Co,\text{hf}}^2(f_s, L_b, V_o) + R_{Co,\text{lf}} I_{Co,\text{lf}}^2. \tag{30}$$

EKMS451VSN470 aluminum electrolytic capacitors are used, and tan δ_{Co} is 0.15 and $R_{Co,\text{lf}}$ is about 0.063 Ω.

Fig. 16 shows the curves of $P_{Co,\text{loss}}$ versus f_s, $P_{Co,\text{loss}}$ versus L_b, and $P_{Co,\text{loss}}$ versus V_o. First, because $R_{Co,\text{lf}}$ and $R_{Co,\text{hf}}$ are inversely proportional to the operation frequency of the capacitor, $R_{Co,\text{hf}}$ is much smaller than $R_{Co,\text{lf}}$. Therefore, the loss generated by $R_{Co,\text{lf}}$ dominates $P_{Co,\text{loss}}$. In addition, the variations of f_s and L_b have no effect on the low-frequency components of i_{Co}; then, $P_{Co,\text{loss}}$ has nothing to do with f_s and L_b, as shown in Fig. 16(a) and (b). On the contrary, the variations of V_o have a direct effect on the low-frequency component of i_{Co}, and $I_{Co,\text{lf}}$ decreases with V_o; then, $P_{Co,\text{loss}}$ decreases with V_o, as shown in Fig. 16(c).

G. Other Losses

The other losses include the power loss generated by the driving circuit, the ESR of the PCB, and so on. Compared with the driving loss, the loss generated by the PCB ESR can be

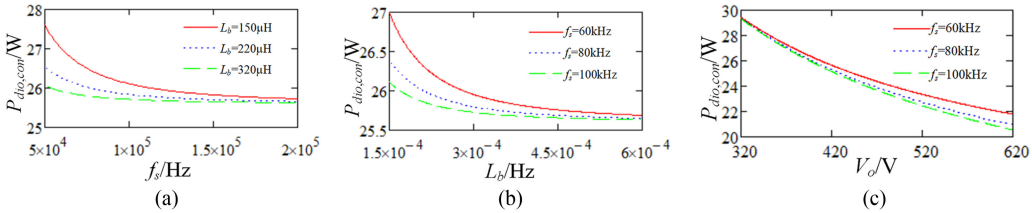


Fig. 13. Curves of (a) $P_{\text{dio, con}}$ versus f_s for $V_{\text{ac}} = 220\,\text{V}$, $V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $L_b = 150$, 220, and 320 μH; (b) $P_{\text{dio, con}}$ versus L_b for $V_{\text{ac}} = 20\,\text{V}$, $V_o = 400\text{V}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz; and (c) $P_{\text{dio, con}}$ versus V_o for $V_{\text{ac}} = 20\,\text{V}$, $L_b = 220\,\mu\text{H}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz.

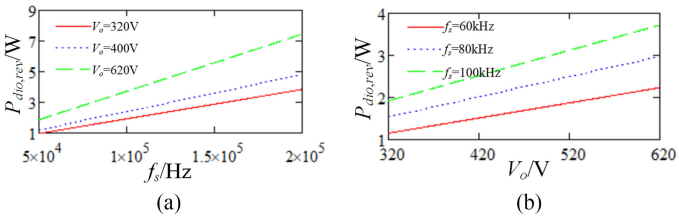


Fig. 14. Curves of (a) $P_{\text{dio, con}}$ versus f_s at $V_o = 320$, 400, and 620 V and (b) $P_{\text{dio, con}}$ versus V_o at $f_s = 60$, 80, and 100 kHz.

ignored. $P_{\text{dri}}(f_s)$ is a function of f_s and can be calculated as follows [27]:

$$P_{\text{dri,loss}}(f_s) = 2Q_g V_{\text{dri}} f_s. \tag{31}$$

The IPP65R150CFD MOSFET is used. According to the datasheet, Q_g is 86 nC. If V_{dri} is too high, it leads to a large driving loss, and if it is too low, it results in slow switching speed and a large switching loss. To comprehensively consider the conduction loss and the switching loss, V_{dri} is designed as 12 V in this paper.

H. Total Loss and Efficiency

$P_{\text{tot, loss}}(f_s, L_b, V_o)$ and $\eta(f_s, L_b, V_o)$ of the IBC PFC are expressed as follows:

$$\begin{aligned} &P_{\text{tot,loss}}(f_s, L_b, V_o) \\ &\quad = P_{\text{emi,loss}}(f_s, L_b, V_o) + P_{\text{bri,loss}}(f_s, L_b, V_o) \\ &\qquad + P_{L,\text{loss}}(f_s, L_b, V_o) + P_{\text{mos,loss}}(f_s, L_b, V_o) \\ &\qquad + P_{\text{dio,loss}}(f_s, L_b, V_o) + P_{Co,\text{loss}}(f_s, L_b, V_o) \\ &\qquad + P_{\text{dri,loss}}(f_s, L_b, V_o) \end{aligned} \tag{32}$$

$$\eta(f_s, L_b, V_o) = \frac{P_o}{P_o + P_{\text{tot,loss}}(f_s, L_b, V_o)} \times 100\%. \tag{33}$$

Both $P_{\text{tot, loss}}(f_s, L_b, V_o)$ and $\eta(f_s, L_b, V_o)$ are the functions of f_s, L_b, and V_o. Therefore, $\eta(f_s, L_b, V_o)$ can be improved by optimizing f_s, L_b, and V_o without adding to the cost and complexity of software and hardware.

V. Optimal Design of the IBC

In the design process of the IBC, especially for PFC application, several factors should be considered, including the PF, maximum magnetic flux density of the magnetic core, current ripple, and efficiency. First, the required PF should be satisfied to well realize the PFC function. Second, the actual maximum magnetic flux density must be smaller than the saturation magnetic flux density. Otherwise, the magnetic cores have a saturation risk. Moreover, the current ripple should be controlled at a proper level to reduce the volume of the EMI and the output capacitor. Finally, the efficiency should be as high as possible to reduce the total loss and the volume of heatsink.

A. Power Factor

The PF of the IBC PFC can be estimated as follows [29]:

$$\text{PF}(V_o) = \frac{\sqrt{\frac{2}{\pi}} \int_0^{\pi} \frac{V_o \sin^2(\omega t)}{V_o - \sqrt{2}V_{\text{ac}}|\sin(\omega t)|} d\omega t}{\sqrt{\int_0^{\pi} \left(\frac{V_o|\sin(\omega t)|}{V_o - \sqrt{2}V_{\text{ac}}|\sin(\omega t)|}\right)^2 d\omega t}}. \tag{34}$$

Fig. 17 shows the curves of PF versus V_o. A high V_o results in a high PF. A high V_o also results in a large current ripple and low efficiency. Therefore, the design of V_o should simultaneously consider the requirements of efficiency and PF. In this paper, the required PF is set as 96% at $V_{\text{ac}} = 220\,\text{V}$, and V_o is designed as 400 V.

B. Maximum Magnetic Flux Density of Boost Inductors

Equation (22) shows that $B_{L,\max}$ is a function of f_s, L_b, and V_o. As mentioned previously, V_o has been determined as 400 V based on the required PF. In this case, V_o is concerned, $B_{L,\max}$ is the function of f_s and L_b only. Fig. 18 shows the surface map of $B_{L,\max}$.

$B_{L,\max}$ decreases with f_s because a large f_s can decrease the current ripple of i_{L1} and, then, reduce I_{pk} flowing through the windings of the boost inductors. The effect of L_b on $B_{L,\max}$ is complex. From (22), it can be seen that $B_{L,\max}$ has a linear relationship with $N_L \times I_{pk}$. On the other hand, if f_s is large enough, I_{pk} is almost a constant value, and N_L dominates $N_L \times I_{pk}$. On this occasion, $B_{L,\max}$ increases with N_L (or L_b). On the other hand, if f_s is in a range of small values, I_{pk} is large and will quickly decrease with L_b. In this case, I_{pk} dominates $N_L \times I_{pk}$, and increasing L_b can quickly reduce I_{pk}. Then, $B_{L,\max}$ decreases as L_b increases.

C. Current Ripple of Boost Inductors

The current ripple directly affects the volume and lifetime of the EMI and the output capacitor. A large f_s and L_b bring a

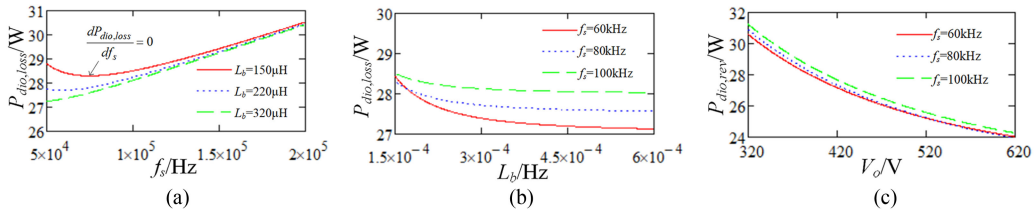


Fig. 15. Curves of (a) $P_{\text{dio, loss}}$ versus f_s for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $L_b = 150$, 220, and 320 μH; (b) $P_{\text{dio, loss}}$ versus L_b for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz; and (c) $P_{\text{dio, loss}}$ versus V_o for $V_{\text{ac}} = 220\,\text{V}, L_b = 220\,\mu\text{H}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz.

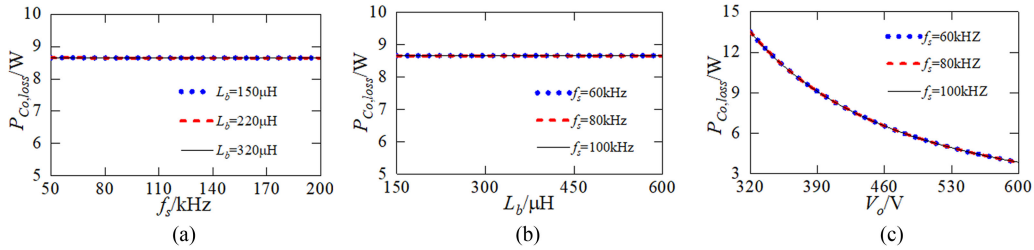


Fig. 16. Curves of (a) $P_{Co,\text{loss}}$ versus f_s for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $L_b = 150$, 220, and 320 μH; (b) $P_{Co,\text{loss}}$ versus L_b for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz; and (c) $P_{Co,\text{loss}}$ versus V_o for $V_{\text{ac}} = 220\,\text{V}, L_b = 220\,\mu\text{H}$, and $P_o = 3.3\,\text{kW}$ at $f_s = 60$, 80, and 100 kHz.

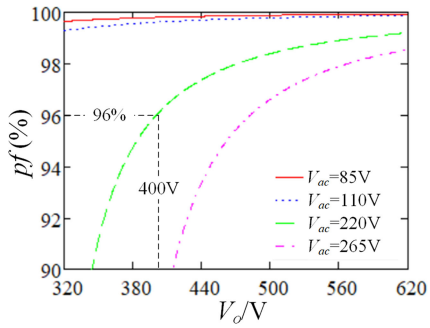


Fig. 17. PF versus V_o curves of the IBC PFC at $V_{\text{ac}} = 80$, 110, 220, and 265 V.

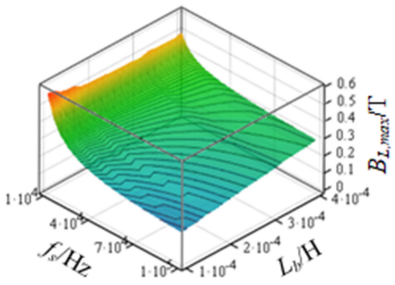


Fig. 18. Surface map of $B_{L,\max}(f_s, L_b)$ for $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$.

small current ripple. However, the window space of the magnetic core limits the maximum turn number and the maximum inductance of the boost inductor. If f_s is too large, $P_{\text{mos, swit}}$ quickly increases with f_s and dominates $P_{\text{mos, loss}}$. A very large value of $P_{\text{mos, loss}}$ resulting from a large f_s will break the heat limitation of MOSFETs. Therefore, the current ripple should be

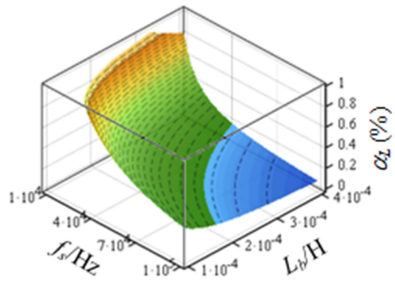


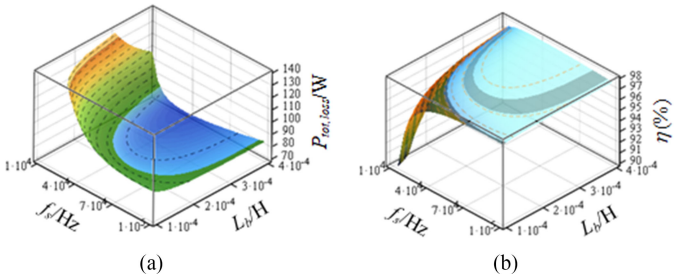
Fig. 19. Surface map of $\alpha_L(f_s, L_b)$ when $V_{\text{ac}} = 220\,\text{V}, V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$.

well considered. The current ripple ratio of i_{L1} is as follows:

$$\alpha_L(f_s, L_b) = \frac{\Delta I_{pk}(f_s, L_b)}{2I_{\max,\text{avg}}} = \frac{\frac{\sqrt{2}V_{\text{ac}}}{2f_s L_b}\frac{V_o - \sqrt{2}V_{\text{ac}}}{V_o}}{\frac{\sqrt{2}P_o}{2V_{\text{ac}}}}$$
$$= \frac{1}{P_o}\frac{V_{\text{ac}}^2}{f_s L_b}\frac{V_o - \sqrt{2}V_{\text{ac}}}{V_o}. \tag{35}$$

A small α_L brings small rms currents and small turn-OFF currents, which means that reducing α_L can decrease the conduction loss and switching loss. Moreover, the volume of passive components can be decreased if α_L is reduced. It seems that α_L should be as small as possible. Fig. 19 shows the surface map of $\alpha_L(f_s, L_b)$. α_L decreases with f_s and L_b. If the optimization target is only a small α_L, f_s and L_b should be as large as possible.

However, a small α_L sacrifices the power density because bulky boost inductors are needed. Therefore, α_L should be well designed by comprehensively considering the volume limitation of boost inductors and the requirement of efficiency. Comprehensively considering the current stress, filter volume, and effi-



(a) (b)

Fig. 20. Surface maps of (a) $P_{\text{tot, loss}}(f_s, L_b)$ and (b) $\eta(f_s, L_b)$ for $V_{\text{ac}} = 220\,\text{V}$, $V_o = 400\,\text{V}$, and $P_o = 3.3\,\text{kW}$.

ciency, $\alpha_L = 0.3$ is acceptable for many industrial applications [28].

D. Efficiency of the IBC

On the one hand, $\eta(f_s, L_b)$ depends on the performance of components. High performance brings high $\eta(f_s, L_b)$. Meanwhile, high performance leads to high hardware cost, which is not practical for industrial applications. On the other hand, from (32), $\eta(f_s, L_b)$ is a function of f_s, L_b, and V_o; then, $\eta(f_s, L_b)$ can be improved by optimizing f_s and L_b without increasing the hardware cost. Fig. 20 shows the surface maps of $P_{\text{tot, loss}}(f_s, L_b)$ and $\eta(f_s, L_b)$. Both $P_{\text{tot, loss}}(f_s, L_b)$ and $\eta(f_s, L_b)$ have nonlinear relationships with f_s and L_b.

In this paper, the allowed maximum α_L is set as 0.3. The saturation magnetic flux density of magnetic cores is 0.4 T at 100 °C. To decrease ferrite loss, therefore, the allowed maximum $B_{L,\max}$ is set as 0.3 T. The required minimum efficiency is set as 97.6%. To simultaneously meet the requirements of efficiency, maximum magnetic flux density, and current ripple ratio, the final design point of (f_s, L_b) must be in the target region, as shown in Fig. 21(d). There are four boundary lines around the target region. The best design point is at the center of the target region, where three requirements can be well compromised. However, in actual applications, some conditions make the best design point away from the center point. For example, the switching speed brings an upper limit to f_s. Additionally, the volume of the selected magnetic cores brings a lower limit to f_s. The window space and turn number limit the maximum inductance of boost inductors, which brings an upper limit to L_b. Therefore, the design of (f_s, L_b) should consider these limits.

In practical applications, the selection of (f_s, L_b) should follow the following rules.

1) If a condition is allowed, then (f_s, L_b) should be at the center of the target region to well compromise the requirement of efficiency, magnetic flux density, and current ripple.
2) If the efficiency requirement is first satisfied, then (f_s, L_b) should simultaneously be near the boundary lines I, II, and the boundary point ①, or simultaneously near the boundary lines I, IV, and the boundary point ④.
3) If the requirement of the current ripple needs to be first satisfied, then (f_s, L_b) should simultaneously be near the boundary lines II, III, and the boundary point ②.
4) If a low magnetic flux density is first needed, then (f_s, L_b) should simultaneously be near the boundary lines III, IV, and the boundary point ③.

The maximum inductance of magnetic cores is given by

$$L_b \le L_{b,\max} = \frac{\mu_0 A_e}{l_g}\left(\frac{4A_w K_u}{\pi d_{\text{litz}}^2 S_{\text{strand}}}\right)^2 \tag{36}$$

where $L_{b,\max}$ is the upper limit of L_b, A_e and A_w are the effective sectional area and window space area, respectively, d_{litz} is the diameter of a single litz wire, and S_{strand} is the strand number of litz wires. In this paper, the expected K_u is 0.4. The conductor of boost inductors is $\phi 0.11\,\text{mm} \times 200$ (strands). l_g is set as 2.4 mm. PQ35/35 (DMR44) cores are selected. A_e and A_w are 196 and 220.6 mm^2, respectively. Therefore, $L_{b,\max} = 222\,\mu\text{H}$. To fully utilize the window space, L_b is designed as 220 μH.

The energy stored in the magnetic core is given by

$$E_L = \frac{1}{2}L_{\min} I_{pk}^2 = \frac{1}{2}L_{\min}\left[\frac{\sqrt{2}P_o}{2V_{\text{ac}}} + \frac{\sqrt{2}V_{\text{ac}}}{L_{\min}}\frac{1}{f_s}\frac{V_o - \sqrt{2}V_{\text{ac}}}{V_o}\right]^2. \tag{37}$$

The minimum required AP value is given by

$$\text{AP}_{\min} = \frac{2E_L}{B_{L,\max} J_c K_u} \tag{38}$$

where J_c is the current density of windings, and K_u is the utilization coefficient of the window space.

The relationship between the volume and $\text{AP}_{\min}$ of magnetic cores is given by

$$V_{L,\min} = k_c \text{AP}_{\min}^{0.75} \tag{39}$$

where $V_{L,\min}$ is the minimum required volume of magnetic cores and k_c is equal to 5.6.

Substituting (37) into (38) and, then, (38) into (39), the relationship between $V_{L,\min}$ and f_s can be obtained and expressed as follows:

$$V_{L,\min}(f_s) = \frac{\left(\sqrt{2}V_{\text{ac}}^2 V_o - 2V_{\text{ac}}^3 + 0.5\sqrt{2}L_{\min}P_o V_o f_s\right)^2}{B_{L,\max} J_c K_u L_{L,\min} V_{\text{ac}}^2 V_o^2 f_s^2}. \tag{40}$$

Fig. 22 shows the curves of $V_{L,\min}$ versus f_s. $V_{L,\min}$ decreases with f_s, which means that a high f_s brings a high power density to the boost inductors. For the concerned magnetic core, there is a lower limit of $f_{s,\min}$ that is determined by the volume, and the actual f_s should be larger than $f_{s,\min}$.

The total loss of MOSFETs limits the upper limit of f_s, which can be obtained from the thermal equation of a MOSFET, as follows:

$$P_{\text{mos,loss}} R_{\text{th,JC}} = T_{j,\text{mos}} - T_{\text{case,mos}} \tag{41}$$

where $R_{\text{th, JC}}$ is the junction–case thermal resistor, and $T_{j,\text{mos}}$ and $T_{\text{case, mos}}$ are the junction temperature and the case temperature, respectively. According to the datasheet of IPP65R105CFD

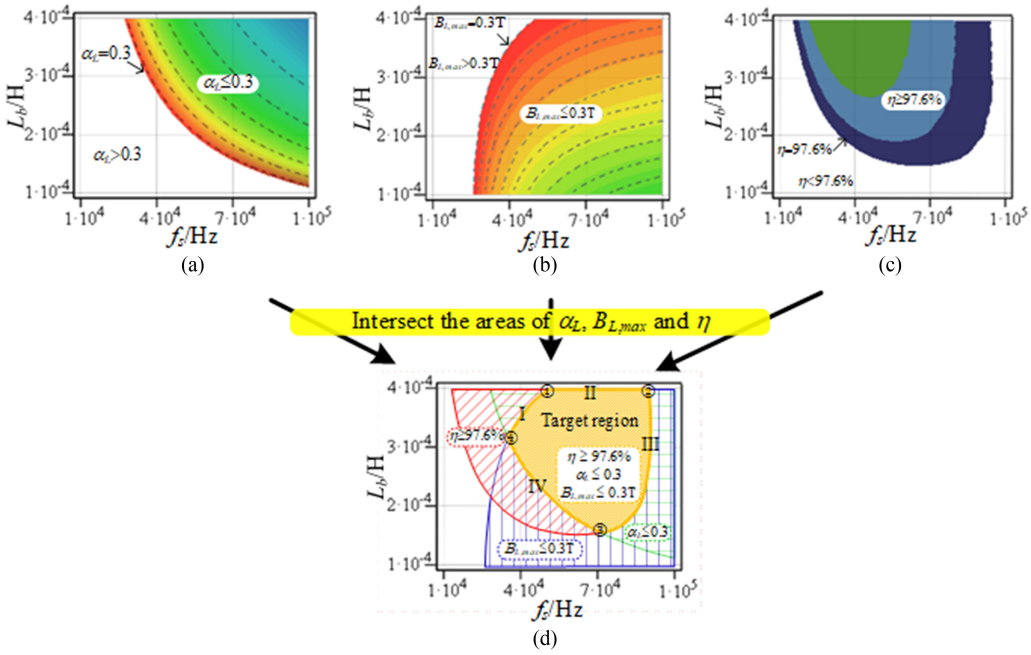


Fig. 21. Target (f_s, L_b) region based on the requirements of efficiency, magnetic flux density, and current ripple. (a) $\alpha_{\mathrm{L},}$ distribution. (b) $B_{\mathrm{L},\max}$ distribution. (c) η distribution. (d) Target region of (f_{s}, L_{b}).

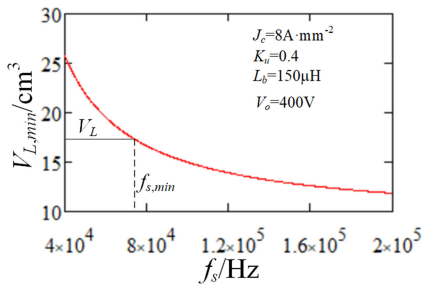


Fig. 22. Curve of the relationship between $V_{L,\min}$ and f_s for $J_c = 8\,\mathrm{A\cdot mm^{-2}}$, $K_u = 0.4$, $L_b = 150\,\mu\mathrm{H}$, $V_o = 400\,\mathrm{V}$, $B_{L,\max} = 0.3\,\mathrm{T}$, and $P_o = 3.3\,\mathrm{kW}$.

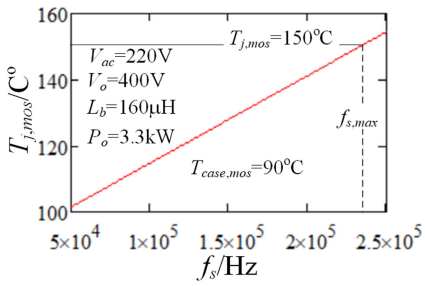


Fig. 23. $T_{j,\mathrm{mos}}$ versus f_s curve of IPP65R150CFD MOSFET for IBC PFC application when $V_{\mathrm{ac}} = 220\,\mathrm{V}$, $V_o = 40\,\mathrm{V}$, $P_o = 3.3\,\mathrm{kW}$, $L_b = 160\,\mu\mathrm{H}$, and $T_{\mathrm{case,\ mos}} = 90\,^{\circ}\mathrm{C}$.

MOSFET, $R_{\mathrm{th,\ JC}}$ is 3.6 °C/W, and the recommended $T_{j,\mathrm{mos}}$ is 150 °C or lower.

From (41), if $R_{\mathrm{th,\ JC}}$ and $T_{\mathrm{case,\ mos}}$ are determined, then $T_{j,\mathrm{mos}}$ is directly determined by $P_{\mathrm{mos,\ loss}}$. Since $P_{\mathrm{mos,\ loss}}$ is affected by f_s, $T_{j,\mathrm{mos}}$ will also be affected by f_s. Fig. 23 shows the curve of $T_{j,\mathrm{mos}}$ versus f_s. $T_{j,\mathrm{mos}}$ increases with f_s. According to the datasheet, the allowed highest junction temperature is 150 °C, which brings an upper limit to f_s. f_s should be lower than this upper limit $f_{s,\max}$.

Based on the aforementioned analyses, the volume of magnetic cores gives a lower limit of f_s. The allowed highest junction temperature of a MOSFET brings an upper limit of f_s. Therefore, the design range of f_s should be as follows:

$$f_{s,\min} \le f_s \le f_{s,\max}. \tag{42}$$

In this paper, f_s can be designed in the range of $74.2\,\mathrm{kHz} \le f_s \le 231.5\,\mathrm{kHz}$.

E. Design Flow of the Proposed Optimization Method

The design flowchart of the proposed method is illustrated in Fig. 24. It has the following 14 steps in the process.

Step 1: Determine V_{ac} and P_o based on actual applications.

Step 2: Select V_o from the curves of PF versus V_o , as shown in Fig. 18, based on the required PF.

Step 3: Select the components of the IBC PFC, including the EMI filter, the rectifier bridge, magnetic cores, MOSFETs, freewheeling diodes, output capacitors, etc. To fully utilize the horizontal space, the height of mass components should be close.

Step 4: Obtain the characteristic parameters of the selected components based on datasheets. Characteristic parameters include the forward voltage-drop $V_{F,\mathrm{bri}}$ of the selected rectifier bridge, the volume V_L of the selected magnetic cores, the reverse recovery charge Q_{rr} of the selected freewheeling diodes, etc. These characteristic parameters will be used to estimate the power loss.

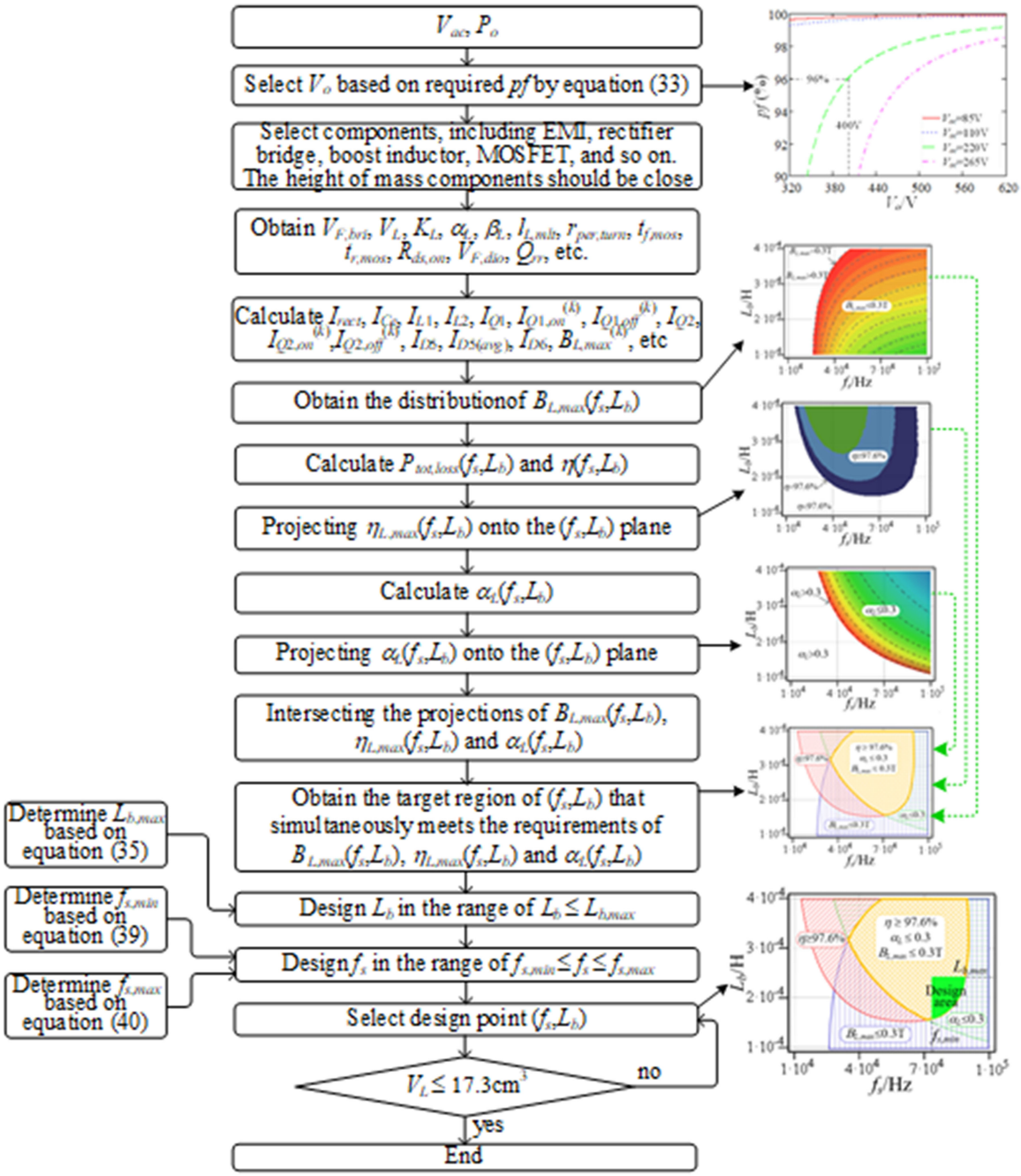


Fig. 24. Design flowchart of the proposed optimization design method for high-efficiency IBC PFC.

Step 5: Calculate rms currents I_{Ce}, I_{rect}, I_{L1}, I_{L2}, I_{Q1}, I_{Q2}, I_{D5}, I_{D6}, $I_{Co,\text{lf}}$, and $I_{Co,\text{hf}}$ to estimate the conduction loss. Calculate switching currents $I_{Q1,\text{on}}^{(k)}$, $I_{Q1,\text{off}}^{(k)}$, $I_{Q2,\text{on}}^{(k)}$, and $I_{Q2,\text{off}}^{(k)}$ to estimate the switching loss. Calculate $B_{L,\max}^{(k)}$ to estimate the ferrite loss of magnetics.

Step 6: Plot the $B_{L,\max}(f_s, L_b)$ surface and project it onto the (f_s, L_b) plane. Find out the design region that satisfies the limitation "$B_{L,\max} \le B_{\text{allowed},L,\max}$", where $B_{L,\max}$ is the actual maximum magnetic flux density, and $B_{\text{allowed},L,\max}$ is the allowed maximum magnetic flux density.

Step 7: Calculate the total power loss $P_{\text{tot, loss}}(f_s, L_b)$ and the efficiency $\eta(f_s, L_b)$. This is used to analyze the relationship between the efficiency η, switching frequency f_s, and boost inductance L_b.

Step 8: Plot the $\eta(f_s, L_b)$ surface and project it onto the (f_s, L_b) plane. The projection is used to find out the design region that satisfies the limitation "$\eta_{\text{required}} \le \eta_{\text{design}}$", where η_{required} is the minimum required efficiency, and η_{design} is the theoretical efficiency at the design point (f_s, L_b).

Step 9: Calculate the current ripple $\alpha_{L,\text{rip}}(f_s, L_b)$ and project its surface onto the (f_s, L_b) plane. The projection is used to find

TABLE III
REQUIREMENTS OF THE IBC

Requirement	Quantity
Power factor *pf*	≥ 96% (V_{ac}=220 V)
Minimum efficiency at the full load state $\eta_{min,full}$	≥ 97.6%
Allowed maximum magnetic flux density $B_{max,allowed}$	≤ 0.3 T
Normal output power P_o	3.3 kW
Input voltage V_{ac}	220 V
Allowed ratio of current ripple $\alpha_{L,allowed}$	≤ 0.3

TABLE IV
DESIGN RESULT

Parameters	Quantity
Output voltage V_o	400 V
Boost inductor L_b	220 μH
Switching frequency f_s	80 kHz

out the design region that satisfies the limitation "$\alpha_{L,\text{rip}} \leq \alpha_{L,\text{rip, allowed}}$", where $\alpha_{L,\text{rip}}$ is the actual current ripple, and $\alpha_{L,\text{rip,allowed}}$ is the allowed maximum current ripple.

Step 10: Intersect the projections obtained from Steps 6, 8, and 9; then, the target region of (f_s, L_b) can be obtained. This target region can simultaneously satisfy the limitations "$B_{L,\max} \leq B_{\text{allowed},L,\max}$", "$\eta_{\text{required}} \leq \eta_{\text{design}}$", and "$\alpha_{L,\text{rip}} \leq \alpha_{L,\text{rip,allowed}}$".

Step 11: Determine the maximum inductance $L_{b,\max}$ of the selected magnetic cores using (36). The actual inductance should be smaller than $L_{b,\max}$.

Step 12: Determine the minimum switching frequency $f_{s,\min}$ based on the volume limitation of the selected magnetic cores. Determine the maximum switching frequency $f_{s,\max}$ based on the thermal limitation using (41). The actual switching frequency should be designed in the range of $f_{s,\min} \leq f_s \leq f_{s,\max}$. Considering the limitations of f_s and L_b in the target region obtained in Step 10, a final design area can be obtained.

Step 13: Select (f_s, L_b) point in the final design area, considering the order of the three requirements.

Step 14: Check whether the minimum required volume of magnetic cores is more than the volume of the selected magnetic cores. If not, jump the flowchart to Step 13. If yes, the design process is complete.

VI. EXPERIMENTAL VERIFICATION

In this paper, the IBC PFC is used as the front-stage circuit of an OBC; its requirements are listed in Table III. Based on the listed components in Table II and the design flowchart in Fig. 24, a set of optimized parameters that meet the requirements presented in Table III are obtained and is presented in Table IV.

Litz wire is used for boost inductors. The type of litz wire is ϕ0.1 mm × 200. For the selected magnetic core, K_L, α_L, and β_L are 4.578, 2.56, and 1.23, respectively. The gap length l_g is set as 2.4 mm. $A_{L,l}$ and N_L are 0.099 μH and 47, respectively. The actual inductance L_b is about 220 μH. The window utilization coefficient is about 0.4. The effective permeability $\mu_{L,\text{eff}}$ is about 34.237.

TABLE V
COMPARISON BETWEEN THEORETICAL RESULTS AND EXPERIMENTAL RESULTS

Electrical Parameters	Theoretical	Simulation	Experimental	Error
I_{ac}	15 A	15.27 A	15.39 A	2.6%
I_{Ce}	1.72 A	1.74 A	1.76 A	2.3%
I_{rect}	15.21 A	15.24 A	15.36 A	1.2%
I_{L1}	7.60 A	7.60 A	7.65 A	0.6%
I_{Q1}	4.41 A	4.41 A	4.45 A	0.9%
I_{D5}	6.20 A	6.20 A	6.24 A	0.6 %
I_{Co}	6.55 A	6.56 A	6.62 A	1.1%

Based on the components given in Table II and the optimal design results given in Table IV, a 3.3 -kW IBC PFC prototype applied for an OBC is developed. Fig. 25(a) shows the layout of the PCB. To fully utilize space, the PCB is divided into three parts, namely, the main circuit board, the auxiliary power supply board, and the input EMI filter board. The main circuit board includes the ac/dc stage and the dc/dc stage. An IBC is used for the ac/dc stage to stabilize the dc-link voltage and to improve the PF. The auxiliary power supply provides the power for the driving circuits, the sampling circuit, the digital signal processer, etc.

The input EMI filter and the auxiliary power supply are installed over the main circuit board. Two-dimensional scales of the main circuit, the auxiliary power supply, and the EMI are 220 mm × 156 mm, 108 mm × 77 mm, and 145 mm × 33 mm, respectively. According to the design drawing of the 3.3-kW OBC, as shown in Fig. 25(b), a prototype is developed, and its physical picture is shown in Fig. 25(c). The outer three-dimensional (3-D) scale of the OBC prototype is 241 mm × 175 mm × 75 mm. The outer volume is about 193 in^3, and the power density of the OBC is about 17.1 W/in^3. Excluding the dc/dc stage, the power density of the IBC is about 36.5 W/in^3.

Measured waveforms of the prototype are shown in Fig. 26(b). Measured results are close to simulation results. Both simulation results and measured results are consistent with theoretical results shown in Fig. 4.

Table V presents the comparison of theoretical and experimental results under full-load condition. The difference between experimental and theoretical results is less than 2.6%. Experimental results verify that the proposed method can accurately calculate rms currents of the IBC PFC. Since the conduction loss has a square relationship with rms currents, the efficiency difference between theoretical and experimental results will be very small.

The actual maximum magnetic flux density is about 0.3 T. Fig. 27 shows the power loss distribution of the 3.3-kW IBC PFC prototype. Under full-load condition, $P_{\text{tot, loss}}$ and η are about 91.8 W and 97.3%, respectively. The driving loss is about 0.2 W and can be ignored. The sum of rectifier bridge loss,

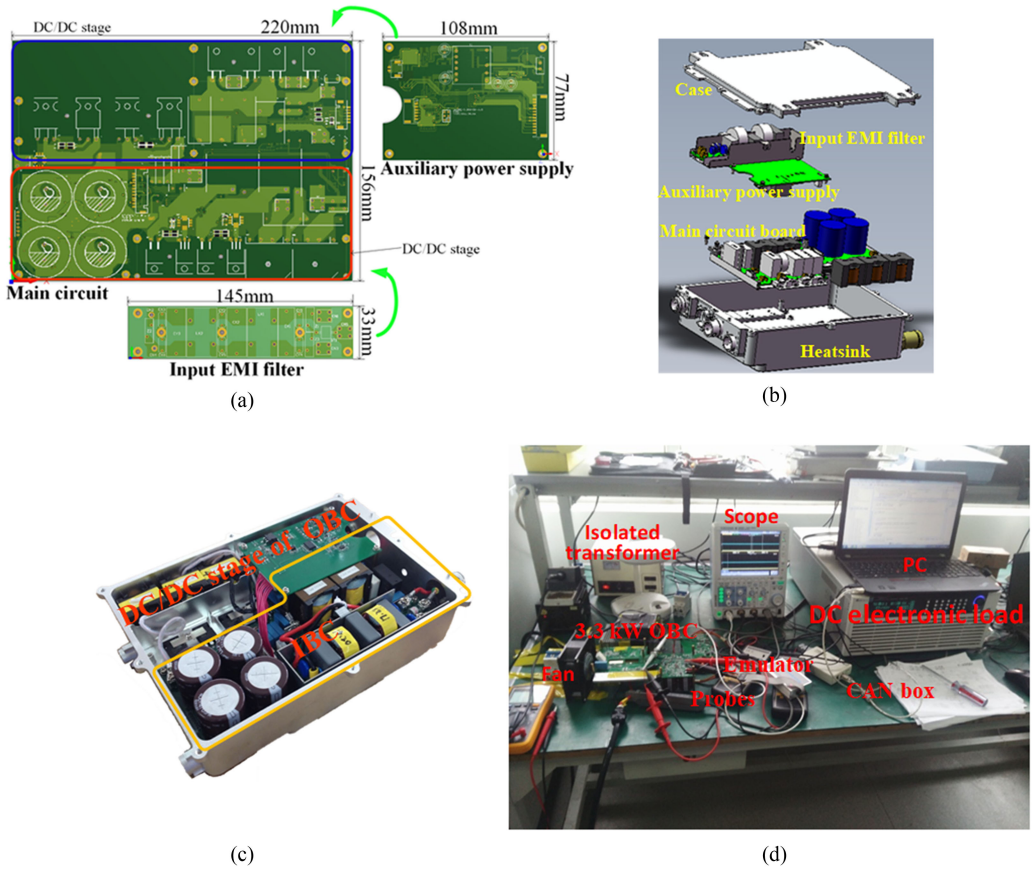


Fig. 25. Pictures of the experimental platform of the developed 3.3-kW OBC prototype. (a) PCB layout. (b) Component arrangement. (c) Physical picture. (d) Testbench.

MOSFET loss, and freewheeling diode loss dominates the total loss, which is about 85.8% of the total loss.

Theoretical and measured efficiency curves are shown in Fig. 28. When $V_{ac} = 220$ V, the measured full-load efficiency is about 97.2%. When $V_{ac} = 230$ V, the efficiency at the full-load state is about 97.8%, which means that the efficiency is improved by about 0.8% compared with comparison prototypes.

The measured curve can well match with the theoretical curve. The error between theoretical and experimental curves is less than 0.8% in the full-load range, which means that the proposed method can accurately precalculate the efficiency. In this paper, all devices are Si-based. By contrast, the SiC diode IDH10SG60C is used to implement a 2.2-kW IBC applied for PFC in [30]. The SiC JFET SJDP120R085 and the SiC diode SDT12S60 are utilized to realize a 1.2-kW IBC PFC in [31]. Infineon CoolMOS IPW60R045CP with a low ON-resistor and the Cree SiC diode C3D20060D are adopted for a 3.7-kW IBC PFC in [32]. In [33], the MOSFET IIPW60R041C6 with a low ON-resistor and the SiC diode CSD10060 are used to implement a 1.4-kW IBC PFC. Compared with the works presented in [30]–[34], characteristic parameters of devices in this paper are poorer, and the cost of devices in this paper are lower, which is helpful in reducing the cost for industrial applications. Even in this case, the measured efficiency in the full-load range of the prototype in this paper is still higher than that of comparison prototypes proposed in [30]–[34]. This means that the efficiency of an IBC can be improved by the proposed optimization design method, even though the characteristic parameters of devices are poorer.

Table VI presents a comparison of characteristic parameters. Compared with the works presented in [30]–[35], characteristic parameters in this paper are poorer; for example, the ON-resistance of MOSFETs is much higher than that in [31]–[35]. High-performance SiC devices presented in [30]–[34] have no reverse recovery charge and reverse recovery loss. If Si-based devices are replaced by high-performance SiC devices, the efficiency of the prototype in this paper can be further increased. The 3-D scale and power density of the 3.3-kW OBC prototype are 245 mm × 175 mm × 75 mm and 17.1 W/in^3, respectively. This is higher than that reported in [32]. In [35], an all Si-based IBC prototype is developed, and the comprehensive characteristic of devices is better than that presented in this paper.

Fig. 29 shows the curves of the relationship between efficiency and input voltage. Limited by the current-handling capability, the maximum input rms current I_{ac} is set as 12 A. In the range of 85 V $\leq V_{ac} \leq$ 206 V, the normal output power of the prototype is 12 A × V_{ac}. In the range of 206 V $\leq V_{ac} \leq$ 270 V, the normal output power is set as 3.3 kW; then, the input rms current is equal to 3.3 kW/ V_{ac}. Compared with the Si-based IBC

TABLE VI
PERFORMANCE PARAMETERS OF SEMICONDUCTOR DEVICES

Parameters	This paper	Literature [30]	Literature [31]	Literature [32]	Literature [33]	Literature [34]	Literature [35]
R_{Le}	23 mΩ	——	——	——	——	——	——
R_{Ce}	226 mΩ	——	——	——	——	——	——
$V_{F,bri}$ (25°C)	1.1 V	0.83 V	1.1 V	——	0.87 V	≤1.19V	——
R_L	43 mΩ	22 mΩ	——	——	——	——	——
$R_{ds,on}$ (25°C)	150 mΩ	160 mΩ	85 mΩ	45 mΩ	≤40 mΩ	125 mΩ	70 mΩ
$t_{mos,r}$	5.6 ns	13 ns	none (SiC)	20 ns	none	5 ns	27 ns
$t_{mos,f}$	7.6 ns	8 ns	none (SiC)	10 ns	none	5 ns	8 ns
$V_{F,dio}$	2.05 V	1.8 V	1.5 V	1.5 V	1.6 V	1.5 V	1.95 V
t_{rr}	15 ns (Si)	none (SiC)	none (SiC)	none (SiC)	none (SiC)	none (SiC)	16 ns (Si)
R_{dio}	66 mΩ	——	——	——	——	——	47 mΩ
$R_{Co,lf}$	254 mΩ	1237 mΩ	——	——	——	——	
P_o	3.3 kW	1.4 kW	1.2 kW	3.7 kW	1.4 kW	4 kW	1.2 kW
η	97.3%(220V) 97.7%(230V)	96.8 %(230V)	96.2 %(230V)	96.9 %(230V)	96.8 %(220V)	97.2%(220V)	96.9%(220V) 97.0%(230V)
Cost of power devices	7.5 $	21.8 $	——	31.3 $	46.1 $	——	——
Power density	36.5W/in^3	——	——	15.2W/in^3	——	——	——

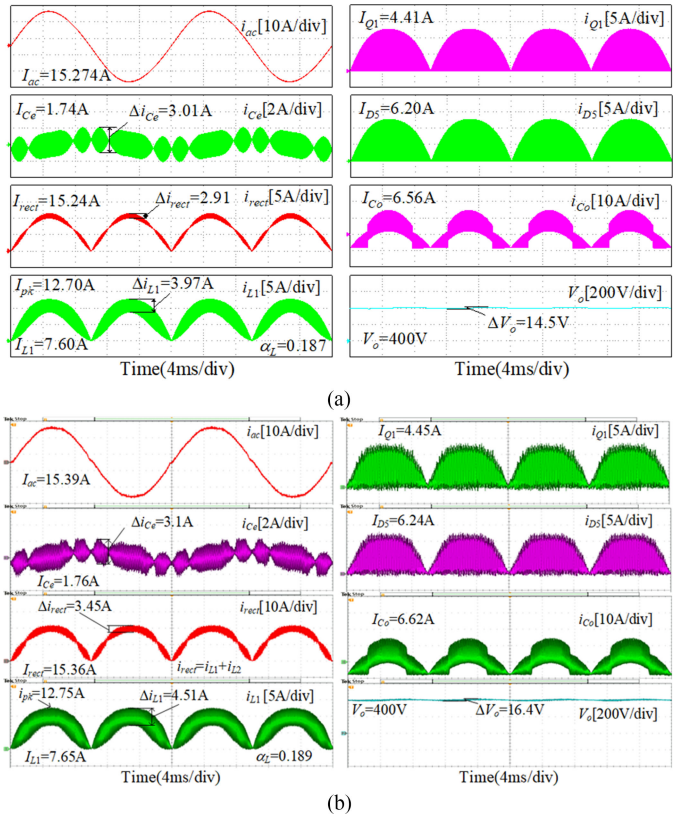


Fig. 26. Waveforms of $i_{\rm ac}, i_{Ce}, i_{\rm rect}, i_{L1}, i_{Q1}, i_{D5}, i_{Co}$, and V_o for the 3.3-kW IBC PFC from (a) simulation results and (b) experiment results.

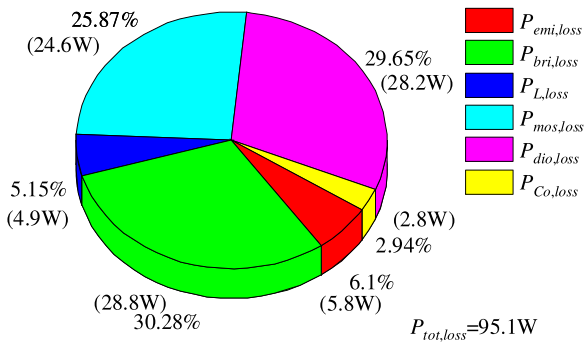


Fig. 27. Power loss distribution of the 3.3-kW IBC prototype under the full-load condition.

proposed in [35], as shown in Fig. 26, the measured efficiency, in this paper, is higher in the input voltage range of 80–270 V.

Compared with conventional Si-based IBC prototype presented in [35], at $V_{\rm ac} = 85$ V, the efficiency can be improved by about 2.4%. At $V_{\rm ac} = 220$ V and $V_{\rm ac} = 230$ V, the efficiency differences are about 0.4% and 0.8%, respectively. If $V_{\rm ac}$ increases to 270 V, the efficiency difference will increase to 1%.

Fig. 30 shows the measured waveforms of $i_{\rm ac}, v_{\rm ac}, i_{L1}$, and V_o. The peak-to-peak voltage of V_o is about 16.4 V. $i_{\rm ac}$ can well track $v_{\rm ac}$. The rms value of $i_{\rm ac}$ is about 15.36 A. The current ripple of i_{L1} is about 4.51 A. The current ripple ratio is about 0.21, which is lower than 0.3.

Fig. 31 shows the measured PF. Compared with the work presented in [34], the PF in this paper is higher in the full-load range. In particular, under the full-load condition, the PF is higher than 99.5%, which is higher than that of the comparison prototype in [34].

The environment temperature is 28 °C. The working temperature of components are measured and listed in Table VII. Since the EMI filter is installed in air and has no heatsink, its working temperature is the highest among the components given in Table VII. The liquid cooling method is used to cool the rectifier bridge, MOSFETs, and freewheeling diodes. The working temperature of the rectifier bridge, MOSFETs, and freewheeling diodes are relatively lower than that of the EMI inductor at normal output power. The working temperature of freewheeling

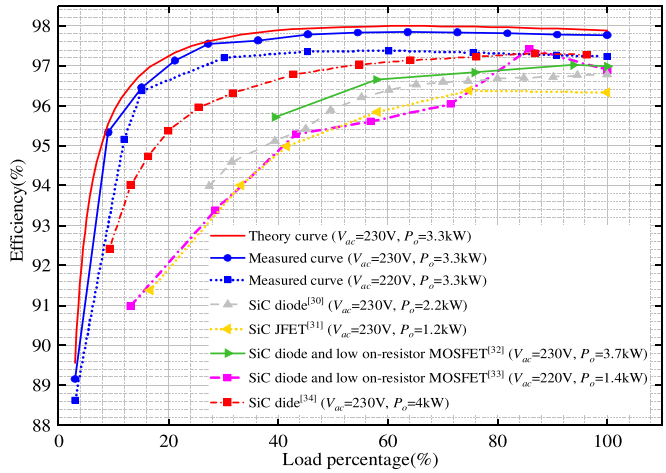


Fig. 28. Measured curves of efficiency.

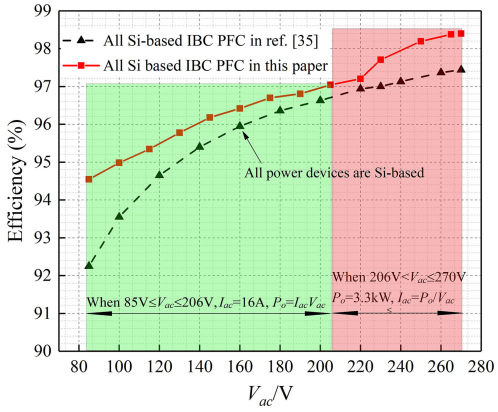


Fig. 29. Curves of the relationship between measured efficiency and input voltage.

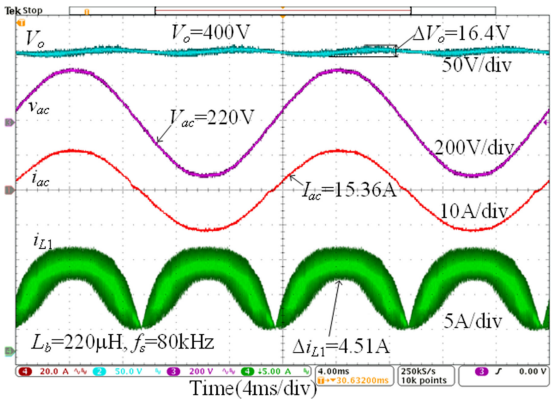


Fig. 30. Measured waveforms of $i_{\rm ac}$, $v_{\rm ac}$, i_{L1}, and V_o for $f_s = 80$ kHz, $L_b = 220\,\mu$H, and $P_o = 3.3$ kW.

diodes is the lowest because they are installed above the liquid cooling path, which has a relatively higher cooling ability and speed.

Fig. 32 shows the volume distribution of components. Heatsink volume is integrated with the case, which is used to seal and fasten the system; its volume is about 31.31 in^3. The volume of passive components is about 31.6 in^3, which occupies

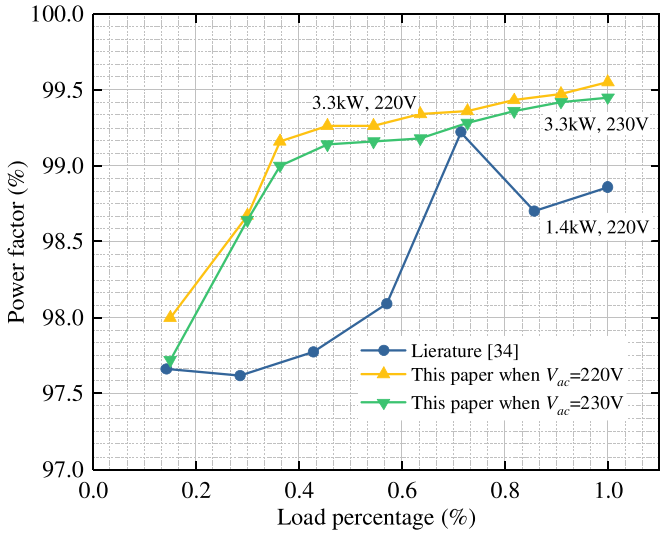


Fig. 31. Measured PF in this paper and literature [34].

TABLE VII
WORKING TEMPERATURE OF SEMICONDUCTOR DEVICES

Components	Temperature
EMI capacitor	77.1°C
EMI inductor	92°C
Rectifier bridges	76.3°C
Boost inductor wires	87.8°C
Boost inductor cores	79.4°C
MOSFETs	65.2°C
Freewheeling diodes	63°C
Output capacitors	65.9°C

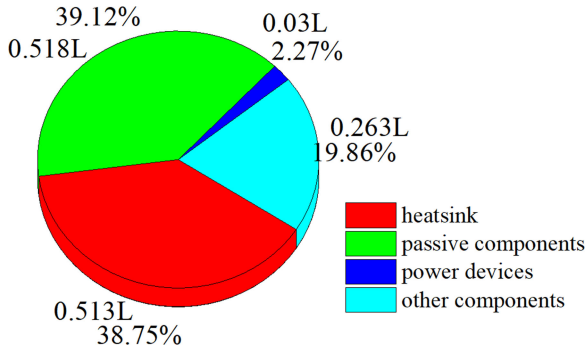


Fig. 32. Volume distribution of the used space for a 3.3-kW OBC, including the IBC PFC and dc/dc stage.

the largest part of the 3.3-kW OBC. Other components include plug-ins, the PCB, SMT components, and so on.

VII. CONCLUSION

Three intrinsic parameters affecting the efficiency of the IBC PFC are found and optimized based on the requirements of efficiency, current ripple, PF, volume, and maximum magnetic flux density of magnetic cores. A 3.3-kW IBC PFC prototype applied for an OBC is developed. Power densities of the OBC and the IBC are about 17.1 and 36.5 W/in^3, respectively. At the full-load state, the efficiency of the IBC PFC can reach 97.7%

at $V_{ac} = 230\,V$ and 97.2% at $V_{ac} = 220\,V$. Compared with the traditional Si-based IBC, the measured results verify that the efficiency of the IBC PFC can be increased by at least 0.7% ($V_{ac} = 230\,V$) and 0.4%($V_{ac} = 220\,V$) by using the proposed optimization design method, even if the performance of devices is poor. The proposed design method can be used to design high-efficiency IBCs while limiting hardware costs.

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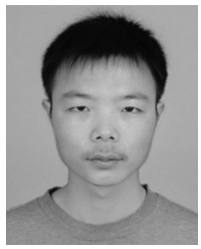

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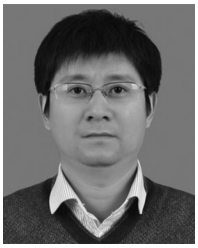

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