Leakage Current Reduction of Three-Phase Z-Source Three-Level Four-Leg Inverter for Transformerless PV System

Xiaoqiang Guo, *Senior Member, IEEE*, Yong Yang, Baocheng Wang, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Leakage current reduction is one of the important issues for transformerless photovoltaic (PV) systems. Many interesting solutions have been reported to reduce the leakage current for three-phase PV inverters. However, most of them are limited to two-level inverters. Moreover, there is a potential risk of the overcurrent phenomenon. In order to solve the problem, a *Z*-source three-level four-leg inverter with a new modulation strategy is proposed in this paper. First, the mathematical modeling of the three-level four-leg *Z*-source inverter for leakage current reduction is established for the first time. Second, a new carrier-based modulation strategy is proposed by utilizing the effective large, medium, small, and zero vectors, instead of the invalid vectors, to achieve the constant common-mode voltage, as well as the leakage current suppression. Finally, the proposed solution is carried out on the Texas Instruments TMS320F28335 DSP + Xilinx XC3400 field-programmable gate array digital control hardware platform. The experimental results verify the effectiveness of the proposed solution.**

***Index Terms*—Four-leg inverter, leakage current, three-level inverter, Z-source inverter (ZSI).**

I. Introduction

DUE TO environmental pollution and government incentives in the renewable energy system, the photovoltaic (PV) power system has received widespread attention in recent years [1]–[5]. A transformer usually is installed for the conventional PV inverter to connect the grid. However, it increases the cost, size, and decreases the efficiency of the overall system. That is the reason why the transformerless PV inverters are popular in recent years [6], [7].

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it is inherently a step-down converter. Besides, in practice, the PV panel voltage depends on many factors such as the weather conditions, which will cause the f output voltage variation of PV panel. In this case, a boost converter has to be installed to the low-voltage PV panel [34]. Due to the existence of the additional switch in the boost converter, the additional gating driver is needed. Also, both the switch and diode of the boost converter need the heat sink [35]. Moreover, there is a potential risk of overcurrent, which reduces the system reliability. In order to solve the problem, the *Z*-source inverter (ZSI), originally proposed by Peng, can be used [36]. The amplitude of the output voltages can reach high levels due to the step-up characteristic. Both the risk of the overcurrent phenomenon and additional boost switch circuit are avoided [37].

For leakage current reduction in ZSI, Bradaschia *et al.* presented an improved modulation strategy for three-phase ZSI [38], where three odd or even vectors were used to eliminate the high-frequency CMV, so the leakage current can be well attenuated. However, the modulation index is limited. And it was pointed out in [39] that there is an undesired operation mode in [38], which could lead the system to instability. To solve this issue, a ZSI-S topology with two additional insulated-gate bipolar transistors is proposed in [39]. Meanwhile, to reduce the leakage currents, an improved pulsewidth modulation technique is presented to achieve the constant CMV. The undesired operation modes are avoided. However, two additional switches are needed, and the complexity of the control as well as the switching loss is increased. Another modified ZSI is presented in [40]. Only one additional switch is needed, compared with the conventional ZSI. And the leakage currents can be well suppressed due to dual-grounding structure. Besides, there are many other papers which are devoted to reduce the leakage current for the *Z*-source and *qZ*-source inverter [41]–[44]. However, the aforementioned topologies and modulation methods for ZSI are limited to three-leg inverters. For the leakage current reduction in the three-phase four-leg ZSI, an interesting solution is presented in [45] to achieve the constant CMV. However, it is limited to a two-level inverter in nature. So far, the analysis and solution regarding the leakage current reduction of three-level four-leg ZSI has not been explored in the literature. That is the motivation of this paper to deal with this unsolved problem. The importance of the three-level four-leg ZSI is listed as follows.

1) For the three-level inverter, it has the advantage over the two-level inverter in both high-power and low-power systems [46]. It can decrease the total harmonic distortion (THD), voltage stress of dv/dt on switches, electromagnetic interference, and improve the output waveform quality [47].
2) For the four-leg inverter, it has the advantage over the three-leg inverter for unbalanced deal capability and more flexible to achieve optimal objective [30].
3) For the ZSI, it can avoid the potential risk of the overcurrent phenomenon of the inverter and need not install the additional boost converter [34].

The contributions of this paper are shown as follows. First, the leakage current behavior for three-level four-leg ZSI is established with a mathematical description. Second, a new carrier-based modulation strategy is proposed by utilizing the effective large, medium, small, and zero vectors, instead of the invalid vectors, to achieve the constant CMV, as well as the leakage current suppression. Finally, the experimental evaluation of the conventional and proposed solution is presented.

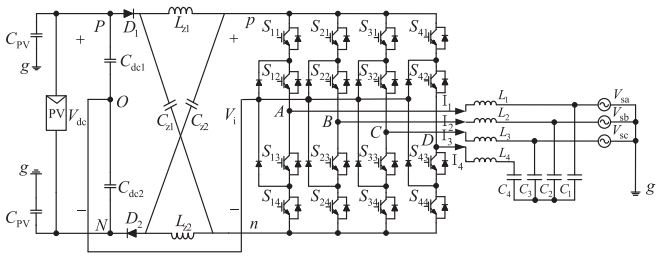

Fig. 1. Schematic diagram of *Z*-source three-level four-leg inverter.

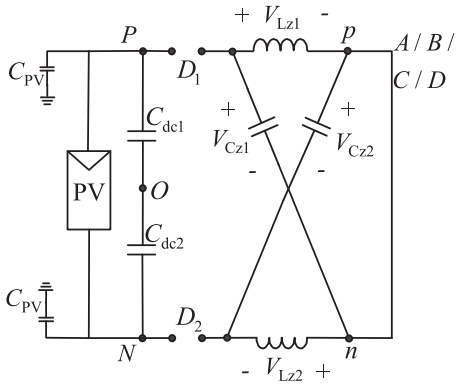

Fig. 2. Shoot-through state.

The rest of this paper is organized as follows. Section II presents the operation principle of the *Z*-source three-level four-leg inverter. The common-mode behavior is discussed in Section III. The conventional and proposed modulation strategies are presented in Section IV. The simulation and experimental results are provided in Section V. Finally, the conclusion is reached in Section VI.

II. Operation Principle

Fig. 1 illustrates the schematic diagram of the three-phase *Z*-source three-level four-leg inverter for the transformerless PV system, where $C_{\rm PV}$ is the parasitic capacitance between the PV panel and ground. $V_{\rm dc}$ is the dc input voltage. The leakage current will arise on condition as the parasitic capacitor voltage or CMV varies in a high-frequency way.

The system operation mode can be divided into two states. One is the shoot-through state, and the other is the non-shoot-through state. For simplicity of analysis, the capacitance C_{Z1} and C_{Z2} of the Z-source network are equal, and the capacitor voltage can be expressed as $V_{Cz1} = V_{Cz2} = V_{Cz}$. The inductance $L_{Z1} = L_{Z2}$, and inductor voltage can be expressed as $V_{Lz1} = V_{Lz2} = V_{Lz}$.

During shoot-through states, the diodes of D_1 and D_2 are reversely OFF, as shown in Fig. 2. During non-shoot-through

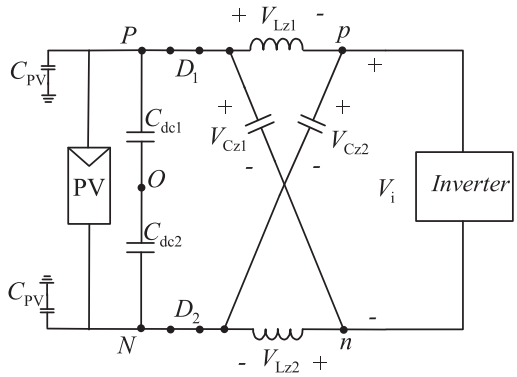

Fig. 3. Non-shoot-through state.

state, as shown in Fig. 3, the input voltage can be expressed as follows:

$$V_{Lz} = V_{\rm dc} - V_{Cz} \tag{1}$$

$$V_i = V_{Cz} - V_{Lz} = 2V_{Cz} - V_{\rm dc} \tag{2}$$

where $V_{\rm dc}$ is the dc input voltage and V_i is the *Z*-source voltage. It is defined that T_0 is the shoot-through period, T_1 is the non-shoot-through period, and *d* is the shoot-through duty cycle. The average voltage of the inductor over one switching period of T_s should be zero, and thus

$$\frac{T_0 V_{Cz} + T_1(V_{\rm dc} - V_{Cz})}{T_s} = 0. \tag{3}$$

The voltage values of V_i, V_{Cz}, and V_{Lz} can be derived from (1) to (3) as follows:

$$V_i = V_{Cz} - V_{Lz} = 2V_{Cz} - V_{\rm dc} = \frac{T}{T_1 - T_0} V_{\rm dc} = \frac{1}{1-2d} \cdot V_{\rm dc} \tag{4}$$

$$V_{Cz} = B_B \cdot V_{\rm dc} \tag{5}$$

$$V_{Lz} = (1 - B_B) \cdot V_{\rm dc} \tag{6}$$

where $B_B = (1-d)/(1-2d)$.

III. Common-Mode Behavior Analysis

In this section, the common-mode behavior of *Z*-source three-level four-leg inverter is discussed. First, the relationship between the switching states and output voltages is shown in (7), where $S_{ij} = 1$ if the switch is ON, while $S_{ij} = 0$ if the switch is OFF. $X = A, B, C, D. i = 1, 2, 3, 4. j = 1, 2, 3, 4$

$$V_{\rm XN} = \begin{cases} B_B V_{\rm dc} & S_X = 2 \;\; S_{i1} = 1, S_{i2} = 1, S_{i3} = 0, S_{i4} = 0 \\ V_{\rm dc}/2 & S_X = 1 \;\; S_{i1} = 0, S_{i2} = 1, S_{i3} = 1, S_{i4} = 0 \\ (1-B_B)V_{\rm dc} & S_X = 0 \;\; S_{i1} = 0, S_{i2} = 0, S_{i3} = 1, S_{i4} = 1. \end{cases} \tag{7}$$

The phase voltage to ground for each leg of V_{Ag}, V_{Bg}, V_{Cg}, and V_{Dg} can be derived from Fig. 1 as follows:

$$V_{Ag} = \left(B_B S_{11} S_{12} + \frac{S_{12} S_{13}}{2} + (1 - B_B) S_{13} S_{14}\right) V_{\rm dc} + (S_{11} S_{12} + S_{12} S_{13} + S_{13} S_{14}) V_{Ng} \tag{8}$$

$$V_{Bg} = \left(B_B S_{21} S_{22} + \frac{S_{22} S_{23}}{2} + (1 - B_B) S_{23} S_{24}\right) V_{\rm dc} + (S_{21} S_{22} + S_{22} S_{23} + S_{23} S_{24}) V_{Ng} \tag{9}$$

$$V_{Cg} = \left(B_B S_{31} S_{32} + \frac{S_{32} S_{33}}{2} + (1 - B_B) S_{33} S_{34}\right) V_{\rm dc} + (S_{31} S_{32} + S_{32} S_{33} + S_{33} S_{34}) V_{Ng} \tag{10}$$

$$V_{Dg} = \left(B_B S_{41} S_{42} + \frac{S_{42} S_{43}}{2} + (1 - B_B) S_{43} S_{44}\right) V_{\rm dc} + (S_{41} S_{42} + S_{42} S_{43} + S_{43} S_{44}) V_{Ng} \tag{11}$$

$$V_{Ag} = I_1 \cdot sL_1 + V_{sa} \tag{12}$$

$$V_{Bg} = I_2 \cdot sL_2 + V_{sb} \tag{13}$$

$$V_{Cg} = I_3 \cdot sL_3 + V_{sc} \tag{14}$$

$$V_{Dg} = I_4 sL_4 + \frac{2}{3} V_{c4}. \tag{15}$$

The V_{Ng} is the voltage between positive (P) or negative (N) dc bus and ground point "*g*." V_{Lz} is the voltage across inductor of *Z*-source network. V_{sa}, V_{sb}, and V_{sc} are the grid voltages. L_1, L_2, L_3, and L_4 are the filter inductances and $L_1 = L_2 = L_3 = L_4 = L$. I_1, I_2, I_3, and I_4 are the current shown in Fig. 1. And *s* is the Laplace operator.

From (8) to (11), it can be calculated as

$$V_{Ag} + V_{Bg} + V_{Cg} + V_{Dg} = aV_{\rm dc} + bV_{Ng} \tag{16}$$

where

$$a = B_B S_{11} S_{12} + S_{12} S_{13}/2 + (1 - B_B) S_{13} S_{14} + B_B S_{21} S_{22} + S_{22} S_{23}/2 + (1 - B_B) S_{23} S_{24} + B_B S_{31} S_{32} + S_{32} S_{33}/2 + (1 - B_B) S_{33} S_{34} + B_B S_{41} S_{42} + S_{42} S_{43}/2 + (1 - B_B) S_{43} S_{44}$$

and

$$b = S_{11} S_{12} + S_{12} S_{13} + S_{13} S_{14} + S_{21} S_{22} + S_{22} S_{23} + S_{23} S_{24} + S_{31} S_{32} + S_{32} S_{33} + S_{33} S_{34} + S_{41} S_{42} + S_{42} S_{43} + S_{43} S_{44}.$$

From (12) to (15), it can be derived as follows:

$$V_{Ag} + V_{Bg} + V_{Cg} + V_{Dg} = (I_1 + I_2 + I_3 + I_4) sL + 2V_{c4}/3 = V_{Ng} s^2 C_{\rm PV} L + 2V_{c4}/3. \tag{17}$$

The parasitic capacitor voltage V_{Ng} can be derived from (16) to (17) as follows:

$$V_{Ng} = \left(aV_{\rm dc} - \frac{2}{3} V_{c4}\right) / (s^2 L C_{\rm pv} - b). \tag{18}$$

From Fig. 1, V_{c4} can be calculated as

$$V_{c4} = \left(6 - 3s^2 L_Z C_{\rm PV} - \frac{3}{2} s^2 L C_{\rm pv}\right) V_{Ng} - 6V_{\rm CM} + 6V_{LZ}. \tag{19}$$

Substituting (19) into (18), the parasitic capacitor voltage V_{Ng} can be rewritten as follows:

$$V_{Ng} = \frac{1}{4 - 2s^2 L_Z C_{\rm PV} - b}[aV_{\rm dc} - 4V_{Lz} + 4V_{\rm CM}]. \tag{20}$$

From (20), it can be observed that the parasitic capacitor voltage V_{Ng} is mainly dependent on the following factors such as $V_{\rm dc}$, V_{LZ}, $V_{\rm CM}$, a, and b. In general, the dc voltage of $V_{\rm dc}$ is constant. From (6), it can be seen that V_{LZ} depends only on the shoot-through duty cycle. When shoot-through duty cycle is constant, V_{LZ} would be constant. The coefficients a and b are depended on the switching states shown in (16) and can be constant through proper control of the switching states; it will be analyzed in Section IV. Therefore, V_{Ng} is mainly determined by the $V_{\rm CM}$.

The CMV $V_{\rm CM}$ for both shoot-through and non-shoot-through states is defined as

$$V_{\rm CM} = (V_{\rm AN} + V_{\rm BN} + V_{\rm CN} + V_{\rm DN})/4. \tag{21}$$

In case of the shoot-through state, the diode is OFF, and the common-mode circuit is switched OFF. Each phase voltage is

$$V_{\rm AN} = V_{\rm BN} = V_{\rm CN} = V_{\rm DN} = V_{Cz} + V_{D2}. \tag{22}$$

The inductor voltage, capacitor voltage, and diode voltage in the shoot-through state are

$$V_{Lz} = V_{Cz} = B_B \cdot V_{\rm dc} \tag{23}$$

$$V_{D2} = \frac{V_{\rm dc} - 2V_{Cz}}{2} = \frac{(1 - 2B_B)}{2} V_{\rm dc}. \tag{24}$$

With (21)–(24), the CMV in the shoot-through state can be obtained

$$V_{\rm CM} = (V_{\rm AN} + V_{\rm BN} + V_{\rm CN} + V_{\rm DN})/4 = V_{\rm dc}/2. \tag{25}$$

According to the aforementioned analysis, the $V_{\rm CM}$ is constant in the shoot-through state. Therefore, if the CMV is also constant under non-shoot-through states, the leakage current will be effectively suppressed. Thus, it is important to find a modulation strategy to make the $V_{\rm CM}$ constant in the non-shoot through, which will be discussed in the next section.

IV. Modulation Strategy

For three-level inverters, the modulation can be classified into two categories. One is the carrier-based modulation, and the other is the space vector modulation. In practice, the space vector modulation needs complex implementation procedure, where it is necessary to calculate the dwell time and select the sector of vector. Therefore, the carried-based modulation is utilized in this paper.

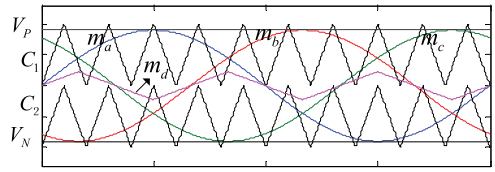

Fig. 4. Conventional modulation.

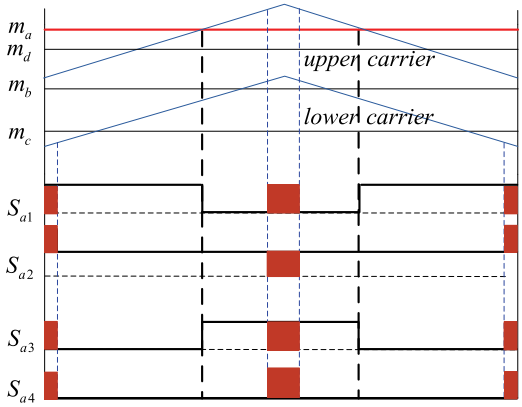

Fig. 5. Switching states within a cycle for A phase.

A. Conventional Modulation

For the three-level four-leg inverter, the conventional way to generate the gating signal is the dual-carrier modulation strategy, as shown in Fig. 4, where the gating signals of first three legs are generated by comparing the modulation wave with the carrier while the gating signal of the fourth leg is generated by comparing the zero sequence component with the triangular carrier. Finally, the shoot-through signal is inserted in the each carrier cycle, as shown in Fig. 5.

However, as shown in Fig. 6, the CMV is time-varying with the conventional modulation. Therefore, the leakage current is not able to be suppressed due to the high-frequency CMV.

B. Proposed Modulation Strategy

As discussed in the previous section, the parasitic capacitor voltage in the conventional solution is time-varying in a high-frequency way. So, the leakage current is not able to be effectively reduced. In order to solve it, a new modulation strategy is proposed by coordinating the switching states to achieve the constant CMV. According to the aforementioned analysis in Section III, the CMV is constant at $V_{\rm dc}/2$ in case of shoot-through state. So, the CMV would be constant all the time on condition that it is controlled to be $V_{\rm dc}/2$ in non-shoot-through state, which can be achieved by

$$S_A + S_B + S_C + S_D = 4. \tag{26}$$

In order to simplify the implementation, the switching states of the fourth leg can be controlled in the following way:

$$S_D = 4 - S_A - S_B - S_C. \tag{27}$$

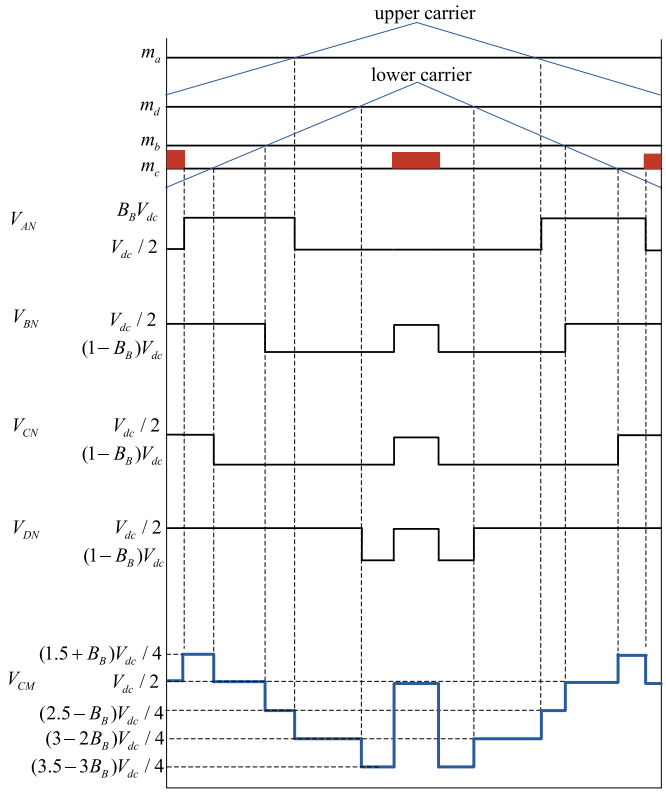

Fig. 6. Phase voltage and V_{CM} with conventional modulation.

TABLE I
CMV AND SWITCHING STATES

	Vector		S_A	S_B	S_C	S_D	a	b	V_{CM}
non-shoot through state	Effective vectors	large vector	0	2	0	2	2	4	$V_{dc}/2$
			2	2	0	0	2	4	$V_{dc}/2$
			2	0	0	2	2	4	$V_{dc}/2$
			2	0	2	0	2	4	$V_{dc}/2$
			0	0	2	2	2	4	$V_{dc}/2$
			0	2	2	0	2	4	$V_{dc}/2$
		medium vector	1	2	0	1	2	4	$V_{dc}/2$
			2	1	0	1	2	4	$V_{dc}/2$
			2	0	1	1	2	4	$V_{dc}/2$
			1	0	2	1	2	4	$V_{dc}/2$
			0	1	2	1	2	4	$V_{dc}/2$
			0	2	1	1	2	4	$V_{dc}/2$
		small vector	1	2	1	0	2	4	$V_{dc}/2$
			1	1	0	2	2	4	$V_{dc}/2$
			2	1	1	0	2	4	$V_{dc}/2$
			1	0	1	2	2	4	$V_{dc}/2$
			1	1	2	0	2	4	$V_{dc}/2$
			0	1	1	2	2	4	$V_{dc}/2$
		zero vector	1	1	1	1	2	4	$V_{dc}/2$
	Invalid vectors	-	0	1	0	X	-	-	-
			2	2	1	X	-	-	-
			1	2	2	X	-	-	-
			1	0	0	X	-	-	-
			0	0	1	X	-	-	-
			2	1	2	X	-	-	-
			0	0	0	X	-	-	-
			2	2	2	X	-	-	-

In this way, the switching states and corresponding CMV are listed in Table I.

Table I shows all the possible non-shoot-through states, the CMVs, and the values of "a," "b" when (27) is adopted, where X indicates that this state does not exist. In Table I, there are two groups of vectors for non-shoot-through state. One is the effective vector, and the other is the invalid vector. For the latter, (26) and (27) cannot be satisfied no matter what the switching state of the fourth leg is. Besides, from (7), it can be observed that S_D is limited, where the values of S_D only are three states: 0, 1, 2. Therefore, the states similar with $S_A = S_B = S_C = 0, S_D = 4$ and $S_A = S_B = S_C = 2, S_D = -2$ do not exist because of $S_D \notin 0, 1, 2$. On the other hand, for the effective vectors such as the large, medium, small, and zero vector, there is always a switching state S_D of the fourth leg, which meet the requirement of (26) and (27). Fig. 7 shows the effective vector distribution, which is for understanding the switching states distribution.

The CMV of those effective vectors in Fig. 7 is analyzed as follows. Take the 2101 as an example, the corresponding switching states are $S_{11} = 1$, $S_{12} = 1$, $S_{13} = 0$, $S_{14} = 0$, $S_{21} = 0$, $S_{22} = 1$, $S_{23} = 1$, $S_{24} = 0$, $S_{31} = 0$, $S_{32} = 0$, $S_{33} = 1$, $S_{34} = 1$, $S_{41} = 0$, $S_{42} = 1$ $S_{43} = 1$, $S_{44} = 0$. At this time, from (7), V_{AN}, V_{BN}, V_{CN}, and V_{DN} are $B_B V_{\mathrm{dc}}, V_{\mathrm{dc}}/2, (1 - B_B)V_{\mathrm{dc}}$, and $V_{\mathrm{dc}}/2$, respectively. Then, by (21), the CMV V_{CM} can be calculated as $V_{\mathrm{CM}} = V_{AN} + V_{BN} + V_{CN} + V_{DN} = (B_B V_{\mathrm{dc}} + V_{\mathrm{dc}}/2 + (1 - B_B)V_{\mathrm{dc}} + V_{\mathrm{dc}}/2)/4 = V_{\mathrm{dc}}/2$. Similarly, the CMVs V_{CM} of other effective vectors in Fig. 7 are also $V_{\mathrm{dc}}/2$. Therefore, V_{CM} is constant when (27) is adopted in non-shoot-through state. It is worth noting that, unlike the conventional method where only the medium and zero vectors are used to eliminate the high-frequency CMV, the proposed solution uses all the effective vectors, that is, the large, medium, small, and zero vectors to control the CMV constant. Comparing Fig. 6 with Fig. 7(b), it can be observed that there are 24 turn-on losses and turn-off losses in a carrier cycle for the traditional solution while there are 26 turn-on losses and turn-off losses in a carrier cycle for the proposed solution. That is, there are two more turn-on losses and turn-off losses for the proposed solution than the traditional scheme in a carrier cycle. Although the number of switching for the proposed solution is slightly increased than the traditional scheme, both the leakage current and the THD of grid current are reduced. Moreover, with the development of wide band gap semiconductor device, the switching loss can be further reduced. Therefore, it is an attractive solution. For the coefficients a and b, take the effective vectors 2101 as example; from (7), the corresponding switching states are $S_{11} = 1$, $S_{12} = 1$, $S_{13} = 0$, $S_{14} = 0$, $S_{21} = 0$, $S_{22} = 1$, $S_{23} = 1$, $S_{24} = 0$, $S_{31} = 0$, $S_{32} = 0$, $S_{33} = 1$, $S_{34} = 1$, $S_{41} = 0$, $S_{42} = 1$, $S_{43} = 1$, $S_{44} = 0$. As defined by (16), the coefficients a and b are 2 and 4, respectively. In a similar way, the coefficients a and b are calculated as 2 and 4 in other effective vectors. Therefore, a and b are also constant when the effective vectors in Table I and Fig. 7 are used.

In summary, because both the V_{CM} and coefficients a, b are constant, therefore, from (20), the parasitic capacitor voltage V_{Ng} is constant in the proposed solution. Fig. 8 shows the block diagram of the hardware implementation and control unit part.

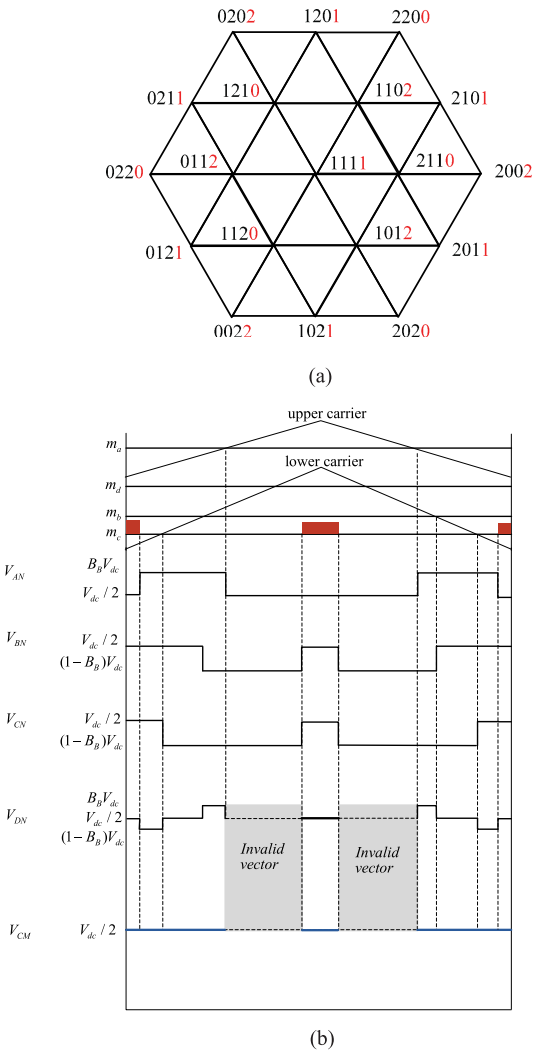

Fig. 7. Proposed method. (a) Diagram of the effective vector distribution. (b) Switching states and CMV.

The grid voltages are measured by the transducers LV 28-P, and then through a phase-locked loop to generate the angle for the reference current. The transducer LA 55-P is used to measure the current, which is subtracted by the reference current. The error is regulated by the proportional-resonant controller and the inverse Clarke transformation. And then, the modulation wave m_a, m_b, and m_c can be obtained. These control algorithms are implemented by a TMS320F28335 DSP control board. Considering that the switching state of the fourth leg S_D is generated by S_A, S_B, S_C, the logical operation is implemented by a Xilinx XC3400 field-programmable gate array (FPGA).

In the Xilinx XC3400 FPGA, the logical signals S_{1a}, S_{2a}, S_{1b}, S_{2b}, S_{1c}, and S_{2c} are obtained by comparing the modulation wave m_a, m_b, and m_c with the carriers c1, c2. When m_a is greater than c1, S_{1a} is 1; otherwise, S_{1a} is 0. When m_a is greater than the carrier c2, S_{2a} is 1; otherwise, S_{2a} is 0. In the similar way, S_{1b}, S_{2b}, S_{1c}, and S_{2c} can be obtained. Then, S_A, S_B, and S_C are calculated by $S_A = S_{1a} + S_{2a}$, $S_B = S_{1b} + S_{2b}$, and $S_C = S_{1c} + S_{2c}$. S_D can be obtained by (27). And then, the effective vectors are obtained by eliminating the invalid vectors. The 16 logical signals G_{11}–G_{44} are obtained

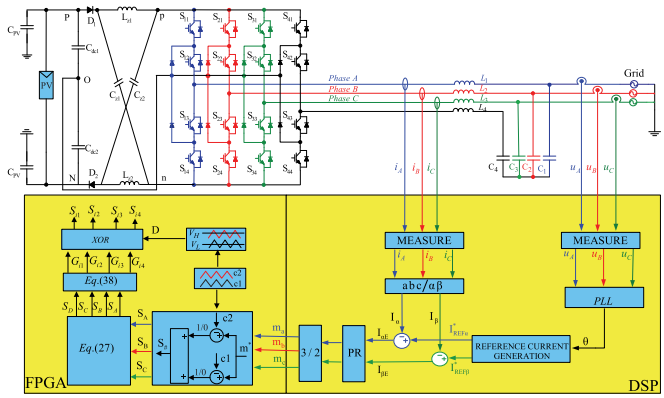

Fig. 8. Block diagram for implementation.

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameter	Simulation value	Experimental value
dc bus voltage V_{dc}	470 V	120 V
Capacitance of Z-source V_{Cz}	940 μH	940 μH
inductance of Z-source V_{Lz}	3 mH	3 mH
line-line voltage V_{AB}	380 V/50 Hz	98 V/50 Hz
rated current of grid	10 A	8 A
Filter inductance L	7 mH	5 mH
Filter capacitor C	9.4 μF	9.4 μF
parasitic capacitor C_{pv}	300 nF	300 nF
shoot-through duty cycle D	0.2	0.2
switching frequency f	10 kHz	10 kHz

by (28), where $X = A, B, C, D$. $i = 1, 2, 3, 4$. For example, when S_A is 2, at this time, G_{11}, G_{12}, G_{13}, and G_{14} are 1, 1, 0, and 0, respectively. Finally, the gating signals are generated by the 16 logical signals and shoot-through signals. V_H and V_L are the signals that control the shoot-through duty cycle

$$\begin{cases} S_X = 2\ G_{i1} = 1, G_{i2} = 1, G_{i3} = 0, G_{i4} = 0 \\ S_X = 1\ G_{i1} = 0, G_{i2} = 1, G_{i3} = 1, G_{i4} = 0 \\ S_X = 0\ G_{i1} = 0, G_{i2} = 0, S_{i3} = 1, G_{i4} = 1. \end{cases} \tag{28}$$

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

The time-domain test of conventional and proposed solutions is carried out in the MATLAB/Simulink environment. The simulation parameters are listed in Table II, where the dc-bus voltage is 470 V. The capacitance and inductance of the Z-source network are 940 μF and 3 mH, respectively. The line–line voltage effective value of the grid is 380 V/50 Hz. The rated current is 10 A. The switching frequency is 10 kHz. The output filter inductor is 7 mH. The parasitic capacitor is 300 nF, and the shoot-through duty cycle is 0.2.

Fig. 9 shows the simulation results of the conventional solution. It observed that the output voltage of Z-source network is in accordance to the theoretical analysis in Section II. The line–line voltage shown in Fig. 9(b) is five level, while output current shown in Fig. 9(c) is sinusoidal. The THD of grid current in traditional schemes is 4.61%. Fig. 9(d) shows that the CMV varies during one switching period, as predicted in Fig. 6. Accordingly, there are high-frequency components in the parasitic capacitor

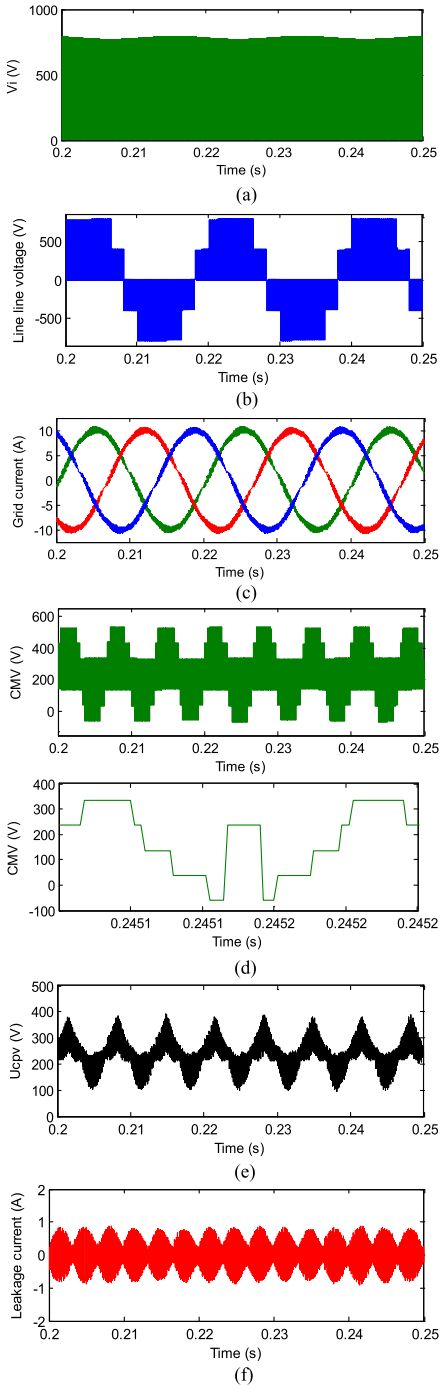

Fig. 9. Simulation results of conventional solution. (a) *Z*-source output voltage V_i. (b) Line–line voltage. (c) Grid current. (d) CMV. (e) Parasitic capacitor voltage U_{cpv}. (f) Leakage current.

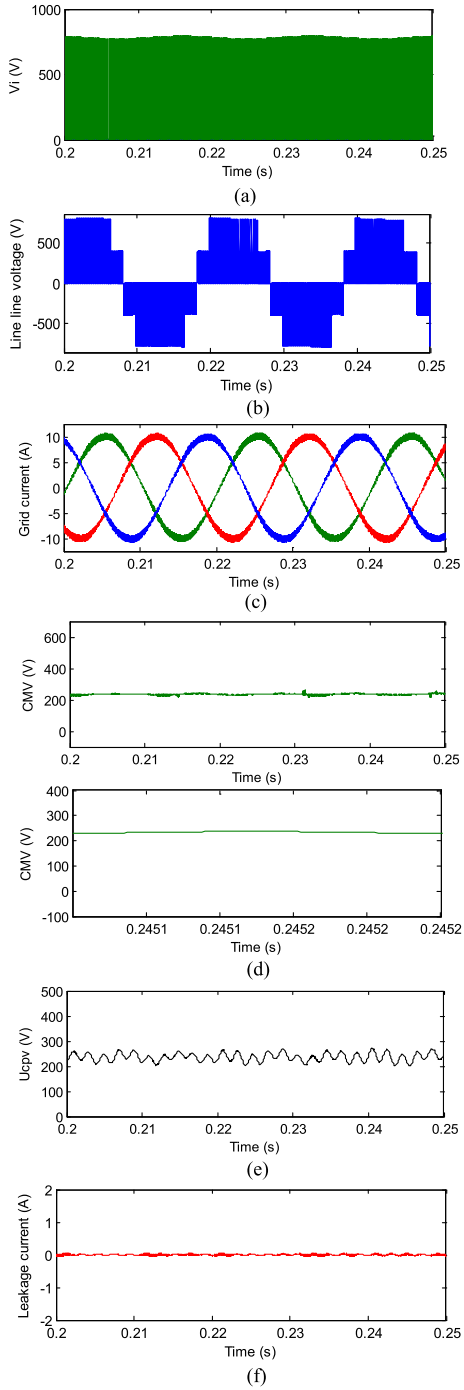

Fig. 10. Simulation results of the proposed solution. (a) *Z*-source output voltage V_i. (b) Line–line voltage. (c) Grid current. (d) CMV. (e) Parasitic capacitor voltage U_{cpv}. (f) Leakage current.

voltage shown in Fig. 9(e). Therefore, the leakage current cannot be effectively suppressed, as shown in Fig. 9(f), where the peak and rms values are 880 and 410 mA, respectively. It is far beyond 300 mA, which cannot meet VDE-0126-1-1 standard.

Fig. 10 shows the simulation results for the proposed solution. As predicted by (4), the output voltage of Z-source network is 780 V in the non-shoot-through state. The grid current is sinusoidal, and its THD is 4.38%. On the other hand, the CMV is constant, and the parasitic capacitor voltage is free of high-frequency components. Therefore, the leakage current is significantly reduced as shown in Fig. 10(f), where the peak and rms values are 54 and 17 mA, respectively. It is well below 300 mA, which complies with the VDE-0126-1-1.

The leakage current curve of simulation results with different parasitic capacitances for both the conventional and proposed modulations is shown in Fig. 11. The detailed data are listed in Table III, where I_{CM} is the leakage current, and C_{pv} is the parasitic capacitance. From Fig. 10 and Table III, it can be

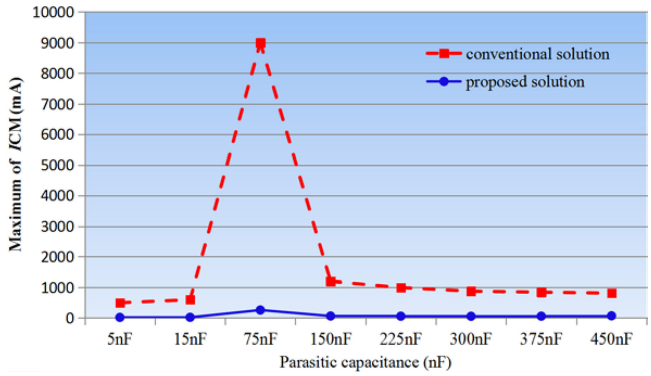

Fig. 11. Leakage current curve for a maximum value.

TABLE III
LEAKAGE CURRENT UNDER DIFFERENT PARASITIC CAPACITANCE

C_{pv}	maximum value of I_{CM}	
	conventional solution	Proposed solution
5 nF	500 mA	18 mA
15 nF	600 mA	20 mA
75 nF	9000 mA	260 mA
150 nF	1200 mA	63 mA
225 nF	1000 mA	57 mA
300 nF	880 mA	54 mA
375 nF	848 mA	58 mA
450 nF	815 mA	70 mA

observed the leakage current can be well attenuated with the proposed solution in case of different parasitic capacitances.

B. Experimental Results

This section will present the experimental evaluation of the conventional and proposed solutions. The control algorithm is implemented in a Texas Instruments TMS320F28335 DSP plus Xilinx XC3S400 FPGA digital platform. The details are shown in Fig. 8. The downscaled system parameters are listed in Table II, where the dc-bus voltage is 120 V. The grid voltage is 98/50 Hz. The rated current is 8 A. The rated power is 1 kW. The switching frequency is 10 kHz. The capacitance and inductance of the *Z*-source network are 940 μF and 3 mH, respectively. The output filter inductor is 5 mH. The parasitic capacitor is 300 nF, and shoot-through duty cycle is 0.2.

Fig. 12 shows the experimental results with traditional solution. Fig. 12(a) and (b) shows the output voltage waveform of the *Z*-source network and dc voltage, which shows that the output voltage V_i of the *Z*-source network is consistent with the theoretical analysis in Section II. Grid current and line–line voltage waveform are shown in Fig. 12(c) and (d), respectively, where the THD of grid current is 6.01%. The line–line voltage is five level. Fig. 12(e) and (f) shows the common-mode characteristics and leakage current waveforms. On the other hand, the CMV, as well as parasitic capacitor voltage is time-varying. Consequently, the leakage current is high as shown in Fig. 12(f), where the RMS and maximum value of the leakage current are 425 and 251 mA, respectively. It fails to comply with the VDE standard.

Fig. 13 shows the experimental results with the proposed solution. The grid current is sinusoidal, where the THD of grid

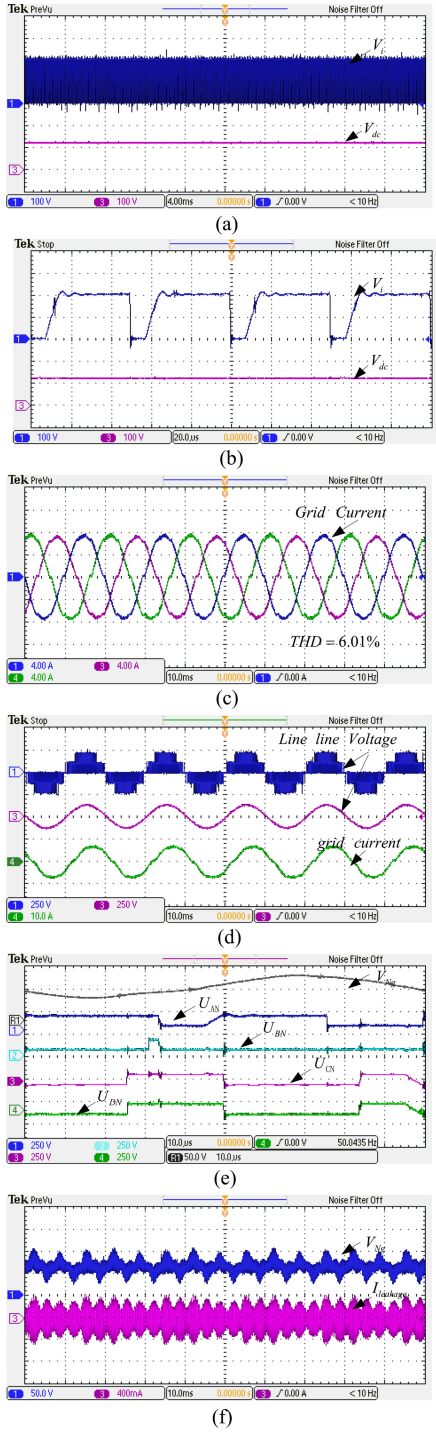

Fig. 12. Experimental results with traditional solution. (a) and (b) Output voltage of the *Z*-source network and dc voltage. (c) Output current. (d) Line–line voltage and output current. (e) Parasitic capacitor voltage and U_{AN}, U_{BN}, U_{CN}, and U_{DN}. (f) Parasitic capacitor voltage and leakage current.

current is 2.84%. On the other hand, with the proposed solution, the CMV is constant, and the parasitic capacitor voltage is free of high-frequency component. Therefore, the leakage current is well suppressed. The maximum value and rms value of leakage current are 102 and 28 mA, respectively, which meets the VDE 0126-01-01 standard.

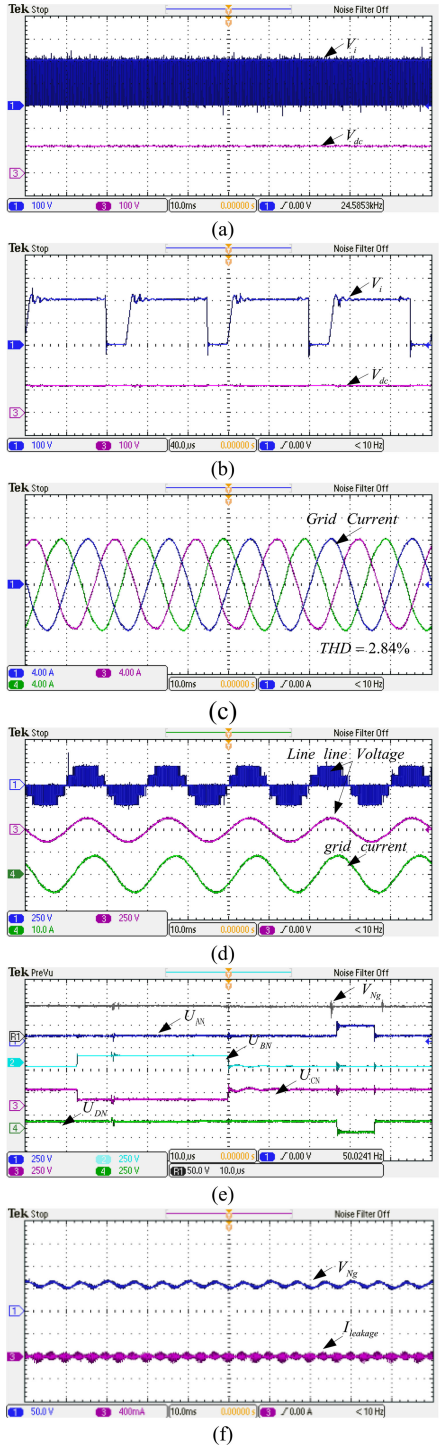

Fig. 13. Experimental results with the proposed solution. (a) and (b) Output voltage of the Z-source network and dc voltage. (c) Output current. (d) Line–line voltage and output current. (e) Parasitic capacitor voltage and U_{AN}, U_{BN}, U_{CN}, and U_{DN}. (f) Parasitic capacitor voltage and leakage current.

VI. Brief Comparison

This section will present the brief comparison of the existing solutions to ZSI for the leakage current reduction, where m is modulation index.

As shown in Table IV, it can be observed that the ZSI-S in [39] and ZSI in [40] have more switches (S) than ZSI-D in [38] and the proposed solution. The number of diodes (D), capacitors (C), and inductors (L) of ZSI-D in [38] is the same as that of the proposed solution. But the modulation index of ZSI-D in [38] is smaller than that of the proposed solution. Aside from that, the existing solutions in [38]–[40] are two-level topologies, while the proposed solution is three-level topology. Furthermore, only the proposed solution has unique features of fault-tolerance deal capability, which cannot be achieved with existing solutions in [38]–[40]. It should be noted that this paper mainly focuses on the leakage current reduction, and the relevant research of zero-sequence deal is ongoing, and a comprehensive analysis and test results would be reported in a future paper.

TABLE IV
Comparison of Recent Three-Phase ZSI for Leakage Current Suppression

	Z Source network				leg number	modulation index	voltage level	Fault tolerance capability
	S	D	C	L				
ZSI-D [38]	0	2	2	2	3	0<=m<=2/3	2	no
ZSI-S [39]	2	0	2	2	3	0<=m<=2/3	2	no
ZSI [40]	1	0	6	6	3	0<=m<=2/sqrt(3)	2	no
Proposed solution	0	2	2	2	4	0<=m<=2/sqrt(3)	3	yes

VII. Conclusion

This paper has presented the analysis and experimental verification of a new solution for the leakage current reduction of a *Z*-source three-level four-leg PV inverter. Different from the previous insights, our findings indicate that the parasitic capacitor voltage is dependent on not only the CMV, but also the switching states, more specifically, the coefficients of a and b in (16) and (20). And the conventional solution fails to eliminate the high-frequency components of the parasitic capacitor voltage, and thus the leakage current cannot be well suppressed. On the other hand, with the proposed solution, the parasitic capacitor voltage is free of high-frequency component. Consequently, the leakage current is effectively reduced. Also, the proposed solution is easy to implement in practice. Therefore, it is attractive for *Z*-source three-level four-leg PV inverters.

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