Interleaved High Step-Up Converter With Coupled Inductors

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***Abstract*—This paper proposes a new interleaved high step-up converter with coupled inductors. Interleaving configuration is employed at the input side to reduce the input current ripple and increase the power level. The series structure at the output side helps achieve a very high step-up voltage gain. Also, the proposed converter has very low switch voltage stress; thus, switching loss can be reduced and low-voltage-rating MOSFETs with small on resistance are allowed to lower the conduction loss. Due to the passive clamp performance, the leakage energy of the coupled inductors can be recycled and large voltage spikes across the switches are alleviated. Furthermore, with the aid of the leakage inductances, zero-current switching of the active switches can be achieved and the reverse recovery problem of the diodes is alleviated. The operating principles, performance analysis, and design considerations of the proposed converter are discussed. A prototype with 20-V input and 400-V output is built, and experimental results are provided to verify the theoretical analysis.**

***Index Terms*—Boost converter, coupled inductor, high step-up converter, high voltage gain, interleaved.**

I. Introduction

In RECENT years, high step-up dc/dc conversion has attracted substantial attention in many application areas, such as renewable energy systems, fuel cell systems, and uninterrupted power supplies [1], [2]. The conventional boost converter has limitations in high step-up applications because extreme duty cycle has to be used, which results in high voltage stress, high current ripple, and high switching and conduction losses [2]. This scenario has motivated extensive research activities and many high step-up converters have been reported in the literature.

In order to achieve large voltage gain, many high step-up converters with various boosting techniques have been proposed. In [3]–[12], switched-capacitor, switched-inductor or voltage-multiplier cells were utilized to extend the voltage gain. These converters can achieve high step-up conversion by adding a

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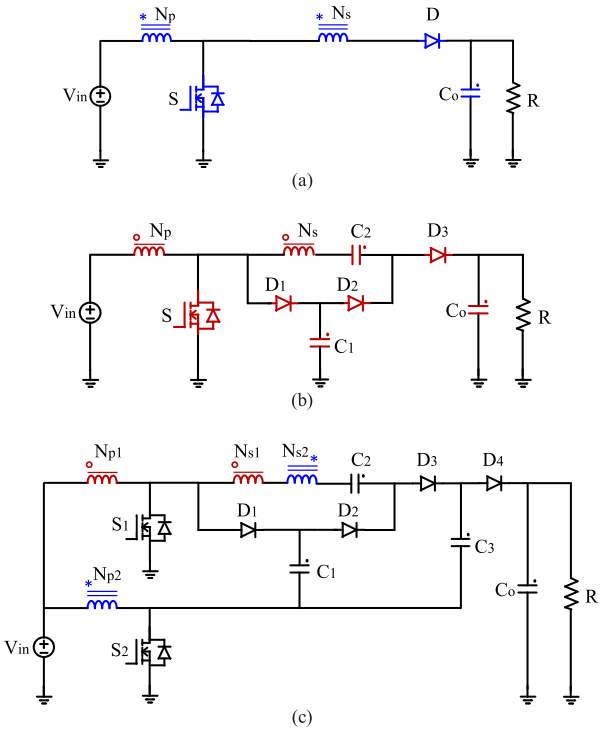

Fig. 1. Derivation of the proposed topology. (a) Conventional coupled-inductor boost converter [13]. (b) Coupled-inductor boost converter with passive regenerative snubber [15]. (c) Proposed interleaved high-step-up converter with coupled inductors.

two single-phase coupled-inductor converters. Fig. 1(a) shows the conventional coupled-inductor boost converter. Fig. 1(b) shows the coupled-inductor boost converter with a passive regenerative snubber. By paralleling the primary sides of the two converters and integrating the secondary sides, the proposed converter is derived as in Fig. 1(c). Due to the interleaved operation in the primary sides, the input current ripple is significantly reduced and the power level is increased. Due to the series structure in the secondary sides, a very high step-up voltage gain is achieved without extreme duty cycle or high turns ratio. Also, the proposed converter has very low switch voltage stress; hence, switching loss can be reduced and low-voltage-rating MOSFETs with small on resistance are allowed to lower the conduction loss. Moreover, the leakage energy can be recycled, which alleviates the large voltage spikes across the switches and improves the efficiency. Furthermore, with the aid of the leakage inductances, ZCS turn-ON of the switches is achieved and the reverse recovery problem of the diodes can be alleviated.

The rest of this paper is organized as follows. The operation principles of the proposed converter are described in Section II. Performance analysis is made in Section III. Design considerations are presented in Section IV. Experimental results are provided in Section V. Conclusions are given in Section VI.

II. Operation Principles

The proposed converter is composed of two coupled inductors, two switches S_1–S_2, four diodes D_1–D_4, three energy transfer capacitor C_1–C_3, and one output capacitor C_o. Fig. 2

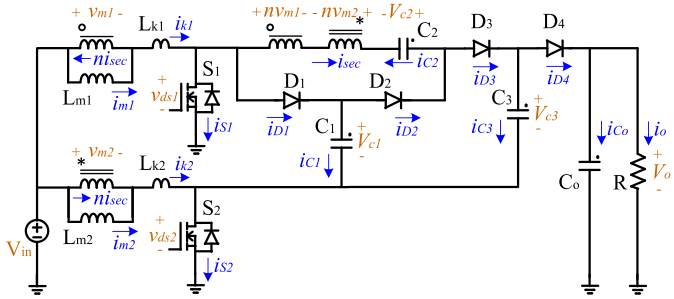

Fig. 2. Equivalent circuit of the proposed converter.

shows the equivalent circuit. Both coupled inductors are modeled as an ideal transformer with magnetizing inductance (L_{m1}, L_{m2}) and leakage inductance (L_{k1}, L_{k2}). The coupling references of the coupled inductors are denoted by "o" and "*". The two switches of the proposed converter are driven in an interleaved manner. The duty cycle D during steady state is larger than 0.5. In order to simplify analysis, the following assumptions are made.

1) All semiconductor devices are considered ideal.
2) All the capacitors are large enough so that the voltages across them are constant without voltage ripples.
3) The parameters of the two coupled inductors are assumed to be the same, i.e., $n = N_{s1}/N_{p1} = N_{s2}/N_{p2}$, $L_{m1} = L_{m2} = L_m$, and $L_{k1} = L_{k2} = L_k$.
4) The converter is operating in continuous conduction mode (CCM).

Fig. 3 shows the key waveforms of the proposed converter. Eight modes are observed during one switching period. The corresponding circuits for each mode are shown in Fig. 4.

Mode 1 $[t_0 - t_1]$: as shown in Fig. 4(a), S_1 and S_2 are ON, and all of the diodes are reverse-biased. The magnetizing inductors and leakage inductors are charged by the input source. Capacitors C_1–C_3 are floating. The output capacitor supplies the load current. As the leakage inductance is negligible compared to the magnetizing inductance, the following equations are obtained:

$$V_{\text{in}} = v_{m1} \tag{1}$$

$$V_{\text{in}} = v_{m2}. \tag{2}$$

Mode 2 $[t_1 - t_2]$: at t_1, S_1 is turned OFF, which makes diodes D_1 and D_3 turned ON, as shown in Fig. 4(b). L_{m2} and L_{k2} are being charged while L_{m1} and L_{k1} are releasing energy. The current through the secondary windings of the coupled inductors is increasing linearly. It discharges C_2 and charges C_3. The current through D_1 is decreasing linearly, which charges C_1. The equations in this mode can be obtained as follows:

$$V_{\text{in}} = v_{m1} + n\left(v_{m1} - v_{m2}\right) - V_{C2} + V_{C3} \tag{3}$$

$$V_{\text{in}} = v_{m2} \tag{4}$$

$$V_{C1} = n\left(v_{m1} - v_{m2}\right) - V_{C2} + V_{C3} \tag{5}$$

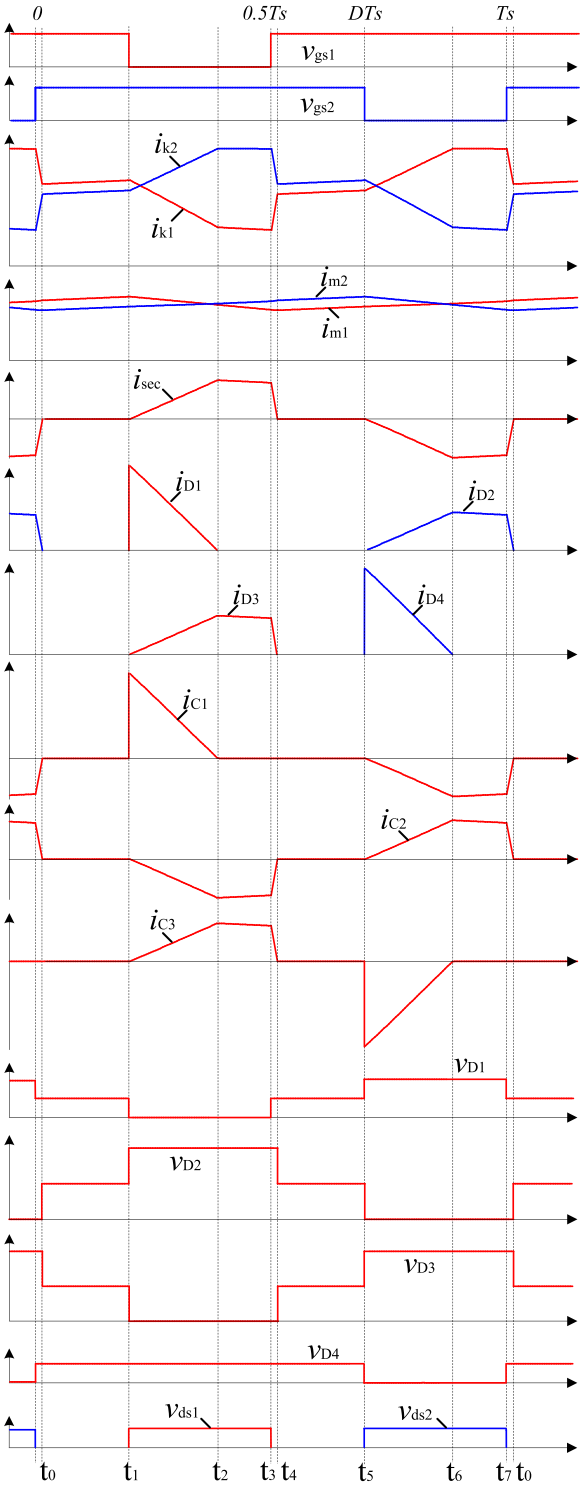

Fig. 3. Key waveforms of the proposed converter.

$$i_{\text{sec}}\ (t) = i_{D3}\ \ (t) = \frac{(n+1)\,V_{C1} + V_{C2} - V_{C3}}{n^2\,(L_{k1}+L_{k2})}\ \ (t-t_1) \tag{6}$$

$$i_{k1}\ (t) = i_{m1}\ \ (t) - n i_{\text{sec}}\ (t) \tag{7}$$

$$i_{k2}\ (t) = i_{m2}\ \ (t) + n i_{\text{sec}}\ (t) \tag{8}$$

$$i_{D1}\ (t) = i_{k1}\ \ (t) - i_{\text{sec}}\ \ (t) = i_{m1}\ \ (t) - (n+1)\,i_{\text{sec}}\ (t)\,. \tag{9}$$

Solving (3) and (4), v_{m1} can be expressed as

$$v_{m1} = V_{\text{in}} + \frac{V_{C2} - V_{C3}}{n+1}. \tag{10}$$

Mode 3 $[t_2 - t_3]$*:* at t_2, the current through D_1 becomes zero and turns OFF naturally. Thus, there is no reverse recovery problem for D_1. As shown in Fig. 4(c), the current of L_{k1} becomes equal to the current through the secondary windings of the coupled inductors. C_2 is discharged and C_3 is charged. C_1 becomes floating. Equations (3), (4), (7), (8), and (10) still hold, and the following equation is obtained:

$$i_{k1}\ \ (t) = i_{m1}\ \ (t) - n i_{\text{sec}}\ \ (t) = i_{\text{sec}}\ \ (t)\,. \tag{11}$$

Then

$$i_{\text{sec}}\ \ (t) = i_{D3}\ \ \ (t) = i_{k1}\ \ \ (t) = \frac{1}{n+1}\,i_{m1}\,(t)\,. \tag{12}$$

Mode 4 $[t_3 - t_4]$*:* at t_3, S_1 is turned ON. Due to the presence of the leakage inductances, ZCS of S_1 can be achieved. The current of D_3 starts decreasing, and the falling rate is determined by the leakage inductances, which alleviates the reverse recovery problem of D_3. The falling rate of D_3 can be expressed by

$$\frac{di_{D3}\,(t)}{dt} = -\frac{V_{C3} - V_{C2}}{n^2\,(L_{k1}+L_{k2})}. \tag{13}$$

Mode 5 $[t_4 - t_5]$*:* at t_4, the current of D_3 decreases to zero, and D_3 is turned OFF. This mode repeats Mode 1.

Mode 6 $[t_5 - t_6]$*:* at t_5, S_2 is turned OFF, which makes diodes D_2 and D_4 turned ON, as shown in Fig. 4(f). L_{m1} and L_{k1} are being charged while L_{m2} and L_{k2} are releasing energy. The current through the secondary windings of the coupled inductors is increasing linearly in the opposite direction. It discharges C_1 and charges C_2. The current through D_4 is decreasing linearly. C_3 serves as a voltage source to extend the voltage gain. The equations in this mode can be obtained as follows:

$$V_{\text{in}} = v_{m1} \tag{14}$$

$$V_{\text{in}} = v_{m2} - V_{C1} + V_{C2} + n\,(v_{m2} - v_{m1}) \tag{15}$$

$$V_{\text{in}} = v_{m2} - V_{C3} + V_O \tag{16}$$

$$i_{\text{sec}}\ \ (t) = -i_{D2}\ \ \ (t) = \frac{-(n+1)\,(V_O - V_{C3}) + V_{C2} - V_{C1}}{n^2\,(L_{k1}+L_{k2})}\ \ (t-t_5) \tag{17}$$

$$i_{k1}\ \ (t) = i_{m1}\ \ (t) - n i_{\text{sec}}\,(t) \tag{18}$$

$$i_{k2}\ \ (t) = i_{m2}\ \ (t) + n i_{\text{sec}}\,(t) \tag{19}$$

$$i_{D4}\ \ (t) = i_{k2}\ \ (t) + i_{\text{sec}}\ \ (t) = i_{m2}\ \ (t) + (n+1)\,i_{\text{sec}}\,(t)\,. \tag{20}$$

Solving (14) and (15), v_{m2} can be expressed as

$$v_{m2} = V_{\text{in}} + \frac{V_{C1} - V_{C2}}{n+1}. \tag{21}$$

Mode 7 $[t_6 - t_7]$*:* at t_6, the current through D_4 becomes zero and turns OFF naturally. Thus, there is no reverse recovery problem for D_4. The current of L_{k2} becomes equal to the current through the secondary windings of the coupled inductors, as

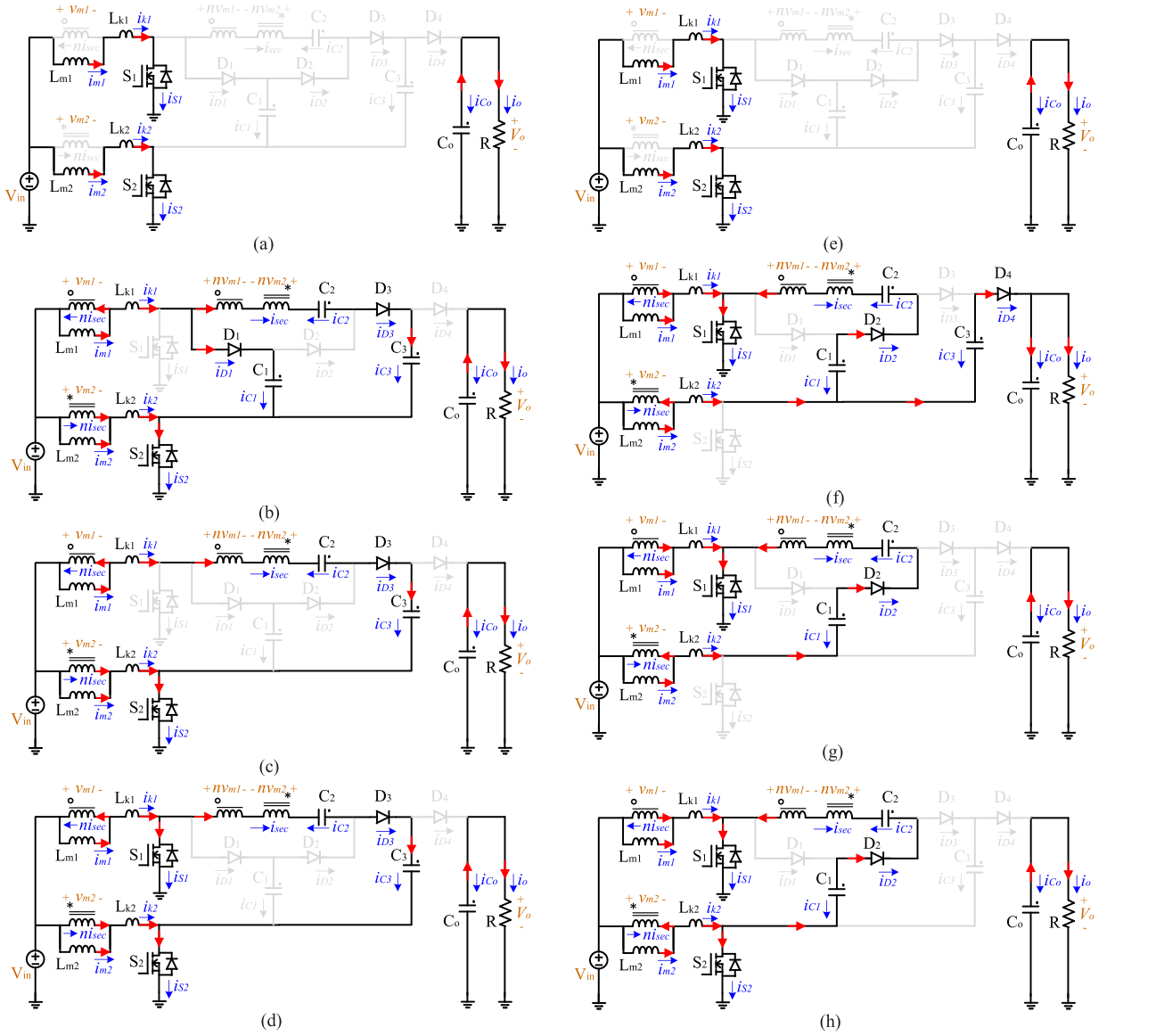

Fig. 4. Operation modes of the proposed converter. (a) Mode 1 $[t_0 - t_1]$. (b) Mode 2 $[t_1 - t_2]$. (c) Mode 3 $[t_2 - t_3]$. (d) Mode 4 $[t_3 - t_4]$. (e) Mode 5 $[t_4 - t_5]$. (f) Mode 6 $[t_5 - t_6]$. (g) Mode 7 $[t_6 - t_7]$. (h) Mode 8 $[t_7 - t_0]$.

shown in Fig. 4(g). C_1 is discharged and C_2 is charged. Equations (14), (15), (18), (19), and (21) still hold, and the following equation is obtained:

$$i_{k2}\ (t) = i_{m2}\ (t) + n i_{\rm sec}\ (t) = -i_{\rm sec}\ (t)\,. \tag{22}$$

Then

$$i_{\rm sec}\ (t) = -i_{D2}\ \ (t) = -i_{k2}\ \ (t) = -\frac{1}{n+1} i_{m2}\,(t)\,. \tag{23}$$

Mode 8 $[t_7 - t_0]$*:* at t_7, S_2 is turned ON. Due to the presence of the leakage inductances, ZCS of S_2 can be achieved. The current of D_2 starts decreasing, and the falling rate is determined by the leakage inductances, which alleviates the reverse recovery problem of D_2. The falling rate of D_2 can be expressed by

$$\frac{di_{D2}\,(t)}{dt} = -\frac{V_{C2} - V_{C1}}{n^2\,(L_{k1} + L_{k2})}. \tag{24}$$

III. Performance Analysis

A. Voltage Gain

By applying the voltage–second balance principle to L_{m1} and L_{m2}, the following equations are obtained:

$$V_{\rm in} D + \left(V_{\rm in} + \frac{V_{C2} - V_{C3}}{n+1}\right)(1 - D) = 0 \tag{25}$$

$$V_{\rm in} D + \left(V_{\rm in} + \frac{V_{C1} - V_{C2}}{n+1}\right)(1 - D) = 0. \tag{26}$$

Based on (3)–(5), the following equation is derived:

$$(n+1)\,V_{C1} + V_{C2} - V_{C3} = 0. \tag{27}$$

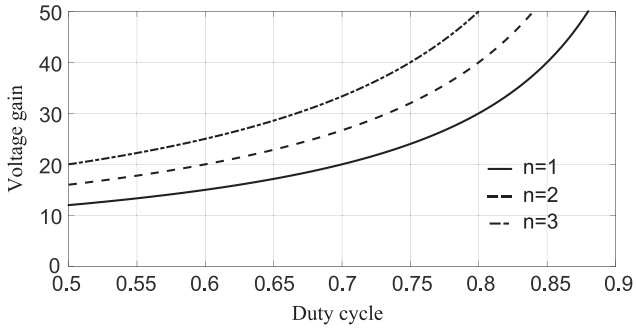

Fig. 5. Voltage gain versus duty cycle under different turns ratios.

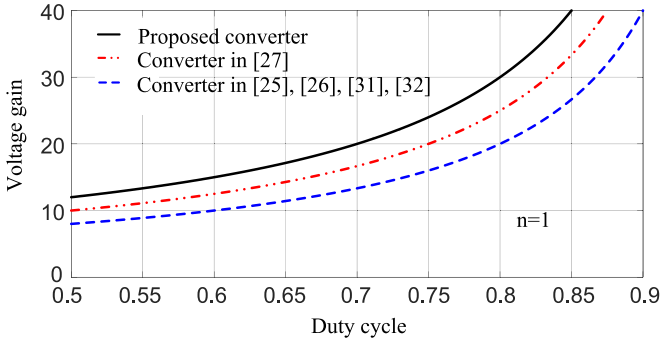

Fig. 6. Comparison of the voltage gain when $n = 1$.

Solving (25)–(27), the capacitor voltages are derived as

$$V_{C1} = \frac{V_{\text{in}}}{1-D} \tag{28}$$

$$V_{C2} = \frac{(n+2)\,V_{\text{in}}}{1-D} \tag{29}$$

$$V_{C3} = \frac{(2n+3)\,V_{\text{in}}}{1-D}. \tag{30}$$

Based on (14)–(16), the following equation is derived:

$$(n+1)\,(V_o - V_{C3}) - V_{C2} + V_{C1} = 0. \tag{31}$$

Substitute (28)–(30) into (31), the voltage gain is derived as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{2n+4}{1-D}. \tag{32}$$

Fig. 5 shows the curves of the voltage gain versus duty cycle under different turns ratios. It is clear that the proposed converter has a high step-up voltage gain without extreme duty cycle or high turns ratio. Fig. 6 gives the voltage gain of the proposed converter compared with other interleaved coupled-inductor converters in [25]–[27], [31], and [32]. It is shown that the voltage gain of the proposed converter is higher.

B. Voltage Stress

The voltage stresses of the capacitors are given by (28)–(30). The voltage stresses of the switches are obtained as

$$V_{S1} = V_{S2} = \frac{V_{\text{in}}}{1-D} = \frac{1}{2n+4}\,V_o. \tag{33}$$

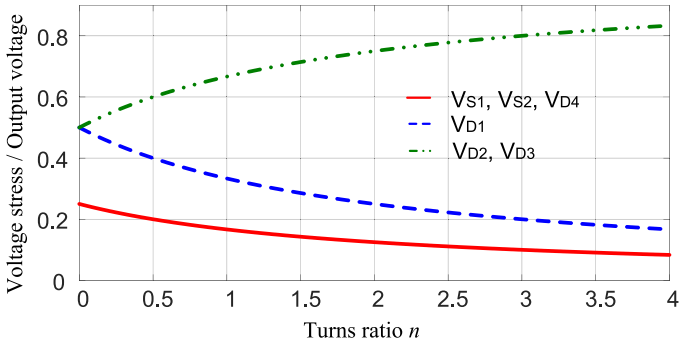

Fig. 7. Normalized semiconductor voltage stress versus turns ratios.

It can be seen that the voltage stress of the switches is much lower than the output voltage. The low voltage stress results in low switching loss. Furthermore, low-voltage-rating MOSFETs with small on resistance can be used, which leads to low conduction loss.

According to Mode 6 in Fig. 4(f), the voltage stresses of D_1 and D_3 are derived as follows:

$$V_{D1} = V_{C1} - V_{C3} + V_o = \frac{2}{1-D}\;V_{\text{in}} = \frac{1}{n+2}\,V_o \tag{34}$$

$$V_{D3} = V_{C3} - V_{C1} = \frac{2n+2}{1-D}\;V_{\text{in}} = \frac{n+1}{n+2}\,V_o. \tag{35}$$

According to Mode 2 in Fig. 4(b), the voltage stresses of D_2 and D_4 are derived as follows:

$$V_{D2} = V_{C3} - V_{C1} = \frac{2n+2}{1-D}\;V_{\text{in}} = \frac{n+1}{n+2}\,V_o \tag{36}$$

$$V_{D4} = V_o - V_{C3} = \frac{1}{1-D}\;V_{\text{in}} = \frac{1}{2n+4}\,V_o. \tag{37}$$

The normalized voltage stresses on all switches and diodes with different turns ratios are shown in Fig. 7. It can be seen that the switch voltage stress becomes lower as the voltage gain is extended by increasing the turns ratio. The voltage stresses on D_1 and D_4 also decrease as the turns ratio increases. The voltage stresses on D_2 and D_3 increase as the turns ratio increases, but they are always lower than the output voltage.

C. Current Stress

In order to simplify the calculation, the magnetizing currents are assumed as I_{m1} and I_{m2} by applying small-ripple approximation. Let $t_2 - t_1 = D_a\,T_s$ and $t_6 - t_5 = D_b\,T_s$. Then, according to the charge balance of capacitor C_1–C_3, the following equations are obtained:

$$\frac{1}{2}I_{m1}\,D_a = \frac{1}{2}\cdot\frac{I_{m2}}{n+1}D_b + \frac{I_{m2}}{n+1}\,(1-D-D_b) \tag{38}$$

$$\frac{1}{2}\cdot\frac{I_{m1}}{n+1}D_a + \frac{I_{m1}}{n+1}(1-D-D_a) = \frac{1}{2}\cdot\frac{I_{m2}}{n+1}D_b + \frac{I_{m2}}{n+1}(1-D-D_b) \tag{39}$$

$$\frac{1}{2}\cdot\frac{I_{m1}}{n+1}D_a + \frac{I_{m1}}{n+1}(1-D-D_a) = \frac{1}{2}\,I_{m2}D_b. \tag{40}$$

Solving (38)–(40), the following relationships are derived:

$$I_{m1} = I_{m2} \tag{41}$$

$$D_a = D_b = \frac{2}{n+2}\,(1-D)\,. \tag{42}$$

It can be seen that the magnetizing currents of the two coupled inductors are balanced due to the charge balance of the capacitors.

Assume $I_{m1} = I_{m2} = I_m$. Based on the charge balance of the output capacitor, the following equation is obtained:

$$\left(\frac{1}{2}I_m - I_o\right)\,D_b = I_o\,(1-D_b)\,. \tag{43}$$

Solving (42) and (43), the magnetizing current is derived as

$$I_m = \frac{n+2}{1-D}\,I_o. \tag{44}$$

According to the operating principle, the average currents flowing through the diodes are equal to the output current, which is given by

$$I_{D1\_\mathrm{avg}} = I_{D2\_\mathrm{avg}} = I_{D3_{\mathrm{avg}}} = I_{D4\_\mathrm{avg}} = I_o. \tag{45}$$

From the steady-state analysis, the RMS current stresses on the switches are expressed as

$$I_{S1\_\mathrm{RMS}} = \frac{n+2}{1-D}\,I_o\sqrt{3-2D-(1-D)\,\frac{10}{3\,(n+2)}} \tag{46}$$

$$I_{S2\_\mathrm{RMS}} = \frac{n+2}{1-D}\,I_o\sqrt{3-2D}. \tag{47}$$

The peak currents of the coupled inductors are derived as

$$I_{k1\_\mathrm{pk}} = I_{k2\_\mathrm{pk}} = I_{m2} + n\cdot\,\frac{I_{m2}}{n+1} = \frac{(2n+1)\,(n+2)}{(n+1)\,(1-D)}\,I_o. \tag{48}$$

The RMS currents of the primary windings of the coupled inductors are given by

$$I_{k1\_\mathrm{RMS}} = I_{k2\_\mathrm{RMS}} = I_{k\_\mathrm{RMS}} = \frac{n+2}{1-D}\,I_o \times\sqrt{2D-1+(1-D)\,\frac{4n^3+\frac{28}{3}n^2+10n+4}{(n+2)\,(n+1)^2}}. \tag{49}$$

The RMS current of the secondary windings of the coupled inductors is given by

$$I_{\mathrm{sec}\_\mathrm{RMS}} = \frac{n+2}{1-D}\,I_o\sqrt{(1-D)\,\frac{\frac{4}{3}+2n}{(n+2)\,(n+1)^2}}. \tag{50}$$

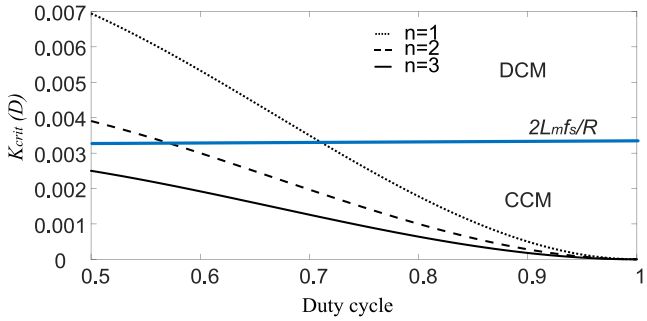

Fig. 8. Boundary condition: K_{crit} versus D.

The RMS currents of the capacitors are given by

$$I_{C1\_\mathrm{RMS}} = I_{C3\_\mathrm{RMS}} = \frac{n+2}{1-D}\,I_o\sqrt{(1-D)\,\frac{2n^2+7n+4}{3\,(n+2)\,(n+1)^2}} \tag{51}$$

$$I_{C2\_\mathrm{RMS}} = \frac{n+2}{1-D}\,I_o\sqrt{(1-D)\,\frac{\frac{4}{3}+2n}{(n+2)\,(n+1)^2}} \tag{52}$$

$$I_{Co\_\mathrm{RMS}} = I_o\,\sqrt{\frac{2\,(n+2)}{3\,(1-D)}-1}. \tag{53}$$

D. Boundary Condition

The aforementioned analysis is under CCM. The condition for CCM is given by

$$I_m > \frac{V_{\mathrm{in}}D}{2L_m f_s}. \tag{54}$$

Substitute (32) and (44) into (54), the following criteria can be obtained:

$$\frac{2L_m f_s}{R} > \frac{D(1-D)^2}{2(n+2)^2} = K_{\mathrm{crit}}\,(D)\,. \tag{55}$$

The curves of $K_{\mathrm{crit}}(D)$ with different turns ratio are shown in Fig. 8. It can be seen that when the turns ratio increases, it is easier to achieve CCM condition.

E. Comparison

In this section, the proposed converter is compared with other interleaved coupled-inductor-based converters in the literature. All these converters use two switches, employ an interleaved operation, have a common ground connection between the input and output, and can be used in high step-up applications. The voltage gain, voltage stresses of the switches and diodes, and the component counts are listed in Table I.

As can be seen, the proposed converter achieves higher voltage gain compared to the other converters. Therefore, the proposed converter is more suitable for high step-up applications. Also, the proposed converter has minimum component count, indicating low cost. Furthermore, the proposed converter has a lower switch voltage stress. As a result, switching loss can be reduced and low-voltage-rating MOSFET with small on resistance can be used to lower conduction loss.

TABLE I
COMPARISON OF THE PROPOSED CONVERTER TO SIMILAR CONVERTERS

Topologies	Proposed	Ref. [25]	Ref. [26]	Ref. [27]	Ref. [31]	Ref. [32]
Voltage gain	$\frac{2n+4}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+3}{1-D}$	$\frac{2n+2}{1-D}$	$\frac{2n+2}{1-D}$
Switch voltage stress	$\frac{V_o}{2n+4}$	$\frac{V_o}{2n+2}$	$\frac{V_o}{2n+2}$	$\frac{V_o}{2n+3}$	$\frac{V_o}{2n+2}$	$\frac{V_o}{2n+2}$
Maximum diode voltage stress	$\frac{n+1}{n+2}V_o$	$\frac{2n}{2n+2}V_o$	$\frac{2n}{2n+2}V_o$	$\frac{2n+1}{2n+3}V_o$	$\frac{2n+1}{2n+2}V_o$	$\frac{2n+1}{2n+2}V_o$
No. of switches	2	2	2	2	2	2
No. of diodes	4	4	6	4	6	6
No. of magnetic cores	2	2	2	2	2	2
No. of windings	4	4	4	4	6	6
No. of capacitors	4	4	5	4	5	5

IV. DESIGN CONSIDERATIONS

A. Coupled-Inductor Design

The turns ratio of the coupled inductors is determined by the required voltage gain and the duty cycle. It is calculated by

$$n = \frac{V_o}{V_{\text{in}}} \cdot \frac{1-D}{2} - 2. \tag{56}$$

According to the aforementioned analysis, the proposed converter operates in CCM. The magnetizing inductances of the coupled inductors can be designed based on the ripple of the magnetizing current. Considering a peak-to-peak current ripple of $\gamma\%$, the magnetizing inductance can be calculated as

$$L_m = L_{m1} = L_{m2} = \frac{V_{\text{in}} D}{\gamma\% I_m f_s} = \frac{V_{\text{in}} D\left(1-D\right)}{\gamma\%\left(n+2\right) I_o f_s}. \tag{57}$$

As seen from the operating principle and waveforms, the leakage inductances of the coupled inductors help to limit the current falling rate of D_2 and D_3 and thus alleviate the diode reverse recovery problem. Therefore, the leakage inductances can be designed based on the current falling rate of the diodes, which are given by

$$L_k = L_{k1} = L_{k2} = \frac{\left(n+1\right) V_o}{4n^2\left(n+2\right)\frac{di_{D2}}{dt}} = \frac{\left(n+1\right) V_o}{4n^2\left(n+2\right)\frac{di_{D3}}{dt}}. \tag{58}$$

The peak currents of the coupled inductors can be calculated from (48). The RMS currents of the primary and secondary windings can be calculated from (49) and (50).

B. Semiconductor Selection

The switches and diodes are selected according to their voltage and current stresses. The voltage stresses of the switches and diodes are given by (33)–(37). The current stresses of the switches and diodes are given by (45)–(47). In practice, considering the voltage overshoot and ringing, the voltage rating of the switches and diodes should be higher than the calculated values.

C. Capacitor Design

The capacitors can be designed based on the voltage ripple and the output power. Assuming that the voltage ripple is $r\%$ and the output power is P_o, the capacitances can be calculated by

$$C_1 > \frac{I_o}{\Delta V_{c1} f_s} = \frac{P_o}{r\% V_{c1} f_s V_o} = \frac{\left(2n+4\right) P_o}{r\% {V_o}^2 f_s} \tag{59}$$

$$C_2 > \frac{I_o}{\Delta V_{c2} f_s} = \frac{P_o}{r\% V_{c2} f_s V_o} = \frac{2P_o}{r\% {V_o}^2 f_s} \tag{60}$$

$$C_3 > \frac{I_o}{\Delta V_{c3} f_s} = \frac{P_o}{r\% V_{c3} f_s V_o} = \frac{\left(2n+4\right) P_o}{\left(2n+3\right) r\% {V_o}^2 f_s} \tag{61}$$

$$C_o > \frac{\left(1-\frac{2}{n+2}\left(1-D\right)\right) I_o}{\Delta V_o f_s} = \frac{\left(n+2D\right) P_o}{\left(n+2\right) r\% {V_o}^2 f_s}. \tag{62}$$

In the proposed converter, the energy transfer capacitors C_1–C_3 are used as dc capacitors to transfer energy from the input to the output. The capacitors may form resonant tanks with the leakage inductances if the capacitances are small. In the design, the capacitors should be selected large enough so that the resonant frequencies are much higher than the switching frequency.

V. EXPERIMENTAL RESULTS

In order to verify the performance of the proposed converter, a 330-W 20-V-input 400-V-output prototype is built and tested. The switching frequency is set to 50 kHz. Both duty cycles of the switches are around 0.7. The key parameters of the prototype are listed as in Table II.

A. Experimental Waveforms

Fig. 9 shows the gate signals and the drain-to-source voltages of the switches at full load. It can be seen that extreme duty cycle is avoided. The voltage stress of the switches is around 68 V, which matches the calculation from (33). Thus, low-voltage-

TABLE II
KEY PARAMETERS OF THE PROTOTYPE

Components	PARAMETERS
Switches S_1-S_2	IPA075N15N3 (150 V, 7.5 mΩ)
Diodes D_1, D_4	STPS20200CT (200 V)
Diodes D_2, D_3	MUR1640CT (400 V)
Coupled inductors	Turns ratio = 1:1 Magnetizing inductance = 102 uH Leakage inductance = 3.6 uH
Capacitor C_1	B32526T3226 (22 uF)
Capacitor C_2, C_3	B32526T6825 (8.2 uF)
Capacitor C_o	56 uF electrolytic capacitor

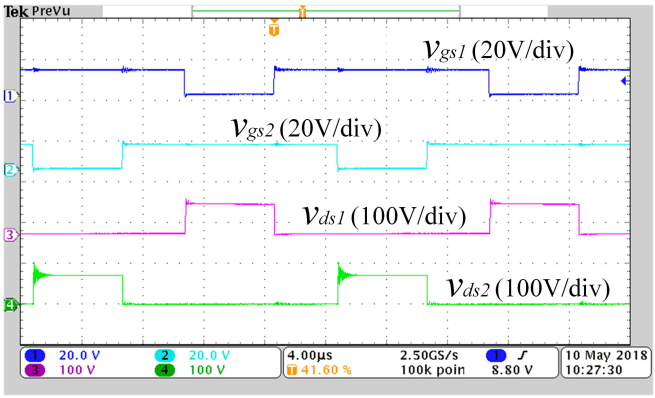

Fig. 9. Gate signals and drain-to-source voltages.

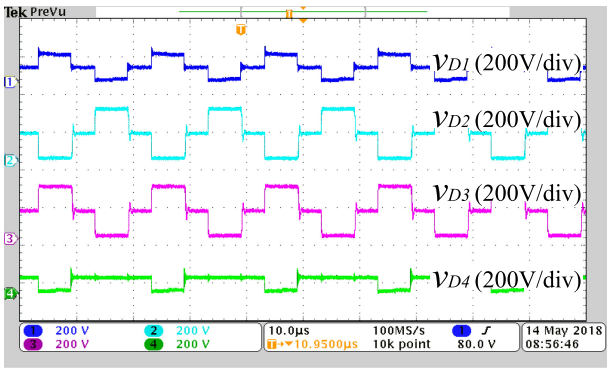

Fig. 10. Voltages across the diodes.

rating MOSFETs with low on resistance can be used to lower conduction loss. Fig. 10 shows the diode voltages v_{D1}–v_{D4}. It can be seen that the waveforms are consistent with the theoretical analysis. The blocking voltages of D_1 and D_4 are around 136 and 68 V, respectively, and the blocking voltages of D_2 and D_3 are around 266 V, which agree well with the calculations from (34)–(37). Fig. 11 shows the input voltage and output voltage waveforms. As can be seen, the input voltage is 20 V and the output voltage is 400 V when the turns ratio is 1, which indicates that high voltage gain is achieved. Fig. 12 shows the capacitor voltages. It is clear that the voltages of C_1, C_2, and C_3 are around 66, 200, and 330 V, respectively, which match the calculations from (28)–(30).

Fig. 13 shows the primary currents of the coupled inductors and the input current. As can be seen, interleaved feature

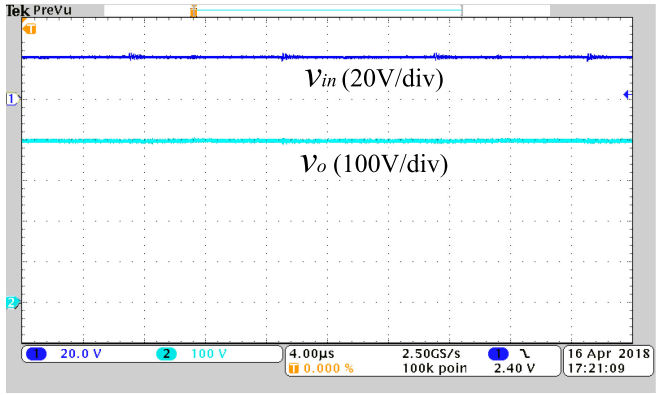

Fig. 11. Input and output voltages.

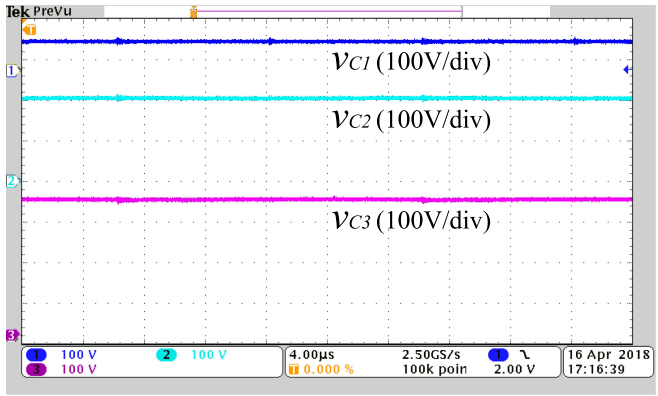

Fig. 12. Capacitor voltages.

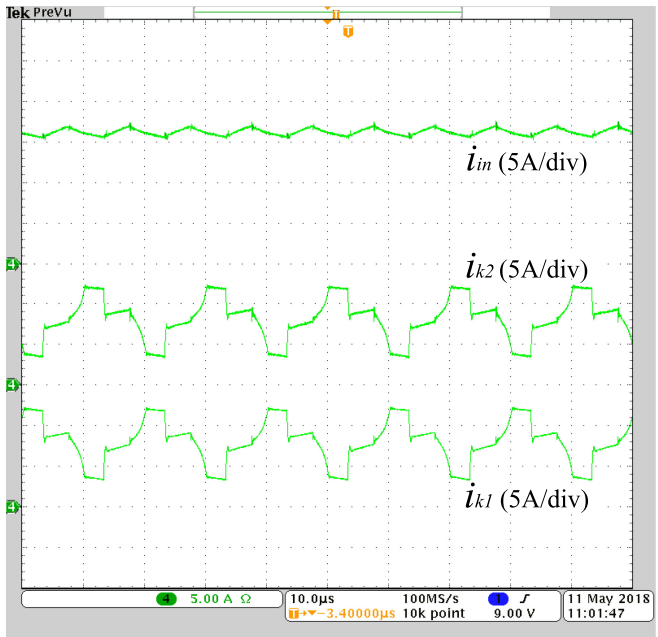

Fig. 13. Primary currents of the coupled inductors and the input current.

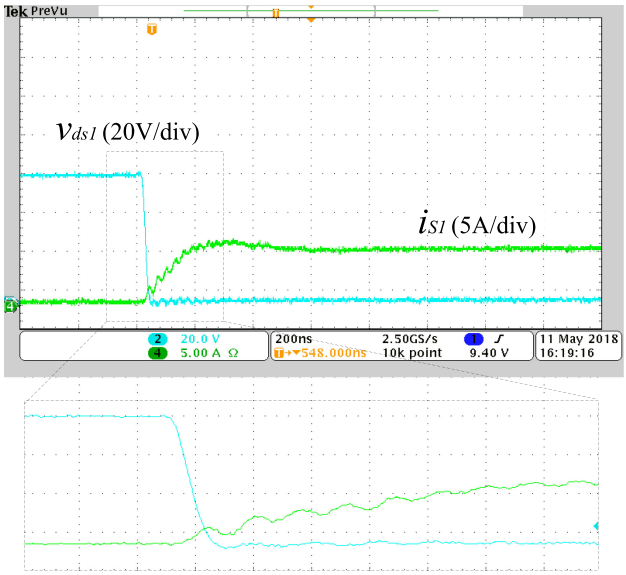

Fig. 14. Current and voltage of switch S_1 at the turn-ON transition.

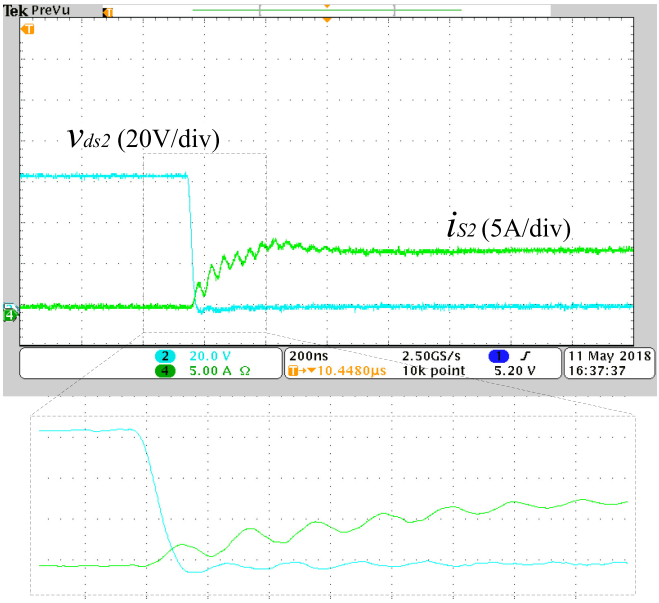

Fig. 15. Current and voltage of switch S_2 at the turn-ON transition.

is achieved. Therefore, the input current ripple is significantly reduced. The measured waveforms of i_{k1} and i_{k2} are slightly different from the theoretical waveforms in Fig. 3. This is caused by the effect of the magnetizing current ripples and the resonance between the leakage inductances and the energy transfer capacitors. Fig. 14 shows the current and voltage of switch S_1 at the turn-ON transition. Fig. 15 shows the current and voltage of switch S_2 at the turn-ON transition. As the leakage inductances limit the current changing rate, the switch currents rise gradually when the switches are turned ON, which help reduce the switching loss greatly. Fig. 16 shows the currents through the diodes. It can be seen that all diodes are turned OFF naturally, and the reverse recovery currents of the diodes are greatly reduced.

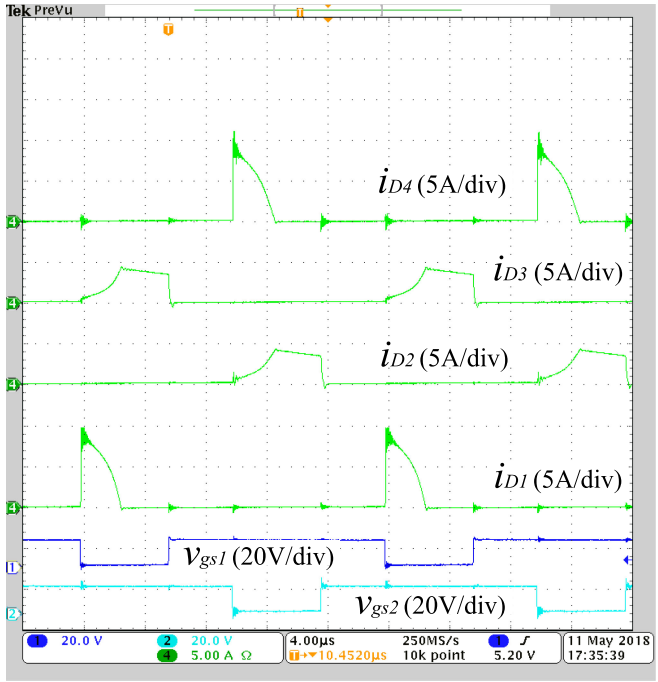

Fig. 16. Currents through the diodes.

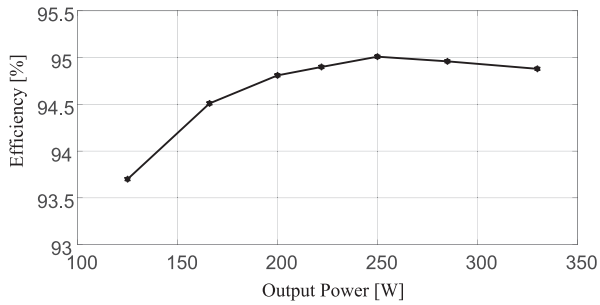

Fig. 17. Measured efficiency versus output power.

The measured waveforms of i_{D1}–i_{D4} are slightly different from the theoretical waveforms in Fig. 3. This is because the leakage inductances resonate with the energy transfer capacitors during Modes 2 and 6.

Table III shows the comparison of the calculated, simulated, and experimentally measured current values at the full load. As can be seen, they are in good agreement. The discrepancy is caused by the effect of the parasitic elements, the small ripple approximation, and the measurement error.

B. *Efficiency and Loss Analysis*

Digital power meter Chroma 66202 is used to measure the efficiency of the prototype. The efficiency versus output power is shown in Fig. 17. The peak efficiency is 95.01%, which is achieved at 250-W output power. The efficiency at full load is measured as 94.88%.

Power losses of the proposed converter include losses of the coupled inductors, switches, diodes and capacitors.

TABLE III
COMPARISON OF THE CALCULATED, SIMULATED, AND EXPERIMENTALLY MEASURED CURRENT VALUES

Current (A)	I_{D1_avg}	I_{D2_avg}	I_{D3_avg}	I_{D4_avg}	I_{S1_RMS}	I_{S2_RMS}	I_{k1_RMS}	I_{k2_RMS}	I_{sec_RMS}
Calculated	0.82	0.82	0.82	0.82	9.28	10.43	8.58	8.58	2.38
Simulated	0.83	0.82	0.82	0.83	9.08	10.24	8.45	8.45	2.31
Experimental	0.86	0.84	0.84	0.87	10.16	11.38	9.34	9.40	2.96

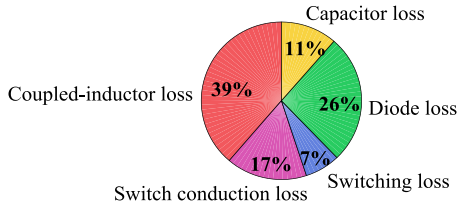

Fig. 18. Loss breakdown of the prototype.

The conduction loss in the coupled inductors is calculated by

$$P_{CI} = 2{I_{k\_\mathrm{RMS}}}^2 r_{\mathrm{pri}} + 2{I_{\mathrm{sec}\_\mathrm{RMS}}}^2 r_{\mathrm{sec}} \tag{63}$$

where r_{pri} is the resistance of the primary windings of the coupled inductor and r_{sec} the resistance of the secondary windings. I_{k_RMS} and $I_{\mathrm{sec}\_\mathrm{RMS}}$ can be calculated from (49) and (50).

The loss of the switches includes both conduction loss and switching loss. The conduction loss of the switches is calculated as

$$P_{S\_\mathrm{Cond}} = {I_{S1\_\mathrm{RMS}}}^2 r_{\mathrm{ds}} + {I_{S2\_\mathrm{RMS}}}^2 r_{\mathrm{ds}} \tag{64}$$

where r_{ds} is the on resistance of the MOSFETs. I_{S1_RMS} and I_{S2_RMS} can be calculated from (46) and (47).

As the switches are turned ON with ZCS, the switching loss of the switches is calculated as

$$P_{S\_\mathrm{SW}} = 2\left(\frac{1}{2} I_m V_{S1} t_f f_s + \frac{1}{2} {V_{S1}}^2 C_{\mathrm{oss}} f_s\right) \tag{65}$$

where t_f is the fall time of the MOSFETs and C_{oss} is the parasitic output capacitance.

The conduction loss of the diodes is calculated as

$$P_D = I_o \left(V_{F1} + V_{F2} + V_{F3} + V_{F4}\right) \tag{66}$$

where V_{Fx} is the forward voltage drop of diode D_x.

The conduction loss of the capacitors is calculated as

$$P_C = {I_{C1\_\mathrm{RMS}}}^2 r_{C1} + {I_{C2\_\mathrm{RMS}}}^2 r_{C2} + {I_{C3\_\mathrm{RMS}}}^2 r_{C3} + {I_{Co\_\mathrm{RMS}}}^2 r_{Co} \tag{67}$$

where r_{Cx} is the equivalent series resistance of capacitor C_x. I_{Cx_RMS} can be calculated from (51)–(53).

Then, the total power loss of the proposed converter is given by

$$P_{\mathrm{Loss}} = P_{CI} + P_{S\_\mathrm{Cond}} + P_{S\_\mathrm{SW}} + P_D + P_C. \tag{68}$$

Based on the selected components of the hardware prototype, the loss breakdown of the proposed converter at full load is performed and shown in Fig. 18. It is observed that the major percent of the losses occurs in the coupled inductors as they carry high currents. The theoretical efficiency of the proposed converter at full load is calculated as 97.3%, which is close to the experimentally measured values.

VI. CONCLUSION

A new interleaved high step-up converter with coupled inductors has been proposed in this paper. It is shown that the presented converter has the following features.

1) The input current ripple is significantly reduced and the power level is increased due to the interleaved operation at the input side.
2) Very high step-up voltage gain is achieved due to the series configuration at the output side.
3) Low-voltage-rating MOSFETs with small on resistance are allowed to reduce the conduction loss thanks to the very low switch voltage stress.
4) Leakage energy is efficiently recycled.
5) ZCS turn-ON of the switches is achieved and the reverse recovery problem of the diodes is alleviated.
6) Common ground connection between the input and the output is achieved.

These features make the proposed converter attractive for high step-up high-power applications, such as renewable energy systems, fuel cell systems, and uninterrupted power supplies. The operation principles and characteristics of the converter were analyzed in detail. A 20-V-input and 400-V-output prototype with a peak efficiency of 95.01% was designed and built. Experimental results have verified the performance of the proposed converter.

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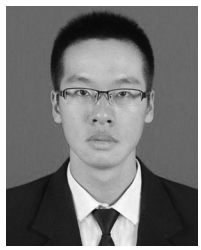

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Dr. Smedley is a recipient of UCI Innovation Award 2005. Her work with One-Cycle Control, Inc., won Department of the Army Achievement Award in the Pentagon in 2010.