Effects of Junction Capacitances and Commutation Loops Associated With Line-Frequency Devices in Three-Level AC/DC Converters

Bo Liu, *Member, IEEE*, Ren Ren, *Student Member, IEEE*, Edward A. Jones, *Member, IEEE*, Handong Gui, *Student Member, IEEE*, Zheyu Zhang, *Member, IEEE*, Ruirui Chen, *Student Member, IEEE*, Fei Wang, *Fellow, IEEE*, and Daniel Costinett, *Member, IEEE*

***Abstract*—This paper identifies extra junction capacitances and switching commutation loops introduced by line-frequency devices (i.e., non-active every other half line cycle) in three-level ac/dc converters and investigates the corresponding effects. Junction capacitances and power loops are well known as the key factors that impact converter switching loss and device stress, thus influence device selection, power stage layout, and thermal design. By examining switching transients of the commonly used T-shaped and I-shaped three-level converters, the cause and mechanism of the extra junction capacitances and power loops are presented. The impacts on switching loss, device voltage stress, and ac-side voltage/current distortion are respectively reported and analyzed. A loss calculation scheme for the three-level converter to include that extra loss is proposed. A power layout scheme to mitigate the device voltage stress is provided. Compensation and modeling of the voltage and current distortion are also proposed. Experimental results conducted on several types of three-level converter prototypes including a gallium nitride based 115 V_{ac}/650 V_{dc}/1.5-kW/450-kHz Vienna-type rectifier and a SiC MOSFET based 1-kV/10-kW/280-kHz three-level active neutral-point-clamped inverter confirm the presented effects and verify the associated analysis and solutions.**

***Index Terms*—Commutation loops, device stress, junction capacitances, loss calculation, three-level ac/dc converter, voltage/current distortion.**

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B. Liu, R. Ren, H. Gui, and R. Chen are with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, TN 37996 USA (e-mail:

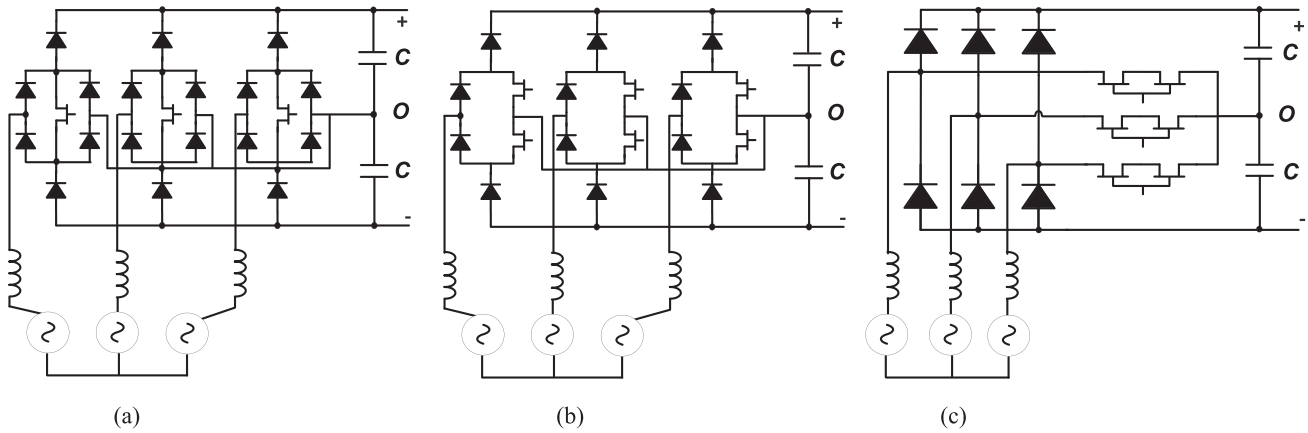


Fig. 1. Three common Vienna-type variants. (a) [31]. (b) [32]. (c) [33], [34], and [29].

power layout, therefore, is essential for high efficiency, high reliability, and high density converter design, especially when fast speed devices and high switching frequency operation become favored nowadays.

Although these aspects of 3L converters have been studied for decades in Si-based converters, e.g., the analytical loss calculation for Vienna-type rectifiers in [15]–[18], device commutation and loss analysis for T-type converters in [19] and [20] and for NPC converters in [21]–[24], some important effects of other switching commutation paths and related junction capacitances inherent in 3L ac/dc converters have not been discussed in the past. For example, all the above-mentioned switching commutation analysis and loss calculation for both Si and SiC 3L converters still follow the basic traditional approach, i.e., based on the two-level double pulse tester (DPT) setup, which has been widely used in characterizing devices, in obtaining conduction and switching loss [25]–[27], and in producing datasheet of the commercial devices. However, whether the switching energy data $E_{\rm on}$ and $E_{\rm off}$ of DPT can be readily utilized for the 3L converter loss calculation has seldom been carefully considered. The feasibility was questioned when a highly mismatched switching loss was observed between the calculation and experiment in [17]. The heatsink/cold plate coupled capacitance in the actual 3L converter prototype was highlighted to partially account for the significantly higher switching loss. However, the major cause was attributed to device parasitic capacitance introduced by "unfavorable" PCB layout induced in the actual 3L converter, and no further investigation was conducted. Observing the similar loss mismatch, this paper conducts a deep investigation and finds that this part of extra capacitance is actually related to the line-frequency devices or non-active devices every half line cycle in 3L converters. A simple approach that takes account of the additional loss but still utilizes the typical DPT data is, thereafter, proposed for 3L converters.

Moreover, the non-active devices are also found to be the cause of excessive device stress and voltage/current distortion in 3L converters. Hence, it is of general significance to 3L converters. The cause and impacts that may be less important at low switching speed and low frequencies become significant at high switching speed and high switching frequencies. Therefore, different mitigation solutions are demanded.

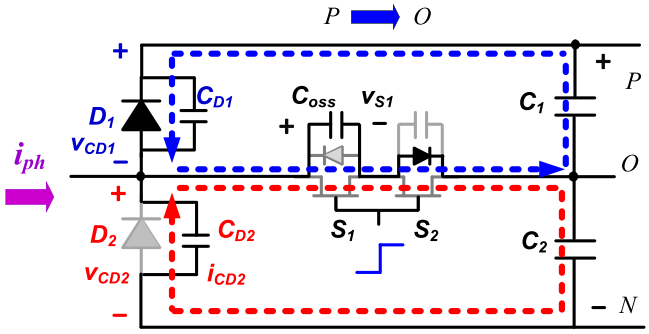


Fig. 2. Commutation loops with extra capacitance involved in Vienna-type three-level rectifier variant (c), illustrated in red.

In this paper, the extra device junction capacitances and commutation paths in different types of 3L converters are presented in Section II. Their impact on switching loss is analyzed with a new loss calculation method proposed in Section III. The impact on voltage stress of power devices is studied in Section IV. Section V analyzes the effect on PWM voltage and ac current distortion, where a modulation compensation method and a distortion model are thereafter proposed. Experimental results to verify these effects from the three aspects are given in Section VI. Finally, Section VII concludes this paper.

II. Extra Junction Capacitances and Commutation Loops in Three-Level AC/DC Converters

A. Vienna-Type Rectifiers

Three widely used Vienna-type rectifier variants, as shown in Fig. 1, are analyzed in this section.

Owing to the simplicity in its topology structure, variant (c) will be studied first, and only a positive half line cycle is illustrated in Fig. 2 for brevity. In the traditional analysis, the switching commutation takes place between S_1 and D_1. At the turn-ON transient, when the gate voltage passes the gate threshold, S_1 channel starts to conduct and channel current increases. Then, the phase current is commutated from D_1 to S_1. Once this commutation ends, D_1 is blocked. And junction capacitance C_{D1} of D_1 is charged by dc bus through S_1 channel, where output capacitance $C_{\rm oss}$ of S_1 is discharged.

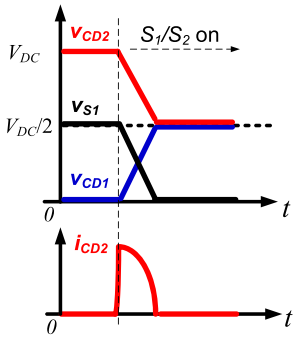


Fig. 3. Ideal waveforms of three junction capacitor voltages and the discharging current of the line-frequency switch during the turn-ON transient of the main switch.

However, the missing part is when $C_{\rm oss}$ is discharged from $V_{\rm DC}/2$ to 0, the terminal voltage v_{CD2} also drops from $V_{\rm DC}$ to $V_{\rm DC}/2$, as illustrated in Fig. 3. Therefore, the joint junction capacitance $C_{\rm D2}$ of the bottom diode D_2 will be discharged by the channel resistance of S_1. Since this path does not conduct load current for a half line cycle, it was unnoticed in the prior work.

The root cause of this effect is that there are three switching branches (positive branch, neutral branch, and negative branch) in the phase leg of three-level converters which forms a T connection, instead of the two positive and negative branches formed by the switch/switch (S-S) or switch/diode (S-D) pair in two-level converters. Consequently, in each half line cycle, although the complementary branch does not conduct, the junction capacitance of this branch is still charged or discharged as long as it has a switching potential. This capacitance can be regarded as a parallel output capacitance across the active switch from the ac signal perspective if assuming the dc-link capacitor is shorted.

The similar analysis is carried out on the other two variants (a) and (b). The extra capacitances involved in the commutation from the positive level to the neutral level are marked in red in Fig. 4(a) and (b), respectively. For variant (a), if the structurally undefined voltage stress for D_{LF1-} and D_{HF-} can be balanced at half $V_{\rm DC}$ with the proper balance design [28]–[30], the voltage of D_{HF-} will maintain at $V_{\rm DC}/2$, whereas the voltage of $D_{\rm LF2--}$ maintains at 0 V during the S_1 turn-ON transition. As a result, C_{LF-} and C_{LF2+} are discharged from $V_{\rm DC}/2$ to 0 V via the main switch S_1, respectively. Therefore, these are the capacitances in addition to junction capacitances of the main switching devices S_1 and D_{HF+}.

Similarly, for the variant (b), S_1 and S_2 share the same gate signal, and the voltage stress of D_{LF-} and D_{HF-} can be balanced. The voltage of D_{HF-} is maintained at $V_{\rm DC}/2$ in the designated current flow direction, whereas the voltage of S_2 maintains at 0 V during the S_1 turn-ON transition. The junction capacitance C_{LF-} of D_{LF-} forms an extra $C_{\rm oss}$ capacitance to the main switch S_1.

B. T-Type Converter

Fig. 5 shows a phase leg of the T-type 3L converter. Because of the replacement of two diodes with active switches from the Vienna-type rectifier, commutation of the T-type converter can be current independent and in four quadrants. However, the similar capacitance effect can still be observed. Transitions from the positive level to the neutral level in both the rectifier mode and the inverter mode are analyzed as examples. In both cases, in addition to the conventional switching loop marked in blue, another discharging path from the junction capacitance $C_{\rm oss2}$ of the non-active S_2 to the channel of the neutral switch $S_{\rm N1}$ is concurrent, as illustrated in red.

C. I-Shaped 3L Converters

I-shaped phase leg based 3L converter is widely applied. One of the commonly used topologies is the NPC converter. It is also worth noting that the variants (a) and (b) of Vienna-type rectifiers also belong to this category, although they have been discussed under the group of Vienna-type.

1) Diode NPC Converters (DNPC): The modulation schemes and switching commutation loops of DNPC have been extensively studied [23], [24]. As shown in Fig. 6, taking the positive half line cycle as an example, in the unity power factor (PF = 1) case, i.e., the first quadrant, the outer switch S_1 and clamping diode D_p are operated at high frequency (HF), and S_2 is fully ON to form the positive level and neutral level in the positive half line cycle (i.e., outer mode).Whereas, the S_4 and D_n are fully OFF. In the PF = −1 case, i.e., the second quadrant, when the phase current flows into the converter, the inner switch S_1/D_1 and S_3 are switched at HF to synthesize the positive level and neutral level, respectively (i.e., inner mode), whereas S_2 and S_4/D_4 are fully OFF and will be active in the other half line cycle.

There are also device junction capacitances and commutation paths missed in the prior analysis. Assuming PF = 1 operation in the first quadrant with the outer mode modulation, in addition to the well-studied commutation loop as marked in blue, an additional loop exists as shown in red. During the S_1 turn-ON transient, the switching node voltage on the drain of S_3 increases from $V_{\rm DC}/2$ to $V_{\rm DC}$, therefore, $C_{\rm oss}$ of the blocked switches S_3 and S_4 as well as $C_{\rm n}$ of the clamping diode $D_{\rm n}$ will be also charged, forming extra output capacitances across the main switch S_1.

This is also seen in the PF = –1 operation with the inner mode modulation, as shown in the second quadrant of Fig. 5. Since the voltage of S_4 remains at $V_{\rm DC}/2$ before and after the turn-ON transient of S_3, thanks to D_n clamping, $C_{\rm oss4}$ and C_n do not contribute to extra $C_{\rm oss}$. However, since the voltage across D_p decreases from $V_{\rm DC}/2$ to zero during the transition, an additional junction capacitance and a switching loop are introduced by D_p, as marked in red.

To summarize, based on the observation and analysis, the outer mode modulation of the NPC that was previously believed to have a short switching loop can introduce extra charged/discharged junction capacitances and another longer commutation loops from the complementary branch during the switching commutation, whereas the inner mode that was previously believed to have a larger main commutation loop owing to the extension of the switching loop into the complementary branch has no extra junction capacitances from the

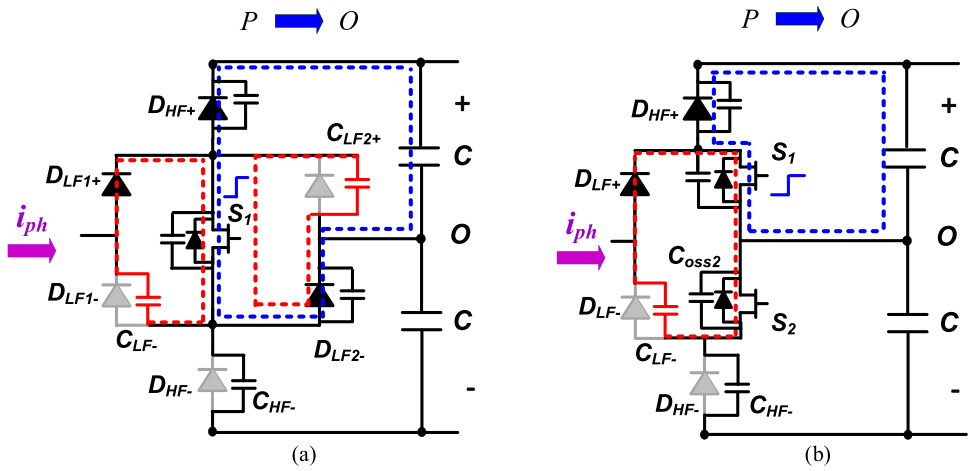


Fig. 4. Commutation loops with extra capacitance involved in Vienna-type three-level rectifier variant (a) and (b), illustrated in red.

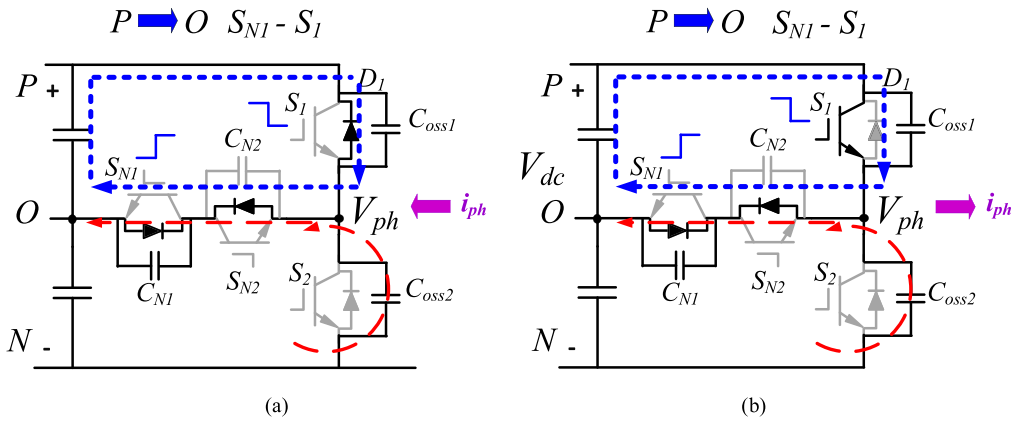


Fig. 5. Commutation loops with extra capacitance involved in T-type three-level converter. (a) Rectifier mode. (b) Inverter mode.

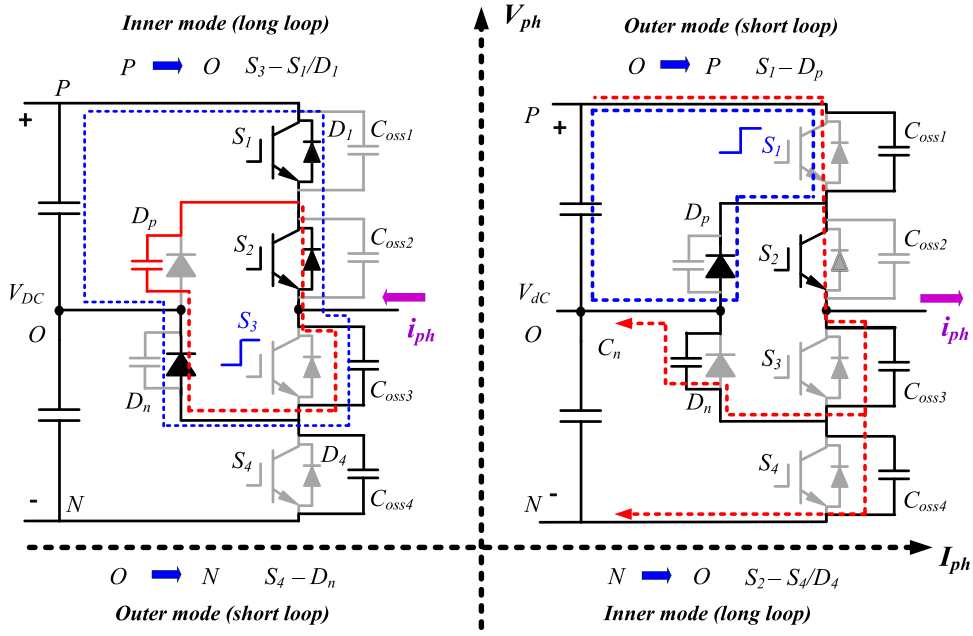


Fig. 6. Commutation loops with extra capacitances in DNPC with the four-quadrant operation. (Third and fourth quadrants not shown.)

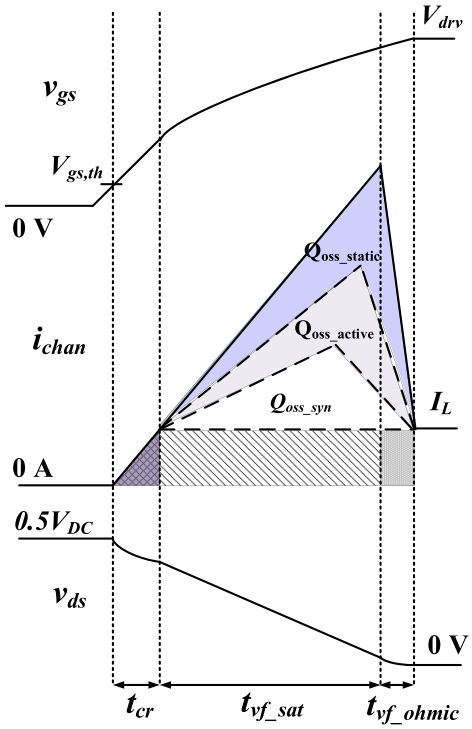


Fig. 7. Theoretical turn-ON transient of the active neutral device in a three-level converter.

complementary branch but additional capacitances and another shorter commutation loop. Since PF = 1 condition only operates in the outer mode, PF = −1 condition only operates in the inner mode, and other PF operations have the mixed modes [23], the analyzed general effects will be exerted on the DNPC in a mixed manner and to different degrees as PF varies.

2) Active NPC Converters (ANPC): Because of the flexibility in controlling the clamping switches, ANPC has more freedom in modulations. Two conventional modulations are summarized in [23], i.e., the outer mode modulation and inner mode modulation applicable for all four quadrants and all PFs. An improved modulation was also proposed in [23], which is equivalently a combination of the inner mode and the outer mode. Since all schemes are rooted in the two basic modes in DNPC, the aforementioned effects and conclusions are also applicable for these different modulations in ANPC. Detailed analysis of the effect on device stress is provided in Section IV.

III. Impact on Switching Loss and New Calculation Method

The existence of the above-mentioned extra commutation loops and device capacitance inevitably introduces switching loss to all types of three-level converters. The first part of the additional loss is the $C_{\text{oss\_static}}$ energy stored on the non-active device and dissipated during the turn-ON of the active device, as illustrated by charge $Q_{\text{oss\_static}}$ in Fig. 7, where $Q_{\text{oss\_active}}$ and $Q_{\text{oss\_syn}}$ are the charge of active and synchronous switches, respectively. The second part is overlap loss caused by the increased duration of saturation region t_{vf_sat} due to this extra charge at turn-ON and turn-OFF. Due to the near-zero voltage drop in the ohmic region, the overlap loss during t_{vf_ohimc} is negligible [35].

In the prior study, the loss analysis was only conducted on the S/S or S/D switching pair using the two-level half-bridge model per each half line cycle. And the loss estimation also directly employed the energy obtained from the traditional half-bridge DPT.

To achieve correct loss calculation, a straightforward solution is to build a DPT phase-leg with a three-level structure, instead of the half-bridge. However, this requires two dc power supplies, two bulky energy storage capacitors with balanced voltage, and a full revision of the widely adopted two-level DPT set up. Moreover, $E_{\text{on}}/E_{\text{off}}$ data of commercial devices are all based on two-level DPTs.

To facilitate the loss calculation taking into account the extra loss, a method combining device C_{oss} information and the conventional DPT data is proposed.

A. C_{oss} Loss Calculation

The additional C_{oss} energy loss $E_{\text{on\_Coss\_extra}}$ contributed by the non-active device per half line cycle can be calculated in (1) as its voltage $v_{\text{coss\_static}}$ increases from $V_{\text{DC}}/2$ to V_{DC}, using the Vienna-type rectifier in Fig. 2 as an example. Here, T_{s} and T_{on} denote the switching cycle and turn-ON interval, respectively

$$\begin{aligned} E_{\text{on\_Coss\_extra}} &= \int_{T_s}^{T_s+T_{\text{on}}} (v_{\text{Coss\_static}} - V_{\text{DC}}/2)\cdot i \cdot dt \\ &= \int_{V_{\text{DC}}/2}^{V_{\text{DC}}} v_{\text{Coss\_static}} \cdot C(v_{\text{Coss\_static}}) dv_{\text{Coss\_static}} \\ &\quad - V_{\text{dc}}/2 \int_{V_{\text{DC}}/2}^{V_{\text{DC}}} C(v_{\text{Coss\_static}}) dv_{\text{Coss\_static}}. \end{aligned} \tag{1}$$

If defining the energy equivalent capacitance $C_{\text{eq},E}$ for this three-level case as

$$C_{\text{eq},E} = \frac{\int_{V_{\text{DC}}/2}^{V_{\text{DC}}} v_{ds}\cdot C(v_{ds}) dv_{ds}}{\frac{1}{2}{V_{\text{DC}}}^2}. \tag{2}$$

Equation (1) can be reformatted as

$$E_{\text{on\_Coss\_extra}} = \frac{1}{2} C_{\text{eq},E,\text{Coss\_static}} \left(\frac{V_{\text{DC}}}{2}\right)^2 - \frac{V_{\text{DC}}}{2} Q_{\text{oss\_static}} \tag{3}$$

where $C_{\text{eq},E,\text{Coss\_static}}$ is the energy equivalent capacitance of $C_{\text{oss\_static}}$ and can be calculated from the device voltage-dependent capacitance curve on its datasheet.

B. Overlap Loss Calculation

The overlap energy loss $E_{\text{on\_overlap}}$ under a given load current level I_L is simplified as in

$$E_{\text{on\_overlap}} = E_{\text{on\_}cr} + E_{\text{on\_}vf} \approx \frac{1}{2}(t_{cr} + t_{vf\_\text{sat}}) V_{\text{DS}} I_L. \tag{4}$$

Here, $E_{\text{on\_cr}}$ is the overlap energy during the current rising time t_{cr} and $E_{\text{on\_}vf}$ is the overlap energy during the voltage falling interval t_{vf_sat} in the saturation region. Although people tend to calculate this time from gate circuitry, it is favorable to revisit the derivation from the output junction capacitances as the gate charging and C_{oss} discharging conduct simultaneously during the device saturation region. As will be analyzed, t_{vf_sat} can be strongly impacted by the extra C_{oss}. Therefore, additional C_{oss} not only increases the C_{oss}-type loss, but also indirectly enlarges the overlap loss.

For devices with non-flat gate voltage v_{gs} in the Miller plateau region, such as GaN or SiC WBG devices, the total displacement charge in the phase leg of the three-level converter $Q_{\text{oss\_}T}$ is the sum of three device junction capacitances per phase leg, and can be derived based on the shaded triangle area of the i_{chan}–t curve in Fig. 7. Since the device channel current i_{chan} in the current rising region and saturation region is determined by the gate voltage as in

$$i_{\text{chan}} = g_{fs}(v_{gs} - v_{\text{th}}) \tag{5}$$

where g_{fs} is the average transconductance of the device and v_{th} is the gate threshold voltage, the slope of i_{chan} can be calculated from the derivative of (5).

Then, it is easy to obtain the $Q_{\text{oss\_}T}$ as in

$$\begin{aligned} Q_{\text{oss\_}T} &= Q_{\text{oss\_syn}} + Q_{\text{oss\_active}} + Q_{\text{oss\_static}} \\ &= \frac{1}{2} g_{fs} \frac{dv_{gs}}{dt} {t_{vf\_\text{sat\_}T}}^2 \end{aligned} \tag{6}$$

where $t_{vf\_\text{sat\_}T}$ denotes the voltage falling period of the main active device in the three-level phase leg during the saturation region.

Whereas for Si devices, the flat Miller plateau effect should be considered and the reverse recovery charge should be excluded.

From (6), the overlap time is proportional to the root square of the displacement charge as in

$$t_{vf\_\text{sat\_}T} = \sqrt{\frac{2Q_{\text{oss\_}T}}{g_{fs}\frac{dv_{gs}}{dt}}} \propto \sqrt{Q_{\text{oss\_}T}}. \tag{7}$$

Therefore, the overlap energy $E_{\text{on\_}vf\_T}$ of the three-level phase leg in the saturation region can be scaled by the ratio of total displacement charge in three-level phase leg and in two-level phase leg, from the overlap energy $E_{\text{on\_}vf\_H}$ of the two-level DPT, given as follows:

$$E_{\text{on\_}vf\_T} = \sqrt{\frac{Q_{\text{oss\_}T}}{Q_{\text{oss\_}H}}} \cdot E_{\text{on\_}vf\_H} \tag{8}$$

where $Q_{\text{oss\_}H}$ is the total C_{oss} of the two-level half-bridge leg or DPT and the subscript "T" and "H" denote three-level and two-level, respectively.

Note that $E_{\text{on\_}vf\_H}$ is, however, difficult to be directly measured from DPT. An intrinsic relationship between the switching energy and DPT data is first established in the following section, which is the key to realize the loss scaling scheme.

C. Intrinsic Relationship Between Switching Energy and DPT Data

From Fig. 7, the current rising time t_{cr} can be also derived in (9), in addition to the overlap time in (7)

$$t_{\text{cr}} = \frac{I_L}{g_{fs}\frac{dv_{gs}}{dt}}. \tag{9}$$

Thus, based on (4), (7), and (9), the total turn-ON switching energy in a general bridge set up can now be expressed as

$$\begin{aligned} E_{\text{on}} &= E_{\text{on\_cr}} + E_{\text{on\_}vf} + E_{\text{Coss\_total}} \\ &= \frac{V_{\text{DS}}}{2} \frac{1}{g_{fs}\frac{dv_{gs}}{dt}} I_L^2 + \frac{V_{\text{DS}}}{2} \sqrt{\frac{2Q_{\text{oss}}}{g_{fs}\frac{dv_{gs}}{dt}}} I_L + E_{\text{Coss\_total}} \end{aligned} \tag{10}$$

where $E_{\text{Coss\_total}}$ consists of both the C_{oss} energy stored in the main active device and the energy stored in the synchronous device during the turn-OFF of the main active device.

As well known, the measured energy loss $E_{\text{on\_DPT}}$ and $E_{\text{off\_DPT}}$ data from the conventional DPT can be typically curve-fitted well by a quadratic function

$$\begin{cases} E_{\text{on\_DPT}} = k_1 I_L^2 + k_2 I_L + k_3 \\ E_{\text{off\_DPT}} = k_4 I_L^2 + k_5 I_L + k_6 \end{cases} \tag{11}$$

where $k_1 \sim k_6$ are curving-fitting coefficients.

By matching the two types of expressions, an interesting and important relationship hidden between the physical device parameters and measured data is revealed

$$\begin{cases} E_{\text{on\_cr}} = k_1 I_L^2 = E_{\text{on\_cr\_DPT}} \\ E_{\text{on\_}vf} = k_2 I_L = E_{\text{on\_}vf\text{\_DPT}} \\ E_{\text{Coss\_total}} = k_3 + k_6 = \sum E_{\text{Coss\_DPT}} \end{cases} \tag{12}$$

where the measured constant k_6 in the turn-OFF transient represents C_{oss} energy of the active device dissipated during the next turn-ON transient, thus is added to $E_{\text{Coss\_total}}$. The subscript "DPT" indicated the energy loss of the DPT.

From (12) and (8), the total overlap energy $E_{\text{on\_}vf\_T}$ of the 3L phase leg can be finally scaled from the linear term $E_{\text{on\_}vf\text{\_DPT}}$ (i.e., $E_{\text{on\_}vf-H}$) of the two-level half-bridge DPT result. And the added overlap energy introduced by the non-active device is the difference between $E_{\text{on\_}vf\_T}$ and $E_{\text{on\_}vf\_H}$.

D. Discussion

For the turn-OFF transient, the actual overlap loss excluding the C_{oss} energy should also be considered. However, for Si MOSFET or WBG devices, this loss is often quite low compared to the actual turn-ON loss, such that the extra turn-OFF overlap loss caused by the displacement charge of the non-active device becomes further smaller. Therefore, this overlap loss could be omitted to simplify the method.

The final switching loss $P_{\rm sw}$ of the upper half or bottom half of the ac/dc three-level phase leg would be

$$P_{\rm sw} = \frac{1}{T_0}\int_0^{T_0/2} \left(\begin{matrix} k_1 \cdot {i_L}^2 + k_2 \cdot i_L \cdot \sqrt{\frac{Q_{\rm oss\_T}}{Q_{\rm oss\_H}}} \\ +k_4 \cdot i_L^2 + k_5 \cdot i_L \end{matrix} \right) \cdot f_s \cdot dt + (k_3 + k_6 + E_{\rm on\_Coss\_extra}) \cdot f_s \quad (13)$$

based on the two-level DPT data, where i_L is the instantaneous phase current, and T_0 is the line period.

Although the presented analysis and proposed method are conducted on a Vienna-type 3L converter, they could be applied to other 3L converters as well.

In general, for fast switching speed WBG device and CoolMOS-based 3L converters, the power loss impact of non-active devices on the active switch is mainly reflected by the extra $C_{\rm oss}$-type loss instead of the extra overlap loss due to the superfast overlap transition. This part of loss can be as high as 17% of the total switching loss as given later in the experiment. Whereas for low-speed Si MOSFET or IGBT-based 3L converters with typical 5∼10 V/ns *dv/dt* instead of 100 V/ns above *dv/dt* of WBG devices, the loss effect will be mainly shown as extra overlap loss due to the significantly longer switching transition and relatively lower $C_{\rm oss}$-type loss.

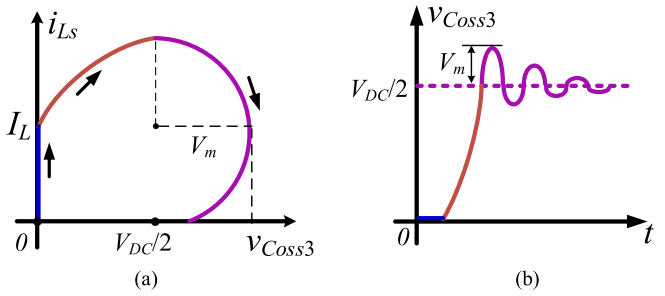


Fig. 8. Mode analysis for multi-commutation loop during positive cycle. (a) Steady-state when $V_x = 0$. (b) Switching transition from $V_x = 0$ to $V_x = 0.5$ VDC. (c) Steady-state when $V_x = 0.5$ VDC.

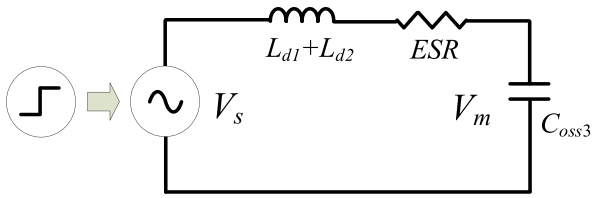


Fig. 9. Overvoltage analysis of the line-frequency switch S_3 in ANPC phase-leg during the turn-on transient of the main switch S_1. (a) State trajectory of current and voltage in the extra commutation loop. (b) Voltage ringing and resonance spike.

IV. Impact on Device Stress

In an actual converter, stray inductance from device package, PCB trace, and power switching loop can resonate with the junction capacitances of the devices in a bridge configuration, leading to higher current stress of the active device and higher voltage stress of the synchronous device during the turn-ON, and higher voltage stress of the active device during the turn-OFF.

A. Overvoltage Due to Additional Loop Inductance

Different from the traditional analysis that only considers the stray inductance in the half-bridge configuration, this paper will focus on the added stray inductance associated with the non-active device in 3L converters. Because of the participation of the non-active devices in the switching commutation and the extra power loops in parallel to the main commutation loop, an additional *LC* resonance occurs due to the added $C_{\rm oss}$ and loop inductance, imposing higher voltage stress on the non-active devices in the T-shaped/I-shaped phase leg of three-level converters. This is particularly severe when using high-speed power devices, where significant *dv/dt* is the main excitation source for the *LC* resonant tanks.

The high device stress is more significant in the I-shaped three-level phase leg such as in Vienna-type variant (a), (b), and NPC converters, compared to the T-shaped three-level phase leg used in Vienna-type variant (c) and T-type ac/dc converters.

This is mainly because the power loops in the T-shaped converters are usually carefully laid out in the PCB design stage, as both the positive and negative power loops are high-frequency switching loops for a half line cycle. Whereas, for the I-shaped phase leg, extra commutation loops are introduced via the line-frequency diodes or switches. Since they were regarded as non-critical loops in the past and overlooked, surprisingly high additional loop inductance could be introduced.

To illustrate this effect, an example is given based on the ANPC inverter. From the conventional analysis, ANPC also has two types of main power commutation loops, depending on whether it is in the outer mode or the inner mode. The outer mode is often considered superior to the inner mode under high switching frequency operation in terms of switching loss and device voltage stress [21], since its main commutation loop formed by switches S_1, S_p, and decoupling capacitors is much shorter than that of the inner mode.

However, even for the outer mode, a long commutation loop exists due to the effect from the non-active switches [36]. Fig. 8 shows a mode analysis of the multi-loops during a positive half line cycle. First, $S_{\rm p}$ is turned OFF, and the load current is transferred to the freewheeling diode of S_p. Then, S_1 is turned ON and commutates this load current. Once the load current is fully commutated to S_1, the decoupling capacitor discharges the junction capacitance of S_1 and charges the junction capacitance of S_p. In the meantime, the junction capacitance of the non-active switch S_3 is also charged from 0 V to $V_{\rm DC}/2$, since it is paralleled with S_p via S_2 and S_n. And a long commutation loop is also formed via the switches S_1, S_2, S_3, $S_{\rm n}$, and the dc-link decoupling capacitor, as marked in red in Fig. 8(b).

For this additional commutation loop, a resonance occurs between the loop inductance $L_{\rm d1} + L_{\rm d2}$ and the $C_{\rm oss}$ of S_3, following two preceding intervals during the turn-ON transient of the main active switch S_1: first, the load current $I_{\rm L}$ is fully commutated from synchronous switch $S_{\rm p}$ to S_1; and second, S_2 voltage is charged by the dc bus via S_1 channel until it reaches 0.5 $V_{\rm DC}$. The first resonant cycle can be illustrated by the state trajectory of the stray inductor current $i_{\rm Ls}$ and $C_{\rm oss}$ voltage

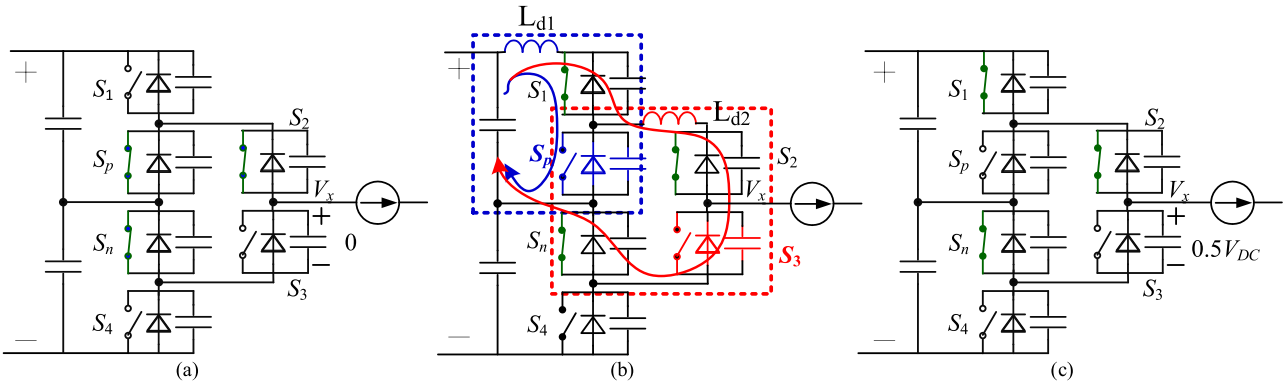


Fig. 10. Simplified equivalent circuit of the resonance tank during the turn-on transient of the main switch S_1.

v_{Coss3} of S_3, as given in Fig. 9. The first and highest voltage peak appears when i_{Ls} returns to I_{L} level, indicating the inductive energy stored by the loop inductance is fully transferred to C_{oss} of the non-active device S_3. Assuming the first resonance amplitude of v_{Coss3} is V_m, and the resonance amplitude of the excitation voltage generated by the turn-ON switching action of S_1 is V_{s}, a simplified equivalent circuit can be obtained, as shown in Fig. 10. Here, the impact of the original L_{d1} loop is neglected to simplify the analysis. Further in-depth analysis of this multiloop transient itself could be an interesting research topic in the future.

From the frequency domain circuit analysis, a simple relationship is held at the resonance frequency

$$V_m = \frac{V_s}{\mathrm{ESR}} Z_0 = \frac{V_s}{\mathrm{ESR}} \sqrt{\frac{L_{d1} + L_{d2}}{C_{\mathrm{oss3}}}} \tag{14}$$

where ESR is the total loop resistance and Z_0 is the characteristic impedance of the resonance tank.

Therefore, the overvoltage stress is proportional to the root square of the loop inductance. And the previously unnoticed loop could be poorly laid out on the PCB and may introduce high device overvoltage.

From simulation results in Fig. 11 using the Pspice-based behavior model of Wolfspeed C3M0065090J devices under 1000 $\mathrm{V_{DC}}$ voltage, S_3 and S_p will suffer the same voltage spike during the turn-ON transition of S_1, assuming the longer commutation loop inductance is $L_{d2} = 0$. However, once L_{d2} is not zero, the voltage spikes of two devices become significantly different, as shown in Fig. 11(b). A resonance is formed by the inductance of the long commutation loop and junction capacitance of S_3. Consequently, the non-active switch S_3 suffers a much higher voltage spike in the positive half line cycle compared to the switch S_p. This could be even worse as L_{d2} increases.

B. Overvoltage Mitigation

To alleviate this effect, the basic principle in (14) can be applied to derive different approaches.

1) Reduce excitation source V_s: By slowing down the device turn-ON speed, lower ac source V_s is achieved and results in lower V_m. The common approach is to increase the gate resistance, however, at the expense of increased overlap switching loss.
2) Increase *ESR*: By increasing the *ESR* in the power loop, ringing voltage V_m can also be reduced. The typical approaches include inserting a damping resistor and inserting a ferrite bead in the power loop. Although both will introduce power loss, the ferrite bead has lower dc loss and higher ac resistance at the resonance frequency thus shows the better damping performance and relatively lower loss. However, choosing a proper bead is complicated and should be wary due to the frequency-dependent impedance characteristics of the bead and its involvement in the switching dynamics along the wide frequency range.
3) Increase resonance capacitance: On the other hand, adding the snubber circuit can increase the resonance capacitance, thus also reduces the V_m. However, snubbers slow down both the turn-ON and turn-OFF transitions, leading to high switching loss especially for high switching frequency converter design.
4) Reduce loop inductance: Therefore, the most straightforward and effective way is reducing the loop inductance, which has the least side effect on switching loss. The loop inductance includes the series inductance from the device leads or package, self-partial inductance from PCB traces, and mutual-partial inductance from the loop area [37], as well as the serial inductance of dc-link capacitors, which is often minimized by paralleling low-profile surface mount ceramic decoupling capacitors next to switches. The mutual-inductance is negative and inversely proportional to the distance between loop traces [37], therefore, shrinking the loop area will maximize this inductance and reduce the total loop inductance. The key factor is the power PCB layout.

In fact, the additional loop could become a potential hazard to three-level converters mainly because its participation in the switching commutation was not noticed before. Once the component placement and power trace arrangement are carefully considered in the first place, this effect will be less severe. Table I shows the loop inductance comparison from two different types of PCB layouts, all for ANPC inverters, based on ANSYS Q3D parameter extraction from the actual power PCB files, where the switches and dc-decoupling capacitors are

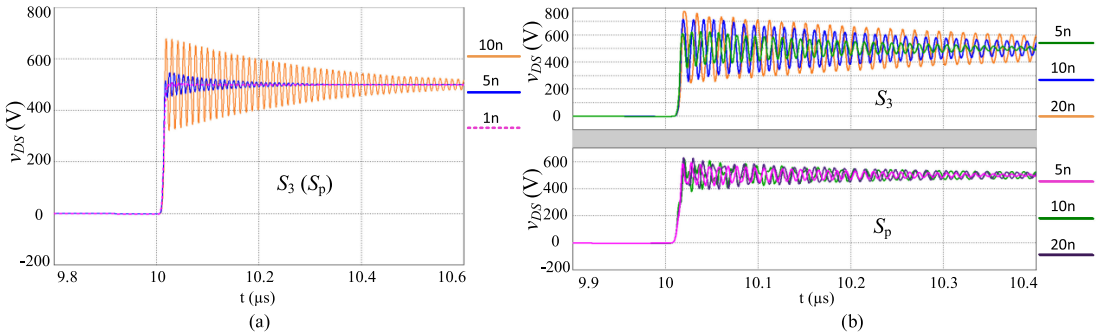


Fig. 11. Overvoltage in the simulation. (a) $L_{d1} = 1$ nH, 5 nH, 10 nH, and $L_{d2} = 0$ nH. (b) $L_{d1} == 5$ nH and $L_{d2} = 5$ nH, 10 nH, and 20 nH.

TABLE I
COMPARISON OF JUNCTION CAPACITANCE, LOOP INDUCTANCE, AND VOLTAGE STRESS BETWEEN TWO ANPC LAYOUTS

Design case	Junction capacitance of non-active device S_3	Additional loop inductance	Overvoltage percentage on S_3 (steady-state stress: 500 V)
ANPC with SiC MOSFET C3M0065090J, 900 V/35 A, TO263	70 pF@500 V	57.5 nH	84% (420 V)
ANPC with SiC MOSFET C3M0065100K,	70 pF@500 V	12.4 nH	39% (195 V)

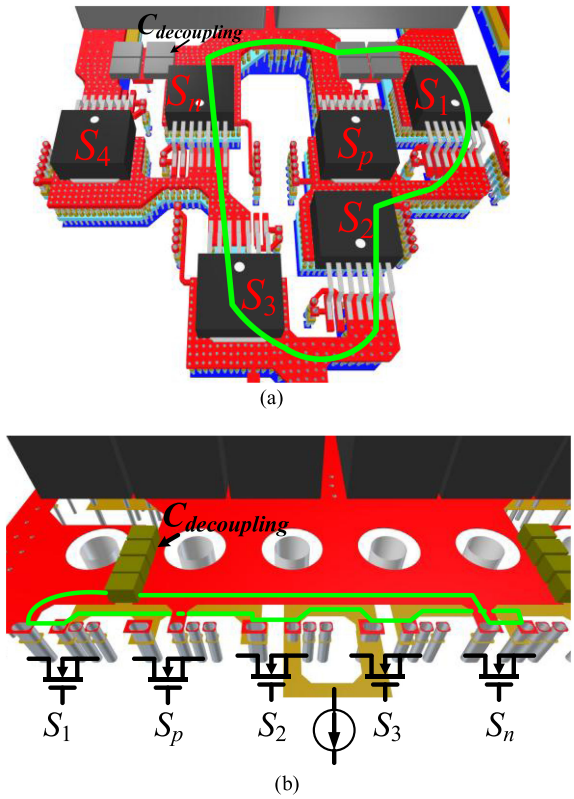


Fig. 12. PCB layout schemes for outer mode modulated ANPC phase-leg. (a) Original layout without considering the extra loop effect associated with the line-frequency switches. (b) Improved layout with minimized lateral device-placement and vertical trace-placement to reduce the extra loop inductance. (Green lines depict the additional loop.)

replaced by a copper bar. The first design was conducted when the presented non-active device effect had not been known. Its additional loop inductance is surprisingly high, 57.5 nH, whereas the improved design optimizes the layout to minimize the additional loop associated with the line-frequency devices, and the inductance has been reduced to 12.4 nH.

The physical layout schemes for the two cases are illustrated in Fig. 12. The original design places two line-frequency switches next to the four high-frequency switches following a traditional structure similar to the structure of the circuit diagram drawing. Consequently, a large loop area is encompassed by the two low-frequency devices and two high-frequency devices, whereas the improved design places the four high-frequency switches and two line-frequency switches of the phase leg in the same line. Hence, the horizontal area of the line-frequency loop is also minimized in addition to the well-known high-frequency switching loop. To realize this layout, the device package has been changed from the surface mount D2PAK package to the lead-through package to mitigate conflicts between the device physical space and the minimal lateral loop target. In addition, the interconnection of power devices is through the multi-layer trace placement, following the widely adopted vertical layout scheme. The trace width shall be maximized within the given layout space to further reduce the loop inductance [38].

V. IMPACT ON PWM VOLTAGE AND AC CURRENT DISTORTION

A. C_{oss} *Induced Distortion*

The fast switching intensifies the effects of parasitics on switching commutation, negatively affecting power quality of the power converter. For example, when ac/dc converters are operated at high switching frequency, non-ideal commutation can cause severe voltage distortion such as the slow transition during device turn OFF due to the charging of device junction capacitances [9], [39].

Higher switching frequency exacerbates the voltage distortion as a result of a shorter switching period. And it gets even worse in switch-diode configured converters, such as three-level Vienna-type rectifiers. Taking the Vienna-type variant (c) in Fig. 13 as an example, similar to previous analysis for the turn-ON transition, during turn-OFF in the positive half line cycle, C_{D2} of the non-conducting diode D_2 is also charged from 0.5 V_{DC} to V_{DC},

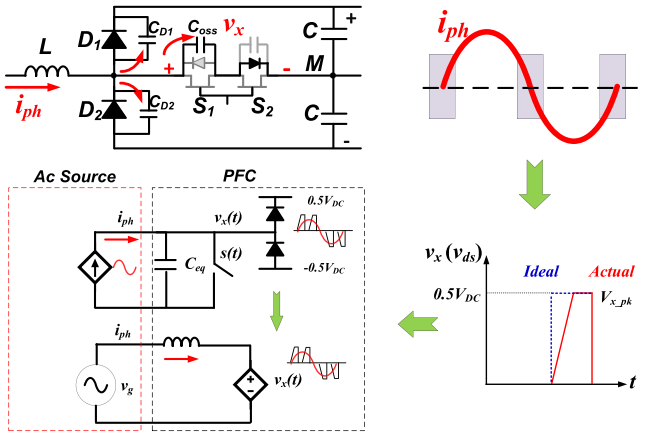


Fig. 13. Illustration of voltage and current distortion in a three-phase Vienna-type rectifier due to the PWM loss caused by charging of device junction capacitances at turn-OFF.

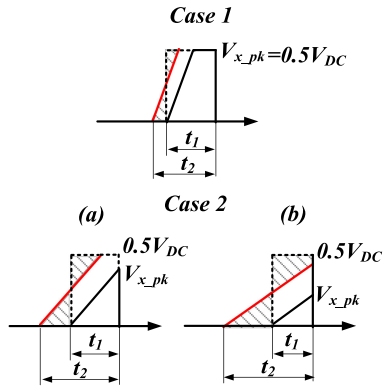


Fig. 14. Two voltage distortion cases associated with different current level and the proposed turn-OFF compensation scheme considering the voltage shape before and after compensation. The dashed line shows the ideal PWM voltage, the solid black line shows the actual uncompensated turn-OFF voltage, and the red line shows the compensated voltage based on the shaded volt–second area.

in addition to the charging of the output capacitance of the active switch from 0 V to 0.5 $V_{\rm DC}$ and the discharging of junction capacitance C_{D1} from 0.5 $V_{\rm DC}$ to 0 V. Therefore, C_{D2} should also be included. However, these instantaneous capacitances are different for each device during the transient, because they are nonlinear and voltage dependent.

According to [9], it is effective to use the charge-based equivalent capacitance to represent the nonlinear voltage-dependent total junction capacitances $C_{\rm total}(v_x)$ of the three T-connected devices, since this capacitance determines the total voltage ramping and charging interval expressed as follows:

$$t_{\rm charge} = \int_0^{V_{x\_\rm pk}} dt = \frac{\int_0^{V_{x\_\rm pk}} C_{\rm total}(v_x)dv_x}{i_{ph}} = \frac{V_{x\_\rm pk}C_{{\rm eq},Q}}{i_{ph}} \tag{15}$$

where $C_{eq,Q}$ is the charge-based equivalent output capacitance over the voltage range $[\,0, V_{x\_pk}]$ for the three T-shaped connected devices per phase-leg.

From the above-discussed analysis, the added $C_{\rm oss}$ not only impacts the switching loss and device stress in the extra power loop but also introduces extra distortion on ac PWM voltage and ac current. It is interesting to notice that for loss evaluation, energy-based equivalent $C_{\rm oss}$ should be adopted, and for the device overstress analysis, instantaneous and voltage-dependent $C_{\rm oss}$ should be the choice, whereas for distortion evaluation and compensation, the charge-equivalent $C_{\rm oss}$ should be used.

B. Distortion Compensation

Since the average of the ideal PWM voltage over a switching cycle represents the average fundamental voltage, the distortion voltage due to the slow charging process introduces volt–second loss. From this perspective, a feedforward turn-OFF compensation scheme can be applied [9], to reshape the actual PWM voltage such that the compensated PWM voltage has the same volt–second as the ideal case. A simple approach, as shown in Fig. 14 is to equalize the two-shaded volt–second areas, since the remaining areas are commonly shared. The compensated duty cycle Δd for both sinusoidal PWM (SPWM) and SPWM+third schemes is unified in (16), with the only difference in a phase-angle related factor α [9]. In (16), $d_{\rm th}$ denotes the boundary turn-OFF duty cycle represented by d, and $R_{\rm target}$ represents the equivalent input impedance of PFC

$$\Delta d = \begin{cases} \frac{R_{\rm target}C_{{\rm eq},Q}}{2T_s}\frac{\alpha(\theta)}{d}, & (d \geq d_{\rm th}) \\ \sqrt{\frac{2R_{\rm target}C_{{\rm eq},Q}}{T_s}\alpha(\theta)} - d, & (d < d_{\rm th}). \end{cases} \tag{16}$$

C. Distortion Modeling and Quantification

This presented approach not only compensates the current distortion, in fact, it can also be exploited to form an analytic model for output PWM voltage distortion as a function of dc-link voltage, ac operation point, device junction capacitances, and switching frequency. The impacts of these variables can all be predicted through this model without running simulation or experimental tests.

The voltage distortion can be evaluated from the ratio of total distorted voltage ($\rm TD_V$) to fundamental main voltage, which can be easily derived as (17), based on the fact that duty cycle compensation term equalizes to the distorted duty cycle. Its relationship with total distorted harmonic voltage ($\rm THD_V$) is given in (18). The only difference is that the fundamental component ΔV_1 of the compensation term $\Delta V_{\rm RMS}$ is not regarded as harmonic voltage

$$\rm TD_V = \frac{\Delta V_{RMS}}{V_{1\_RMS}} = \frac{\Delta d_{RMS}}{d_{RMS}} = \frac{\Delta d_{RMS}}{M/\sqrt{2}} \tag{17}$$

$$\rm THD_V = \frac{\sqrt{\sum_{h=2} V_h^2}}{V_{1\_RMS}} = \frac{\sqrt{\Delta V_{RMS}^2 - \Delta V_1^2}}{V_{1\_RMS}} = \sqrt{\rm TD_V^2 - \left(\frac{\Delta V_1}{V_{1\_RMS}}\right)^2}. \tag{18}$$

Current distortion, on the other hand, as illustrated in Fig. 15, is not only determined by voltage distortion but also impacted by the filter's frequency-dependent impedance. Moreover, for three-phase three-wire converters, the current of one phase is

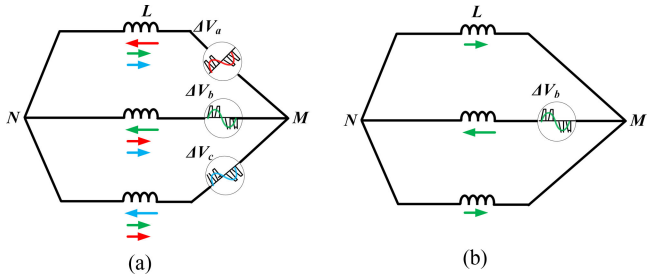


Fig. 15. Illustration of the harmonic current derivation based on superposition law in a three-phase converter. (a) Current flow in the three-phase equivalent circuit. (b) Considering individual phase using superposition law.

also determined by the voltage of other two phases. Meanwhile, it is noticed that the current feedback controller also partially suppresses the harmonics, depending on controller bandwidth and control gains at specific harmonic frequencies. Nonetheless, the harmonic current induced by phases b and c on phase a, i.e., $\Delta i_{b,a}$ and $\Delta i_{c,a}$ can be derived via the superposition law

$$\Delta i_a = \Delta i_{a,a} - \Delta i_{b,a} - \Delta i_{c,a} = \frac{\Delta v_a - 0.5(\Delta v_b + \Delta v_c)}{1.5 Z_L} = \frac{0.5\, V_{\rm dc}\,(\Delta d_a - 0.5(\Delta d_b + \Delta d_c))}{1.5 Z_L}. \tag{19}$$

Let

$$\Delta d_{a,\rm eq} = \Delta d_a - 0.5(\Delta d_b + \Delta d_c). \tag{20}$$

For any phase, its current THD can be derived as a function of $\Delta d_{\rm eq}$

$$\begin{aligned} \mathrm{THD}_I &= \frac{\sqrt{\sum_{h=2} \Delta i_h^2}}{I_1} \\ &= \frac{\sqrt{\sum_{h=2} \left(V_{\rm dc}\Delta d_{{\rm eq},h}\right)^2/\left(3\cdot 2\pi f_0 h L\right)^2}}{I_1} \\ &= \frac{V_{\rm dc}}{6\pi f_0 L I_1}\sqrt{\sum\nolimits_{h=2}\left(\Delta d_{{\rm eq},h}/h\right)^2}. \end{aligned} \tag{21}$$

It should be mentioned that the distortion term itself constrains all odd harmonics, as shown in Fig. 16. However, $3k$ (k is a non-zero integer) order harmonics are all removed due to the three-wire setup. And the fundamental distortion component should also be removed because the feedback control has almost zero error tracking for the fundamental current. Moreover, it is up to the users to determine whether the partial rejection from the feedback control should be considered for the fifth or seventh, depending on the specific control bandwidth and line frequency. In fact, from (21), although it seems high f_0 reduces the current THD, the dropped ratio of control bandwidth/f_0, on the other hand, reduces the harmonic rejection capability of the feedback control, leaving $\mathrm{THD_i}$ more dependent on the voltage distortion. It is also clear that the lower order current harmonics contribute more than the higher order harmonics due to higher $\Delta d_{{\rm eq},h}/h$.

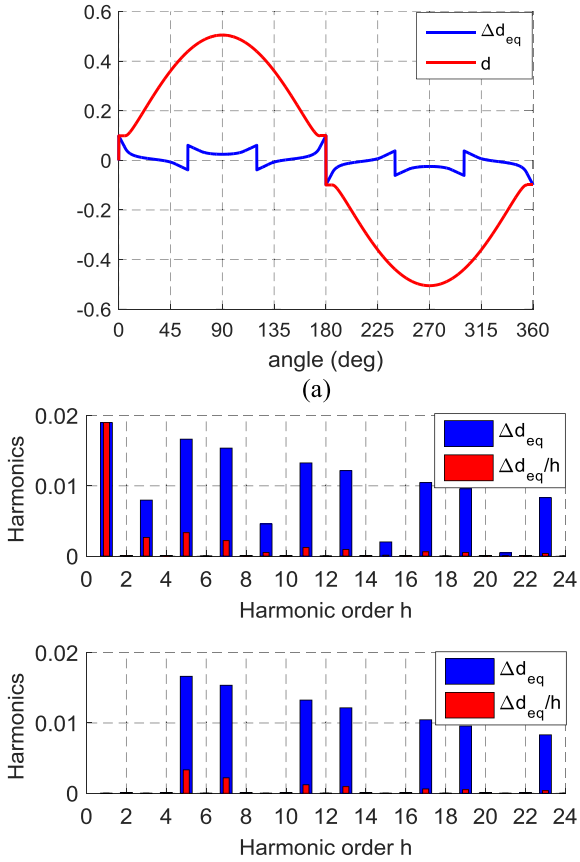


Fig. 16. Distorted duty cycle. (a) Duty cycle waveform. (b) Harmonic spectra of the distorted duty cycle.

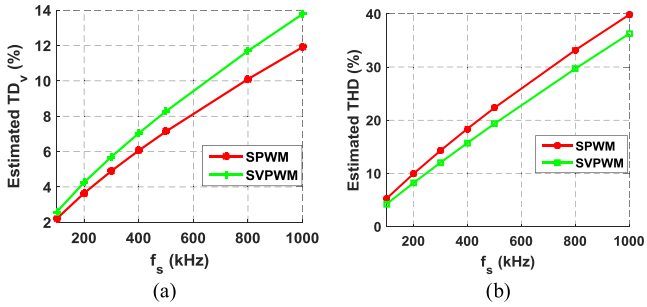
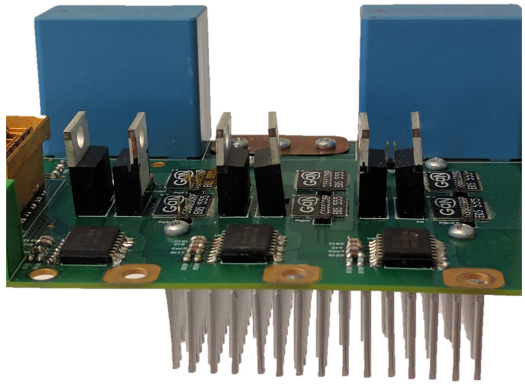
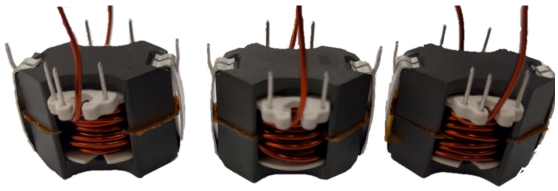


Fig. 17. Modeling of the turn-OFF distortion versus switching frequency for three-phase Vienna-type converters. (a) Modeled terminal voltage distortion versus f_s. (b) Modeled ac current distortion versus f_s.

As an example, the theoretical impacts of switching frequency on voltage and current distortion in a Vienna-type rectifier, are illustrated in Fig. 17. For the given device and operation condition, only when the switching frequency is above 100 kHz, this distortion gets pronounced. Please notice that in the subject design case, the theoretical current THD without compensation is relatively high, since the fundamental current is quite low, only 4.3 $\mathrm{A_{rms}}$. And the result here also excludes the effect of partial harmonic rejection from the current controller in an actual converter.



(a)



(b)

Fig. 18. Photos of a 650-V_{DC} GaN-based three-phase Vienna-type rectifier. (a) Power stage. (b) Three ac input boost inductors.

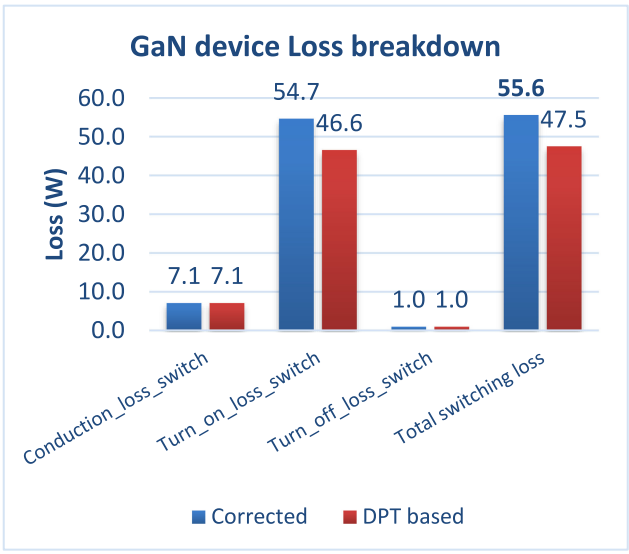


Fig. 19. Comparison of the calculated device losses with and without correction of the disclosed effect in a Vienna-type rectifier. (Actual turn-OFF loss is negligible.)

VI. Experimental Verification

A. Switching Loss Impact in Vienna-Type Rectifier

A Vienna-type rectifier variant (c) has been built to verify the loss impact, as shown in Fig. 18, where each phase leg consists of two 650-V anti-series connected GS66508P GaN devices to from the directional switch and two 1200-V Cree SiC diodes.

The calculated switching losses without and with considering the identified effect are 47.5 and 55.6 W, respectively, as indicated in Fig. 19, under 450 kHz, 115 V_{rms}, 650 V_{DC}, and 1.5 kW power, based on E_{on} and E_{off} data from a conventional half-bridge DPT reported in [27]. The energy equivalent junction capacitances of GaN device and two diodes are also derived for this estimation. Additionally, associated loss from heatsink coupled capacitances and other minor losses are included in both cases as the baseline. As clearly shown, the pure turn-OFF loss is very small, confirming the validity of ignoring its extra loss from the capacitance of the non-active device.

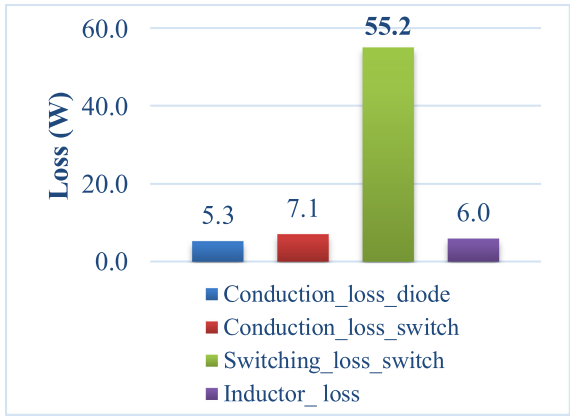


Fig. 20. Measured converter losses under the experimental condition 1.5 kW, 450 kHz.

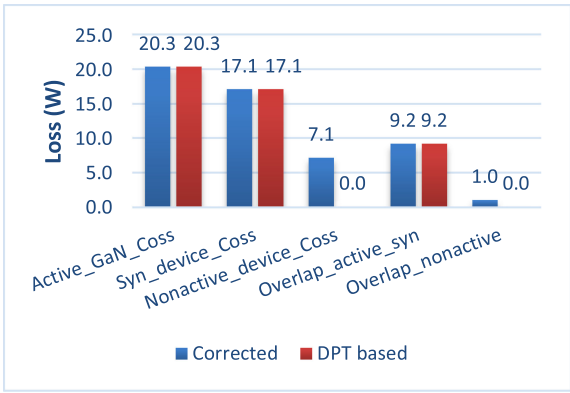


Fig. 21. Turn-ON switching loss breakdown.

The actual power loss of the converter was measured using Yokogawa power analyzer PZ4000 and given in Fig. 20. It is evident that the predicted total switching loss after adding the extra C_{oss} is 55.6 W, very close to the actual switching loss 55.2 W, and the impact from the non-active device is 8.1 W. Further breakdown of the turn-ON switching loss is given in Fig. 21 including the C_{oss} loss of active GaN devices, the high-frequency synchronous diodes, and non-active diodes, and the overlap loss, where the extra overlap loss introduced by the non-active diodes is only 1.0 W, whereas the extra C_{oss} loss is 7.1 W.

B. Overvoltage Impact in ANPC Inverter

The overvoltage stress effect is verified in a SiC MOSFET based ANPC prototype, operated at 1-kV/10-kW/280-kHz switching frequency, as shown in Fig. 22. Two versions of PCB layout designs are tested. In the original design as given in Fig. 12(a), without considering the additional commutation loop effect,

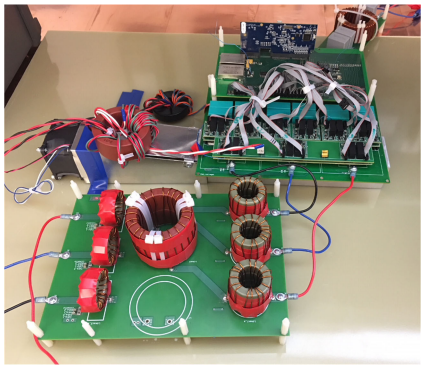


Fig. 22. Prototype photo of SiC MOSFET based 3L-ANPC.

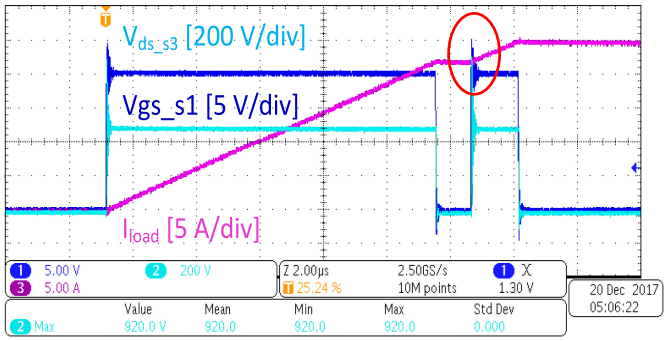


Fig. 23. High device overvoltage observed in pulse test with original power loop layout at 1-kV dc bus voltage.

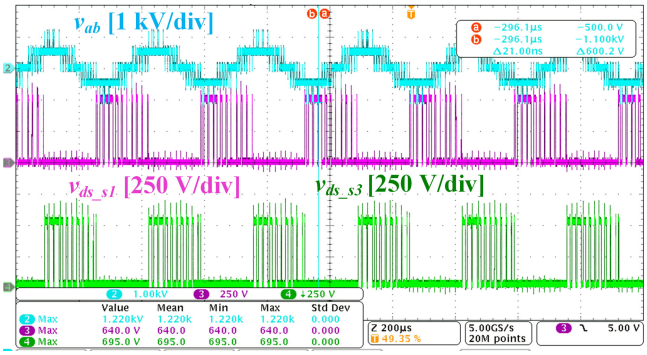


Fig. 24. Device overvoltage observed in ANPC continuous operation with improved layout at 1-kV dc bus voltage.

57.5-nH loop inductance associated with the line-frequency switch S_3 is introduced and its voltage spike is up to 920 V, as given in Fig. 23. Due to the 84% higher voltage spike compared to its 500-V steady-state voltage, the device switching speed has to slow down to safely operate the converter at the rated bus voltage.

With the improved PCB layout as shown in Fig. 12(b), the commutation loop inductance associated with the line-frequency device has been reduced to 12.4 nH, more than four times drop. Consequently, the maximum overvoltage of the line-frequency switch S_3 over a line cycle has decreased to 695 V, as shown in Fig. 24. And its alleviated drain-source voltage resonance is clearly shown in a zoomed-in waveform recorded at an arbitrary phase angle, as given in Fig. 25.

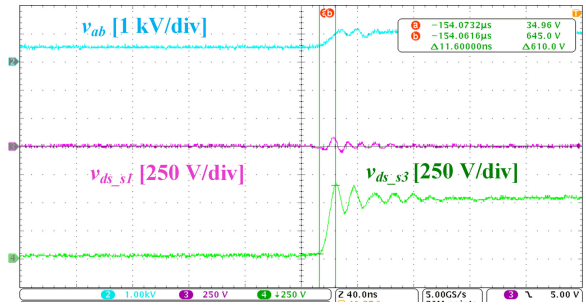


Fig. 25. Zoomed-in switching transient with improved layout at 1-kV dc bus voltage.

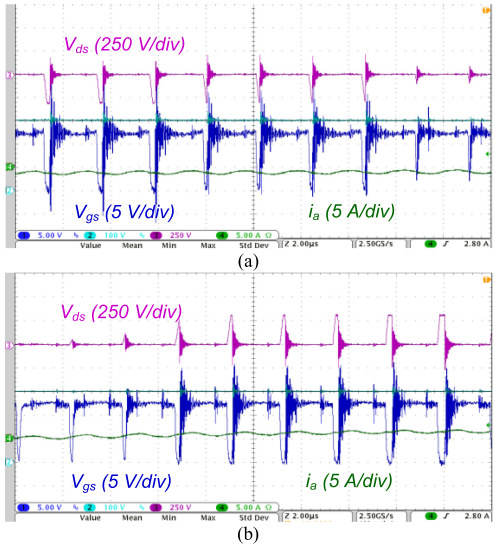


Fig. 26. Experimental waveforms of voltage distortion. (a) Before zero crossing. (b) After zero crossing.

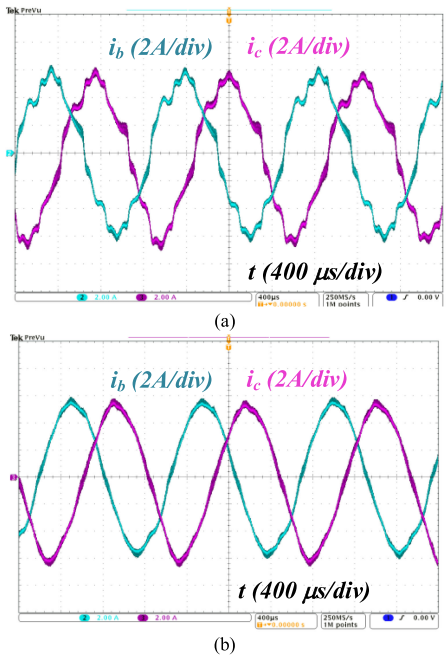


Fig. 27. Experimental comparison of current quality with and without the proposed compensation scheme at 450 kHz, 115 V_{rms}, and 600 V_{DC}. (a) i_b and i_c current without compensation. (b) i_b and i_c current with compensation.

C. AC Voltage/Current Distortion and Compensation in Vienna-Type Rectifier

The effect on PWM voltage distortion by the $C_{\rm oss}$ charging at the turn-OFF transient of the Vienna-type rectifier is given in Fig. 26, indicating that the worst distortion indeed appears at the zero crossings of the ac input current.

Without voltage error compensation, an obvious distortion was observed in the input currents, consisting of 6 k $\pm$ 1-order harmonics due to the significant distortion around six zero crossings of the three phases, as shown in Fig. 27. After applying the proposed scheme, those harmonics were significantly reduced, and the current THD drops from 10.3% to 3.0%.

VII. Conclusion

This paper identified extra junction capacitances and communication loops caused by non-conducting devices in each half line cycle. Their impacts on switching loss, device stress, and converter voltage/current distortion on different types of 3L topologies are analyzed. The extra switching loss is dominated by the $C_{\rm oss}$-type loss for high-speed WBG device based converters, whereas the overlap-type loss might also be considerably high if using low-speed devices. This highlights the necessity of three-level phase leg DPT aiding the future 3L converter design. The proposed loss estimation through traditional DPT data successfully predicts 17% extra switching loss, providing an efficient way to correct the 3L converter loss for sufficient thermal design. The likely 100% or even higher device overvoltage induced by the extra communication loops has urged caution and requirement on optimal power loop layout in high switching speed 3L converters. An improved PCB layout for an ANPC converter has achieved four times reduction of this loop inductance and 50% reduction of the device overvoltage. Exacerbated ac voltage/current distortion due to $C_{\rm oss}$ charging during turn-OFF or dead time transition further affects converter power quality of 3L topologies, especially for phase-leg with diode-switch-diode configuration and for high switching frequency applications. Presented modeling and compensation methods have set an example in evaluation and mitigation of this impact, reducing THD from 10.3% to 3.0%. The analytical modeling of the THD as a function of switching frequency and dc bus voltage can help optimize the converter parameter selection.

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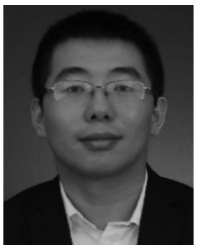
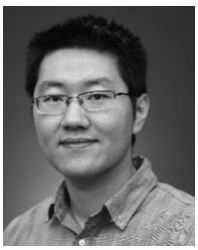


Bo Liu (S'11–M'18) received the B.S. and M.S. degrees from Xi'an Jiaotong University, Xi'an, China, and the Ph.D. degree from The University of Tennessee, Knoxville, TN, USA, in 2009, 2012, and 2018, respectively, all in electrical engineering.

His research interests include wide bandgap device based high-frequency high-density converters for aircraft application, conducted EMI, power quality control, high-power transmission systems, power grid emulation, and grid-tied solar inverters.



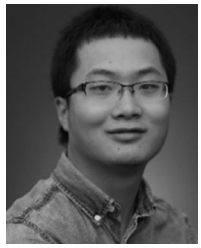
Ren Ren (S'14) received the B.S. degree in electrical engineering, in 2012, from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, where he has been working toward the Ph.D. degree in electrical engineering since 2012. Since 2017, he has been working toward the Ph.D. degree in electrical engineering at The University of Tennessee, Knoxville, TN, USA.

His research interests include high-frequency converters design using wide bandgap devices, design optimization and automation in power electronics, soft-switching resonant converters, and high-frequency digital control.

Edward A. Jones (S'12–M'18) received the B.S. degree from Virginia Tech, Blacksburg, VA, USA, in 2007, and the M.S. and Ph.D. degrees from The University of Tennessee, Knoxville, TN, USA, in 2016 and 2017, respectively.

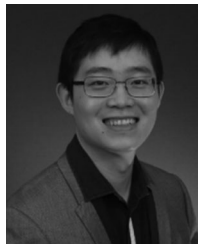
He is currently with the Efficient Power Conversion Corporation as a Senior Applications Engineer, designing converters that highlight the performance benefits of GaN FETs and helping customers do the same.

He has authored or coauthored more than 20 journal and conference papers, a professional education seminar, a patent, and the book *Characterization of Wide Bandgap Power Semiconductor Devices* (IET, 2018).



Handong Gui (S'14) received the B.S. and M.S. degree in electrical engineering from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2013 and 2016, respectively. He is currently working toward the Ph.D. degree at the University of Tennessee, Knoxville, TN, USA.

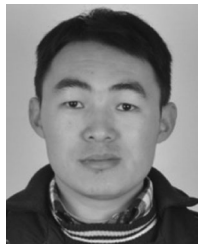
His research interests include the widebandgap device applications, multi-level converters, and battery management systems.



Zheyu Zhang (S'12–M'15) received the B.S. and M.S. degrees from Huazhong University of Science and Technology, Wuhan, China, and the Ph.D. degree from The University of Tennessee, Knoxville, TN, USA, in 2008, 2011, and 2015, respectively, all in electrical engineering.

He is a Lead Power Electronics Engineer with the General Electric Global Research, Niskayuna, NY, USA. He was a Research Assistant Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, from 2015 to 2018. He has authored/coauthored more than 60 papers in the most prestigious journals and conference proceedings, four patent applications with one licensed, and two IEEE tutorial seminars. His research interests include wide bandgap power electronics, cryogenic power electronics, highly efficient, ultra-dense, cost-effective power conversion systems for aircrafts, renewables, and energy storage systems.

Dr. Zhang was the recipient of two prize paper awards from the IEEE Industry Applications Society and IEEE Power Electronics Society. He currently serves as Associate Editor for IEEE Transactions on Industry Applications.



Ruirui Chen (S'15) received the B.S. degree from the Huazhong University of Science and Technology, Wuhan, China, and the M.S. degree from Zhejiang University, Hangzhou, China, in 2010 and 2013, respectively. He is currently working toward the Ph.D. degree at The University of Tennessee, Knoxville, TN, USA.

From 2013 to 2015, he was an Electrical Engineer with FSP-Powerland Technology, Inc., China. His research interests include high-density high-power motor drives, three-phase converter designs, parallel operation, and EMI filter techniques.

Fei (Fred) Wang (S'85–M'91–SM'99–F'10) received the B.S. degree from Xi'an Jiaotong University, Xi'an, China, and the M.S. and Ph.D. degrees from the University of Southern California, Los Angeles, CA, USA, in 1982, 1985, and 1990, respectively, all in electrical engineering.

He was a Research Scientist with the Electric Power Laboratory, University of Southern California, from 1990 to 1992. He joined the GE Power Systems Engineering Department, Schenectady, NY, USA, as an Application Engineer in 1992. From 1994 to 2000, he was a Senior Product Development Engineer with GE Industrial Systems, Salem, VA, USA. During 2000 to 2001, he was the Manager of the Electronic and Photonic Systems Technology Laboratory, GE Global Research Center, Schenectady, NY, and Shanghai, China. In 2001, he joined the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, as a Research Associate Professor and became an Associate Professor in 2004. From 2003 to 2009, he also served as the CPES Technical Director. Since 2009, he has been with The University of Tennessee and Oak Ridge National Laboratory, Knoxville, TN, USA, as a Professor and the Condra Chair of Excellence in Power Electronics. He is a Founding Member and the Technical Director of the Multi-University NSF/DOE Engineering Research Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks led by The University of Tennessee. His research interests include power electronics, power systems, controls, electric machines and motor drives.

Dr. Wang is a fellow of the U.S. National Academy of Inventors.

Daniel Costinett (S'10–M'13) received the B.S. and M.S. degrees in 2011, and the Ph.D. degree in 2013 from the University of Colorado Boulder, Boulder, CO, USA.

Since 2013, he has been an Assistant Professor with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville (UTK), Knoxville, TN, USA. Prior to joining UTK, he was an instructor with Utah State University in 2012. He is also a Joint Faculty with the Power Electronics and Electric Machinery Research Center, Oak Ridge National Laboratory, Oak Ridge, TN. His research interests include resonant and soft switching power converter designs, high efficiency wired and wireless power supplies, on-chip power conversion, medical devices, and electric vehicles.

Dr. Costinett is currently the Co-Director of Education and Diversity with the National Science Foundation/Department of Energy Research Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks. He currently serves as an Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and the IEEE TRANSACTIONS ON POWER ELECTRONICS.