Digital Closed-Loop Control Strategy to Maintain the Phase Shift of a Multi-Channel BCM Boost Converter for PFC Applications

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***Abstract*—This paper presents a novel closed-loop digital control scheme to maintain proper interleaving operation of a multi-channel boundary-conduction-mode boost converter used in power-factor-correction applications. The proposed control scheme is suitable for implementation on a low-cost microcontroller. This is made possible by executing the control scheme at a constant sampling rate that is much slower than the maximum switching frequency of the converter. The performance of the control scheme is further improved by using an adaptive gain that scales with the ON-time of the converter, which provides optimal phase-shift control and stability under all operating conditions. The digital closed-loop control scheme is validated experimentally on a three-channel 1-kW prototype ac–dc converter. The converter has an output voltage of 400 V and a universal input voltage range of 85–265 V. The prototype converter uses a low-cost microcontroller while demonstrating correct interleaving operation.**

***Index Terms*—Boundary-conduction mode, critical-conduction mode, interleaved boost converter, power factor correction (PFC), valley switching.**

NOMENCLATURE

v_{line}	Input line voltage.
v_{in}	Rectified input voltage.
v_{gs}	Gate–source voltage.
v_{gs_n}	Gate–source voltage of the nth channel.
v_o	Output voltage.
V_{EA}	Error-amplifier output voltage.
V_{EA_n}	Adjusted error-amplifier output voltage.
v_{ramp}	Analog PWM-generation ramp voltage.
v_{ds}	MOSFET drain–source voltage.
v_{zcd}	ZCD-circuit output voltage.
v_L	Boost-inductor voltage.
i_{line}	Input line current.

Manuscript received August 29, 2018; accepted September 25, 2018. Date of publication October 9, 2018; date of current version May 2, 2019. This work was supported by the Irish Research Council under the project EPSPG/2015/112. Recommended for publication by Associate Editor F. J. Azcondo. *(Corresponding author: Robert T. Ryan.)*

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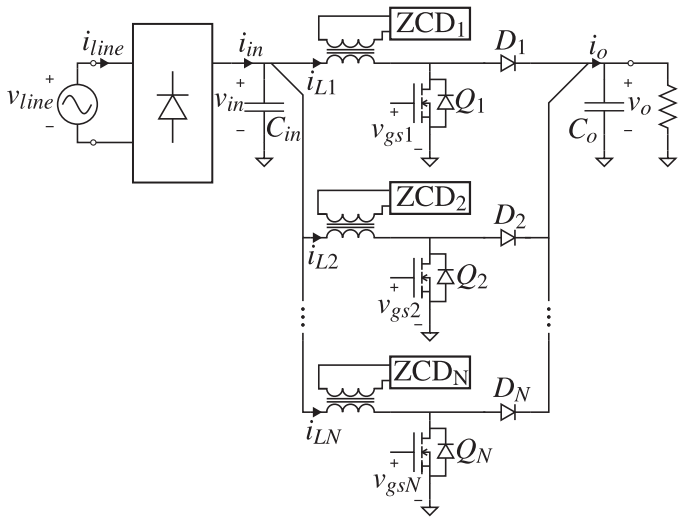

Fig. 1. Simplified circuit schematic of a multi-channel BCM boost converter.

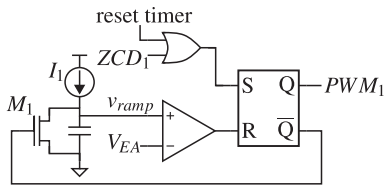

Fig. 2. PWM generation of the master channel using analog circuitry.

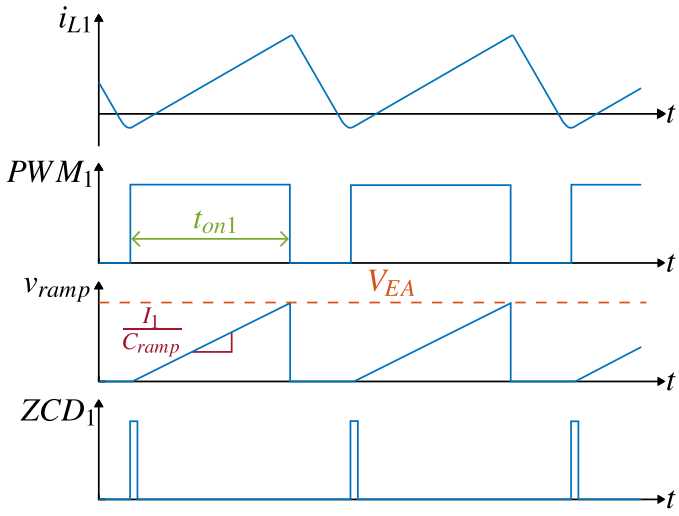

Fig. 3. Master channel constant-on-time PWM generation using analog circuitry.

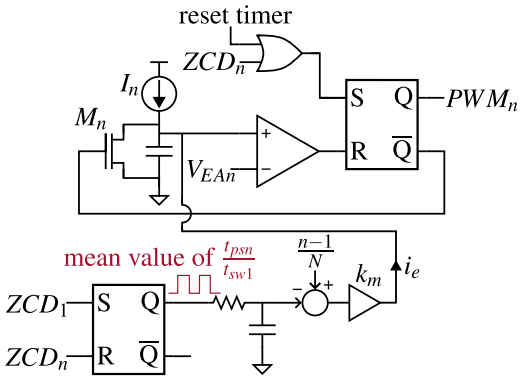

Fig. 4. Phase-shift control and PWM generation of a single slave channel using analog circuitry with the PLL method and turn-OFF adjustment by altering the PWM generation ramp signal.

requiring the converter to use a large DM EMI filter. Interleaving to create a two-channel BCM boost converter is a common technique used to reduce the input-current ripple, thus extending the power level of the BCM boost converter to 600 W [5]. For higher power levels, the continuous-conduction mode (CCM) boost converter becomes more advantageous, due to its naturally low input-current ripple and low peak inductor current [6]. The use of the BCM topology can be extended to higher power levels by interleaving more channels together. In this paper, a closed-loop digital control scheme is designed for maintaining correct interleaving operation of a multi-channel BCM boost converter shown in Fig. 1.

A. Existing Analog Closed-Loop Solutions

Fig. 2 demonstrates how the PWM signal PWM$_1$ that controls MOSFET Q_1 is generated for the master channel using analog circuitry and constant-on-time control (COTC) [2]. Fig. 3 shows the corresponding timing diagram for the circuit. The signal PWM$_1$ is set by the signal ZCD$_1$, which is created by a zero-current-detection (ZCD) circuit. The ZCD circuit detects when the energy stored in the drain–source capacitor of Q_1 has discharged back into the input capacitor $C_{\rm in}$. This causes the inductor current i_{L_1} to become negative before the turn-ON instant of the switch. The switch is turned OFF after an ON-time of $t_{\rm on_1}$ has elapsed. This is implemented by using the constant-current source I_1, transistor M_1, and a capacitor to make a ramp signal that is compared to the voltage $V_{\rm EA}$, to trigger the switch's turn-OFF instant. The voltage denoted $V_{\rm EA}$ is the output of the voltage error amplifier, which is proportional to the ON-time and is adjusted by the voltage compensator to maintain the output voltage at its setpoint value.

For the correct interleaving operation of a multi-channel BCM boost converter, a phase shift of $\frac{n-1}{N} \times 360^\circ$ must be maintained between the inductor currents of each channel, where N is the number of boost converter channels that are enabled, and n is the index number of a particular channel. However, the switching frequency of the BCM boost converter varies with input voltage and output power [7]. This makes interleaving of a multi-channel BCM boost converter a challenging design task.

In existing analog solutions [8]–[11], the phase shift is sensed and a feedback network is formed to adjust the turn-OFF instant of the slave channel MOSFET to maintain the desired phase shift. The closed-loop method uses ZCD circuits to trigger MOSFET turn-ON of all interleaved channels, thus ensuring perfect valley switching of all switches under all conditions, and therefore, lower switching losses. Using a separate ZCD circuit for each channel also ensures the converter cannot enter CCM, which may cause damage to components. The phase-locked-loop (PLL) method is a commonly adopted analog closed-loop control scheme [8], [11]. This method is shown in Fig. 4. In this method, the phase shift is sensed by passing the ZCD signals of

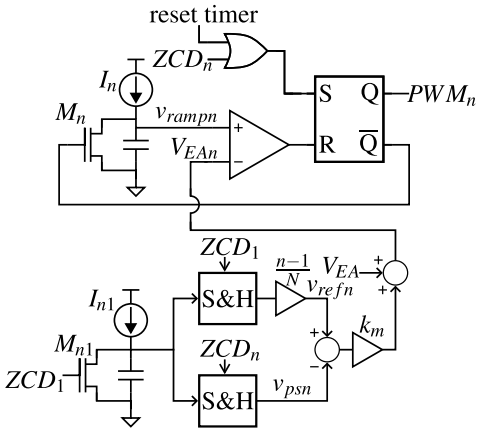

Fig. 5. Phase-shift control and PWM generation of a single slave channel using analog circuitry with the closed-loop method and turn-OFF adjustment by altering the voltage error amplifier signal.

the master and slave channels through a flip flop. This creates a square wave with a mean value proportional to the ratio of the phase shift of the nth channel t_{ps_n} to the switching period t_{sw_1} of the master channel. This square wave is passed through an *RC* low-pass filter and subtracted from a constant voltage setpoint proportional to $\frac{n-1}{N}$ to create an error signal. The current i_e is then generated proportional to the error signal, and is used to adjust the turn-OFF instant of the slave channel by adjusting the slope of the v_{ramp_n} signal used in the PWM generation. Selecting the correct gain value for k_m ensures the phase shift tracks the desired setpoint. The turn-OFF instant of the slave channel can also be adjusted by adding a voltage to the V_{EA} signal of the slave channel.

The downside of the PLL method is that the use of the low-pass filter to sense the phase shift leads to a slow dynamic response of the control loop and can lead to significant phase error. In [10], a closed-loop scheme is adopted where the phase shift and switching period are sensed using sample-and-hold blocks. This method is more advantageous than the closed-loop PLL method as it does not require low-pass filtering of the sensed phase shift, thus improving the tracking performance of the control loop. This method is depicted in Fig. 5. The constant current source I_{n_1}, transistor M_{n_1}, and ramp capacitor are used to generate a ramp signal. This ramp signal is then fed into two separate sample-and-hold blocks triggered by ZCD_1 and ZCD_n. The output of the sample-and-hold triggered by ZCD_1 is a voltage proportional to the switching period of the master channel. The signal is scaled by the factor $\frac{n-1}{N}$ to generate the reference signal of the control loop, and is denoted v_{ref_n}. The output of the sample-and-hold block triggered by ZCD_n is a voltage proportional to the current phase shift between the master channel and the n^{th} slave channel. This voltage is denoted v_{ps_n}. An error signal is generated by subtracting v_{ps_n} from v_{ref_n}. A closed feedback loop is formed by adjusting the error signal by a gain of k_m, and adding the signal to the voltage error signal to adjust the switches turn-OFF instant. It is also possible to adjust the switches turn-OFF instant by adjusting the slope of the PWM ramp signal of the slave converter, as shown in Fig. 4.

B. Other Existing Solutions

It is also possible to interleave multiple channels of a BCM boost converter using an open-loop method [12]–[14]. The open-loop method works by assigning one of the interleaved channels as the master and the others as the slaves. The master works as a standalone converter with its own ZCD circuit, therefore, the master channels MOSFET turn-ON instant is always triggered by it's own ZCD circuit. The turn-ON instants of the MOSFETs in the slave channels are obtained by delaying the ZCD signal of the master channel with a time delay of $\frac{n-1}{N} \times t_{\mathrm{sw}_1}$. The open-loop method suffers from severe subharmonic oscillations when implemented using voltage-mode control for duty cycles greater than 0.5 [14], meaning that it must be implemented with current-mode control that requires additional sense circuitry. The slave converter must have a lower inductance than the master channel to prevent it entering into CCM. As a result, the open-loop method also requires the ability to sense which channel has the lowest inductance. If there is only a small mismatch in the boost inductance of each channel, the slave converter operates slightly in DCM, and valley switching is ensured. However, if there is significant mismatch between the boost inductances of both channels, the slave channel operates in DCM and loses its valley-switching operation.

Several examples of digitally controlled interleaved BCM boost converters already exist in the literature. These examples maintain their phase shift by either open-loop master–slave control [15], or by the use of feedforward algorithms to estimate the converter's switching period [16], however, this method also does not ensure the BCM operation and valley switching if the system is disturbed.

There are very few examples of three-channel interleaved BCM boost converters [16], [17] described in the literature, compared with two-channel interleaved BCM boost converters [8]–[15]. Similarly, although there are many commercially available analog PFC control integrated circuits (ICs) available in the market for two-channel BCM boost converters, such as the FAN9611, UCC28063, and NCP1631, there are currently no PFC control ICs for more than two channels. Using a digital microcontroller makes it possible to build an interleaved BCM boost converter with more than two channels, provided that the microcontroller has sufficient suitable peripherals for the number of channels.

C. Proposed Digital Closed-Loop Solution

In this paper, a digital closed-loop solution is proposed to maintain the correct phase shifts for a multi-channel BCM boost converter. The last few decades have seen significant improvement in microcontroller and digital-signal-processor technologies, with better CPUs and dedicated power electronics peripherals at lower costs. Digital microcontroller technology is also less prone to temperature and process variations. Digital control also gives the designer much more design flexibility, for instance, in [2], the output voltage transient response of a two-channel BCM boost converter is improved with digital control by using an adaptive gain to increase the systems bandwidth at

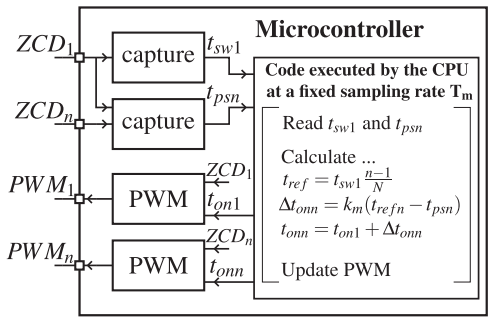

Fig. 6. Phase-shift control and PWM generation of the master and a single slave channel using digital circuitry with the closed-loop method and turn-OFF adjustment made by altering the slave channels ON-time.

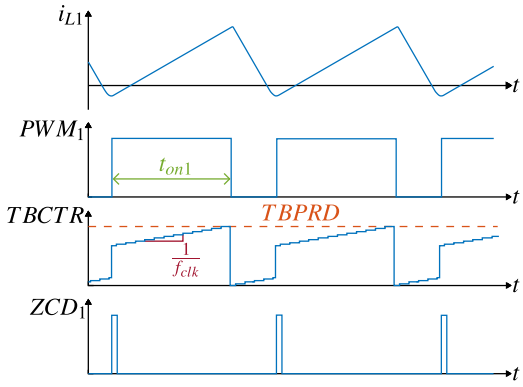

Fig. 7. Timing diagram for the PWM generation of the master channel using digital circuitry.

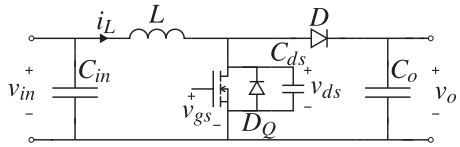

Fig. 8. Single channel of the interleaved boost converter including the MOSFET drain–source capacitance and body diode.

low input voltage. These advantages have led to the widespread adoption of digital control by power supply designers [18].

The implementation of the phase-shift feedback control, and the PWM generation of the master and a single slave channel, as described in this paper, is shown in Fig. 6. The switching period of the master channel is measured by feeding the ZCD_1 signal of the master channel into a capture peripheral on the microcontroller. The capture peripheral has a digital timer independent of the CPU that can be used to measure the time between the ZCD pulses. As a result, it is possible to measure the switching period of the master channel every switching period. This is equivalent to the sample-and-hold method used in the analog solution of Fig. 6. The feedback control is accomplished by executing a feedback algorithm in the microcontroller CPU. The feedback algorithm reads the sensed switching period and phase shift from each capture peripheral. It then calculates the reference for each slave channel t_{ref_n} based on the sensed switching period of the master channel. The phase-shift error is determined by subtracting the sensed phase shift from the reference phase shift. The phase-shift error is used to adjust the ON-time of each channel to ensure the desired phase shift is maintained. This method uses a similar feedback control as the analog solution shown in Fig. 6. The analog solution has an advantage that the turn-OFF instant of the slave channels are updated by the feedback network on every switching cycle. Attempting to update the turn-OFF instant of the microcontroller cycle-by-cycle requires a very expensive microcontroller. This is because the phase-shift algorithm executed by the CPU would have to run in an interrupt every switching instance, and therefore, the microcontroller needs to execute the phase-shift control algorithm faster than the minimum switching period of the boost converter. This would require a microcontroller with a powerful CPU and high clock frequency, which is more expensive. A better solution is to run the phase-shift control algorithm at a fixed sampling period T_m, which is much lower than the minimum switching period of the converter. This enables a much cheaper microcontroller to be used.

The microcontroller uses a compare or PWM peripheral to generate the PWM signals of each boost converter channel. The timing diagram of Fig. 7 demonstrates how the PWM peripheral for each channel is configured. The PWM signal is configured to turn ON when the counter register of the PWM timer TBCTR has a value of $\mathrm{TBPRD} - t_{\mathrm{on}_n}$, where TBPRD is the constant value stored in the period register of the PWM peripheral. The PWM peripheral is also configured to load the TBCTR register with a value of $\mathrm{TBPRD} - t_{\mathrm{on}_n}$ when the ZCD signal is triggered. When the TBCTR reaches a value of TBPRD, the PWM signal is set low, and the counter restarts. Using this method results in the PWM signal of each channel having a natural reset timer. If the ZCD signal is not triggered, the TBCTR continues counting until it reaches a value of $\mathrm{TBPRD} - t_{\mathrm{on}_n}$. This method is helpful as sometimes the ZCD signal is not triggered, for instance, during converter start-up or at very light load when the ON-time becomes zero.

This paper is divided into four different sections as follows. Section I provides a brief review of how the valley-switching operation works and how it reduces power losses. Section II describes the operation and design of the phase-shift control loop. Section IV demonstrates the experimental results of a prototype 1-kW multi-channel BCM converter, demonstrating correct interleaving action for two-channel operation and three-channel operation.

II. Valley Switching

The main advantage of using a closed-loop control scheme to maintain the correct phase shifts is that each channel has its own ZCD circuit that ensures valley-switching operation is always maintained. This reduces switching losses. The valley switching of the BCM converter can be explained by looking at a single channel of the boost converter with the MOSFET drain–source capacitance C_{ds}, as shown in Fig. 8.

Figs. 9 and 10 show the behavior of the drain-to-source voltage v_{ds} and inductor current i_L during MOSFET turn-OFF. As the inductor current discharges to zero, the diode D is forward biased, therefore, $v_{\mathrm{ds}} = v_o$, where v_o is the output voltage. Once

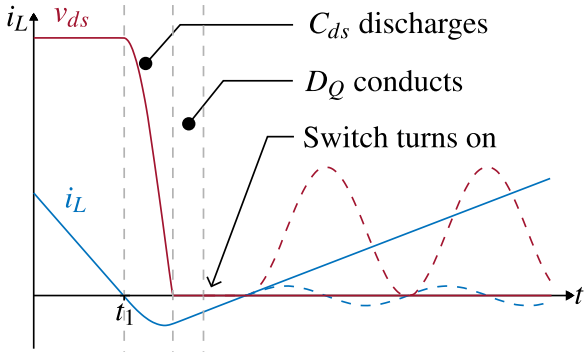

Fig. 9. Zero-voltage switching $v_{\rm in} < \frac{1}{2}v_o$.

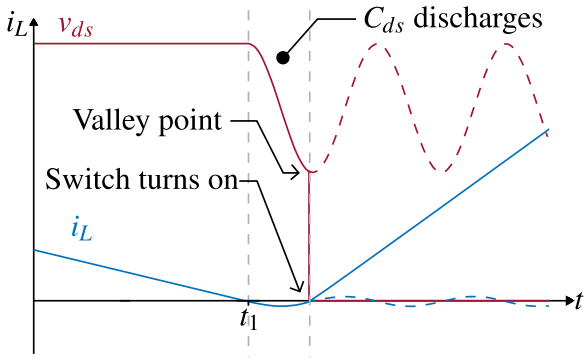

Fig. 10. Near-zero-voltage switching $v_{\rm in} > \frac{1}{2}v_o$.

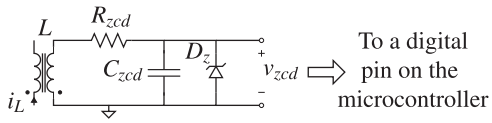

Fig. 11. Zero-current-detection circuit.

i_L reaches zero, the MOSFET remains OFF, and the capacitance $C_{\rm ds}$ begins to discharge through boost inductor L into the input capacitor $C_{\rm in}$. During this region, $i_L(t)$ and $v_{\rm ds}(t)$ can be described using (1) and (2), respectively, where the time t_1 is defined in Figs. 9 and 10

$$i_L(t) = -\omega_r C_{\rm ds}(v_o - v_{\rm in})\sin(\omega_r(t-t_1)) \tag{1}$$

$$v_{\rm ds}(t) = v_{\rm in} + (v_o - v_{\rm in})\cos(\omega_r(t-t_1)) \tag{2}$$

where $v_{\rm in}$ is the input voltage and $\omega_r = 1/\sqrt{LC_{\rm ds}}$ is the circuit's resonant frequency. Zero-voltage switching is achieved when $v_{\rm in} < \frac{1}{2}v_o$. Once $v_{\rm ds}$ fully discharges to 0 V, the negative inductor current forces the MOSFET's body diode D_Q to conduct. The ZCD circuit then triggers the switch to turn ON while $v_{\rm ds} = 0$, as shown by the solid lines of Fig. 9. If the MOSFET remains OFF, the circuit enters DCM, as shown by the dashed lines of Fig. 9.

If $v_{\rm in} > \frac{1}{2}v_o$, then $C_{\rm ds}$ does not fully discharge, but instead reaches a valley at $v_{\rm ds} = 2v_{\rm in} - v_o$, as shown in Fig. 10. The ZCD ensures that the switch turns ON at this valley to minimize the switching losses.

The valley switching is achieved in the experimental prototype by using the ZCD circuit shown in Fig. 11. The ZCD

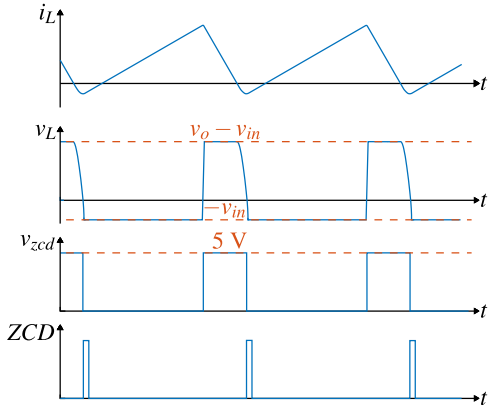

Fig. 12. Timing diagram for the ZCD generation.

circuit consists of an auxiliary winding on the boost inductor, a current-limiting resistor $R_{\rm zcd}$, a capacitor $C_{\rm zcd}$ that adds a small amount of low-pass filtering, and a zener diode D_z that clamps the voltage $v_{\rm zcd}$ to between 0 and 5 V, so that it can be input to a microcontroller pin. Fig. 12 shows a timing diagram of the inductor current, inductor voltage v_L, and the voltage $v_{\rm zcd}$ created by the ZCD circuit. The voltage $v_{\rm zcd}$ is a square wave, with a falling edge that corresponds to the instant the boost converter MOSFET should be turned ON to achieve valley switching. The voltage $v_{\rm zcd}$ is connected to a regular digital pin on the microcontroller, and the PWM peripheral is configured to trigger MOSFET turn-ON on a falling edge of this signal. This method is advantageous because it does not require a comparator, which makes the implementation cheaper. Requiring an external comparator would add cost and, also, any available comparators in the microcontroller can now be used for safety functions, such as overvoltage and overcurrent protections.

Fig. 13 shows experimental results of the prototype converter operating in BCM with valley switching when $v_{\rm in} = 100$ V and $v_{\rm in} = 300$ V.

III. Phase-Shift Control

In this section, the design of the phase-shift control algorithm is discussed. The phase-shift control is responsible for maintaining the correct phase shift between the boost inductor currents.

The output voltage of the boost converter described in this paper is regulated using COTC [2]. By this method, the sensed output voltage is subtracted from a constant reference to generate an error signal, which is input to a voltage compensator. The voltage compensator calculates the required ON-time $t_{\rm on}$ so that the output voltage tracks the reference signal.

The time-averaged input-current drawn by the converter can be calculated using the following:

$$i_{\rm in} = \frac{N}{2}\frac{v_{\rm in}}{L}t_{\rm on}. \tag{3}$$

Given that N and L are constant in (3), the converter has near unity power factor provided $t_{\rm on}$ is near constant, therefore, $i_{\rm in}$ equals a constant multiplied by $v_{\rm in}$. This is the basis of COTC.

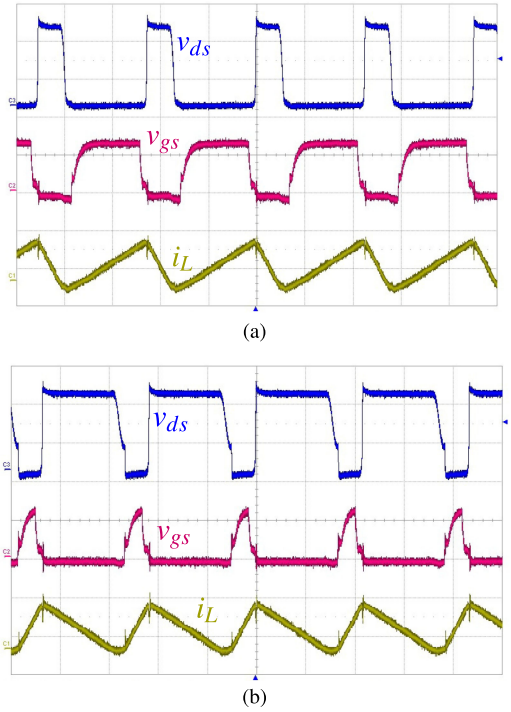

Fig. 13. $v_{\rm ds}$, $v_{\rm gs}$, and i_L waveforms showing valley switching for (a) $v_{\rm in}$ = 100 V and (b) $v_{\rm in}$ = 300 V ($v_{\rm ds}$: 200 V/div, $v_{\rm gs}$: 10 V/div, i_L: 2 A/div, time base : 2 μs/div).

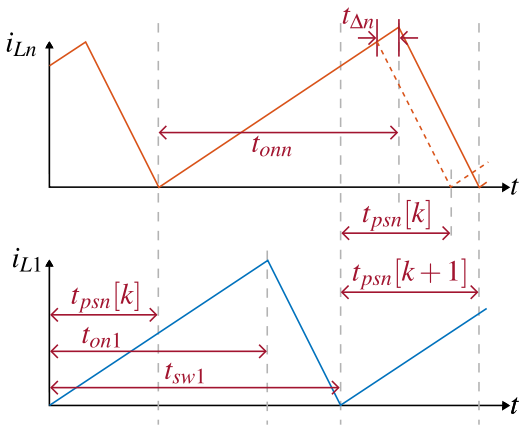

Fig. 14. Change in phase shift due to an ON-time perturbation t_{Δ_n}.

The phase-shift control algorithm takes the ON-time calculated by the voltage compensator and adjusts it to calculate the individual ON-time for each channel of the converter to maintain the desired phase shift between the different channels.

A. System Model

To design the phase-shift control algorithm, it is necessary to first develop a mathematical system model describing how adding a perturbation of t_{Δ_n} to the individual ON-time of a slave channel effects the phase shift $t_{\rm ps_n}$ between the master and the n_{th} slave channel of the converter. The effect of adding the perturbation t_{Δ_n} to $t_{\rm on_n}$, so that $t_{\rm on_n} = t_{\rm on_1} + t_{\Delta_n}$ is shown in Fig. 14 over a single switching cycle of the inductor currents i_{L_1} and i_{Ln}. In order to simplify our analysis, it is assumed that the

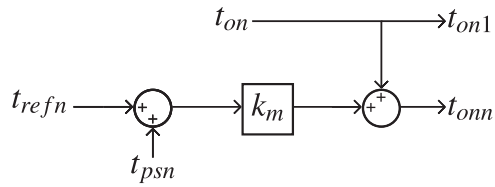

Fig. 15. Phase-shift control loop block diagram structure.

effects of the resonance between the boost inductor and MOSFET drain–source capacitance are negligible. If $t_{\rm ps_n}[k]$ is the phase shift between the master and $n_{\rm th}$ slave channel during the kth switching cycle, the phase shift of the $(k+1)$th switching cycle can be calculated by

$$t_{\rm ps_n}[k+1] = t_{\rm ps_n}[k] + \frac{t_{\Delta_1} t_{\rm sw_1}}{t_{\rm on_1}} \tag{4}$$

where $t_{\rm sw_1}$ is the switching period of the master channel. This change in the phase shift is graphically displayed in Fig. 14.

By expanding (4) over a total of K switching cycles, the phase shift of the $(k+K)$th switching cycle can also be calculated by (5), where it is assumed that $t_{\rm sw_1}$ and $t_{\rm on_1}$ remain constant over the K switching cycles

$$t_{\rm ps_n}[k+K] = t_{\rm ps_n}[k] + K\frac{t_{\Delta_n} t_{\rm sw_1}}{t_{\rm on_1}}. \tag{5}$$

The open-loop system model is now described by (5). This equation is in the following section to design a closed feedback loop to control the phase shift $t_{\rm ps_n}$.

B. Closed-Loop Control

Closed-loop control is used to ensure that the phase shift $t_{\rm ps_n}$ tracks a reference phase shift $t_{\rm ref_n}$. Fig. 15 shows the proposed structure of the phase-shift control loop. The error signal given by $t_{\rm ref_n} - t_{\rm ps_n}$ is multiplied by the gain k_m to form a proportional controller, and the result is added to the ON-time $t_{\rm on_1}$ to give the ON-time $t_{\rm on_n}$ for that slave channel.

The value of k_m must be selected to obtain the best tracking performance while still ensuring the stability of the system under all operating conditions. Based on Fig. 15, the phase-shift control algorithm can be described by the following equation:

$$t_{\rm on_n} = t_{\rm on_1} + k_m\left(t_{\rm ref_n} - t_{\rm ps_n}[k]\right). \tag{6}$$

Substituting $t_{\Delta_n} = t_{\rm on_n} - t_{\rm on_1}$ into (6), the following expression is obtained:

$$t_{\Delta_n} = k_m\left(t_{\rm ref_n} - t_{\rm ps_n}[k]\right). \tag{7}$$

By combining (7) with the expression obtained earlier in (5), the effect the phase-shift control feedback has on the phase shift $t_{\rm ps_n}$ after K switching cycles can be obtained as follows:

$$t_{\rm ps_n}[k+K] = t_{\rm ps_n}[k] + Kk_m\frac{t_{\rm sw_1}}{t_{\rm on_1}}\left(t_{\rm ref_n} - t_{\rm ps_n}[k]\right). \tag{8}$$

The phase-shift control algorithm given in (6) is executed at a constant sampling rate, with a sampling period of T_m. A total of $K = T_m/t_{\rm sw_1}$ switching cycles occur over a single execution of the phase-shift control algorithm. A time-averaged

approximation is taken by substituting this value of k into (8). As a result, the value of the phase shift t_{ps_n} after a single execution of the algorithm can be obtained as follows:

$$t_{\mathrm{ps}_n}[i+1] - t_{\mathrm{ps}_n}[i] = k_m \frac{T_m}{t_{\mathrm{on}_1}}(t_{\mathrm{ref}_n} - t_{\mathrm{ps}_n}[i]) \tag{9}$$

where i is an integer number describing the number of executions of the phase-shift control algorithm that have taken place. For ideal phase-shift tracking, the value of t_{ps_n} after a single execution of the algorithm should equal t_{ref_n}. Therefore, (9) becomes

$$t_{\mathrm{ref}_n} - t_{\mathrm{ps}_n}[i] = k_m \frac{T_m}{t_{\mathrm{on}_1}}(t_{\mathrm{ref}_n} - t_{\mathrm{ps}_n}[i]). \tag{10}$$

By rearranging (10), the value of k_m that gives the best tracking performance can be calculated by

$$k_m = \frac{t_{\mathrm{on}_1}}{T_m}. \tag{11}$$

C. Phase-Shift Control Stability

The phase-shift control loop remains stable provided that after a single execution of the phase-shift control algorithm, the phase shift t_{ps_n} stays bound to the region $0 < t_{\mathrm{ps}_n} < t_{\mathrm{sw}_1}$. Rearranging (9), the following equation can be found to describe the phase shift t_{ps_n} after $(i+1)$ execution cycles of the control algorithm

$$t_{\mathrm{ps}_n}[i+1] = k_m \frac{T_m}{t_{\mathrm{on}_1}}(t_{\mathrm{ref}_n} - t_{\mathrm{ps}_n}[i]) + t_{\mathrm{ps}_n}[i]. \tag{12}$$

The phase shift $t_{\mathrm{ps}_n}[i]$ is bound to the region $0 < t_{\mathrm{ps}_n}[i] < t_{\mathrm{sw}_1}$. The worst case scenario occurs when either $t_{\mathrm{ps}_n}[i] = 0$ or $t_{\mathrm{ps}_n}[i] = t_{\mathrm{sw}_1}$. Looking first at the case where $t_{\mathrm{ps}_n}[i] = 0$, $t_{\mathrm{ps}_n}[i+1]$ is given by

$$t_{\mathrm{ps}_n}[i+1] = k_m \frac{T_m}{t_{\mathrm{on}_1}} t_{\mathrm{ref}_n}. \tag{13}$$

Applying this result to the inequality $0 < t_{\mathrm{ps}_n}[i+1] < t_{\mathrm{sw}_1}$, the following inequality can be obtained for the values of k_m for which the system is stable

$$0 < k_m < \frac{t_{\mathrm{on}_1}}{T_m}\frac{t_{\mathrm{sw}_1}}{t_{\mathrm{ref}_n}}. \tag{14}$$

Now, looking at the case where $t_{\mathrm{ps}_1}[i] = t_{\mathrm{sw}_1}$, $t_{\mathrm{ps}_n}[i+1]$ is given by

$$t_{\mathrm{ps}_n}[i+1] = k_m \frac{T_m}{t_{\mathrm{on}_1}}(t_{\mathrm{ref}_n} - t_{\mathrm{sw}_1}) + t_{\mathrm{sw}_1}. \tag{15}$$

Again, applying the result from (15) to the inequality $0 < t_{\mathrm{ps}_n}[i+1] < t_{\mathrm{sw}_1}$, a second inequality can be obtained for the values of k_m for which the system remains stable

$$0 < k_m < \frac{t_{\mathrm{on}_1}}{T_m}\frac{t_{\mathrm{sw}_1}}{t_{\mathrm{sw}_1} - t_{\mathrm{ref}_n}}. \tag{16}$$

The inequalities given in (14) and (16) now describe the values of k_m for which stability is achieved in terms of the tracking reference t_{ref_n}. The reference signal is calculated from the switching period t_{sw_1} by $t_{\mathrm{ref}_n} = t_{\mathrm{sw}_1}\frac{n-1}{N}$. Substituting this value for t_{ref_n} into the inequalities (14) and (16) gives the following:

$$0 < k_m < \frac{t_{\mathrm{on}_1}}{T_m}\frac{N}{n-1} \tag{17}$$

$$0 < k_m < \frac{t_{\mathrm{on}_1}}{T_m}\frac{N}{N-n+1}. \tag{18}$$

However, n is an integer number, with a value in the region $2 \le n \le N$. The strictest condition to satisfy (17) occurs when n is at its maximum value of $n = N$. Similarly for (18), the strictest condition occurs when n is at its minimum value of $n = 2$. Applying the strictest condition for n to both (17) and (18) results in the following single inequality:

$$0 < k_m < \frac{t_{\mathrm{on}_1}}{T_m}\frac{N}{N-1}. \tag{19}$$

For two-channel operation $N = 2$, therefore, k_m must satisfy $0 < k_m < 2\frac{t_{\mathrm{on}_1}}{T_m}$ to remain stable. Fig. 16 demonstrates the wave shape of the input current drawn by the converter in two-channel operation when k_m satisfies the stability inequality and when k_m is increased so that it no longer satisfies this inequity.

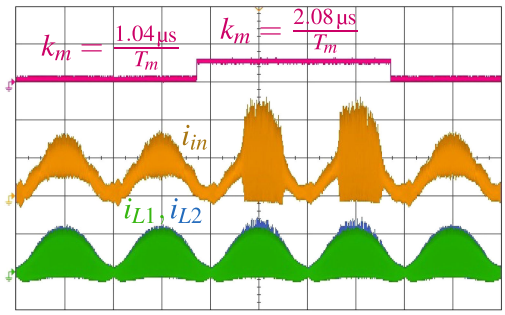

Fig. 16. Input current i_{in} and inductor currents i_{L_1} and i_{L_2} when the gain k_m is toggled from a value of $k_m = \frac{1.04\,\mu s}{T_m}$ to a value of $k_m = \frac{2.08\,\mu s}{T_m}$ at $P_o = 225$ W, $t_{\mathrm{on}} = 0.9\ \mu$s and an rms line voltage of 200 V. (i_{in}: 2 A/div, i_{L_1}: 2 A/div, i_{L_2}: 2 A/div, time base : 5 ms/div).

Fig. 16 is taken at an output power of 225 W, and an input rms voltage of 200 V. Under this condition, the measured ON-time t_{on_1} is 0.9 μs. For the initial two half-line cycles, the gain k_m is set to a value of $k_m = \frac{1.04\,\mu s}{T_m}$. Therefore, the stability inequality given by $0 < k_m < \frac{1.8\,\mu s}{T_m}$ is satisfied, and the input current maintains the correct interleaving with low peak-to-peak current ripple. Then, the gain k_m is increased to $k_m = \frac{2.08\,\mu s}{T_m}$ so that the stability inequality is not satisfied. The phase-shift control loop is no longer able to maintain correct interleaving and the input current has a very large peak-to-peak ripple. For the last half-line cycle shown in the figure, k_m is reduced again to $k_m = \frac{1.04\,\mu s}{T_m}$ and the system becomes stable once more.

D. Adaptive Gain

If a proportional control scheme is used where k_m has a constant value, then k_m must be set to satisfy the stability inequality (19). Therefore, the value of k_m is designed based on the minimum ON-time $t_{\mathrm{on(min)}}$ that occurs for multi-channel operation and can be calculated by $k_m = \frac{t_{\mathrm{on(min)}}}{Tm}$. A minimum ON-time exists because at lighter loads, the converter turns OFF channels

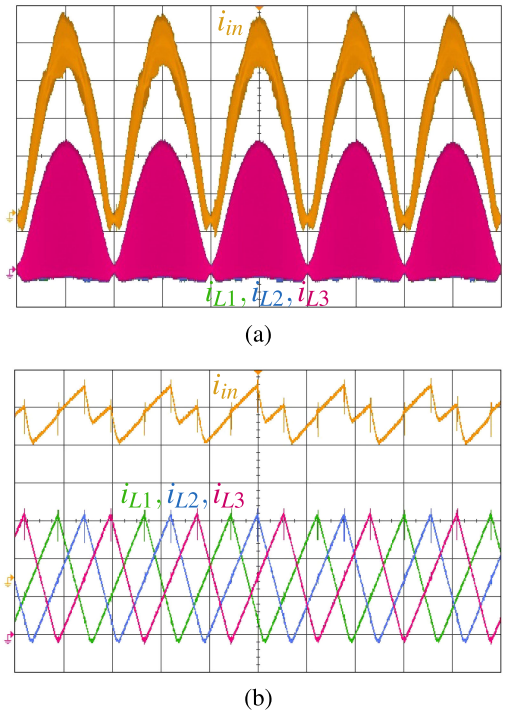

Fig. 17. i_{L_1}, i_{L_2}, i_{L_3}, and i_{in} when all three boost converter channels are enabled at $P_o = 700$ W and an rms line voltage of 115 V when k_m is a constant gain (i_{in}: 2 A/div, i_{L_1}: 2 A/div, i_{L_2}: 2 A/div). (a) Line frequency components (time base : 5 ms/div). (b) Switching frequency components (time base : 5 μs/div).

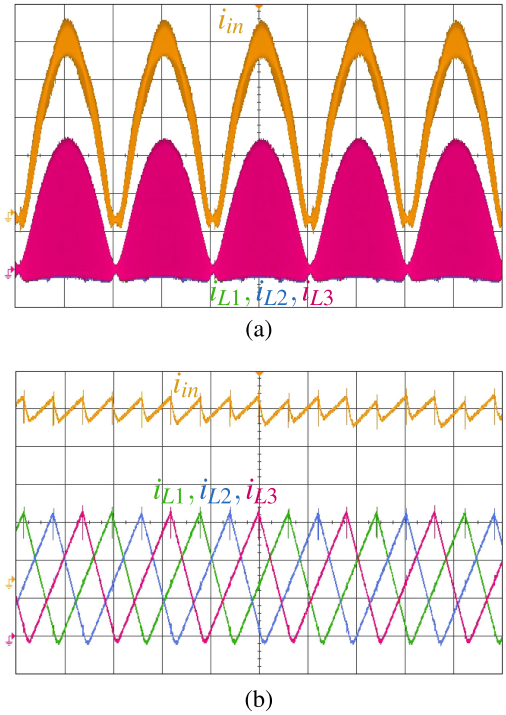

Fig. 19. i_{L_1}, i_{L_2}, i_{L_3}, and i_{in} when all three boost converter channels are enabled at $P_o = 700$ W and an rms line voltage of 115 V when k_m is an adaptive gain (i_{in}: 2 A/div, i_{L_1}: 2 A/div, i_{L_2}: 2 A/div). (a) Line frequency components (time base : 5 ms/div). (b) Switching frequency components (time base : 5 μs/div).

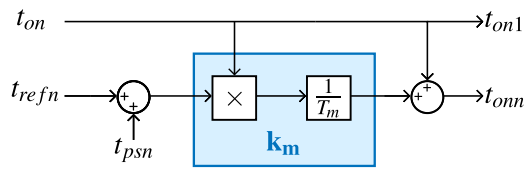

Fig. 18. Phase-shift control loop block diagram structure when an adaptive gain is used.

until only a single channel is operating. At low power levels, this value for k_m works fine because its value is close to the value that gives best tracking performance described by (11). However, when the converter is operating at high power levels and low input voltage, the ON-time dramatically increases. As a result, the chosen value for k_m becomes much less than the value given by (11). This effect is shown in Fig. 17 when the ON-time is at its maximum operating value at $P_o = 700$ W and an rms line voltage of 115 V. This is the maximum rated power of the prototype converter at low line. The value of k_m has been set to $\frac{0.8\,\mu\text{s}}{T_m}$.

The input current shown in Fig. 17 has a large peak-to-peak input-current ripple. This is caused by the poor tracking performance of the phase-shift control at this condition. This problem can be overcome by introducing an adaptive gain that scales the value of k_m with the operating ON-time t_{on_1} using the value of k_m obtained in (11). Thus, for best tracking performance, the proportional gain k_m is replaced with a multiplier block that multiples the error signal by t_{on_1} and a proportional gain of $1/T_m$, as shown in Fig. 18.

Fig. 19 shows the same waveforms as shown in Fig. 17 at the same operating condition but when an adaptive gain is used for k_m. By comparing the waveforms of Fig. 17–19, it is clear using an adaptive gain dramatically reduces the input current peak-to-peak ripple, and improves the tracking performance of the phase-shift control loop. As well as this, given that the value of k_m used for the adaptive gain always satisfies the stability inequality given in (19), it is evident the use of an adaptive gain always ensures the phase-control loop remains stable for all values of t_{on}.

E. Appropriate Value for T_m

Choosing an appropriate value of the rate of execution of the phase-shift control algorithm is important, because the slower the control algorithm, the less computational power is required to execute it. Therefore, the cheaper the microcontroller that can be used. However, if the value of T_m is set too slow, there exists significant quantization error in the phase-shift control loop. This phenomenon is worst at low levels of ON-time and switching period, which exist at high input voltage, and the lowest power level for the operation of a given number of channels. Fig. 20 demonstrates the wave shape of the input current and inductor currents when three channels of the boost converter are enabled, at an output power of 600 W, and an input rms line voltage of 230 V.

This is the near worst case operating condition for the quantization noise created when T_m is too slow, as it is near the maximum input voltage and minimum power for three-channel

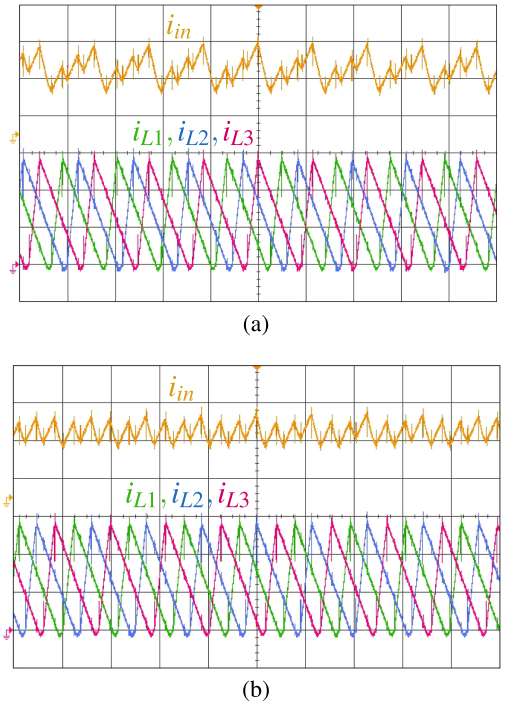

Fig. 20. i_{L_1}, i_{L_2}, i_{L_3}, and i_{in} when all three boost converter channels are enabled at $P_o = 600$ W and an rms line voltage of 230 V (i_{in}: 2 A/div, i_{L_1}: 2 A/div, i_{L_2}: 2 A/div, time base : 5 μs/div). (a) When T_m is set to have an execution frequency of 34 kHz. (b) When T_m is set to have an execution frequency of 100 kHz.

TABLE I
LIST OF PARAMETERS

Parameter	Value
Microcontroller	XMC1402-Q040X0032
Boost inductance L	130 µH
Input rms voltage	85 V to 265 V
Output voltage	400 V
Switching frequency	100 kHz to 550 kHz
Sampling period T_m	14.3 µs
Output Power P_o	0 W to 1000 W

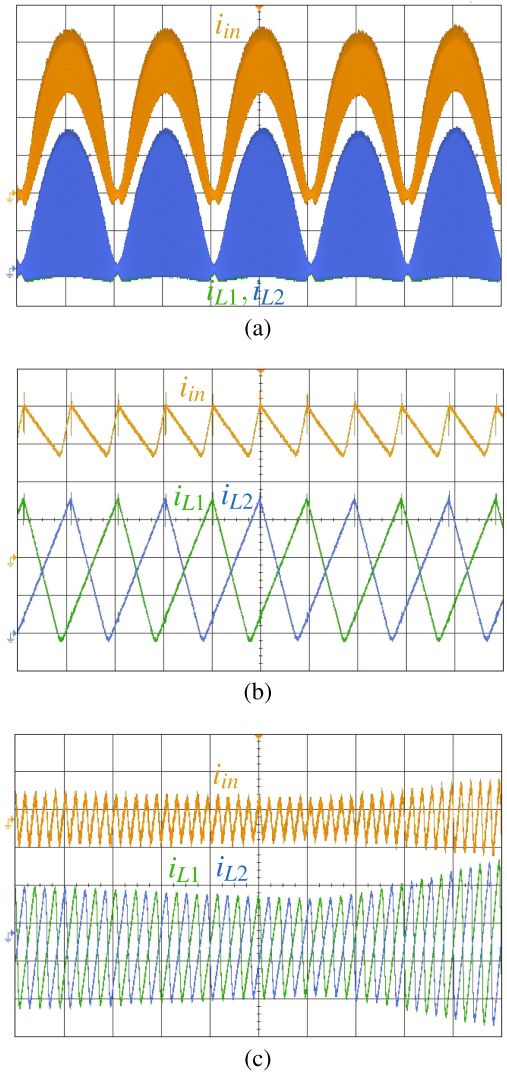

Fig. 21. i_{L_1}, i_{L_2}, and i_{in} when two boost converter channels are enabled at $P_o = 500$ W and an rms line voltage of 115 V (i_{in}: 2 A/div, i_{L_1}: 2 A/div, i_{L_2}: 2 A/div). (a) Line frequency components (time base: 5 ms/div). (b) Switching frequency components (time base : 5 μs/div). (c) At the zero-crossing point of the line voltage (i_{in}: 200 mA/div, i_{L_1}: 100 mA/div, i_{L_2}: 100 mA/div, time base: 20 μs/div).

operation. Below this power level, the converter switches to two-channel operation, therefore, the switching period and ON-time are increased and this type of quantization error reduces. In Fig. 20(a), the value of T_m is set to 30 μs, whereas in Fig. 20(b), the value of T_m is set to 10 μs. It is clear from comparing both figures that having T_m set to too low, a value results in poor tracking performance.

IV. EXPERIMENTAL RESULTS

A three-channel BCM boost converter prototype was built to verify the proposed control scheme. The main parameters of the three-channel boost converter are given in Table I. The microcontroller runs the code for the voltage-loop in a slow 5-kHz interrupt. The code for the phase-shift control is run in a faster 70-kHz interrupt.

Fig. 21 shows the inductor currents and input current when operating at a low input rms line voltage of 115 V in two-channel operation. Near-perfect interleaving operation is maintained at this operating condition. Fig. 21(c) shows the same wave shapes, but at the zero-crossing point of the line voltage, demonstrating the control scheme also works well at this point.

Fig. 22 shows the converter operating at 500 W with an input rms line voltage of 230 V. Near-perfect interleaving operation can be observed when operating in two-channel mode at this operating condition, as demonstrated by the perfect shape of the input current i_{in}, and the low peak-to-peak current ripple.

Similarly, Fig. 23 shows the converter operating with three channels enabled at the full rated output power of 1000 W with an input rms line voltage of 230 V. There is near-perfect interleaving operation at this operating condition, as demonstrated again by the low peak-to-peak current ripple of the input current.

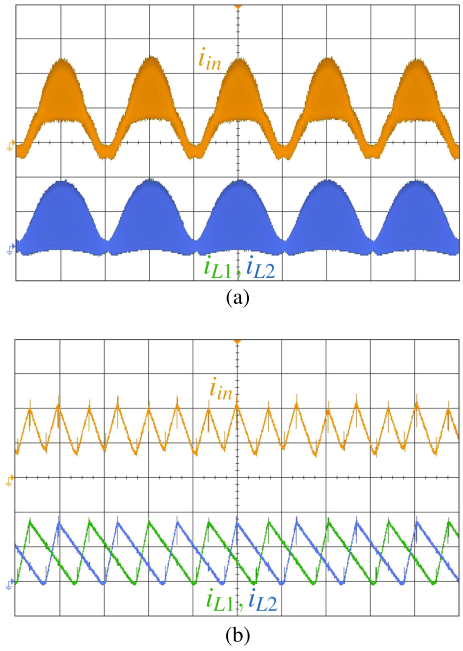

Fig. 22. i_{L_1}, i_{L_2}, and i_{in} when two boost converter channels are enabled at $P_o = 500$ W and an rms line voltage of 230 V (i_{in}: 2 A/div, i_{L_1}: 2 A/div, i_{L_2}: 2 A/div). (a) Line frequency components (time base: 5 ms/div). (b) Switching frequency components (time base: 5 μs/div).

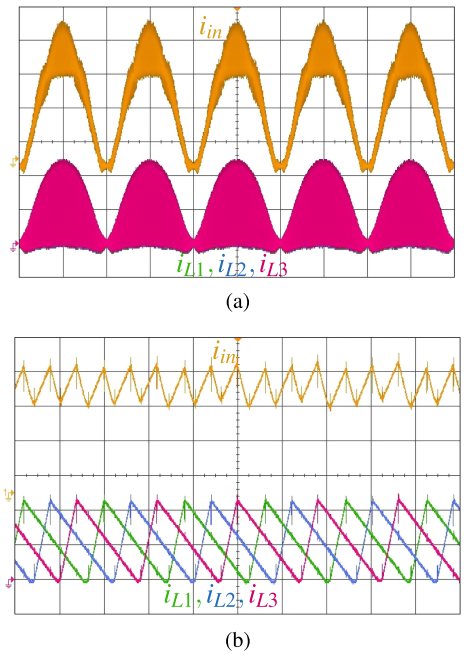

Fig. 23. i_{L_1}, i_{L_2}, i_{L_3}, and input current i_{in} when all three boost converter channels are enabled at $P_o = 1000$ W and an rms line voltage of 230 V (i_{in}: 2 A/div, i_{L_1}: 2 A/div, i_{L_2}: 2 A/div). (a) Line frequency components (time base: 5 ms/div). (b) Switching frequency components (time base: 5 μs/div).

At lighter loads, either one or two channels of the converter are shut-off to improve the converter's efficiency and also reduce the switching frequency of the converter, which increases drastically at lighter loads. Therefore, the phase-shift control algorithm needs to be capable of operating with either one channel enabled, two channels enabled, or with all three channels enabled. Fig. 24

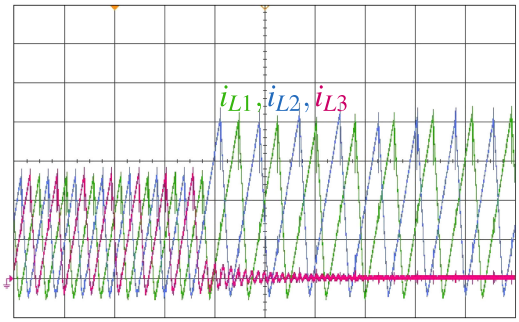

Fig. 24. i_{L_1}, i_{L_2}, and i_{L_3} when entering two-channel BCM (i_{L_1}: 1 A/div, i_{L_2}: 1 A/div, i_{L_3}: 1 A/div, time base: 30 μs/div).

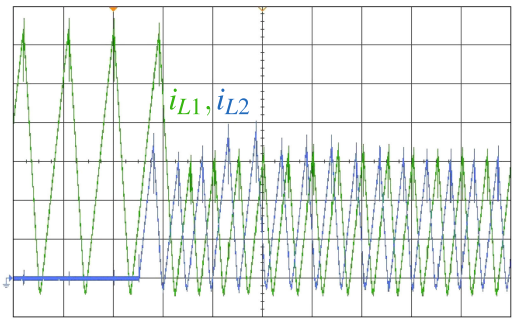

Fig. 25. i_{L_1} and i_{L_2} when entering two-channel BCM (i_{L_1}: 1 A/div, i_{L_2}: 1 A/div, time base: 30 μs/div).

shows the wave shape of the inductor currents and input currents when the converter transitions from three-channel operation to two-channel operation.

At the instant, the phase-shift control loop changes from three-channel operation to two-channel operation, the third channel is disabled, and the ON-time t_{on} is scaled by a factor of $3/2$. This keeps the average instantaneous input current the same. The phase-shift control loop that controls t_{ps_3} is disabled and the reference of the phase-shift control loop controlling t_{ps_2} is stepped from $t_{\text{sw}_1}/3$ to $t_{\text{sw}_1}/2$. It then takes the controller two to three cycles of the phase-shift control algorithm execution to transition from a 120° phase shift, to a 180° phase shift. A similar transition occurs when the converter transitions from two-channel operation to three-channel operation.

Fig. 25 shows the inductor currents as the converter transitions from single-channel operation to two-channel operation. When the second channel and phase-shift control loop for t_{ps_2} are re-enabled, t_{ps_2} has a random initial value in the range $0 < t_{\text{ps}_2} < t_{\text{sw}_1}$. The phase-shift control loop takes two to three executions before t_{ps_2} settles to it's reference at $t_{\text{sw}_1}/2$. This transition is shown in Fig. 25.

The main advantage of disabling boost converter channels at lower power levels is that it increases the converter's efficiency at lighter load. The efficiency of the prototype converter is given in Fig. 26(a) for an input rms line voltage of 230 V, whereas Fig. 26(b) gives the efficiency for an rms line voltage of 115 V. It is clear that at lighter load, reducing the number of channels increases efficiency. This is mainly due to the lower switching frequency that reduces switching losses and inductor core losses.

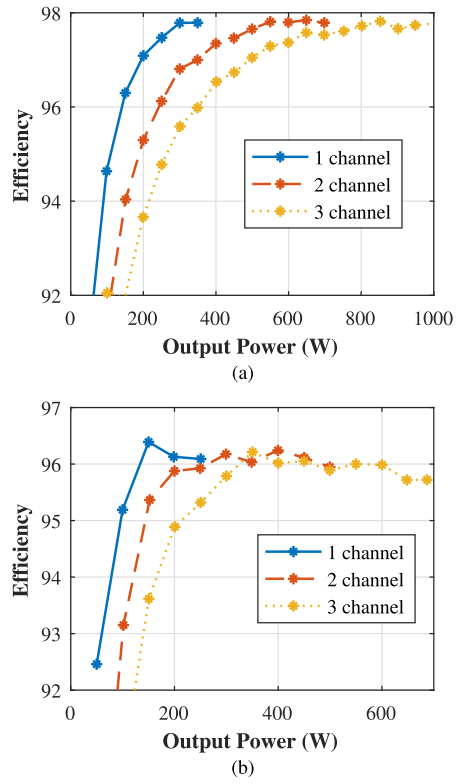

Fig. 26. Efficiency against output power for one-channel, two-channel, and three-channel operations. (a) At an input rms line voltage of 230 V. (b) At an input rms line voltage of 115 V.

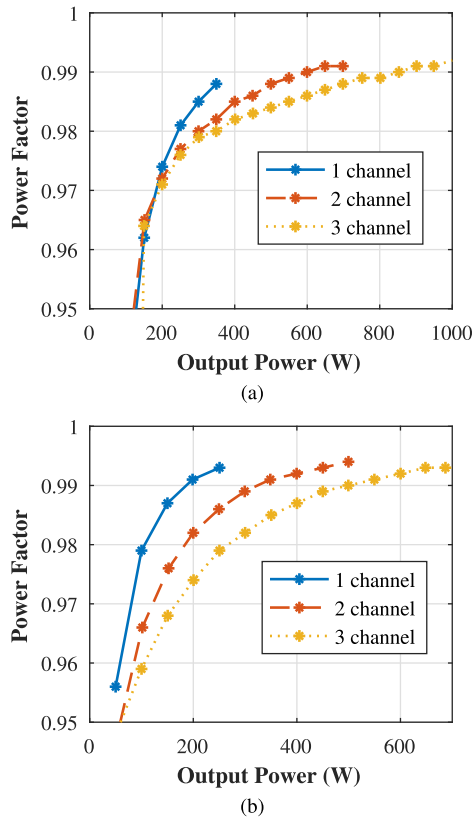

Fig. 27. Power factor against output power for one-channel, two-channel, and three-channel operations. (a) At an input rms line voltage of 230 V. (b) At an input rms line voltage of 115 V .

A similar effect is seen when comparing the power factor in one-channel, two-channel, and three-channel operations. This comparison against output power is given in Fig. 27(a) for an rms line voltage of 230 V, and in Fig. 27(b), for an rms line voltage of 115 V. It is evident from these figures that disabling the number of channels at lighter load increases the power quality of the converter. At higher power levels, it is better to use multiple channels to reduce current stress and thermal stress in components as well as the DM conducted EMI drawn by the converter.

V. Conclusion

A closed-loop digital control strategy that maintains correct interleaving operation of a multi-channel BCM boost converter has been presented. The importance of using separate ZCD circuits for each channel of the interleaved converter to maintain valley-switching operation has been discussed, and details of how the ZCD circuit interfaces with the microcontroller were given.

A digital closed-loop control scheme to maintain correct interleaving operation of the converter was proposed. A mathematical analysis was derived to find the gain of a proportional controller, which provided the best tracking performance and maintained stability of the control loop. An adaptive gain was incorporated into the control loop to give the best tracking performance and ensure stability under all operating conditions.

Finally, the experimental results of a prototype three-channel converter were shown, demonstrating correct interleaving operation of the converter operating in two-channel and three-channel modes.

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