Design of a High-Power Resonant Converter for DC Wind Turbines

Catalin Gabriel Dincan, *Student Member, IEEE*, Philip Kjaer, *Senior Member, IEEE*, Yu-Hsing Chen, Eduard Sarrá-Macia, Stig Munk-Nielsen, *Member, IEEE*, Claus Leth Bak, *Senior Member, IEEE*, and Sriram Vaisambhayana

***Abstract*—This paper presents a design procedure and loss estimation for a high-power, medium-voltage series resonant converter (entitled SRC#), intended for application in megawatt medium-voltage dc wind turbines. The converter is operated with a novel method of operation, entitled pulse removal technique, characterized by variable frequency and phase-shift modulation, below the resonant point of the *LC* tank. A step-by-step design procedure is proposed and circuit component ratings and efficiency are compared for two variants. The new method of operation reduces transformer size to below 50%, whereas losses are kept below 1.5% from zero to nominal power, due to soft-switching characteristics. An experimental setup, rated for 10 kW and 5 kV output was assembled to extract losses and validate the semiconductor loss model.**

***Index Terms*—Medium-frequency transformer, medium-voltage direct current (MVdc), offshore wind farm, series resonant circuit (SRC), sub-resonant mode.**

NOMENCLATURE

CCM	Continuous conduction mode.
DCM	Discontinuous conduction mode.
HVdc	High-voltage direct current.
LVdc	Low-voltage direct current.
MVdc	Medium-voltage direct current.
SRC	Series resonant converter.
C_r	Resonant (tank) capacitor.
C_{in}	Input dc-link capacitance.
C_{out}	Output dc-link capacitance.
δ	Inverter legs phase displacement.
F_{sw}	Switching frequency.
F_r	Resonant frequency.
M	Voltage gain.
N	Transformer turns ratio.

Manuscript received July 17, 2018; revised August 23, 2018 and October 6, 2018; accepted October 7, 2018. Date of publication October 15, 2018; date of current version May 2, 2019. This work was supported by the Department of Energy Technology, Aalborg University, Denmark. Recommended for publication by Associate Editor B. Lehman. *(Corresponding author: Catalin Gabriel Dincan.)*

C. Dincan, P. Kjaer, Y.-H. Chen, E. Sarra-Macia, S. Munk-Nielsen, and C. L. Bak are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail:

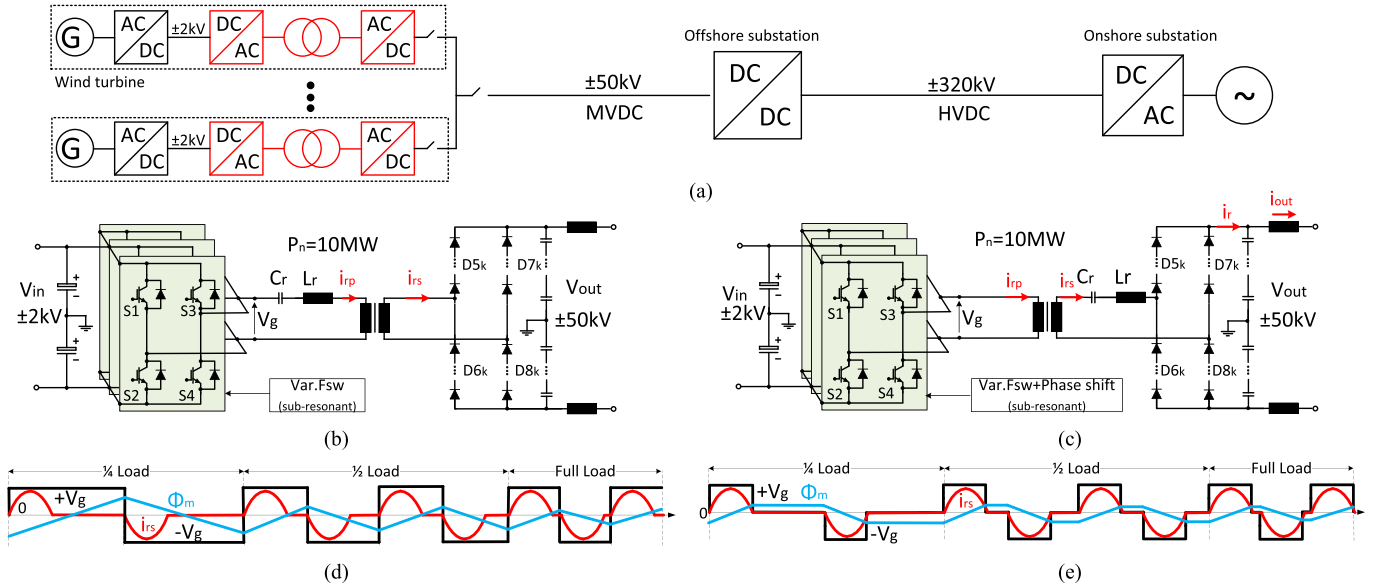

Fig. 1. (a) Single line diagram with dc wind turbines, MVdc power collection, and HVdc power export. (b) Frequency controlled series resonant converter (SRC). (c) Series resonant converter operated with pulse removal technique. (d) SRC operational waveforms (inverter voltage V_g, secondary resonant current i_{rs}, flux linkage Φ_m). (e) SRC# operational waveforms (inverter voltage V_g, secondary resonant current i_{rs}, flux linkage Φ_m).

TABLE I
RATINGS FOR DC/DC CONVERTER

Parameter	Value
Nominal power, P_n	10 MW
Nominal input voltage, V_{in}	± 2 kV
Nominal output voltage, V_{out}	± 50 kV
Insulation level	± 75 kV
Inverter	4x3 in parallel IGBT(6500 V-x-750 A)
Rectifier	4x40 in series diode (6500 V-x-750 A)

TABLE II
SRC# SPECIFICATIONS RANGE

Parameter	Range	Selected value
Nominal power, P_n	5 to 15 MW	10 MW
Input DC Voltage, V_{in}	± 0.5 to ± 8.0 kV	± 2.0 kV
Output DC Voltage, V_{out}	± 35 to ± 50.0 kV	± 50.0 kV
Switching frequency, F_{sw}	0.5 to 5 kHz	1.0 kHz
Power overload	1.1 x P_n	
V_{in} variation	±10%	
V_{out} variation	±10%	
$V_{out,max}$ transient	1.4 x V_{out}	
MV short circuit level	50 x I_{out}	
LV short circuit level	1.5 x I_{in}	
Primary peak current $i_{rp,max}$	2 x I_{in}	
C_r voltage $V_{Cr,max}$	1 x V_{out}	

TABLE III
LIST OF REQUIREMENTS

Expected efficiency	$\geq 98\%$
Isolation type	Galvanically isolated
Modularity	Modular inverter
	Monolithic transformer
	Modular capacitor bank
Cooling type	De-ionized water on inverter level
	Passive oil circulation for transformer
	Passive oil circuilation for rectifier
	Natural air cooling for resonant tank
	Natural air cooling for output filter
Power flow	Unidirectional
Online monitoring of	IGBTs, Diodes, Capacitors

dc/dc topology in this paper is a unidirectional series resonant converter (SRC) composed of the followings: low-voltage (LV) inverter, one monolithic transformer (high turns ratio, with one primary winding and one secondary winding), and a medium-voltage (MV) rectifier built with series connected diodes. Two different designs are proposed and compared with respect to ratings and losses. First design, entitled SRC [see Fig. 1(b)] has the resonant tank on the transformer primary side and it is controlled through variable frequency alone. An improved version of the classic SRC, entitled *SRC#* is shown in Fig. 1(c) and has the *LC* tank moved on the rectifier side and uses a novel mode of operation, entitled *pulse removal technique*. The new converter arrangement and operating mode were previously introduced in [5]–[7].

Common ratings for both variants are listed in Table I, while SRC# specifications range are shown in Table II. Further on, the necessary list of requirements is illustrated in Table III.

The SRC has been proposed in high-power applications, such as traction converters [8]–[11] and in solid-state transformer [13]–[15]. The topology was operated at constant frequency, in open loop and in sub-resonant mode. Its main functionality was to couple two different dc-link voltages with a fix voltage transfer ratio, but without any control possibility.

In [50], a hybrid MV resonant dc–dc converter is proposed, composed of two full bridge inverters, sharing a common leg, one main and one auxiliary transformer. A prototype with reduced ratings (150–1500 V and 2 kW) is evaluated to verify the operating principle, but without mentioning the estimated efficiency on the experimental or theoretical circuit. Another step-up transformerless, resonant dc–dc topology with modular step-up resonant cells is discussed in [51], where simulation results have been provided for a 2-MW turbine system with an output voltage of 50 kV, whereas experimental results on

a laboratory setup 200 V/1.6 kV were provided. Each modular cell consists of resonant parallel converter and employs a high-frequency transformer. No practical details are given for a megawatt approach with respect to the transformer design and discussion regarding the failure of one cell on the impact on converter operation are not given. Furthermore, a modular multilevel converter for high step-up dc–dc converter is introduced in [52]. The topology is based on the standard boost converter, but with the normal single switch replaced by a number of capacitor-clamped submodules. The step-up ratio is dependent on the number of submodules and the inductor charging ratio. The converter is able to reach conversion ratios of 1:10, but the lack of galvanic separation will impose tougher restriction on the nacelle insulation and will lead to increased volume and size. Compared to the work performed in the mentioned papers, this paper suggests practical design approach on the megawatt converter, suggesting an initial design guideline while efficiency estimation is performed on both the theoretical and experimental circuits.

For wind turbine applications, the grid connected converter will have the functionality of controlling the LV dc bus voltage while offering galvanic separation and a high voltage gain. In [46], a per-phase configuration of the SRC is suggested, with three single-phase rectifiers series-connected on the output. The topology is controlled through variable duty cycle and constant frequency while being operated exclusively in super-resonant mode. No efficiency analysis was performed on scaled experiment and the authors believe high losses will occur due to the hard turn-OFF switching. Furthermore, the circuit appears to suffer from technical barriers on implementing 2–3 MVA, 10-kHz monolithic transformers. Other solutions have also been proposed in prior art: Jovcic [48], [49] suggested a single- and three-phase topology while using low-cost thyristors in non-isolated high-gain topology. The topology is similar to a parallel resonant converter, but it will suffer from high voltage stress across the semiconductors and resonant tank. In this paper, the proposed SRC topology is able to control the LV dc bus voltage while delivering high power density and high efficiency. Further critical review of operating methods for the SRC is performed in [7].

The objectives of this paper are to deliver a design procedure and loss estimation of the target circuit, accompanied by scaled experimental validation. The proposed SRC# circuit with pulse removal technique was initially introduced in [5] and [6]. In [7], the corresponding modes of operation were identified and analyzed, but there was no relevant experimental setup with a high turns ratio transformer and medium-voltage rectifier, assembled with series connected diodes. This paper aims at feeling the gap with tests results of 10 kW, 500–5000 V SRC#, operated below 1000 Hz. The main goal of the experiment was not to design a high efficiency SRC# at these power, voltage, and frequency levels but rather to validate the semiconductor loss models before scaling the power level up.

This paper is organized as follows. Section II describes the origins of the SRC# circuit and the necessity of the pulse removal technique, whereas Section III presents design steps of the proposed topology. Section IV elaborates on the loss model, comparison of ratings, and efficiencies of the design variants and Section V shows experimental loss measurements and semiconductor loss model validation. Final conclusions and discussions are presented in Section VI.

II. Series Resonant Converter

A. SRC With Resonant Tank on Primary Side

Consider the first SRC design, with tank on the primary side, as shown in Fig. 1(b), where the transformer magnetizing inductance L_m is considered. Principle waveforms of the circuit are described in Fig. 1(d). When the two complementary switching pairs (S1, S2) and (S3, S4) are opened and closed alternately, a square wave voltage V_g of defined frequency $F_{\rm sw}$ and 50% duty cycle is applied to the resonant *LC* tank, while the rectifying bridge is uncontrolled. A resonant current i_{rp} is induced, which when rectified and filtered is fed into the medium-voltage network $V_{\rm out}$. As the application employs insulated gate bipolar transistors (IGBTs) on the inverter's side and line frequency rectifier diodes, the SRC is operating with variable frequency below resonance, with the characteristic waveforms shown in Fig. 1(d). This mode of operation is favorable as it allows in theory ZCS at turn OFF (or a low current) on both LV and MV semiconductors. Another advantage is that output power becomes a linear function of resonant pulse density, as long as the converter operates in the discontinuous conduction mode (DCM). Low frequency means low output power, whereas high frequency will deliver high output power. The major disadvantage of operating the SRC with variable frequency below resonance is that the medium-frequency transformer needs to be designed for the lowest switching frequency, impacting thus size, weight, and operating range. According to Fig. 1(d), the magnetizing current is varying in direct relation to applied volt–seconds. Below lowest operational frequency, transformer saturation will occur. Furthermore, as shown in [34], low-frequency oscillations caused by the interaction between the *LC* tank and magnetizing inductance will lead to the loss of cyclic stability.

B. SRC# and Pulse Removal Technique

To avoid the issue of excessive transformer size and losses, a new method of operation was introduced, entitled pulse removal technique and the resonant tank was placed on the rectifier side, as shown in Fig. 1(c) with the characteristic waveforms in Fig. 1(e). If V_g is a function of square wave pulses, meaning a pulse with determined length is applied to the inverter, the distance between the pulses will vary as a function of output power. Further on, if the length of the pulse equals half of the resonance period, then frequency control in sub-resonant mode becomes possible and the transformer can be designed for highest operating frequency. With reference to Fig. 1(e), it is noticed that the magnetizing current remains constant during zero voltage periods. So, compared to the classic SRC operated with only frequency control, the SRC# and its method of operation varies also the phase shift between switching pairs (S1, S2) and (S3, S4). As a synthesis, the main advantages of SRC# are: soft-switching capability in entire operating range

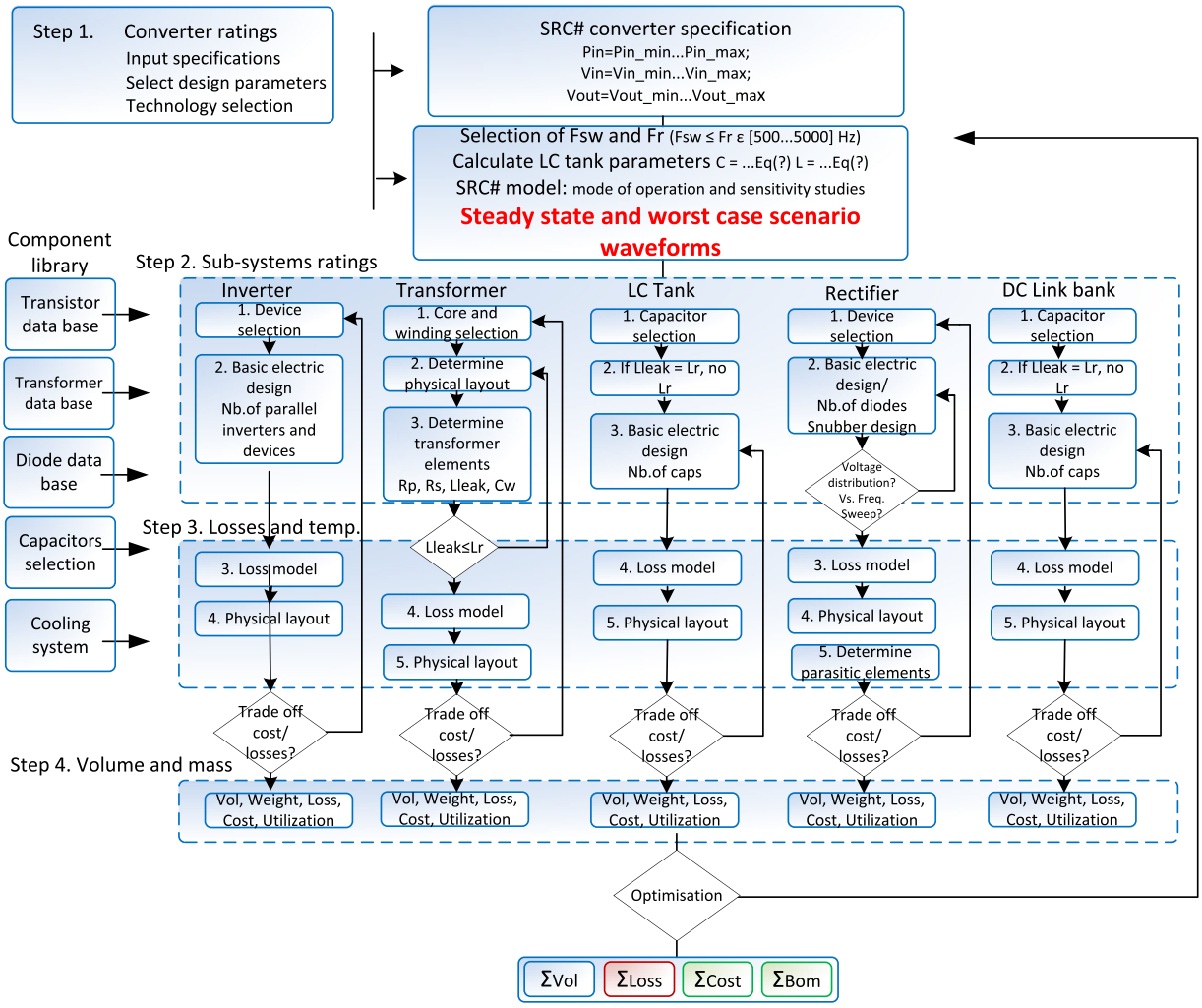

Fig. 2. Proposed design guide line flowchart.

for both inverter and rectifier devices; control of LV-side dc voltage link; possibility to design the high turns ratio transformer for medium-frequency operation even if excited with lower frequency voltage and the incorporation of the resonant inductor into the transformer design as the stray inductance.

Another aspect worthy to be discussed is the chosen modularity of the converter. Considering the tough environment conditions (salty, humid, high- and low-temperature cycles), the long life time expectancy (25 years) and the long distance to shore, it is believed that by reducing the number of components, also the number of possible failure is decreased. From failure mode and effect analysis (FMEA), a system with low number of components exhibits also a low risk priority number (RPN). Therefore, it was chosen to employ only a single transformer (with one core, one primary, and one single winding) and a single rectifier, with series connected diodes.

C. Assumptions Regarding Design Steps and Loss Evaluation

The following assumptions were considered, regarding design steps and loss evaluations.

1) Only active volume is estimated for every sub-system.
2) Snubber and transformer dielectric losses were neglected.
3) Parallel inverters share even current and need no extra inductors for balancing.

III. SRC# Design Considerations

A standard step-by-step design guideline methodology for SRC#, similar to [47] is proposed in Fig. 2. One of the objectives of the design guideline is to address the extremes of the operating points, under assumption of well-working points, which define worst case components loads, and must be designed for. The transients use cases driving the worst case loads must be steps in terminal voltages and steps in power commands. The steady state use cases driving the worst loads must be extreme ratios of Vin/Vout for any active power. Selection of switching frequency, determination of specifications for semiconductors, medium-frequency transformer, resonant tank components, and dc-link capacitors are discussed. Output results are volume, weight, losses, and bill of materials cost, with a design example of a 10-MW converter. The general methodology from Fig. 2 is explained as follows.

Step 1: Converter ratings are determined based on input specifications, user selected design parameters, and technology selection. Different cooling technologies

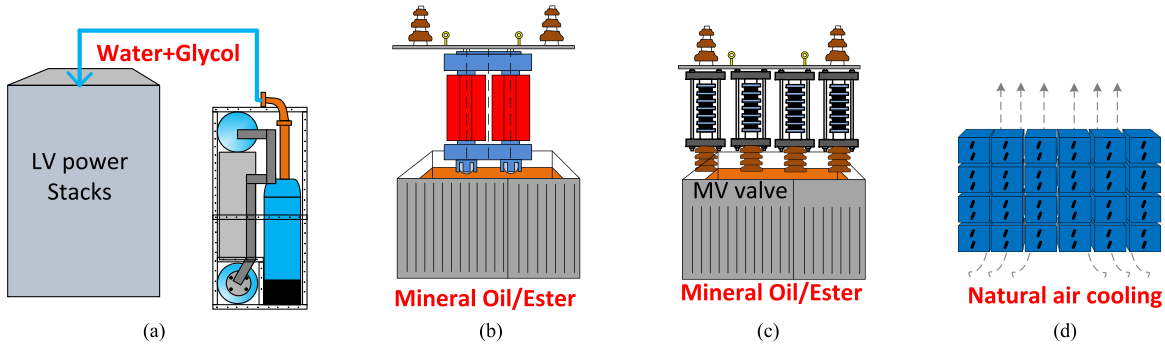

Fig. 3. Cooling technologies. (a) Water+glycol for inverter power stacks. (b) Immersion in mineral oil for MF transformer. (c) Immersion in mineral oil for MV valve. (d) Natural air cooling for all capacitor banks (resonant bank, input and output dc-link banks).

Fig. 4. Different semiconductor packages. (a) Dual diode module. (b) Press pack diode. (c) Press pack integrated gate commuted thyristor (IGCT). (d) Single IGBT module. (e) Press pack IGBT. (f) Press pack injection-enhanced gate transistor (IEGT).

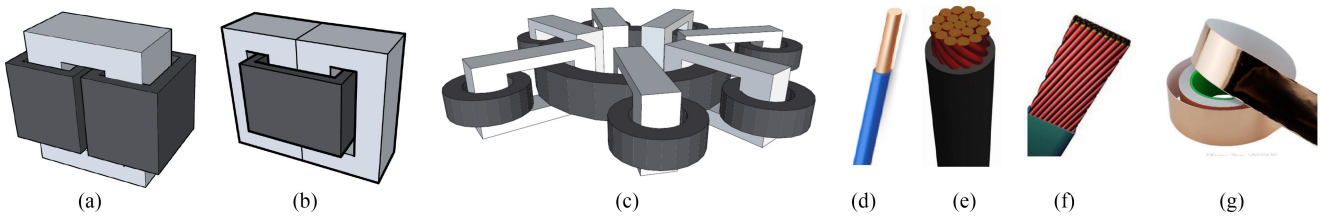

Fig. 5. Transformer core types. (a) C-core. (b) Shell core. (c) Matrix core. Windings type. (d) Round wire. (e) Circular litz. (f) Rectangular litz. (g) Foil windings.

are illustrated in Fig. 3, whereas semiconductor and different transformer options are shown in Figs. 4 and 5. *LC* tank parameters are calculated and peak stress current and voltage are determined from the SRC# simulated and analytical model. Further on, analysis of worst case scenario is performed and the maximum load operating points for semiconductor and transformer are determined based on the performed studies (steady state, dynamic, faults, etc.). These values will define the worst case component loads and must be designed accordingly. Looking at Fig. 6, the frequency to power relation for different voltage difference between V'_{in} and V_{out} is illustrated. For a $\Delta V \approx 0$, the relation is linear and the converter operates in DCM1. If the voltage drop increases, e.g., to 10%, the relation becomes non-linear and converter nominal power is reached at a lower excitation frequency ($\approx$850 Hz), compared to 1000 Hz in DCM1. The worst case scenario is selected to be at $1.1 \times P_n$.

Step 2: Sub-system design is performed, with device selection on the inverter and rectifier sides. Transformer geometry is selected with the condition of using the leakage inductance as part of the resonant inductance.

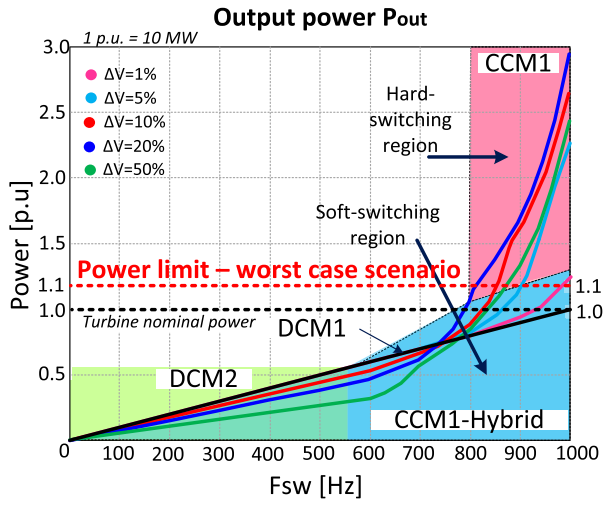

Fig. 6. Frequency to power relation for different voltage differences.

Step 3: At this level, losses and temperature are estimated for all sub-systems, with the transformer thermal model parameters similar to [42].

Step 4: Volume and mass is computed for all sub-systems.

A. Selection of Maximum Switching Frequency and Resonant Tank Frequency

As one of the main goals is to employ a single, monolithic transformer, with one primary and one secondary winding while being designed for medium frequency range, selection of the maximum switching frequency will be a tradeoff between semiconductor, transformer, and passives' losses and weight. Further on, the benefit from increased frequency is a smaller transformer core, however, a compact structure is challenged by winding layout (parasitic capacitance) and heat removal. The impact of stray parameters should be indeed considered if switching frequencies are in the range of tens or hundreds of kilohertz, which are usually specifications for high-frequency pulse transformers, as exemplified in [45], and usually argued against the design of high turns ratio transformers. On the other hand, with MW and kV ratings, the transformer excitation is of hundreds of Hz, and the authors believe that the impact of winding parasitic capacitance is diminished. Therefore, maximum switching frequency should be selected in the range of the following equation:

$$F_{\rm sw} \leq F_r \in [0.5 - 5.0]\ \text{kHz}. \tag{1}$$

Second step is to select the resonant frequency of the tank. If the converter should deliver nominal power P_n at a maximum switching frequency $F_{\rm sw}$, then the resonant frequency F_r should be slightly higher. To allow a finite time for diode recovery, we choose a maximum operating frequency of 1000 Hz and a resonant frequency of 1150 Hz.

B. Resonant Tank

Selection of resonant tank inductance and capacitance is crucial, as they will determine the peak current and period of one resonant pulse. Considering the nominal specifications, maximum switching frequency, and resonant frequency, it is possible to select the resonant tank parameters. According to [6], the converter will operate in sub-resonant mode and output power will be a function of pulse density, meaning capacitor and inductor parameters are calculated in (2) and (3).

Resonant capacitor is calculated from

$$C_r = \frac{P_{\rm out}}{4 \cdot F_{\rm sw} \cdot N \cdot V_{\rm in} \cdot V_{\rm out}}. \tag{2}$$

Resonant inductor is calculated as

$$L_r = \frac{1}{C_r \cdot (2pi \cdot F_r)^2}. \tag{3}$$

There are different ways of implementing the resonant inductor. One way could be to design the transformer with a leakage inductance on the rectifier side equal to that of the resonant inductor. The other option is to design the transformer with a specific leakage inductance [1% to 3% of magnetizing inductance] and the actual resonant inductor will be

$$L_r' = L_r - (L_{lk} \cdot N^2). \tag{4}$$

There are different methods of implementing the resonant capacitor. One possible way would be to use metallized polypropylene capacitors, filled with dry resin. The technology is suitable for high energy density, high-voltage, and high ripple current. They have a high specific ratio capacitance to volume, high capability to withstand surge currents, and offer very good self-healing characteristics [56].

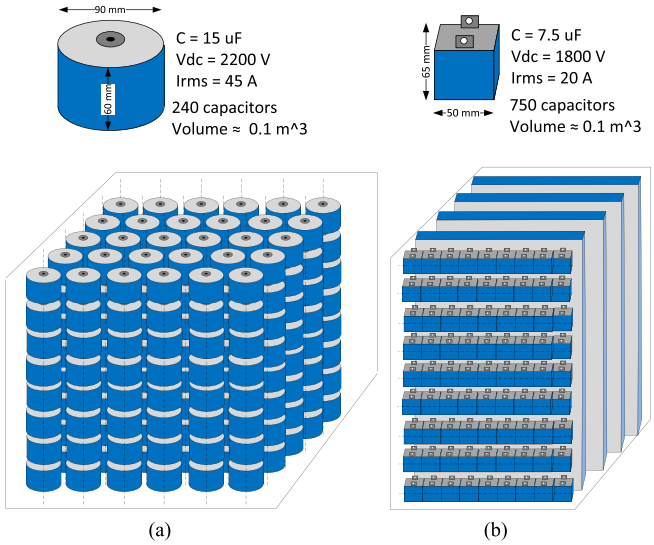

Fig. 7. Resonant capacitor bank.

The resonant capacitor can be implemented through series connection of medium voltage capacitors, as shown in Fig. 7. There are many design, engineering, and mechanical aspects of the resonant capacitor that need to be taken in account. Placing the capacitor bank on the rectifier side, implies high-voltage and low-current specifications, meaning there are higher chances for temperature and dielectric breakdown. The capacitor value is relatively low and a high number of devices in series could also lead to a high equivalent series resistance (ESR). Considering that any variation in capacitor value can impact power flow, capacitors with vary narrow tolerance are required, plus the estimated end of life time value needs to be precise. The whole bank needs to be designed for a long life time, have proper means of accessibility, cooling, repairability, and maintenance.

As an example, two different conceptual solutions are suggested for a resonant capacitor of 250 nF in Fig. 7(a) and (b), rated for 100 kV and an average current of 100 A. Fig. 7(a) presents a capacitor bank based on a 15 μF, 2200 V, and 45 A rms [57], counting in total 240 devices. Fig. 7(b) shows a capacitor bank with 750 devices, each rated for 7.5 μF, 1800 V, and 20-A rms [58]. Both solutions have an active volume of $\approx$0.1 m^3. The estimated capacitor volume is preliminary, as the layout should respect the insulation and air flow requirements, plus electric field control guards might be necessary to steer the electric field outside the strings of capacitors.

According to [16] and [19], the peak resonant capacitor voltage, peak inductor current, and switch currents are dependent strongly on the choice of transformer turns ratio and tank inductance and capacitance. Regardless of conduction modes, peak voltage and current are calculated with the help of the following equation:

$$V_{pk} = \frac{M \cdot K \cdot V_g}{2} \tag{5}$$

$$I_{pk} = \omega_r \cdot C_r \cdot V_g \cdot (M(K+1) - 1) \tag{6}$$

where M is the normalized output voltage and Q_s is the normalized load parameter

$$M = \frac{V_{\text{out}}}{V_g} \tag{7}$$

$$K = \frac{Q_s \cdot \lambda}{2} \tag{8}$$

$$Q_s = \frac{P_{\text{out}}}{\omega_r \cdot C_r \cdot V_{\text{out}}^2} \tag{9}$$

$$\gamma = \frac{F_r \cdot \pi}{F_{\text{sw}}}. \tag{10}$$

C. Inverter

The selection of resonant frequency and *LC* tank parameters will influence the choice of the inverter-side semiconductors. As mentioned previously, IGBT power modules will be employed. Devices should be selected based on the LV bus ratings and primary-side peak current. In this case, it is selected for the semiconductors to be utilized to $K_u = 60\%$ of their blocking voltage ratings, as shown in (11). As modularity will be employed on the inverter level, the number of parallel inverters is calculated with (12)

$$V_{ce,\max} \geq \frac{V_{\text{in}}}{K_u} \tag{11}$$

$$N_{\text{parallel}} = \frac{Ipk}{Ice, nom}. \tag{12}$$

As an example, for a 4-kV dc-link voltage and 4.5 kA peak current, 6.5 kV $\times$ 750 A IGBTs are selected in a full bridge configuration and three parallel inverters will be used to accommodate the load current. Considering the input average current i_{in} of 2.5 kA, for P_n of 10 MW, and V_{in} of 4.0 kV, one could argue if the switches are able to handle the current. It needs to be mentioned that the 750-A rating is the average value where one IGBT is able to turn ON or OFF. Due to soft-switching, the turn-ON current is expected to be zero, whereas at turn-OFF, it is only the value of the magnetizing current limiting the losses. Therefore, in theory and with proper cooling thermal resistance, three parallel inverters can handle even higher power ratings, as long as soft-switching exists.

A conceptual drawing of one power stack is shown in Fig. 8(a) and suggests a state-of-the-art implementation: dc-link capacitors connected close to the power switches, with liquid cooling and low inductance bus bars. Based on a commercial solution [60], an approximated volume of $\approx$0.42 m^3 for three full-bridge configurations is shown in Fig. 8(b). It needs to be mentioned that the approximation is preliminary and assumes an even current sharing through the power stacks. If current sharing inductors are required, their volume should be included too. Selected cooling technology is based on forced water+glycol or deionized water cooling, as shown in Fig. 3(a).

D. Transformer

First design aspects are focused on the medium-frequency transformer, as the turns ratio is used later to calculate resonant

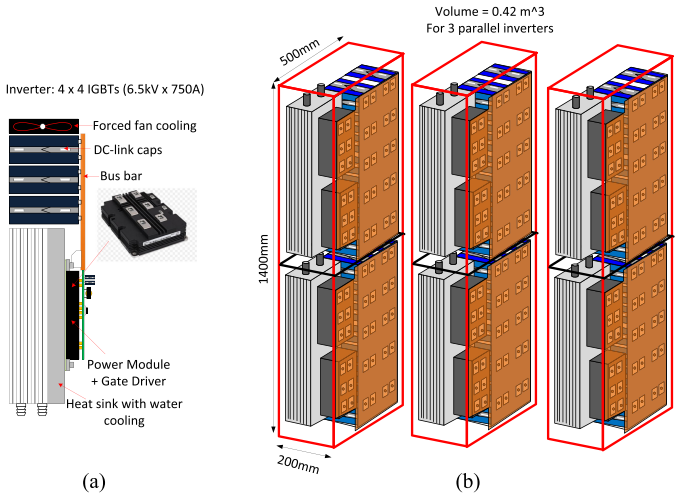

Fig. 8. (a) Inverter power stack simplified structure. (b) Preliminary active volume for three parallel inverters, where structure and volume for 1 inverter is approximated based on [60].

TABLE IV
TRANSFORMER SPECIFICATIONS

Parameter	Value
V_p-Primary voltage	4 kV
V_s-Secondary voltage	100 kV
P_n-Nominal active power	10 MW
N-Turns ratio	1:25
N_p-Primary turns	20 (20 layers x 1 Turn), foil
N_s-Secondary turns	500 (20 layers x 25 Turns), foil
B_{sat}-Saturation flux density	1.5 T
Foil thickness	0.001 m
Core material	Amorphous Metglas 2605SA1 [54]
Oil dielectric strength	10 kV/mm [61]
Oil type	Ester based dielectric oil
M_{Fe}-Core weight	$\approx$ 800 kg
M_{Cu}-Windings weight	$\approx$ 380 kg
M_{Oil}-Oil weight	$\approx$ 400 kg
X-Core window height	1 m
Y_D-Core window width	0.19 m
T_2-Core build	0.16 m
W-Core ribbon width	0.213 m
D_{ins} - primary to secondary distance	0.025 m
Tank size	1.4 m x 0.6 m x 0.4 m

tank parameters. In this design, only one monolithic transformer is used with a single primary and single secondary winding. A standard C-core structure [cf. Fig. 9(a)], while amorphous material is preselected, with the maximum available size of [54]. Windings structure with corresponding design parameters is shown in Fig. 9(b). Different optimal design methodologies have been proposed in [36]–[38] and a similar approach will be followed here. The transformer specifications obtained from the proposed design methodology are illustrated in Table IV.

1) Select Core: Geometry, Material, Size:

$$V_c = \left(\frac{P_n}{4 \cdot J \cdot B_{\max} \cdot F_{\text{sw}}}\right)^{\frac{3}{4}} \tag{13}$$

$$V_c = K_{vol} \cdot A_{p,\max}^{0.75} \tag{14}$$

$$A_p \geq A_{p,\max}. \tag{15}$$

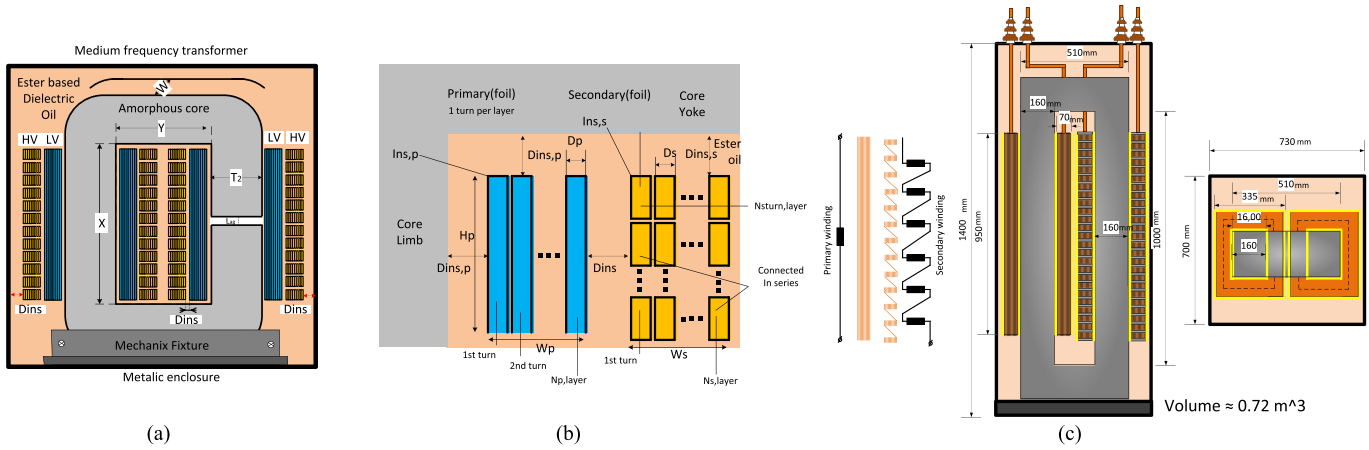

Fig. 9. Transformer with passive circulation of oil. (a) Conceptual drawing. (b) Windings section. (c) Preliminary volume estimation.

2) Select Wire Type and Material: Copper Foil Windings [cf. Fig. 5(g)]:

3) Calculate Turns Ratio N: In order to allow DCM mode in full operational range, the transformer turns ratio are determined from

$$N = \frac{V_{\text{out}}}{V_g}. \tag{16}$$

4) Calculate Primary and Secondary Turns: Further on, primary and secondary turns are calculated based on the selected maximum switching frequency F_{sw}

$$N_p = \frac{Vg}{4 \cdot B_{\max} \cdot A \cdot F_{\text{sw}}} \tag{17}$$

$$N_s = N \cdot N_p. \tag{18}$$

5) Calculate Mean Magnetic Path:

$$L_e = 2 \cdot (X + Y) + 8 \cdot \left(\frac{T2}{2}\right) + L_{ag}. \tag{19}$$

6) Calculate Magnetic Reluctance:

$$R_e = \frac{Le}{\mu_0 \cdot \mu_r \cdot A} \tag{20}$$

$$R_{ag} = \frac{L_{ag}}{\mu_0 \cdot A} \tag{21}$$

$$R_t = R_e + R_{ag}. \tag{22}$$

7) Calculate Magnetizing Inductance:

$$L_m = \frac{N_p^2}{R_t}. \tag{23}$$

8) Compare L_m With $L_{m,\max}$:

$$L_m \leq L_{m,\max}. \tag{24}$$

9) Calculate Leakage Inductance and Stray Capacitance: According to [22], the ratio of leakage inductance L_{ls} and windings stray capacitance C_d can be varied by the mechanical dimensions of the transformer, meaning the distances, heights, and the lengths of the windings. Basically, the leakage inductance are calculated based on the stored energy in the magnetic and electric field

$$L_{lk} = \mu \cdot \frac{{N_p}^2 \cdot l_w \cdot d_w}{h_k} \tag{25}$$

$$C_d = \frac{1}{3} \cdot \epsilon \cdot \left(\frac{N_s}{N_p}\right)^2 \cdot \left(\frac{l_w \cdot h_w}{d_w}\right). \tag{26}$$

where h_k represents the core height, h_w is the winding's height, d_w is the distance between the primary and secondary winding, and l_w is the winding length. Design procedures regarding transformer leakage inductance, stray capacitance, and insulation are investigated in [22] and [23].

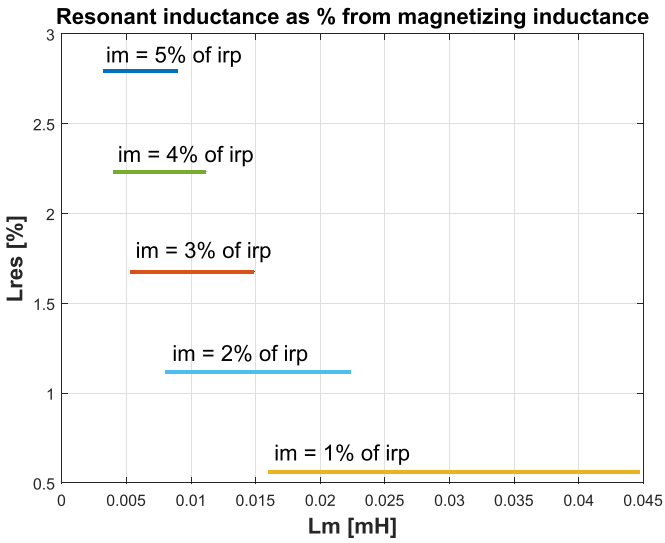

Fig. 10. Transformer leakage inductance versus magnetizing inductance.

Further on, as mentioned earlier, if the resonant inductor should be incorporated in the transformer's own leakage inductance, one notices from Fig. 10, that for 1% ratio of i_m to i_{rp}, the leakage inductance should not be higher than 0.55% of L_m. In practice, transformers with 1% to 2% leakage inductance are considered to be very good designs, so one could say it would be challenging to incorporate the resonant inductor in the

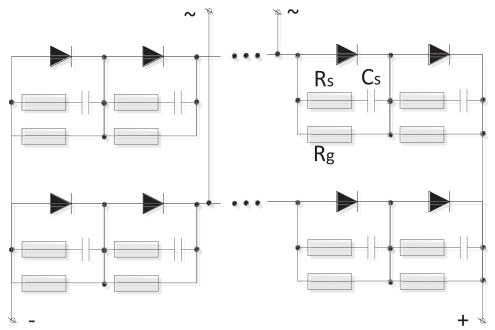

Fig. 11. Rectifier circuit with RC circuit for series connection of diodes.

transformer and have low turn-OFF losses. But, if a ratio of 5% of i_m to i_{rp} is acceptable (meaning lower transformer volume and weight, but higher turn-OFF losses on the IGBTs), the leakage inductance should not be higher than ≈2.8%. Determining range of i_m and $L_{m,\max}$ is shown as follows:

$$i_m = k_c \cdot i_{rp,pk},\ k_c \in [1.0 - 5.0]\% \tag{27}$$

$$L_{m,\max} = \frac{V_{\text{in}}}{4 \cdot k_c \cdot F_{\text{sw}} \cdot i_{rp,pk}}. \tag{28}$$

Transformer core and windings arrangement for the specifications from Table IV, are shown in Fig. 9(c). Each leg has an LV and HV winding. For both windings, copper foils are used. For the primary winding, a layered construction of N_P turns is proposed, whereas the secondary winding is divided into a number of layers, with a certain number of turns. Insulation level is calculated with (29), where E_{ins} is the dielectric strength of the insulation material. Nomex paper is proposed for windings insulation and ester-based dielectric oil as main insulation material and coolant, as mineral oils can be highly flammable, due to their content of corrosive sulphur and poor moisture tolerance. Voltage level and insulator dielectric strength determine the minimum distance between the primary and secondary windings. According to [37], the insulation level is calculated with (29), where λ is a safe margin parameter

$$D_{\text{ins}} = \frac{V_{\text{ins}}}{\lambda \cdot E_{\text{ins}}}. \tag{29}$$

In this paper, dielectric losses are neglected, but it needs to be mentioned that increasing the operating frequency and the insulation requirements, the losses cannot be neglected in the actual prototype.

E. Rectifier

1) Diode Selection: The medium voltage rectifier is implemented in a full-bridge configuration, with series connected diodes, as shown in Fig. 11. Line-frequency press pack diodes (6.5 kV/750 A) [62] are initially chosen for this study, with the particular challenge of 1-kHz operating frequency. Ester-based dielectric oil is selected as the cooling and insulating environment. Design formula (from [35]) for the number of diodes in series is shown in (30) and the parameters are described in Table V

TABLE V
DIODE VALVE PARAMETERS

Parameter	Value
V_{TOV}-maximum valve blocking voltage	140 kV
$V_{RRM,max}$-maximum diode blocking voltage	6 kV
K_A-arrester utilization factor	1
K_D-uneven voltage distribution factor	1
K_U-diode voltage utilization factor	0.6
K_R-redundancy factor	1.025
N_{diodes}-number of diodes per arm	40

$$N_{\text{diodes}} = \frac{V_{\text{TOV}} \cdot K_A}{V_{\text{RRM,max}} \cdot K_V \cdot K_D \cdot K_R}. \tag{30}$$

High-voltage bipolar diodes are used in different converter applications, such as snubber, blocking, antiparallel, or rectifying diodes. For applications requiring ratings of 3.3, 4.5, or 6.5 kV, the silicon bipolar diodes suffer from high switching losses at turn OFF due to the high reverse recovery current and recovery duration. The diode losses limit the operating (fundamental) frequency of the converter. On the other hand, the advantage of using a series resonant topology is that the diodes will have a natural turn-OFF at zero current, decreasing the reverse recovery losses. This characteristic makes the choice of line frequency diodes very attractive, as they are normally cheaper and more robust than fast recovery diodes, being designed for lower conduction losses.

2) RC Circuit for Even Voltage Sharing: Due to very high voltage specifications and series connection, voltage symmetry needs to be guaranteed during turn-ON; turn-OFF; and blocking. Under quasi-static reverse voltage (blocking), the variation of device leakage current (for example, due to manufacturing variation), may lead the devices with the lowest leakage current into avalanche mode. Therefore, it is common practice to connect snubbers and grading resistors in parallel with the diodes, where the resistors help mainly during the blocking state and the capacitor during commutation [35]. Formulas to size the resistance and the capacitor for series connection of *n* diodes, specified reverse voltage V_r are, according to [35]

$$R \leq \frac{nV_r - V_m}{(n-1)\Delta I_{rm}} \tag{31}$$

$$C \geq \frac{(n-1)\Delta Q_{RR}}{nV_r - V_m} \tag{32}$$

where V_m is the maximum series voltage, ΔI_r is the maximum spread of leakage current in the diode, and ΔQ_{rr} is the maximum variation of stored charge of the diodes. According to the previous two equations, the current through the resistor is approximately three to six times the leakage current in the diode and the occurring charge will be up to twice the stored charge of a single diode. Critical points of operation can occur during the transients, due to different switching behavior of the power diodes. In order to evaluate the optimal combination of *R* and *C* parameters, different parameters that influence the voltage balancing should be taken into consideration: output load

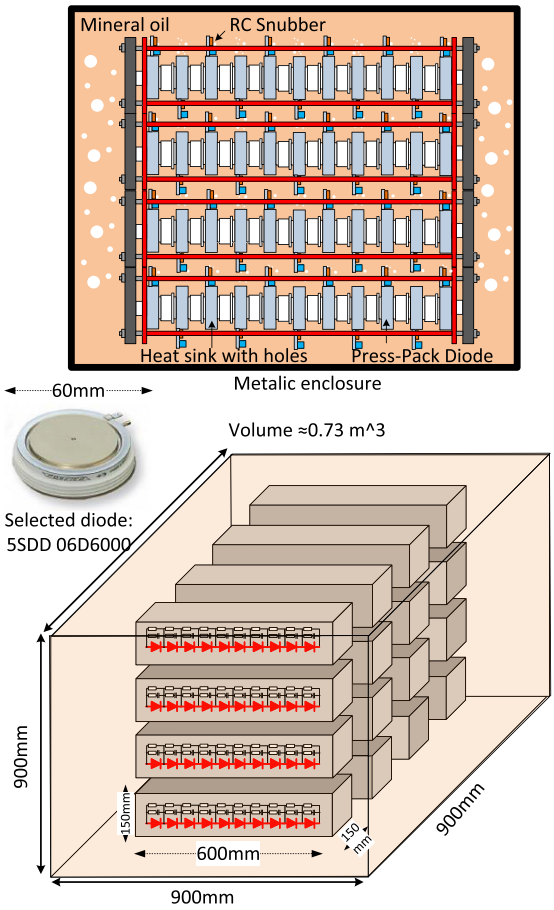

Fig. 12. Diode valve conceptual drawing.

current, dc-link voltage, dynamic characteristics of the diode, and ambient temperature [44].

Based on the selected device package, cooling and insulating environment, a preliminary diode valve internal mechanical layout is shown in Fig. 12, with the assumption that oil cooling and insulation can fulfill the necessary functionalities.

F. DC Link Capacitor Banks

According to [17], the operation with variable frequency in the DCM mode is not adversely affected by the wide range of switching frequency variation, as the low-frequency operation coincides with the low output current, where less filtering is needed. Therefore, the output capacitor value is determined by the maximum power points, which will occur at the highest frequency. Output capacitor voltage and current waveforms for two different frequencies are illustrated in Fig. 13. Compared to the resonant tank values, the output filter has a large time constant and the filter elements are comparably larger, as defined in (33). Output capacitor C_{out} is determined as in (33). The required input dc-link capacitance is obtained by simply scaling the output value with the transformer turns ratio

$$C_{\text{out}} = \frac{2 \cdot E_{\text{cap}}}{V_{\text{out}}^2} = \frac{2 \cdot P_{\text{out}} \cdot \tau}{V_{\text{out}}^2} \tag{33}$$

$$C_{\text{in}} = C_{\text{out}} \cdot N^2. \tag{34}$$

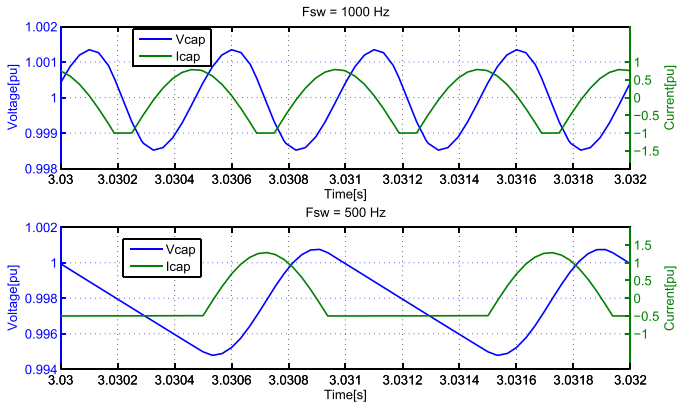

Fig. 13. Voltage and current waveform of output capacitor C_{out} for 1000 and 500 Hz.

TABLE VI
DC-LINK CAPACITOR BANK AND OUTPUT REACTOR

Parameter	Value
P_n-Converter nominal power	10 MW
V_{in}-input voltage	$\pm 2\ kV$
V_{out}-output voltage	$\pm 50\ kV$
C_{out}-output capacitance	50 uF
C_{in}-input capacitance	30 mF
L_{out}-output reactor	200 mH

In order to consider the output current and voltage ripple and according to [46], output capacitance can be calculated with (35), where K_r is the expected ripple

$$C_{\text{out}} = \frac{\sqrt{2} i_r - K_r \cdot i_{\text{out}}}{2piF_r \cdot K_r \cdot V_{\text{out}}}. \tag{35}$$

Output reactor value L_{out} is calculated with (36). The main functionality of output reactor is to limit the short-circuit current

$$L_{\text{out}} = \frac{2 \cdot E_{\text{ind}}}{i_{\text{out}}^2} = \frac{2 \cdot P_{\text{out}} \cdot \tau}{i_{\text{out}}^2}. \tag{36}$$

DC-link capacitor bank and output reactor values are illustrated in Table VI. For input capacitor bank, medium-voltage electrolytic capacitors are suggested, whereas for output side, metallized polypropylene capacitors are a good choice. A suggestion solution based on selected capacitor [59] is shown in Fig. 14 and consists of 400 elements, with a total volume of $\approx 1.6\,\text{m}^3$. As in the case of resonant tank bank, the estimated capacitor volume is preliminary, as the layout should respect the insulation and air flow requirements.

G. Volume Comparison With 10-MVA 50-Hz Transformer

As shown in Fig. 15, if volumes of inverter, rectifier, medium-frequency transformer, resonant capacitor bank, and output filter are added, the total volume will be $\approx 3.55\,\text{m}^3$, which is seven times lower than the volume of a classic, 10-MVA, three-phase, oil-immersed transformer [55]. Therefore, implementing a high-power, dc/dc converter will bring savings in iron and copper materials. Further on, comparison of the approximate volume of the dc/dc converter to a standard shipping container (6 ×

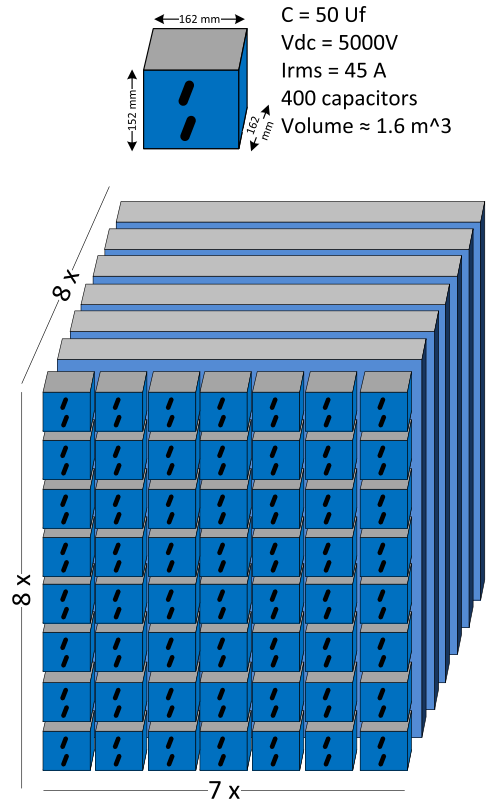

Fig. 14. Output dc-link bank.

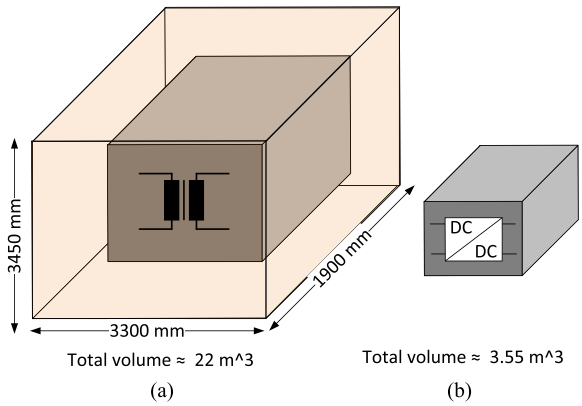

Fig. 15. Volume comparison between (a) a three-phase, oil-cooled, 50-Hz transformer [55] and (b) the high-power, resonant dc/dc converter.

2.5 × 2.6 m) is illustrated in Fig. 16, whereas the estimated sub-system volumes are shown in Table VII.

IV. Loss Estimation

1) Power Semiconductor Loss Model: Semiconductors switching waveforms and loss model are presented in Figs. 17 and 18, respectively. The IGBTs T1 and T4 have both zero voltage switching (ZVS) at turn-ON and a low turn OFF current, whereas rectifier diodes D5 and D8 exibit ZVS at turn ON and ZCS at turn-OFF.

2) Conduction Losses: Methodology proposed in [39] and [40] is used for conduction loss modeling for both IGBTs and diodes. The current is multiplied with the according voltage directly from the datasheet for the highest acceptable temperature, e.g., $T = 125$ °C to extract conduction power loss. Afterward, the curve is approximated with second-order polynomial fitting curves, as described in (37), which uses the current through the ideal switch as input and outputs conduction loss of the device during the simulation. The output is averaged for one switching cycle

$$P_{\text{Cond}} = a \cdot I + b \cdot I^2 \tag{37}$$

$$P_{\text{Sw}} = c \cdot I + d \cdot I^2. \tag{38}$$

3) Switching Losses: Switching losses are determined in similar way like in [14] and [15]. Current dependent E_{ON}, E_{OFF}, and E_{REC} are given in the device datasheet and are considered for a maximum junction temperature of $T = 125$ °C. This dependency is approximated with a second-order polynomial fitting curve, as shown in (38) and multiplied with voltage factor $V_{\text{mes}}/V_{\text{nom}}$ where V_{nom} is the datasheet parameter and V_{mes} the actual applied voltage. When a switching event occurs, losses are calculated and then averaged for one switching cycle.

A. Transformer Loss Model

The simplified transformer loss model is presented in Fig. 19 and it estimates core and winding losses. Transformer loss model parameters are shown in Table VIII.

1) Core Losses: Different methods have been compared in [36]–[38], and [41] for core losses. In the present loss model, the improved generalized steinmetz equation described in [36] was used with K_i, α, and β determined from [43]

$$P_{\text{Core}} = K_i \cdot 2^{\alpha+\beta} \cdot {F_{\text{sw}}}^{\alpha} \cdot B^{\beta} \cdot D^{1-\alpha}. \tag{39}$$

2) Winding Losses: Foil winding losses are calculated, as according to [10] and [11]. The expression from (40) is explained in [36]. The overall losses are calculated by summing the effect of every current harmonic. Skin effect losses are frequency dependent (41), whereas proximity losses (42) are influenced by the number of layers. *D* represents the foil thickness, whereas δ is the skin depth and *m* is the number of layers

$$P_{\text{Winding}} = R_{\text{DC}} \cdot \frac{D}{\delta} \cdot \left[A + \frac{2 \cdot (m^2 - 1)}{3} + B \right] \cdot I_{\text{rms}}^2 \tag{40}$$

$$A = \frac{\sinh\left(\frac{D}{\delta}\right) + \sin\left(\frac{D}{\delta}\right)}{\cosh\left(\frac{D}{\delta}\right) - \cos\left(\frac{D}{\delta}\right)} \tag{41}$$

$$B = \frac{\sinh\left(\frac{D}{\delta}\right) - \sin\left(\frac{D}{\delta}\right)}{\cosh\left(\frac{D}{\delta}\right) - \cos\left(\frac{D}{\delta}\right)}. \tag{42}$$

B. Resonant Tank Losses

To estimate the resonant tank losses, the simplest approach is to predefine the tank quality factor Q_s to a value of 200, and from it calculate the tank equivalent resistance, as shown in (43),

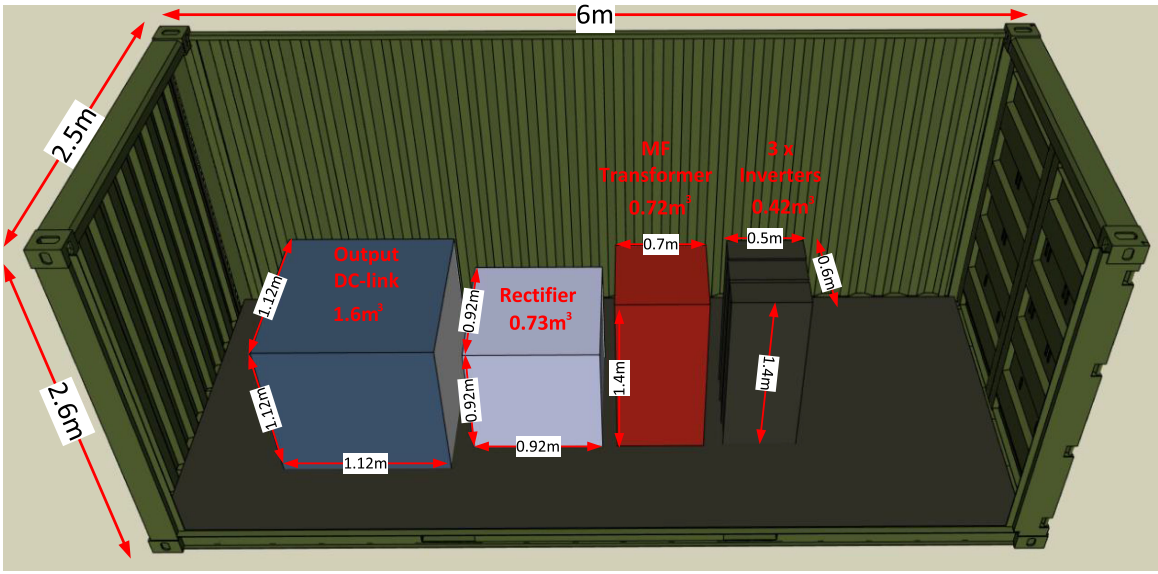

Fig. 16. Comparison of sub-systems' preliminary volume estimation compared to a standard shipping container.

TABLE VII
SUB-SYSTEMS VOLUMES

Parameter	Value
Resonant capacitor bank	$0.1\ m^3$
Inverter	$0.42\ m^3$
Transformer	$0.72\ m^3$
Rectifier	$0.73\ m^3$
Output capacitor bank	$1.6\ m^3$
Total volume	$3.55\ m^3$

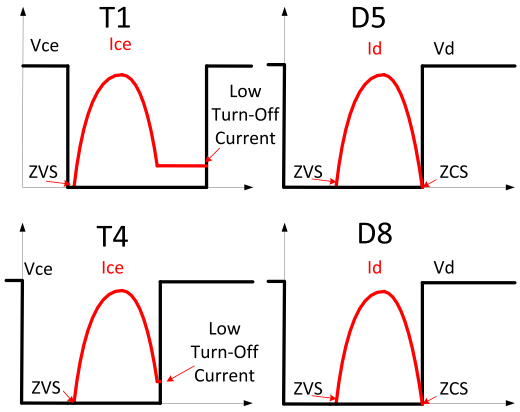

Fig. 17. IGBT and rectifier diode switching waveforms.

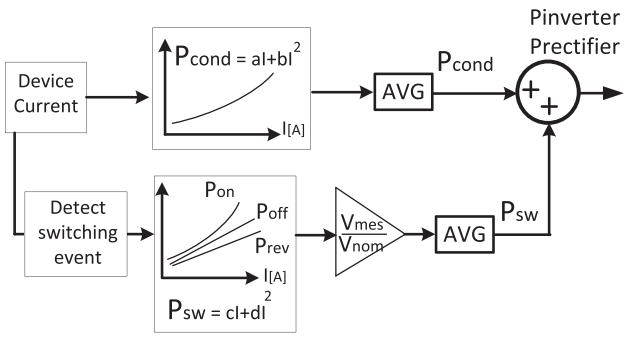

Fig. 18. Power semiconductor loss model.

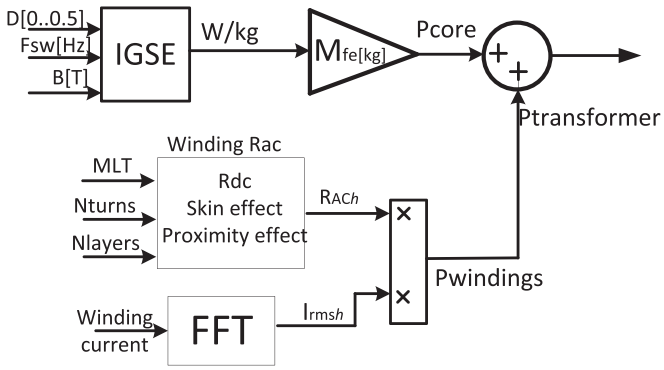

Fig. 19. Transformer loss model.

TABLE VIII
TRANSFORMER LOSS MODEL PARAMETERS

Parameter	Value
D	Waveform duty cycle
MLT	Mean length turn
$Nturns$	Winding number of turns
m	Winding number of layers
R_{dc}	Winding dc resistance
R_{ac}	Winding ac resistance
δ	Foil winding skin depth
I_{rmsh}	RMS current per harmonic

and multiply it with the square of load current

$$R_{\mathrm{LC}} = \frac{Z_c}{Q_s} \tag{43}$$

$$LC_{\mathrm{loss}} = R_{\mathrm{LC}} \cdot I_{\mathrm{out}}^2. \tag{44}$$

To keep resonant tank losses low, the Q_s should be higher than 100, meaning very low inductor resistance and capacitor ESR.

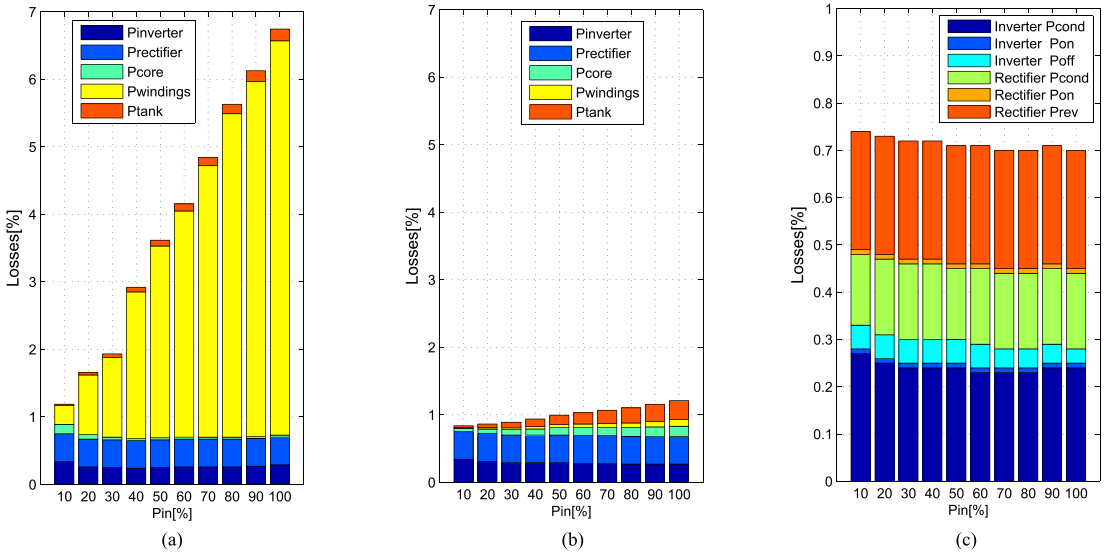

Fig. 20. (a) SRC losses (with *LC* tank on primary side). (b) SRC# losses (proposed solution). (c) SRC# segregation of semiconductor losses.

TABLE IX
SRC AND SRC# COMPARISON OF RATINGS

Parameter	SRC	SRC#
Frequency range F_{sw}	200-1000 Hz	0-1000 Hz
Resonant capacitor C_r	78 uF	0.250 uF
Resonant inductor L_r	250 uH	78000 uH
Magnetizing inductance L_m	100 mH	10 mH
Transformer core weight Fe	880 kg	800 kg
Transformer winding weight Cu	2200 kg	340 kq
Resonant capacitor energy E_{cap}	10000 J	10000 J
Resonant inductor energy E_{ind}	10000 J	10000 J
Resonant tank voltage stress V_{pk}	2 p.u.	25 p.u.
Resonant tank current stress I_{pk}	2 p.u.	0.2 p.u.

TABLE X
EXPERIMENTAL SRC# PARAMETERS

Parameter	Value
Input voltage - V_{in}	500 V
Output voltage - V_{out}	5000 V
Nominal power - P_n	10 kW
Resonant inductor - L_r	182 mH
Magnetizing inductance - L_m	10 mH
Secondary Leakage inductance - L'_{Lk}	12.5 mH
Resonant capacitor C_r	0.1 uF
Snubber capacitor C_s	1.0 nF
Grading resistor R_g	300 kΩ
Load resistors R_{load}	2585 Ω
Primary resistance R_p	0.1 Ω
Secondary resistance R_s	5.0 Ω
Turns ratio N	1:10
Inverter IGBT	4 x SKM150GAR12T4
Rectifier diode	24 x SKKD16/46
Transformer core	4 x AMCC250-Metglas 2605
Windings type	Copper foil
Insulating material	Kepton tape and ester based oil

C. Comparison of Ratings

Based on the previous design procedure, two variants are proposed and compared with respect to ratings, transformer size, and losses. Both variants have the same specifications and number of semiconductors as shown in Table I. First, a design variant for a frequency controlled SRC [as shown in Fig. 1(b)] with resonant tank on the primary side is compared to a second design variant, based on the SRC# concept with pulse removal and tank on the secondary side [as shown in Fig. 1(c)]. A preliminary comparison of ratings is shown in Table IX. The first major disadvantage of variant 1 is that the transformer needs to be designed for the lowest operating frequency, which was selected to be 200 Hz. This impacts the transformer windings weight, increasing it to seven times that of the SRC#. The other disadvantage is that operation below 0.2 per unit (p.u.) is not possible, as transformer saturation will occur. In order to compare losses of the two variants, a semiconductor and transformer model has been arranged. Dielectric and resonant tank losses have not been considered in this comparison.

D. SRC Versus SRC# Loss Comparison

Comparing the ratings of the variants, it is noticed that the SRC will pay a penalty on winding losses, as shown in Fig. 20(a). Compared to Fig. 20(b), it is noticed that semiconductor losses are almost similar between SRC and SRC#, but the difference in transformer designs plays a major role. At elevated frequency, skin and proximity effects increase the winding ac resistance, which impacts losses. For the frequency controlled SRC, this means winding losses are proportional to output power, going up to 6% at nominal power. Pulse removal technique applied for the SRC# allows transformer size reduction below 50% while circuit losses are kept below 1.5% and transformer losses below 0.3%.

V. EXPERIMENTAL VALIDATION

A. Experiment Setup and Diagram

In order to evaluate the validity of the loss model, a scaled 10-kW prototype was built with specifications as shown in Table X, whereas future plans are to investigate the topology

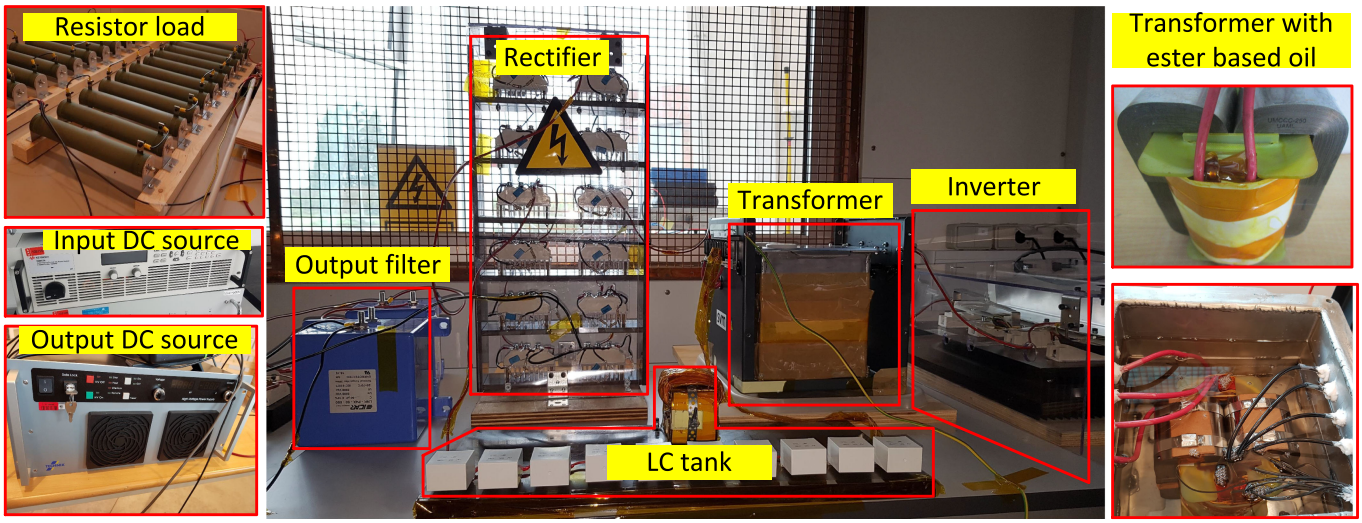

Fig. 21. Experimental setup for SRC#.

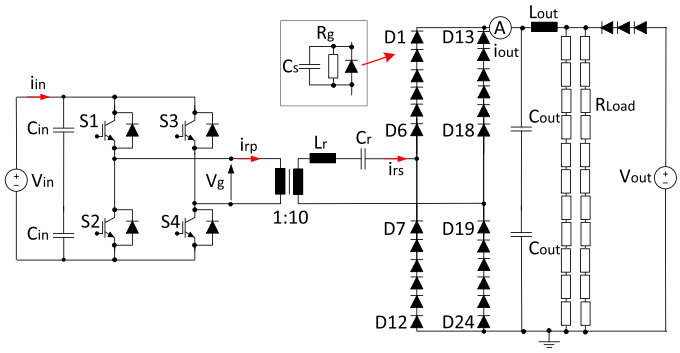

Fig. 22. Experiment diagram.

at megawatt and kilovolt level. The hypothesis was that if the 10-kW loss model (built in *Plecs*) is able to predict the scaled setup losses with low error, then there is higher confidence it will predict the losses also for the target 10-MW converter. The experimental circuit is pictured in Fig. 21 and it's diagram in Fig. 22. The medium frequency transformer is designed for a maximum switching frequency of 1000 Hz and a turns ratio of 1:10. The transformer turns ratio was limited mainly by the laboratory equipment. The rectifier is assembled with 24 line frequency diodes, connected in series, each having a parallel *RC* circuit for voltage balancing. Resonant capacitor bank consists of ten series connected thin film capacitors, whereas the resonant inductor was built around an amorphous core with round wires. Output dc link consists of metallized polypropylene capacitors, whereas on input side, electrolytic capacitors are employed. For this study, the setup was operated in open-loop control up to 1.0 p.u. of nominal power. On the rectifier side, in order to emulate a medium voltage network, a 5-kV dc source is connected to a resistor load through three series connected diodes. Observing Fig. 23, $V_{\rm out}$ is ≈5.0 kV for both 1000- and 200-Hz operation. At 1.0-p.u. operation, the prototype converter delivers 100% of energy to the load and at 0.2-p.u. operation, only 20% of energy is delivered by the prototype, whereas the output dc source covers the rest of 80%, maintaining thus a constant output voltage. The proposed setup emulates a constant MVdc network, as long as the delivered power does not exceed the nominal power of the output voltage source. For higher power and voltage ratings, a setup able to circulate power would be preferred.

B. Characteristic Waveforms

The principal characteristic waveforms for the experimental SRC# are presented in Fig. 23 for two different frequencies, corresponding to 1.0 and 0.2 p.u. of maximum switching frequency. As pulse removal technique is implemented, the distance between applied voltage pulses decreases with frequency, ensuring that the magnetizing current i_m stays constant during the zero voltage periods. Comparing the waveforms of primary and secondary currents, it is noticed that the only differences lay in the scaling factor and addition of magnetizing current on primary side. Another noticeable difference is that at lower frequency, the peak resonant current decreases as compared to higher frequency.

C. Devices Waveforms

In order to understand how pulse removable technique is implemented, inverter- and rectifier-side devices waveforms are presented in Figs. 24 and 25 for two different operating frequencies. The corresponding semiconductor losses are further illustrated in Fig. 26(b) and (c), whereas their segregation in turn-ON, turn-OFF and conduction losses is shown in Fig. 27(b).

1) Inverter IGBTs: Principle device waveforms for switches S1 and S4 are shown in Fig. 24, for 1000 and 500 Hz, whereas for S2 and S3, they are symmetrical. As expected, both devices are experiencing ZVS at turn-ON and a low current at turn-OFF. It is noticed that how the delay between S1 and S4 turn-ON is increasing at lower frequencies. One big difference consists in longer conduction duration of the magnetizing current for S1. The same current will flow through D3 during positive intervals and S2, D4 pair during negative intervals. An important aspect

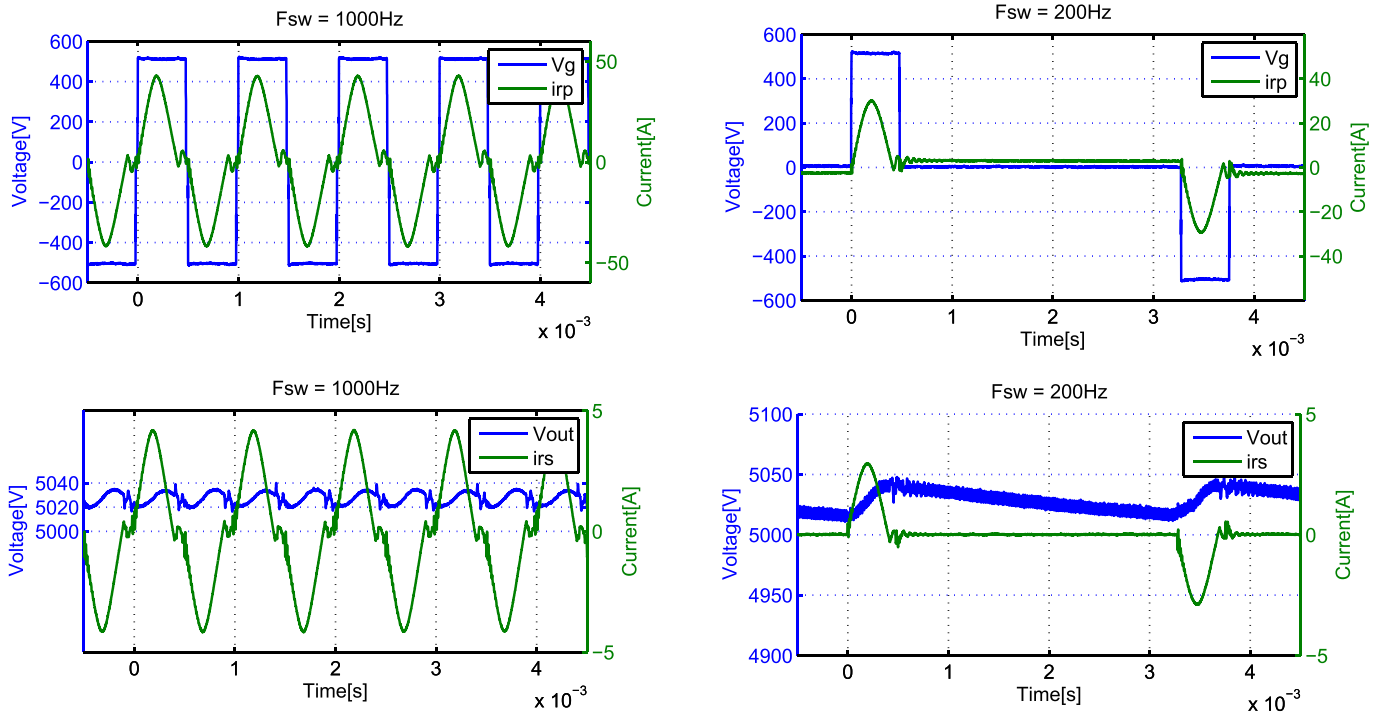

Fig. 23. SRC# characteristic waveforms at 1000 and 200 Hz: inverter voltage V_g, out voltage $V_{\rm out}$, primary resonant current i_{rp}, and secondary resonant current i_{rs}.

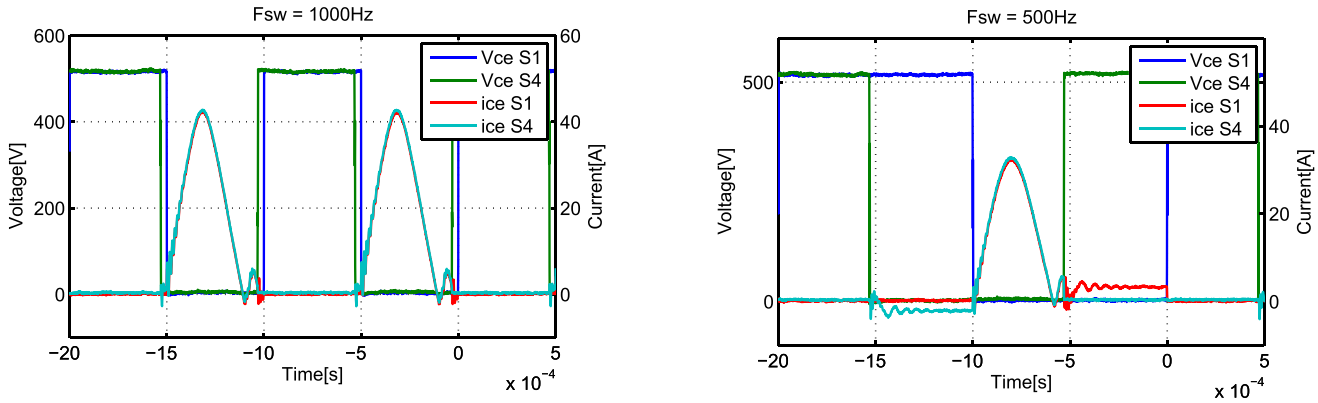

Fig. 24. S1 and S4 collector-emitter voltage and current at 1000 and 500 Hz.

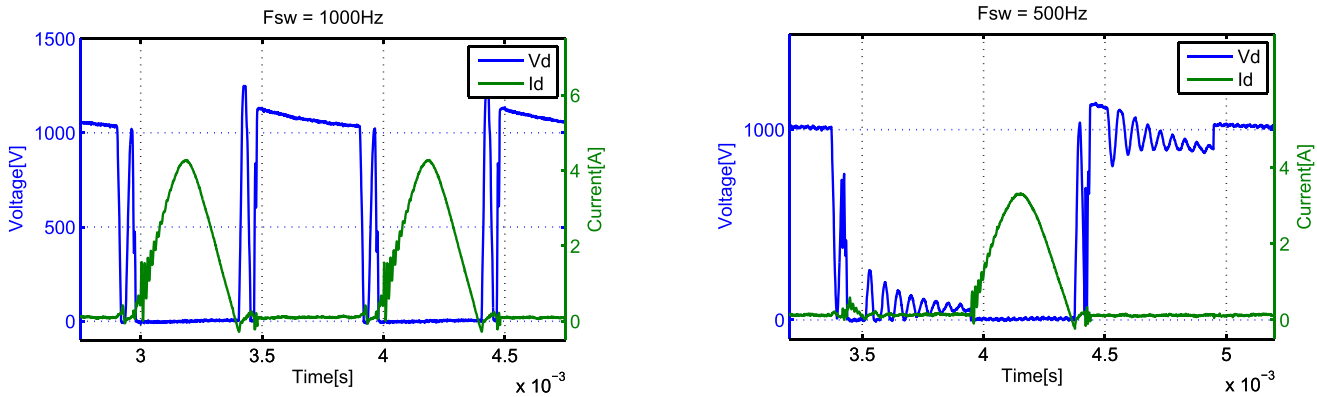

Fig. 25. Rectifier diode forward voltage V_d and current I_d.

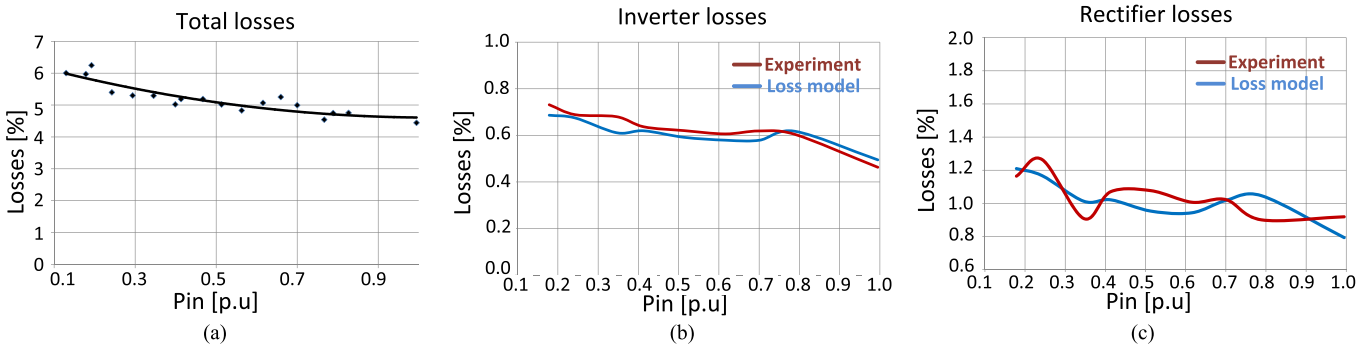

Fig. 26. (a) Measured total losses. (b) Inverter losses. (c) Rectifier losses.

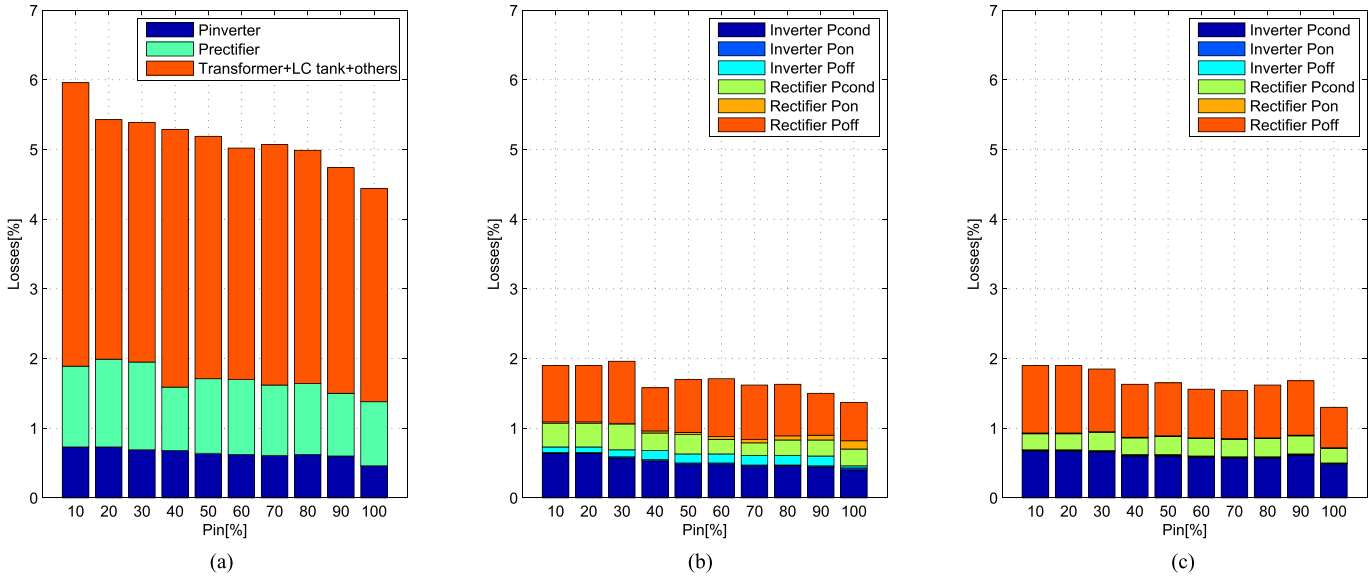

Fig. 27. (a) Loss segregation of measured losses. Loss segregation on (b) measured and (c) simulated semiconductor losses.

is that the ratio between peak resonant current and magnetizing current has to be kept high, preferably above 10, in order to limit conduction and turn-OFF losses.

2) Rectifier Diodes: Characteristic diode waveforms are shown in Fig. 25 for 1000 and 500 Hz. Each diode from the series connection chain will experience ZVS at turn-ON and a low reverse recovery loss. The parallel *RC* circuit will cause, on the other hand, oscillations on V_d, but will not impact conduction losses.

D. Loss Measurements

Total losses of the 10-kW prototype have been evaluated and presented in Fig. 26(a) and they range from $\approx$6% at 0.15 p.u. down to $\approx$4.5% at 1.0 p.u. of P_n. In Fig. 26(b) and (c), it is noticed that the measured losses correspond with the simulated results, increasing the confidence in the semiconductor loss model.

E. Loss Segregation

After measuring the total losses, a segregation was performed and the results are shown in Fig. 27(a). It is noticed that the semiconductor losses are rather flat in the whole operating range. This was expected mainly because the turn-ON and OFF energy losses are the same, regardless of switching frequency and should have the same percentage share. On the other hand, the remaining losses are not possible to segregate at this power level as no test facility was available for this (calorimeter setup or similar). Comparing Fig. 27(b) and (c), it is possible to understand why the experimental results match with the semiconductor loss models. It should be noted that the measured results are also susceptible to errors due to voltage and current probes accuracy, ranging up to $\pm$2% of reading.

F. Discussions

Some important aspects remain to be discussed, such as the relative low efficiency of the experimental demonstrator. First of all, looking only at the semiconductor losses, it is possible to conclude that they remain rather constant in proportion to the load. Further on, it is expected that at this specifications, the transformer core losses have a higher percentage of total losses, as initially expected. But, the percentage of these losses should decrease as nominal power specifications will increase in the

range of MWs. Next, the chosen semiconductors were only utilized at $\approx$25% of their current ratings, as it was not possible to find single IGBT power modules for the setup specifications. Another topic of discussion is the high value of the resonant inductance, which lead to a rather bulky component and a bad quality factor. It is expected as the power and voltage level increase, such as 10 MW and 1:10 turns ratio, even a leakage inductance of 1% to 2% would be enough to replace the physical resonant inductor. As noticed in Fig. 23, the peak resonant current is lower at lower frequencies. These could be the impact of the *RC* parallel circuit, winding resistances, and the emulated MVdc network. Other important subject to be discussed is the position of the resonant inductor on the rectifier side. Ideally, the transformer should be designed so the leakage inductance equals to that of the target resonant inductor, meaning no extra component should be used. Realistically, there are practical challenges in achieving consistency in delivering same leakage inductance for high volume production. To alleviate this aspect, high attention needs to be put on the geometry of the transformer and limiting variations in windings and core dimensions. Further on, assuming 5% to 10% variations in leakage inductance, the resonant capacitor tank can have certain degrees of freedom and can vary in the number of series connected components to achieve the target resonant frequency. On the other hand, placing the resonant inductor on the primary side will imply the design of windings for high current and complexity in heat removal, whereas controlling the resonant converter in sub-resonant mode (with the attributes of soft-switching and high power density) will no longer be valid.

VI. Conclusion

This paper has presented design steps, loss estimation, and experimental validation of an SRC, with *LC* tank on the rectifier side and operated with a novel method, as a highly efficient solution for wind turbines connected to MVdc networks. The proposed topology acts as a niche solution for high-power, high-voltage gain, and -frequency dc/dc topologies. The topology was originated from the classic SRC with *LC* tank on the primary side and operated with frequency control in the sub-resonant mode. This fact had a big disadvantage, mainly because the transformer had to be designed for lower operating frequencies, impacting size, weight, and mainly efficiency. The solution presented in this paper promises a transformer with 50% less weight and high efficiency in whole operating range. This paper has addressed different design aspects for a 10-MW converter, operated at 1000 Hz. Estimated volume for the *LC* tank, inverter, rectifier, transformer, and output dc-link bank have been addressed. For the rectifier side, it is possible to employ line frequency, press-pack diodes connected in series and operated at elevated frequencies, without increasing the reverse recovery losses. A loss model for the semiconductor and transformer was used to estimate the efficiencies and discovered that the proposed SRC# could have losses lower than 1.5% in whole operating range. To validate the semiconductor loss model, a scaled setup, rated for 10 kW, 500–5000 V, and operated up to 1000 Hz was assembled, with measured losses ranging between 6% and 4.5%. It was shown that the measured inverter and rectifier losses correspond to that of the loss model and range from 2% to 1.5% of total losses. This builds confidence in the semiconductor loss model and the promises of the topology. On the other hand, the transformer and *LC* tank losses have not been evaluated independently and more work remains to be done in the future to validate the magnetics loss model.

Acknowledgment

The authors would like to thank C. Shuyu, T. Haonan, M. Palavesha, W. Zhongbao, A, Kumar, and A, Tripathy from the Energy Research Institute, Nanyang Technological University, Singapore, for the technical support on transformer design.

References

[1] C. Meyer, "Key components for future offshore DC grids," Ph.D. dissertation, Inst. Power Electron. Drives, RWTH Aachen Univ., Aachen, Germany, 2007.
[2] C. Meyer and Rik W. De Doncker, "Design of three phase series resonant converter for offshore DC grids," *IEEE Ind. Appl. Annu. Meeting*, 2007, pp. 216–223.
[3] L. Max, "Design and control of a DC grid for offshore wind farms," Ph.D. dissertation, Dept. Energy Environ., Chalmers Univ. Technol., Gothenburg, Sweden, 2009.
[4] W. Chen, A. Q. Huan, C. Li, G. Wang, and W. Gu, "Analysis and comparison of medium voltage high power DC/DC converters for offshore wind energy systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 2014–2023, Apr. 2013.
[5] C. G. Dincan and P. C. Kjaer, "DC-DC Converter and DC-DC conversion method," Patent App., 70 059, 2017.
[6] C. G. Dincan, P. C. Kjaer, Y. H. Chen, S. M. Nielse, and C. L. Bak, "High power, medium voltage, series resonant converter for DC wind turbines," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7455–7465, Sep. 2018.
[7] C. G. Dincan, P. C. Kjaer, Y. H. Chen, S. M. Nielse, and C. L. Bak, "Analysis of a high power, resonant DC-DC converter for DC wind turbines," *IEEE Trans. Power Electron.*, pp. 7438–7454 Nov. 2017.
[8] D. Dujic, F. Kieferndorf, and F. Canales, "Power electronic transformer technology for traction applications-An overview," in *Proc. 7th. Int. Pow. Electron. Motion Control*, 2012, vol. 16, pp. 50–56.
[9] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.
[10] H. Hoffmann, and B. Piepenbreier, "Medium frequency transformer in resonant switching dc/dc-converters for railway applications," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–8.
[11] L. Heinemann, "An actively cooled high power, high frequency transformer with highinsulation capability," in *Proc. 17th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2002, vol. 1, pp. 352–357.
[12] J. W. Kolar and G. I. Ortiz, "Solid state transformer concepts in traction and smart grid applications schedule/outline," in *Proc. Int. Conf. Power Electron. Motion Control*, 2012, pp. 1–166.
[13] G. I. Ortiz, "High-power DC-DC converter technologies for smart grid and traction applications," Ph.D. dissertation, Swiss Fed. Inst. Technol., Zurich, Switzerland, 2014.
[14] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio DC/DC converter cells for phase-modular solid-state transformers," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 5021–5029.
[15] D. Rothmund, J. E. Huber, and J. W. Kolar, "Operating behaviour and design of the half-cycle discontinuous-conduction-mode series-resonant-converter with small DC link capacitors," *IEEE 14th Workshop Control Model. Power Electron.*, 2013, pp. 1–9.
[16] V. Vorperian and S. Cuk, "A complete DC analysis of the series resonant converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 1982, pp. 85–100.
[17] R. W. Erickson, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer, 2013.
[18] F. Wittulski and R. W. Erickson, "Steady-state analysis of the series resonant converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-21, no. 6, pp. 791–799, Nov. 1985.

[19] F. Wittulski and R. W. Erickson, "Design of the series resonant converter for minimum component stress," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-21, no. 4, pp. 356–363, 1986.
[20] J. Jacobs, A. Averberg, and R. De Doncker, "A novel three phase series resonant converter for high power Applications," in *Proc. 35th Annu. Power Electron. Spec. Conf.*, 2004, pp. 1861–1867.
[21] G. Ortiz, D. Bortis, J. W. Kolar, and O. Apeldoorn, "Soft-switching techniques for medium-voltage isolated bidirectional DC/DC converters in solid state transformers," in *Proc. Ind. Electron. Conf.*, 2012, pp. 5233–5240.
[22] D. Bortis, J. Biela, G. Ortiz, and J. Kolar, "Design procedure for compact pulse transformers with rectangular pulse shape and fast rist time," in *Proc. Pow. Modulator High Voltage Conf.*, 2010, pp. 1–4.
[23] M. Jaritz and J. Biela, "Optimal design of a modular series parallel resonant converter for solid state 2.88 MW/115-kV long pulse modulator," *IEEE Trans. Plasma Sci.*, vol. 42, no. 10, pp. 3014–3022, Oct. 2014.
[24] F.-S. Tsai, P. Materu, and F. C. Y. Lee, "Constant-frequency clamped-mode resonant converters," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 460–473, Oct. 1988.
[25] B. S. Nathan and V. Ramanarayanan, "Analysis, simulation and design of series resonant converter for high voltage applications," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2000, pp. 688–693.
[26] F.-S. Tsai and F. C. Y. Lee, "A complete dc characterization of a constant-frequency, clamped-mode, series-resonant converter," in *19th Annu. IEEE Power Electron. Spec. Conf.*, Apr. 1988, pp. 987–996.
[27] R. Lenke, J. Hu, and R. W. De Doncker, "Unified steady-state description of phase-shift-controlled ZVS-operated series-resonant and non-resonant single-active-bridge converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2009, pp. 796–803.
[28] Y. V. Singh, K. Viswanathan, R. Naik, J. A. Sabate, and R. Lai, "Analysis and control of phase-shifted series resonant converter operating in discontinuous mode," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 2092–2097.
[29] P. Ranstad, H. H.-P. H. Nee, and J. Linner, "A novel control strategy applied to the series loaded resonant converter," in *Proc. Eur. Conf. Power Electron. Appl.*, 2005, pp. 1–10.
[30] D. Dujic, A. Mester, T. Chaudhuri, A. Coccia, F. Canales, and J. K. Steinke, "Laboratory scale prototype of a power electronic transformer for traction applications," *Proc. 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.
[31] G. Ortiz, H. Uemura, D. Bortis, S. Member, J. W. Kolar, and O. Apeldoorn, "Modeling of soft-switching losses of IGBTs in DC/DC converters," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 587–597, Feb. 2013.
[32] G. Ortiz, J. Biela and J. W. Kolar, "Optimized design of medium frequency transformer with high isolation requirements," in *Proc. 36th Conf. IEEE Ind. Electron. Soc.*, 2010, pp. 631–638.
[33] L. Lindenmuller, R. Alvarez, P. Kleinichen, and S. Bernet, "Characterization of a 6.5 kV / 500A IGBT module in a series resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 4138–4143.
[34] R. King and T. Stuart, "Transformer induced instability of the series resonant converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-19, no. 3, pp. 474–482, May 1983.
[35] A. Wintrich, "Application manual power semiconductors," *IEEE Trans. Aerosp. Electron. Syst.*, pp. 61–66, 2015.
[36] I. Villar, L. Mir, I. Etxeberria-Otadui, J. Colmenero, X. Agirre, and T. Nieva, "Optimal design and experimental validation of a medium-frequency 400 kVA power transformer for railway traction applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 684–690.
[37] G. Ortiz, J. Biela, and J. W. Kolar, "Optimized design of medium frequency transformers with high isolation requirements," in *Proc. Ind. Electron. Conf.*, 2010, pp. 631–638.
[38] M. Bahmani, "Design and optimization of HF transformers for high power DC-DC applications," Ph.D. dissertation, Dept. Energy Environ., , Chalmers Univ. Technol., Gothenburg, Sweden, 2014.
[39] U. Drofenik, J. W. Kolar, "A general scheme for calculating switching- and conduction-losses of power semiconductors in numerical circuit simulations of power electronic systems," in *Proc. Int. Power Electron. Conf.*, Apr. 2005, pp. 1–7.
[40] K. Lee, Y. Suh, and Y. Kang, "Loss analysis and comparison of high power semiconductor devices in 5 MW PMSG MV wind turbine systems," in *Proc. Int. Power Electron. Conf.*, 2014, pp. 1646–1653.
[41] I. Villar, U. Viscarret, I. Etxeberria-Otadui, and A. Rufer, "Global loss evaluation methods for nonsinusoidally fed medium-frequency power transformers," *IEEE Trans. Ind. Electron.*, vol. 56, no. 10, pp. 4132–4140, Oct. 2009.
[42] I. Villar, U. Viscarret, and A. Rufer, "Transient thermal model of a medium frequency power transformer," in *Proc. Annu. Conf. IEEE Ind. Electron.*, 2008, pp. 1033–1038.
[43] R. Lenke, "A contribution to the design of isolated DC-DC converters for utility applications," Ph.D. dissertation, Inst. Power Gener. Storage Syst., RWTH-Aachen University, Aachen, Germany, 2012.
[44] A. Nagel, S. Bernet, T. Bruckner, P. K. Steimer, and O. Apeldoorn, "Characterization of IGCTs for series connected operation," in *Proc. Ind. Appl. Conf.*, 2000, vol. 3, pp. 1923–1929.
[45] N. Denniston, A. M. Massoud, S. Ahmed, and P. N. Enjeti, "Multiple-module high-gain high-voltage dc-dc transformers for offshore wind energy systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1877–1886, May 2011.
[46] M. T. Daniel, H. S. Krishnamoorthy, and P. N. Enjeti, "A new wind turbine interface to MVDC collection grid with High frequency isolation and input current shaping," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 4, pp. 967–976, Dec. 2015.
[47] T. Soeiro, J. Muhlethaler, J. Linner, P. Ranstad, and J. Kolar, "Automated design of a high power high-frequency LCC resonant converter for electrostatic precipitators," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4805–4819, Nov. 2013.
[48] D. Jovcic, "Step-up DC-DC converter for megawatt size applications," *IET Power Electron.*, vol. 2, no. 6, pp. 675–685, 2009.
[49] D. Jovcic, "Bidirectional, high-power DC-transformer," *IEEE Trans. Power Del.*, vol. 24, no. 4, pp. 2276–2283, Oct. 2009.
[50] L. Shu *et al.*, "A resonant ZVZCS DC-DC converter with two uneven transformers for an MVDC collection system of offshore wind farms," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7886–7895, Oct. 2017.
[51] M. Abbasi and J. Lam, "A step-up transformerless, ZV-ZCS High gain dc/dc converter with output voltage regulation using modular step-up resonant cells for DC grid in Wind systems," *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 5, no. 3, pp. 1102–1121, Sep. 2017.
[52] X. Zhang and T. Green, "The modular multilevel converter for high step-up ratio dc-dc conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4925–4936, Aug. 2015.
[53] Y. Chen, P. Kjaer, R. Olsen, M. Schimmelmann, and C. Bak, "Studies for characterisation of electrical properties of DC collection system in offshore wind farms," in *Proc. CIGRE Gen. Session*, Aug. 2016, pp. 1–13.
[54] 2017. [Online]. Available: http://www.hitachi-hqt.cn/en/core/index.html
[55] 2017. [Online]. Available: http://www.energy.siemens.com. Accessed: Oct. 12, 2017.
[56] "DC link power capacitors for power electronics," ICAR, Milan, Italy, 2017. [Online]. Available: http://www.icar.com/en/product-category/dc-link-power-capacitors. Accessed: Oct. 12, 2017.
[57] *DC Link Capacitor*, LNK-P6X-15-220, ICAR, Milan, Italy, 2017.
[58] *DC Link Capacitor*, LNK-P1X-7.5-180, ICAR, Milan, Italy, 2017.
[59] *DC Link Capacitor*, LNK-P4X-50-500, ICAR, Milan, Italy, 2017.
[60] *Power Stack, SEMISTACK RE*, SKS B2 140 GD 69/12 U-MA PB, Semikron, Nuremberg, Germany, 2017.
[61] *Synthetic Ester-Dielectric Fluid, Midel 7131*, Midel, Manchester, U.K., 2017.
[62] *Line Frequency Diode, 5SDD 06D6000*, ABB, Prague, Czech Republic, 2017.

Catalin Gabriel Dincan (S'17) received the B.Sc. degree in electrical engineering from the Technical University of Cluj-Napoca, Cluj-Napoca, Romania, in 2009, and the M.Sc. degree in power electronics and drives in 2011 from Aalborg University, Aalborg, Denmark, where he is currently working toward the Ph.D. degree in the Department of Energy Technology.

After his studies he worked as a Hardware Engineer with Danfoss Solar Inverters until 2015. His current research interests include the design of high-power, medium-voltage, resonant converters for offshore wind turbines.

Philip Kjaer (S'92–M'93–SM'11) received the M.Sc. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1993, and the Ph.D. degree from the University of Glasgow, Glasgow, U.K., in 1997.

From 1993 to 1998, he was a Research Assistant with the University of Glasgow, working with advanced control of switched reluctance machines and drives. From 1998 to 2003, he was with the ABB Corporate Research, Vasteras, Sweden, where, as a Development Engineer, he worked on servo-motor-based high-voltage circuit breaker drives, factory testing of synchronous machines, power converters for HVdc power transmission, and multi-megawatt variable-speed drives. In 2003, he joined the Vestas Wind Systems, Arhus, Denmark, where he holds the position of the Chief Specialist for Electrical Power Technology. Since 2013, he has been an associated part-time professor with Aalborg University. His research covers control and application of power electronic converters, and he has 100 journal and conference publications and more than 20 patents in this field.

Dr. Kjaer is a Chartered Engineer in the U.K., a member of the Institution of Electrical Engineers, U.K., a member of FEANI, a member of the Danish Academy of Technical Sciences, a member of the Danish national committee of Cigr, and the recipient of the 2004 Richard M. Bass Outstanding Young Power Electronics Engineer Award.

Yu-hsing Chen was born on December 12, 1979, in Kaohsiung, Taiwan. He received the B.S. degree from Kun Shan University, Tainan, Taiwan, in 2002, and the M.S. and Ph.D. degrees from the National Tsing Hua University, Hsinchu, Taiwan, in 2004 and 2010, respectively.

His research interests include voltage sag ride-through technologies and converter controls.

Eduard Sarrà Macia received the B.Sc. degree in energy engineering from the Polytechnic University of Catalonia, Barcelona, Spain, in 2016, and the M.Sc. degree in wind power systems from Aalborg University, Aalborg, Denmark, in 2018.

His interests include control and application of high-power resonant converters in wind turbines, traction, and solid-state transformers.

Stig Munk-Nielsen (S'92–M'97) received the M.Sc. and Ph.D. degrees from Aalborg University, Aalborg, Denmark, in 1991 and 1997, respectively.

He is currently a Professor WSR with the Department of Energy Technology, Aalborg University. For the last ten years, he has been involved or has managed ten research projects, including national and European Commission projects. His research interests include LV and MV converters, packaging of power electronic devices, electrical monitoring apparatus for devices, failure modes and device test systems.

Claus Leth Bak (M'99–SM'07) received the B.Sc. (with honors) and M.Sc. degrees in electrical power engineering from Aalborg University (AAU), Aalborg, Denmark, in 1992 and 1994, respectively, and the Ph.D. degree with the thesis EHV/HV underground cables in the transmission system from the Aalborg University, in 2015.

After his studies, he worked as a Professional Engineer with the Electric Power Transmission and Substations with specializations within the area of Power System Protection at the NV Net TSO. In 1999, he was an Assistant Professor with ET-AAU, where he is currently a Full Professor. He has supervised/cosupervised more than 35 Ph.D. dissertations and more than 50 M.Sc. theses. He is the author/co-author of approximately 250 publications. His main research interests include corona phenomena on overhead lines, power system modeling and transient simulations, underground cable transmission, power system harmonics, power system protection and HVdc-VSC offshore transmission networks.

Prof. Bak is a member of Cigr JWG C4-B4.38, Cigr SC C4, and SC B5 study committees member and Danish Cigr National Committee. He was a recipient of the DPSP 2014 Best Paper Award and the PEDG 2016 Best Paper Award. He serves as the Head of the Energy Technology Ph.D. program (more than 100 Ph.D. dissertations) and as the Head of the Section of Electric Power Systems and High Voltage with AAU and is a Member of the Ph.D. Board at the Faculty of Engineering and Science.

Sriram Vaisambhayana received the Ph.D. degree in electrical and electronics engineering from the Indian Institute of Technology Kharagpur, Kharagpur, India, in 2001.

He has more than 16 years of experience in research, design, and development of power electronics and since 2015, he has been the Principal Investigator in power electronics, with the Energy Research Institute, Nanyang Technological University, Singapore. His main interests include high-power converters design, control, and medium- and high-frequency magnetics design and development.