Design Method of Self-Driving RF-DC Rectifier Based on Waveform-Guided Solutions to Passive Matching Network

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***Abstract*—The design of a self-driving RF-DC rectifier needs to synchronize the gate driving and RF power input. A waveform-based design method is proposed in this paper to get this synchronization through a direct network-parameter calculation of the coupling and matching circuit, other than introducing an adjustable phase shifter on its dual power amplifier prototype. In order to get a practical design at microwave band, nonlinear feedback capacitances, package parasitics, and device's I-V curves are considered in the large-signal RF-DC rectifier circuit analysis. The external passive matching network characterized by its *Z*-parameters can be determined in order to realize a specific high-efficiency operation mode, which is quantified by waveform distance. An RF-DC class-E rectifier example at 2.8 GHz is given to demonstrate this design method based on a modified GaN device model including negative drain voltages. Rectification efficiency of 70.8% is measured for a 10 W input power at 2.8 GHz.**

***Index Terms*—Class-E rectifier, EEHEMT model, high-efficiency transistor rectifier, RF-DC converter, waveform engineering.**

I. Introduction

A MICROWAVE power transfer (MPT) system was proposed for electrical energy distribution in a power grid [1], [2]. Recently, in order to reduce the deploy complexity and to cut the last wires, MPT is an interesting topic in mobile communications [3], charging on sensors with low power level [4], and charging on an electrical vehicle with high power [5].

An RF-DC converter is used to get rectified dc power from microwave input, and it is the final stage of an MPT system [6], [7]. Diode rectifiers are widely used in low power applications and energy harvesting [8]. However, a microwave diode cannot easily handle high voltage and current. Thus, a high-power

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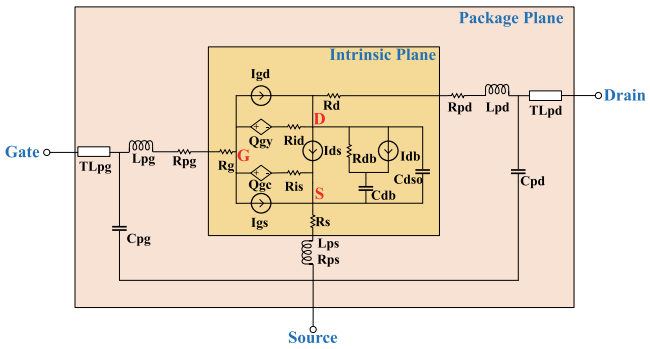

Fig. 1. Architecture of an EEHEMT model.

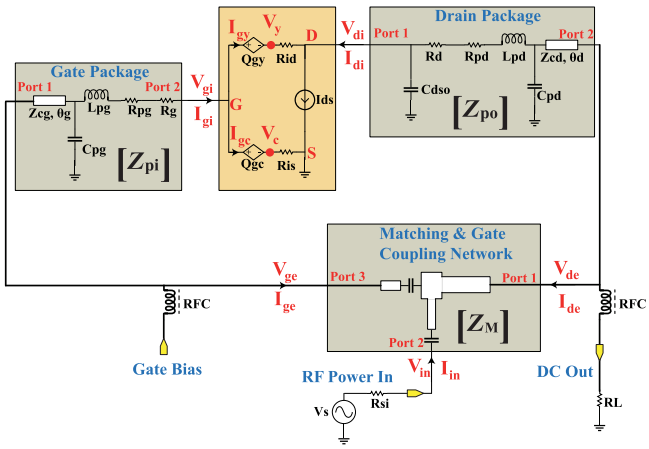

Fig. 2. Self-driving transistor rectifier's circuit topology and variable definitions.

PA test step, and it can offer a practical design result by considering the device's characteristics.

This paper is organized as follows. In Section II, the large-signal circuit analysis method is given for a self-driving RF-DC rectifier. In Section III, the waveform-based design method is shown, and the matching/coupling network calculation flowchart is also given. A rectifier design example and the detailed calculation steps are demonstrated in Section IV, and the modified device model including reverse drain bias can also be found in this section. Section V shows the measurement results and Section VI draws the conclusion.

II. Circuit Analysis of a Self-Driving RF-DC Transistor Rectifier Involving Feedback Path

A. Transistor's Analysis Model and Simplifications

In the following parts, a GaN HEMT transistor is chosen for a rectifier design. There are some new choices for a GaN transistor's model, such as Angelov-GaN and DynaFET [18]. However, due to explicit expressions of an EEHEMT model can be easily obtained from Keysight's product manual [19], [20], it is adopted in the circuit analysis of this paper. The architecture of an EEHEMT model is shown in Fig. 1, but the thermal node is omitted here.

In order to simplify the circuit analysis, we ignored some parasitics and high-order effects listed as follows. The most important factors are kept, such as the nonlinear feedback charges Q_{gy} and Q_{gc}.

1) R_s, L_{ps}, and R_{ps} are ignored.
2) I_{gd} and I_{gs} are not considered within safe operations. Gate-drain and gate-source voltage must be kept well below the device's breakdown and gate forward conduction limit [20], otherwise, the device will have a long-term reliability issue or be damaged.
3) Thermal dynamics [21], trapping effects [22], internal time delay (τ), and dispersion current path I_{db}, R_{db}, and C_{db} are not considered in the analysis.

B. Circuit Analysis of Self-Driving RF-DC Rectifier

As a self-driving rectifier, no additional gate input is used. The circuit schematic and variable definitions are shown in Fig. 2 involving the matching networks and the simplified device model. The synchronized gate control, coupled from a high-power RF input, is the key to design a high-efficiency rectifier.

In Fig. 2, the matching and gate coupling circuits are depicted as an example three-port network, which should be determined for a specific design. The radio frequency choke is lossless and ideal for dc feeding. However, this external coupling connection can also be saved if a direct gate-to-ground termination is adopted [9], [14]. Our analysis can contain this special case with some additional constraints on the network parameters, and we will discuss it later.

Nonlinear device I-V curves are considered in the following circuit analysis, and this will improve the theoretical class-E rectifier's impedance results based on an ideal switching model. As the intrinsic part of a transistor is nonlinear, we will use large-signal analysis accordingly. However, a Fourier series analysis method is adopted for the rest linear networks. Z-parameters are used to represent this passive matching network and to accommodate frequency-domain analysis here. In the following analysis, ω is the fundamental operating frequency in radians.

$Z_{\mathrm{po},k}$ is the drain package's Z-parameter at the kth harmonic frequency, and it can be expressed as

$$\begin{cases} Z_{po,k,11} = \dfrac{1}{jk\omega C_{\mathrm{dso}}} \parallel \left[R_d + R_{pd} + jk\omega L_{pd} + \dfrac{1}{jk\omega C_{pd}} \parallel (-jZ_{cd}\cot k\theta_d) \right] \\ Z_{po,k,12} = \dfrac{1}{jY_{cd}\sin k\theta_d Z_{TA} + \cos k\theta_d / Z_{TB}} \\ Z_{po,k,21} = Z_{po,k,12} \\ Z_{po,k,22} = Z_{cd}\dfrac{Z_A + jZ_{cd}\tan k\theta_d}{Z_{cd} + jZ_A \tan k\theta_d}, \\ \text{where } Z_{TA} = jk\omega C_{\mathrm{dso}}\left(R_d + R_{pd} + jk\omega L_{pd} + \dfrac{1}{jk\omega C_{\mathrm{dso}}}\right) \\ Z_{TB} = \dfrac{1}{jk\omega C_{\mathrm{dso}} + jk\omega C_{pd} - k^2\omega^2(R_d + R_{pd} + jk\omega L_{pd})C_{pd}C_{\mathrm{dso}}} \\ Z_A = \dfrac{1}{jk\omega C_{pd}} \parallel \left(R_d + R_{pd} + jk\omega L_{pd} + \dfrac{1}{jk\omega C_{\mathrm{dso}}}\right) \\ Y_{cd} = 1/Z_{cd}. \end{cases} \tag{1}$$

In (1), Z_{cd} and θ_d are the ideal drain-package transmission line's characteristic impedance and electrical length at the fundamental frequency, respectively.

$Z_{\text{pi},k}$ of the gate package at the *k*th harmonic frequency can be expressed as

$$\begin{cases} Z_{pi,k,11} = Z_{cg}\dfrac{1-k\omega C_{pg}Z_{cg}\tan\theta_g}{jk\omega C_{pg}Z_{cg}+j\tan\theta_g} \\ Z_{pi,k,12} = \cos\theta_g Z_{TC} - jZ_{cg}\sin\theta_g Z_{TD} \\ Z_{pi,k,21} = Z_{pi,k,12} \\ Z_{pi,k,22} = R_g + R_{pg} + jk\omega L_{pg} + \dfrac{1}{jk\omega C_{pg}} \parallel (-jZ_{cg}\cot\theta_g) \\ \quad \text{where} \quad Z_{TC} = \dfrac{1}{jk\omega C_{pg}} \parallel (-jZ_{cg}\cot\theta_g) \\ \quad\quad Z_{TD} = \dfrac{1}{1+k\omega C_{pg}Z_{cg}\cot\theta_g}. \end{cases} \tag{2}$$

In (2), Z_{cg} and θ_g are the ideal gate-package transmission line's characteristic impedance and electrical length at the fundamental frequency, respectively.

The three-port matching and gate coupling network is to be determined through the following waveform-guided method, and its Z-parameter Z_M is expressed as

$$Z_{M,k} = \begin{bmatrix} Z_{M,k,11} & Z_{M,k,12} & Z_{M,k,13} \\ Z_{M,k,12} & Z_{M,k,22} & Z_{M,k,23} \\ Z_{M,k,13} & Z_{M,k,23} & Z_{M,k,33} \end{bmatrix} \tag{3}$$

where this reciprocal passive network reduces some parameters as $Z_{M,k,ij} = Z_{M,k,ji}$. The port number is defined in Fig. 2. If this matching network is lossless, its S-parameter should satisfy the condition of $S_M^H S_M = I$. S-parameter matrix S_M can be transformed from Z_M, and I is the identity matrix. If this matching network is lossy, S_M should satisfy that $I - S_M^H S_M$ is positive definite [23].

The RF power source can be modeled as a voltage source in series with an internal resistance of R_{si}. If the nominal power is P_s, then the fundamental source voltage $V_{s,1}$ can be denoted as

$$V_{s,1} = \sqrt{8R_{si}P_s}. \tag{4}$$

And the harmonic voltage $V_{s,k} = 0$, when $k > 1$. Then, the time-domain expression of source voltage signal is $V_s(t) = V_{s,1}\cos(\omega t)$. The RF power input-port current's Fourier series $I_{in,k}$ can be expressed as

$$I_{in,k} = \frac{V_{s,k} - V_{in,k}}{R_{si}}. \tag{5}$$

Then, the time-domain expression of the input-port current is

$$I_{in}(t) = \sum_{k=1}^{n} |I_{in,k}|\cos(\omega t + \angle I_{in,k}) \tag{6}$$

where n is the maximal harmonic order and $\angle$ is a phase operator. All the following Fourier series are under this type of expansion.

The port voltage and current, defined in Fig. 2, can be linked through the *Z*-parameter matrix. The corresponding results are given as follows. The external drain voltage V_{de} and current I_{de}'s *k*th Fourier coefficients can be calculated by the internal drain voltage V_{di} and current I_{di}

$$\begin{cases} I_{de,k} = \dfrac{-V_{di,k} - I_{di,k}Z_{po,k,11}}{Z_{po,k,12}} \\ V_{de,k} = -I_{di,k}Z_{po,k,21} - I_{de,k}Z_{po,k,22}. \end{cases} \tag{7}$$

From the three-port network definition and (5), the Fourier series of RF power input voltage $V_{in,k}$, the external gate voltage $V_{ge,k}$, and current $I_{ge,k}$ can be determined from (8) as shown at the bottom of this page.

The Fourier series of the internal gate voltage $V_{gi,k}$ and current $I_{gi,k}$ can be calculated by the external gate voltage $V_{ge,k}$ and current $I_{ge,k}$

$$\begin{cases} I_{gi,k} = \dfrac{-V_{ge,k} - I_{ge,k}Z_{pi,k,11}}{Z_{pi,k,12}} \\ V_{gi,k} = -I_{ge,k}Z_{pi,k,21} - I_{gi,k}Z_{pi,k,22}. \end{cases} \tag{9}$$

From (4) to (9), V_{gi} and I_{gi} can be calculated when V_{di} and I_{di} are known.

Besides the passive-network-determined voltage and current relation, the transistor's intrinsic part also plays an important role. From the simplified assumption made in this paper, the current source I_{ds} is controlled by the internal gate voltage V_{gi}

$$\begin{cases} V_{in,k} = \dfrac{R_{si}V_{de}Z_{M,k,23} - V_sZ_{M,k,12}Z_{M,k,23} + V_sZ_{M,k,13}Z_{M,k,22} + I_{de}R_{si}Z_{M,k,12}Z_{M,k,13} - I_{de}R_{si}Z_{M,k,11}Z_{M,k,23}}{R_{si}Z_{M,k,13} - Z_{M,k,12}Z_{M,k,23} + Z_{M,k,13}Z_{M,k,22}} \\ I_{ge,k} = \dfrac{I_{de}Z_{M,k,12}^2 - V_sZ_{M,k,12} + R_{si}V_{de} + V_{de}Z_{M,k,22} - I_{de}R_{si}Z_{M,k,11} - I_{de}Z_{M,k,11}Z_{M,k,22}}{R_{si}Z_{M,k,13} - Z_{M,k,12}Z_{M,k,23} + Z_{M,k,13}Z_{M,k,22}} \\ V_{ge,k} = \dfrac{\begin{array}{c} R_{si}V_{de}Z_{M,k,33} - V_{de}Z_{M,k,23}^2 + V_{de}Z_{M,k,22}Z_{M,k,33} + V_sZ_{M,k,13}Z_{M,k,23} - V_sZ_{M,k,12}Z_{M,k,33} \\ + I_{de}R_{si}Z_{M,k,13}^2 + I_{de}Z_{M,k,11}Z_{M,k,23}^2 \end{array}}{R_{si}Z_{M,k,13} - Z_{M,k,12}Z_{M,k,23} + Z_{M,k,13}Z_{M,k,22}} \\ \qquad + \dfrac{\begin{array}{c} I_{de}Z_{M,k,13}^2Z_{M,k,22} + I_{de}Z_{M,k,12}^2Z_{M,k,33} - I_{de}R_{si}Z_{M,k,11}Z_{M,k,33} - 2I_{de}Z_{M,k,12}Z_{M,k,13}Z_{M,k,23} \\ - I_{de}Z_{M,k,11}Z_{M,k,22}Z_{M,k,33} \end{array}}{R_{si}Z_{M,k,13} - Z_{M,k,12}Z_{M,k,23} + Z_{M,k,13}Z_{M,k,22}} \end{cases} \tag{8}$$

and drain voltage V_{di}. And it is temporally expressed by an implicit time-domain function as follows:

$$I_{ds}(t) = f(V_{gi}(t), V_{di}(t)) \tag{10}$$

where the nonlinear function $f(\cdot)$ will be expanded by dc I-V curves. It is very important to consider the device constraints (nonlinear function $f(\cdot)$ here) in a practical RF-DC rectifier design. First, the knee voltage and nonlinear transconductance of practical I-V curves will lead to matching deviation from the theoretical calculations. It is the reason why large-signal optimizations are usually adopted in a PA/rectifier prototype design. Second, as the I-V curves of a GaN device do not show symmetry about the origin, the waveform duality cannot be automatically satisfied without adjusting the matching network from a PA prototype.

The behaviors of the nonlinear charge paths are a bit complex. In an EEHEMT model, Q_{gy} and Q_{gc} are determined by V_{gi} and V_{di} through a series of nonlinear equations. The lengthy equations are omitted here, and only an implicit equation is used here for a representation

$$\begin{aligned} Q_{gy}(t) &= qy(V_{gc}(t), V_{gy}(t)) \\ &= qy(V_{gi}(t) - V_c(t), V_{gi}(t) - V_y(t)) \end{aligned} \tag{11}$$

$$\begin{aligned} Q_{gc}(t) &= qc(V_{gc}(t), V_{gy}(t)) \\ &= qc(V_{gi}(t) - V_c(t), V_{gi}(t) - V_y(t)) \end{aligned} \tag{12}$$

where $V_c(t)$ and $V_y(t)$ are internal time-domain voltages defined in Fig. 2. The detailed expressions of qc and qy can be found in [20]. Time-domain waveform of every voltage and current can be obtained by Fourier series expansion like (6), which are omitted here.

The current flowing through Q_{gy} and Q_{gc} can be, respectively, expressed as

$$I_{gy}(t) = \frac{dQ_{gy}(t)}{dt} \tag{13}$$

$$I_{gc}(t) = \frac{dQ_{gc}(t)}{dt}. \tag{14}$$

From Kirchhoff's current law

$$I_{gi,k} = I_{gy,k} + I_{gc,k} \tag{15}$$

where $I_{gy,k}$ and $I_{gc,k}$ are their corresponding Fourier series of $I_{gy}(t)$ and $I_{gc}(t)$, respectively.

After $I_{gy,k}$ is calculated, the internal drain port current I_{di} can be calculated as

$$I_{di,k} = I_{ds,k} - I_{gy,k}, \quad k = 1, \ldots, n \tag{16}$$

where $I_{ds,k}$ is the Fourier coefficients of $I_{ds}(t)$ in (10).

Based on Ohm's law, $V_{c,k}$ and $V_{y,k}$ also satisfy the following relation

$$V_{y,k} = I_{gy,k} R_{id} + V_{di,k} \tag{17}$$

$$V_{c,k} = I_{gc,k} R_{is}. \tag{18}$$

Till now, all the rectifier circuit relations are included in (4)–(18). Furthermore, the dc output can be determined from an energy relation.

Due to possible power reflection at the RF input port caused by mismatch, the actual total input power P_{in} is given by

$$P_{in} = \frac{1}{2}\text{Real}\{V_{in,1}\overline{I_{in,1}}\}. \tag{19}$$

Meanwhile, harmonic power is absorbed by the source resistance R_{si} leading to losses $P_{\text{loss},s}$

$$P_{\text{loss},s} = -\frac{1}{2}\sum_{k=2}^{n}\text{Real}\{V_{in,k}\overline{I_{in,k}}\}. \tag{20}$$

The loss in the three-port matching and coupling network $P_{\text{loss},M}$ is determined by the summation of input power at every port

$$\begin{aligned} P_{\text{loss},M} = \frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{de,k}\overline{I_{de,k}}\} + \frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{in,k}\overline{I_{in,k}}\} \\ + \frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{ge,k}\overline{I_{ge,k}}\}. \end{aligned} \tag{21}$$

The loss in the drain package network $P_{\text{loss},po}$ is given by

$$\begin{aligned} P_{\text{loss},po} = -\frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{di,k}\overline{I_{di,k}}\} - \frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{de,k}\overline{I_{de,k}}\} \\ + I_{di,0}^2(R_d + R_{pd}) \end{aligned} \tag{22}$$

where $I_{di,0}$ are the dc voltage at the transistor's internal drain port. The loss in the gate package network $P_{\text{loss},pi}$ is given by

$$P_{\text{loss},pi} = -\frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{ge,k}\overline{I_{ge,k}}\} - \frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{gi,k}\overline{I_{gi,k}}\}. \tag{23}$$

And the loss in the transistor $P_{\text{loss},T}$ is given by

$$P_{\text{loss},T} = \frac{1}{2}\sum_{k=1}^{n}\text{Real}\{V_{di,k}\overline{I_{ds,k}}\} - V_{di,0}I_{di,0}. \tag{24}$$

The loss in the feedback charge path is obtained as follows

$$P_{\text{loss},C} = \frac{1}{2}\sum_{k=1}^{n}|I_{gy,k}|^2 R_{id} + \frac{1}{2}\sum_{k=1}^{n}|I_{gc,k}|^2 R_{is}. \tag{25}$$

The dc output power P_{dc} is consumed by load resistance R_L. And it is given by

$$P_{\text{dc}} = I_{di,0}^2 R_L \tag{26}$$

Thus, the energy conservation leads to the following equation

$$\begin{aligned} P_{in} = P_{\text{loss},s} + P_{\text{loss},M} + P_{\text{loss},po} + P_{\text{loss},pi} \\ + P_{\text{loss},T} + P_{\text{loss},C} + P_{dc}. \end{aligned} \tag{27}$$

From (1) to (27), the circuit performance can be solved if all transistor parameters and the input voltage are given. In Section III, the solution procedure based on a waveform-guided rectifier design method is given.

III. Waveform-Guided Self-Driving RF-DC Rectifier Design Method

Based on the circuit analysis performed in Section II, all the equations are ready for a rectifier design. In order to get a high-efficiency RF-DC rectifier design, specific waveforms must be achieved to reduce the transistor loss. From [12], the waveforms can be borrowed from high-efficiency power amplifiers. Hence, a direct waveform-guided matching network design method is adopted here other than a traditional impedance-guided method.

Usually, the RF nominal input power P_s, the dc load resistance R_L and the transistor are given as initial conditions. And the drain voltage $V_{di}(t)$ and current $I_{ds}(t)$ at the intrinsic port are designed to shape the target waveforms. In order to get a desired high-efficiency operation mode, a waveform-guided tool should be developed to drive the matching and gate coupling network design.

Because of transistor's nonlinearity, impedance distances cannot be used as a performance indicator while the waveform distance can. Thus, it is feasible and physically meaningful to treat a waveform distance as an indicator of a performance difference to the targets. A measure should be defined to quantify the distance between a realized time-domain waveform and the ideal target. In this paper, a simple normalized root-mean-square error $E_{\rm rms}$ is used to calculate the waveform distance

$$E_{\rm rms} = \frac{\int_0^T [x'(t) - x(t)]^2 dt}{\int_0^T x(t)^2 dt} \tag{28}$$

where $x(t)$ is the target voltage or current waveform and $x'(t)$ represents a transistor-rectifier generated waveform. The target waveforms can be determined from the classical PA researches, for example, class-E and class-F waveforms [24]. And it is not necessary to keep the time-reversal duality when determining the waveform targets.

Hence, a waveform-guided RF-DC rectifier design can be achieved in two steps, i.e., waveform generation and matching/coupling network calculation as shown in Fig. 3.

In the waveform generation step, the internal drain voltage V_{di} and current I_{ds} are used to monitor the practical rectifier's operations. Because I_{ds} can be calculated from (10), V_{gi} and V_{di} are adopted as the waveform generation variables. The initial values of V_{gi} and V_{di} are based on a random guess in a reasonable range, which can be estimated from target waveforms' Fourier expansion and transistor's transconductance. A gradient optimizer is used to update V_{gi} and V_{di} to decrease the voltage and current waveform distances. As the ideal target waveforms, which are obtained from classical theories, cannot be precisely reproduced in a practical rectifier, a proper waveform distance E_t is allowed in the waveform decision step.

In the matching/coupling network calculation step, $Z_{M,k}$ is to be determined from both the intrinsic circuit relation and the target waveforms. Internal port voltage and current are calculated to judge the stop criterion as shown in Fig. 3. Because the transistor's nonlinear current and charges are considered in the above discussed circuit analysis, a gradient optimizer is used to solve the equation set from (1) to (27). In this nonlinear solution process, a maximal magnitude of $Z_{M,k}$ below 300 Ω is

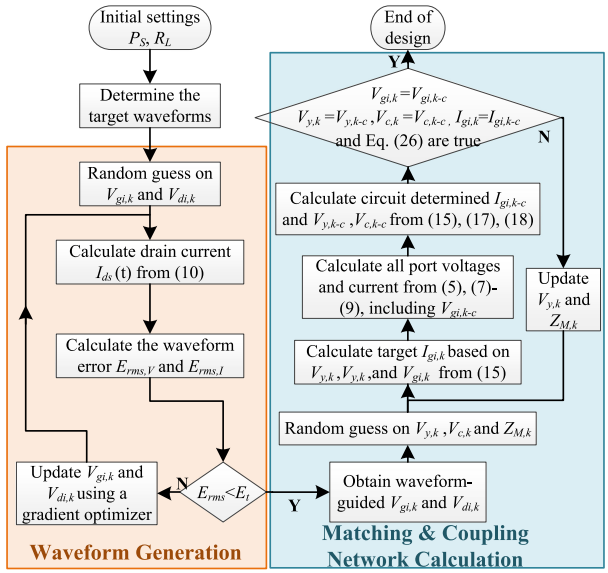

Fig. 3. Waveform-guided RF-DC rectifier's matching and coupling network design flowchart.

recommended for a realistic matching condition and solution convergence, even if the target waveforms cannot be exactly reproduced. We use a subscript "$_{-c}$" to represent the external passive-circuit-determined port-voltage/current, which are calculated from the real-time $Z_{M,k}$ settings. Only if the external circuit-determined voltage/current equal to the transistor's internal port variables, we can get the solution that the output matching and coupling network can generate the desired waveforms. Hence, the transistor's intrinsic-part-determined I_{gi}, the waveform-determined V_{gi}, and the real-time V_y and V_c are selected to be the decision variables.

A program can be coded to calculate the *Z*-parameters of the matching and coupling network based on the above-mentioned flowchart. Once the *Z*-parameters are obtained, a passive network can be synthesized to complete an RF-DC rectifier. A design example is given in Section IV to demonstrate this method.

IV. Self-Driving Class-E RF-DC Rectifier Design Example at 2.8 GHz

A Class-E rectifier operation mode is adopted here to show the waveform generation and passive network calculation method. The operation frequency is 2.8 GHz, and no external gate drive is applied in this example. A GaN device CGH40010F, from Wolfspeed, Co., NC, USA, is used to build this rectifier. However, the vendor's device model of CGH40010F does not include the behaviors under a reverse drain bias. As the rectifier utilizes negative-drain-voltage area as the primary operation region, we should modify its original model to accommodate a correct rectification operation.

A. Modified GaN Device's EEHEMT Model Including Reverse Drain Bias

Because the Wolfspeed's device model is not open to the public, we adopt the EEHEMT model shown in Fig. 1.

TABLE I
FITTED PARAMETERS FOR CGH40010F AT NEGATIVE DRAIN-SOURCE VOLTAGES

I_{dss}	V_{po}	P	W_{neg}	W_{pos}	A_{neg}
3.07	2.10	-3.91e-2	-1.25e-1	1.29	1.46e-2
A_{pos}	V_{knee}	S_{neg}	$gmvp$	S_{satn}	V_{satn}
7.35e-3	5.04e-1	36.94	3.98e-2	1.81e-1	6.13e-1
S_{sat1p}	V_{sat1p}	S_{sat2p}	V_{sat2p}	$atrval$	N
1.66e-1	-1.00	3.32e-2	3.24	-1.79e-1	1.33
V_{pdec}					
-2.03e-1					

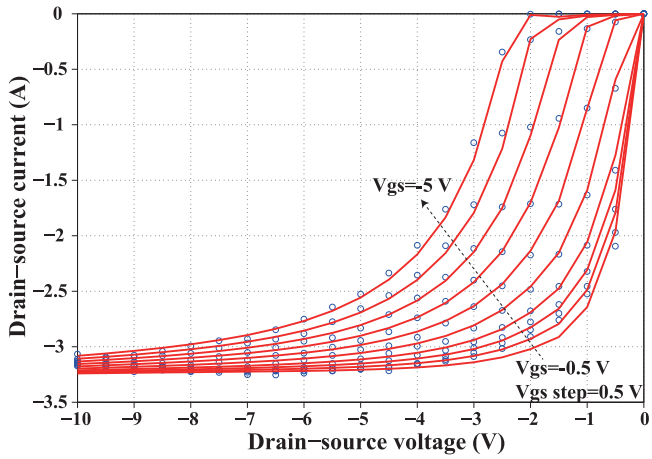

Fig. 4. Measured (circle) and fitted (line) dc I-V data of CGH40010F under negative drain voltages.

Apparently, the nonlinear current source should be expanded to contain the practical measured data of negative drain voltages. The rest parasitics and nonlinear charges are kept the same to the parameters extracted from Wolfspeed's model, as the vendor's characterization is more reliable based on well-equipped massive measurements.

In Section II, the calculation of (10) needs to define $f(\cdot)$ explicitly. This function is expressed as current equations in a GaN device model. For a physical transistor, drain current can be divided into dc and ac parts affected by high-order thermal and trapping effects. In order to highlight the most critical factors, only dc I-V curves are defined for $f(\cdot)$ in this paper by ignoring the high-order effects. The calculation errors can be verified to be small in the following simulations.

As studied in [11], the GaN device's dc I-V relation is not symmetrical when reversely biased. Pulsed isothermal dc measurements at room temperature of 25 °C were performed to collect the physical I-V data of CGH40010F. The transistor's quiescent drain bias is 0 V, and gate bias is −3.4 V, and every pulse was generated from this initial setting. The pulse length was 200 μs with a period of 2 s for sufficient cooling. Due to limited pulse capability, the pulsewidth setting was not short enough to avoid junction temperature changes. The final measured dc I-V curve may contain some of the residual effects of thermal dynamics, which were ignored in our design. The current equations in [11] are also adopted to model the reverse drain-source bias states, while the thermal effects are not considered yet in this regard. The modeling task is not the scope of this paper, and only the fitted parameters are given in Table I. The parameter definitions can be found in [11].

The measured dc data and the fitted results are shown in Fig. 4. In the measurements, V_{ds} was swept from −10 to 0 V by a 0.5 V step, and V_{gs} was swept from −5 to −0.5 V by a 0.5 V step. Concluded from this figure, the minor fitting errors can be accepted in this design. By embedding the current equations at negative drain voltages into the original EEHEMT model of CGH40010F, we can get the modified dc I-V curve from the model across the entire operation region of an RF-DC rectifier as shown in Fig. 5. In the following example, these I-V data

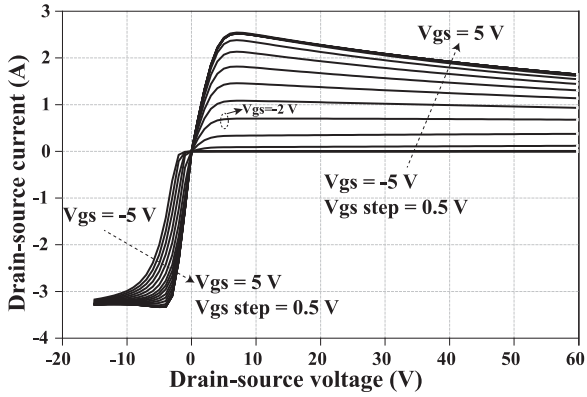

Fig. 5. Simulated dc I-V data of the CGH40010F's EEHEMT model at 25 °C.

are used to define $f(\cdot)$. The related EEHEMT model's parameters, which will be used in this design example, are shown in Table II. And the dc I-V function at the positive drain voltage, the nonlinear charges, and the package parasitics can be found in this table. The detailed information about the parameters can be found in [20].

B. Class-E RF-DC Rectifier's Approximated Waveform Design

The design task is to rectify a 10 W input RF power at 2.8 GHz and deliver it to a 50 Ω dc load. In order to get a high-efficiency operation, class-E waveforms with flipped current are selected to be the targets. According to time-domain analysis, dual component values can be obtained through the time-reversal duality between a class-E PA and a class-E rectifier. Thus, time-reversal duality waveforms become fundamental choices when realizing an RF-DC rectifier [12]. It is not necessary to strictly follow the time-reversal duality with our waveform-guided design method. Our method can help to obtain realizable load impedances under minimized time-domain waveform-distance compared to the targets. The theoretical harmonic load-impedances, if unphysical, will be modified afterward according to the passive network assumption and minimum waveform-distance criterion.

TABLE II
FITTED DC AND CHARGE PARAMETERS FOR CGH40010F'S EEHEMT MODEL

V_{to}	Gamma	V_{go}	V_{delt}	V_{ch}	Gm_{max}
-3.80	2.16e-4	-1.99	0	1	0.83
V_{dso}	V_{sat}	Kapa	P_{eff}	V_{tso}	R_{id}
30.82	6.18	3.28e-3	175.40	-4.34	13.38
C_{dso}	C_{11o}	C_{11th}	V_{infl}	Deltags	Deltads
8.83e-13	4.12e-12	5.46e-16	3.49e-4	3.27	20.65
$Lambda$	$C12_{sat}$	Cgd_{sat}	R_d	R_g	V_{co}
0.05	2.48e-17	7.49e-15	0.01	4.23	-0.91
V_{ba}	V_{bc}	Mu	Deltgm	Alpha	R_{pd}
20.22	3.41	-7.42e-3	4.01	12.82	0.62
L_{pd}	C_{pd}	Z_{cd}/θ_d	R_{pg}	L_{pg}	C_{pg}
0.65e-9	1.13e-12	38.80/1.98	1.98e-3	1.80e-11	4.40e-12
Z_{cg}/θ_g					
31.08/9.80					

TABLE III
OPTIMIZED $V_{gi,k}$ AND $V_{di,k}$, AMPLITUDE/PHASE(rad)

$k=$	1	2	3	4	5
$V_{gi,k}$	2.4/-2.3	0.6/2.0	0.5/1.4	0.5/1.9	0.03/-2.96
$V_{di,k}$	32.3/0.9	17.1/1.8	4.6/2.8	0.04/2.67	0.2/1.8

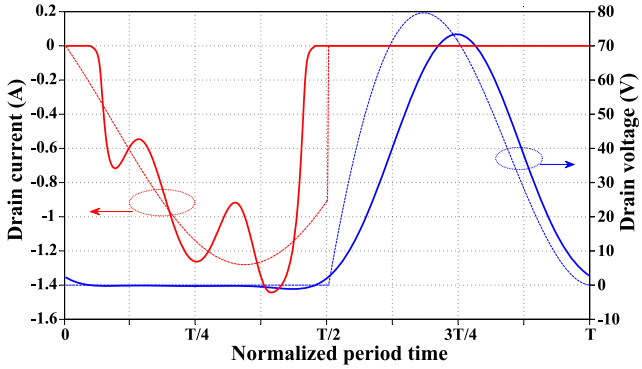

Fig. 6. Optimized class-E rectifier's waveforms (solid) in comparison to the conventional ones (dashed). Current waveforms are in red, and voltage waveforms are in blue.

Thus, approximated operation waveforms can be realized starting from an ideal waveform target.

The standard class-E rectification waveform shapes can be generated by simply flipping the current according to the equations of [24]–[27], but they cannot be precisely reproduced using a practical transistor. Furthermore, very high peak drain voltage can lead to a reliability issue even for a GaN device. In the following design, the gate dc bias is set to be -3.4 V, which is the pinched-off voltage in simulations. The target waveforms are generated from an ideal 10 W class-E power amplifier with $\sqrt{500}$ V drain dc supply. The ideal load impedances from dc to the fifth harmonic are 50 Ω, $-46.6 - \mathrm{j}33.2$ Ω, $-6.7 + \mathrm{j}106.3$ Ω, j55.2 Ω, j38.8 Ω, and j30.2 Ω, respectively. The negative real part of the fundamental tone is a normal result of rectified RF input power, but the negative real part of the second-harmonic means that an additional harmonic power is needed. This unphysical negative impedance can be modified naturally in the waveform generation process by considering the passive network assumption and practical transistor's behaviors with our method. Hence, any kind of high-efficiency PA waveforms can be used as a candidate, if reasonable waveform distance can be acceptable under a certain efficiency requirement.

By using (28) and Fig. 3, approximated class-E waveforms can be generated considering the transistor's physical behaviors. As our rectifier involves a self-driving topology, the feedback drain-to-gate current, caused by nonlinear charges, is critical. Hence, up to the fifth harmonic is considered in calculations to reduce the errors caused by the possible large high-order-derivative current.

The variables $V_{gi,k}$ and $V_{di,k}$ are optimized to get close to the target drain voltage and current waveforms. With our solution algorithm, the two variables can be determined as shown in Table III while guaranteeing good rectifying efficiency and waveform constraints. The optimized waveforms are shown in Fig. 6. The final waveform distances E_{rms} are 0.320 and 0.519 for the voltage and current, respectively. The peak drain voltage has been reduced from 79.7 to 73.4 V. Different from the class-E power amplifier, flipped drain current and negative voltage occur in the ON-state. These target waveforms can offer 19.13 V output dc voltage, 7.32 W output power on an external 50 Ω dc load, and 73.2% rectification efficiency. Also in this step, the actual waveform's phase offset is not determined yet. And possible losses in the matching network are also not considered. When calculating this efficiency, we assume all the input 10 W power is utilized by this rectifier transistor (underlying assumptions of the lossless external network). The target-waveform generation step does not yet involve the undetermined three-port matching and coupling network, which will be considered as a lossy one in the following analysis.

C. Solution to Output Matching and Coupling Network's Z-parameters

The self-driving rectifier's circuit topology is shown in Fig. 2, and it is important to determine the three-port matching and coupling network for high-efficiency operations after the target rectification waveforms are determined. Both the operation modes and rectifier's performances rely on this network. We skipped the step of designing and testing a power amplifier, and directly calculated and designed the matching and coupling network compared to a PA-first design method. In Section II, we used Z-parameters to characterize it. Hence, the current design job is to calculate them.

TABLE IV
Z_M [AMPLITUDE/PHASE(rad)] SOLUTIONS OF THE MATCHING AND COUPLING NETWORK

$k=$	1	2	3	4	5
$Z_{M,k,11}$	90.56/-1.40	11.57/-1.35	7.95/-0.70	51.50/1.57	16.04/1.44
$Z_{M,k,12}$	154.65/1.78	25.70/1.70	54.17/1.44	1.03/-2.08	20.03/1.92
$Z_{M,k,13}$	19.84/3.08	1.30/2.75	36.80/-1.58	4.12/1.82	21.34/-1.09
$Z_{M,k,22}$	215.61/-1.24	75.28/-0.93	22.77/1.13	50.03/0.03	108.13/-1.36
$Z_{M,k,23}$	42.14/-0.05	8.83/0.17	109.12/-1.55	1.70/1.08	91.50/1.94
$Z_{M,k,33}$	28.18/-0.48	10.28/-1.38	120.99/1.27	104.57/1.80	88.57/-0.99

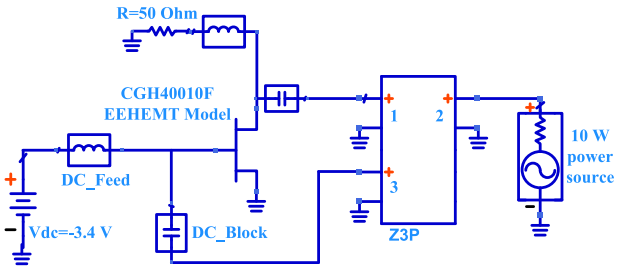

Fig. 7. Virtual test circuit of the calculated Z_M.

In this step, the practical waveform's phase offset is also determined with the *Z*-parameters using the program flowchart shown in Fig. 3. First, this passive matching network is assumed to be reciprocal and lossy, because practical microstrip lines and discrete capacitors are lossy components. The passive elements' physical models will be considered in the network synthesis section. A part of 10 W input power will dissipate in these lossy components, and it will lead to a bit efficiency drop compared to the above waveform calculations. The port variables and *Z*-parameters can be solved based on (1)–(27) and Fig. 3. *Z*-parameters of this matching network is shown in Table IV.

In order to verify that these Z_M solutions can produce the desired waveforms and performances, a virtual test circuit is built up as shown in Fig. 7, including a Z_M-based three-port passive network and the modified EEHEMT model of CGH40010F. This three-port passive matching network, denoted as "Z3P", is parameterized by the solutions of Table IV. Ideal dc feeds and blocks are used to present Z3P's impedances to the transistor's terminals. A harmonic-balanced (HB) simulation in *Keysight's advanced design system* (ADS), using a complete EEHEMT model, is carried for this test circuit. The HB simulated waveforms are shown in Fig. 8. In this figure, the calculated current and voltage are redrawn from Fig. 6 with a phase offset in order to align the waveforms. The realized waveforms have a phase offset of 1.1 rad compared to the calculated ones shown in Fig. 6.

Apparently, the simulated drain voltage closely follows the calculation results. However, the HB simulated current has different fluctuations, when compared to the calculations. The main reason is the HB simulation results only keep five-order results, while our drain current is directly determined from (10) based on nonlinear dc I-V curves. After truncating high-order harmonics

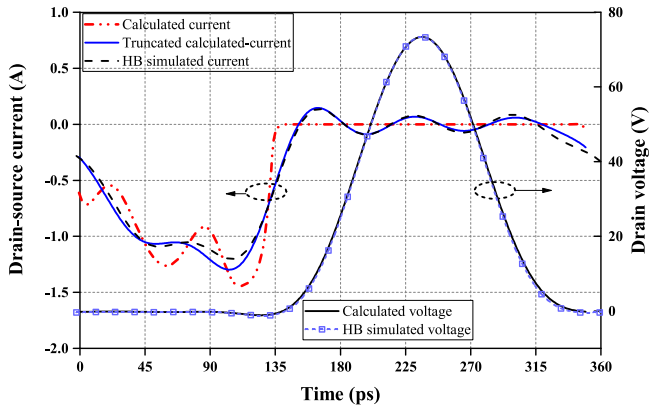

Fig. 8. Harmonic-balanced simulation waveforms in comparison to the calculated drain current (with truncations) and voltage.

from the calculated current, its fluctuations become synchronous with the HB simulations. The simulated rectification efficiency is 70.9%, and the output dc voltage is 18.83 V for a full EEHEMT model. Compared to the calculation value, the output dc power is lower by 0.23 W (3.1% lower compared to the theoretical calculated power), and it is mainly caused by the losses in the matching network, ignored thermal effects, dispersion current slightly affecting high-frequency performance [22], and different solution mechanisms between ADS and our program.

D. Synthesis of the Matching and Coupling Network

If we can realize Z_M shown in Table IV, a rectifier can be built according to our desired class-E waveforms and performances. However, it is hard to find such a precise network synthesis result satisfying all parts of Z_M, by using practical lossy microstrip lines and capacitors. Hence, the most sensitive Z_M terms must be identified and assigned with the highest weight before the synthesis work begins.

However, S-parameters are more popular for microwave passive network synthesis. Thus, Z_M is transformed into its corresponding S-parameters S_M in this section. A sensitivity analysis is performed in ADS using the test circuit of Fig. 7. The sensitivity was calculated as its rectification efficiency's (RE) partial derivate on every S_M variable's phase (in radians) and magnitude, namely sensitivity $= \partial \mathrm{RE}/\partial S_M|_{S_M}$, and the calculation method can be found in ADS help documents [28]. And the S-parameters with the top eight sensitivity (higher than 0.15) will be realized as the first priority. The target S_M, which is transformed from Table IV, is shown in Table V. The tabular cells with yellow color and a "†" symbol have the first priority, the blue cells with a "⋆" symbol have the second priority (with sensitivity higher than 0.04). And the rest is not controlled in the network synthesis step. The top eight sensitivity terms contain the fifth harmonic impedance at the drain port because this self-driving rectifier's efficiency is very sensitive to the feedback path's harmonic current Its magnitude sensitivity result is 0.50, which is ranked the fifth among these top eight items. It is the reason why we include harmonic number up to 5.

The final topology and dimensions of the matching and coupling network are shown in Fig. 9. The laminate is Rogers 4350 b

TABLE V
REALIZED S_M OF THE MATCHING AND COUPLING NETWORK

$k=$	1	2	3	4	5
$S_{M,k,11}$	$\frac{0.34/2.49}{0.35/2.48}$ *†	$\frac{0.77/-2.86}{0.88/-2.86}$ †	$\frac{0.50/-1.94}{0.52/-2.17}$ ⋆	$\frac{0.93/1.44}{1/1.54}$ ⋆	$\frac{0.96/2.39}{0.96/2.39}$ †
$S_{M,k,12}$	$\frac{0.86/2.68}{0.88/2.68}$ †	$\frac{0.37/-0.80}{0.40/2.39}$	$\frac{0.37/1.64}{0.45/1.61}$ †	$\frac{0.01/2.60}{0.01/-2.83}$	$\frac{0.07/-0.39}{0.17/2.87}$
$S_{M,k,13}$	$\frac{0.17/-0.91}{0.19/-0.87}$ †	$\frac{0.15/2.20}{0.03/-0.81}$	$\frac{0.05/-1.51}{0.42/-3.08}$	$\frac{0.07/-0.58}{0.05/-0.10}$ ⋆	$\frac{0.02/-0.69}{0.20/-0.80}$
$S_{M,k,22}$	$\frac{0.35/0.03}{0.39/0.03}$ ⋆	$\frac{0.84/-2.26}{0.47/-0.99}$	$\frac{0.80/2.00}{0.50/-0.74}$	$\frac{0.95/0.56}{0.02/1.59}$	$\frac{0.92/-0.15}{0.42/-1.53}$
$S_{M,k,23}$	$\frac{0.16/0.75}{0.17/0.75}$ †	$\frac{0.06/-2.98}{0.14/0.92}$	$\frac{0.03/-2.50}{0.50/-0.74}$	$\frac{0.00/2.41}{0.02/-0.01}$	$\frac{0.01/-2.05}{0.79/2.99}$
$S_{M,k,33}$	$\frac{0.45/-2.34}{0.46/-2.34}$ †	$\frac{0.87/-2.75}{0.95/-2.72}$	$\frac{0.92/-2.77}{0.53/0.21}$	$\frac{0.87/0.92}{1.00/0.91}$ ⋆	$\frac{0.73/-0.66}{0.15/-2.66}$

* S-parameter is written in polar form, $\frac{\text{Realized}}{\text{Target}}$.

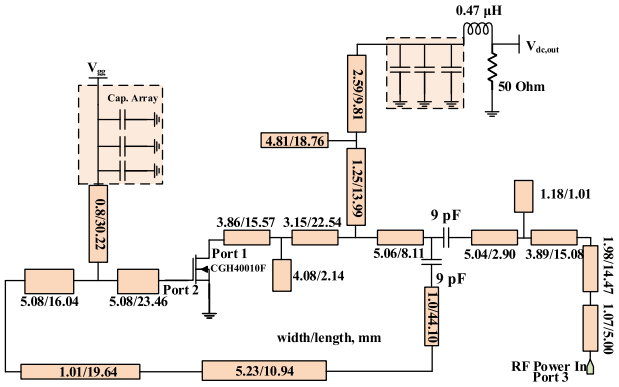

Fig. 9. Circuit topology and line dimensions of the realized matching and coupling network.

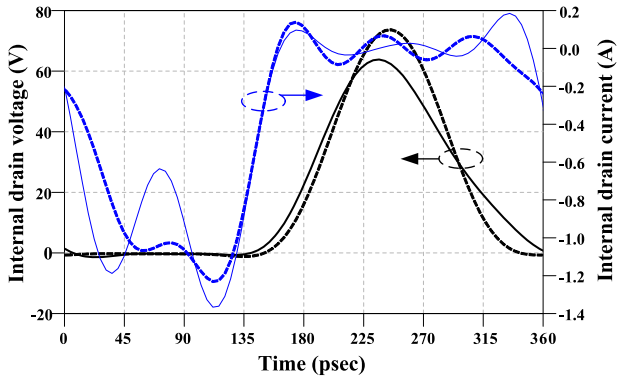

Fig. 10. HB simulated internal drain voltage and current waveforms (solid lines) for the realized rectifier circuits in comparison with the results of ideal Z_M (dashed lines).

TABLE VI
NORMALIZED FOURIER COMPONENTS (MAG/RADIANS) FOR IDEAL FLIPPED CLASS-E, APPROXIMATED WAVEFORMS, AND THE REALIZED WAVEFORMS

$k=$		DC	1	2	3	4	5
Ideal	Voltage	0.60	1.00/0.00	0.54/2.46	0.16/-1.04	0.06/2.72	0.03/-0.57
	Current	0.69	1.00/0.00	0.29/-1.70	0.17/1.14	0.09/-1.38	0.06/1.61
Approxi-mated	Voltage	0.59	1.00/0.00	0.55/2.00	0.16/-2.30	0.00/-1.17	0.01/-1.40
	Current	0.63	1.00/0.00	0.43/-1.58	0.13/1.60	0.19/-0.89	0.17/2.95
Realized	Voltage	0.64	1.00/0.00	0.41/2.13	0.11/-1.25	0.04/1.16	0.01/0.28
	Current	0.63	1.00/0.00	0.34/-1.44	0.30/0.68	0.44/-0.67	0.14/-1.86

with a thickness of 20 mils and the relative dielectric constant of 3.66. Because universal network parameters are determined to realize the target waveforms prior to the determination among various line topologies and dimensions, the matching topology can be changed and optimized for a specific waveform target considering the sensitive items. The initial topology was chosen based on experiences, and it was modified during optimizations in order to best fit the matching S-parameters. The T-junction and microstrip-line step are omitted in this figure. The dc feed line was not optimized independently, and all the network, including the non-ideal capacitor array, are optimized together to satisfy the S-parameter requirements. The three-port passive network's line dimensions are optimized in a small-signal S-parameter simulator in ADS. With considerations on the priority settings obtained from the sensitivity results, the realized S-parameters are also shown in Table V. All the yellow and blue cells are realized with comparatively low errors.

We adopt this three-port network with coupling connection to provide a stable gate power injection, which will be helpful at high frequency. However, it is still an excellent choice to realize a self-driving rectifier through the intrinsic capacitor feedback only [9], [14]. If no external coupling connection is needed, the gate termination results can also be directly obtained from our circuit analysis method by presetting the corresponding $Z_{M,k,23}$ and $Z_{M,k,12}$ to infinity (or $S_{M,k,23}$ and $S_{M,k,12}$ to zeroes in the S-parameters). We can delete the coupling connection in the three-port network, and realize this alternate matching with the calculated Z_M/S_M parameters. Thus, our method can accommodate both network configurations if necessary.

In order to verify the designed matching and coupling network, an HB simulation at 2.8 GHz is run for the complete rectifier circuit. The simulated output dc voltage and power are 18.8 V and 7.07 W, respectively. Thus, a 70.7% rectification efficiency is obtained. The results are close to those of Section IV-C, which were directly obtained from the ideal *Z*-parameters. This simulation proves that the network realization based on sensitivity priority is feasible.

The simulated internal voltage and current waveforms are shown in Fig. 10. Because not all of the S-parameters have been realized, the waveforms deviate from the virtual simulations and calculations but with acceptable errors. In order to verify the approximated and realized waveforms are close to standard class-E, the corresponding Fourier components, normalized to the fundamental tone, are shown in Table VI. The normalized-ratio-vector errors, which are higher than 15% compared to the ideal class-E, are highlighted in orange cell color. As we can see, most approximated harmonic components are close to the ideal targets.

As we assumed a practical passive load matching network in our calculations, the second and other necessary higher harmonic components were modified to realizable values. Furthermore, the realized current collects the most errors, partly due to limited matching capability when realizing the S_M table. The

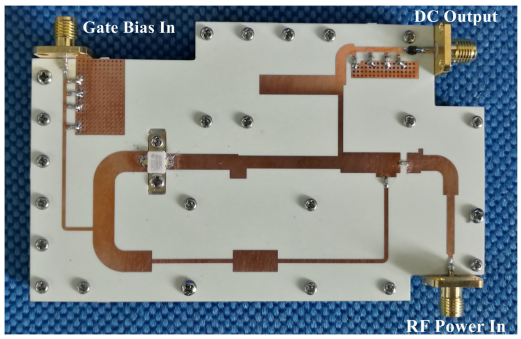

Fig. 11. Photo of the self-driving RF-DC rectifier.

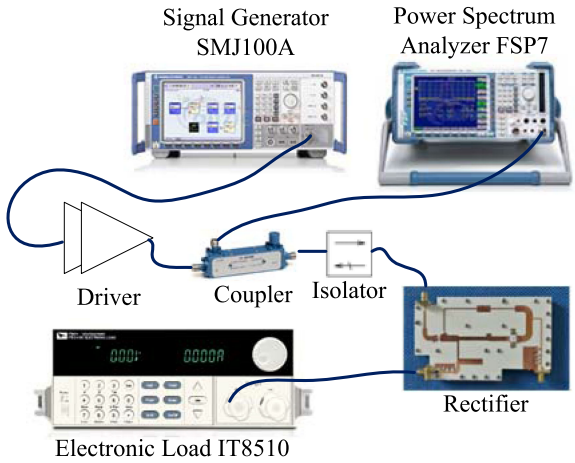

Fig. 12. Measurement setup of this rectifier.

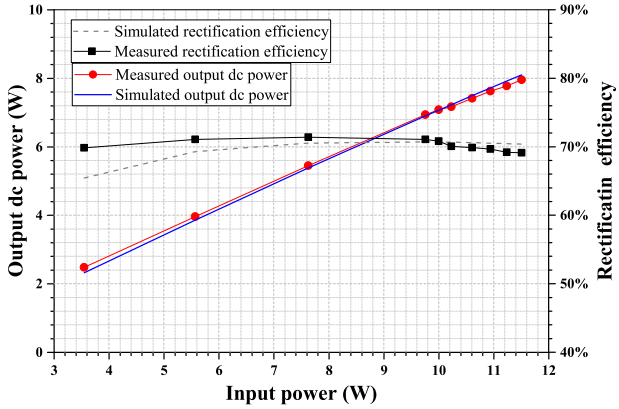

Fig. 13. Output dc power and rectification efficiency versus input RF power.

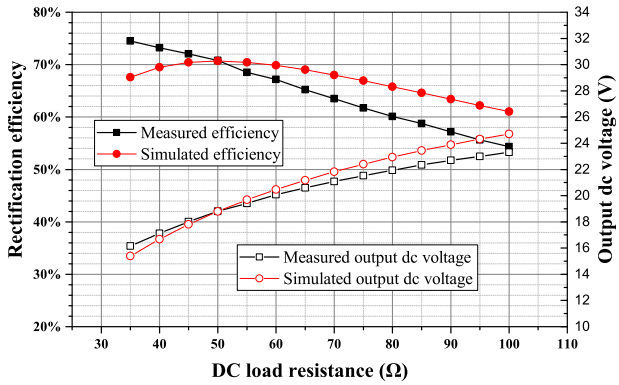

Fig. 14. Rectification efficiency versus load resistances.

realized load impedances at the drain current generator plane are 50.7 Ω, −51.0−j15.1 Ω, 52.1 + j38.8 Ω, 79.5 + j72.6 Ω, 3.5 + j3.6 Ω, and 7.1−j1.8 Ω from dc to the fifth harmonic, respectively. From the impedances, there does exist a discrepancy between the ideal and realized ones. The impedance deviations are caused by realizable waveform differences at microwave band with a practical transistor and by our algorithm's modifications on unphysical impedances. Furthermore, it is not a good choice to use the ideal class-E impedances as a design target if it cannot be precisely realized, because it is difficult to evaluate the rectifier performance difference by impedance distance. Usually, a small waveform error can induce a large harmonic impedance distance. Compared to Fourier components of an ideal inverse Class-F waveforms, the approximated and realized waveforms deviate far from them especially for the nulling values of even current harmonics and odd voltage harmonics [24]. Thus, the approximated and realized waveforms can be defined as a modified class-E mode according to its moderate time-domain and frequency-domain errors.

V. Experiments and Measurements

With the line dimensions shown in Table V, this rectifier is fabricated as shown in Fig. 11. In order to get a compact circuit, some of the microstrip lines are bent with a slight dimension adjustment.

The measurement setup is shown in Fig. 12. The RF input power is amplified through a two-stage driver, and it is fed into the rectifier with an isolator. The constant 50 Ω resistance is realized through an electronic load IT8510 from ITECH Co., Nanjing, China. The real-time input power is measured through a coupler after calibration with R&S power spectrum analyzer FSP7. The output dc power and current are read from IT8510.

The measured rectification efficiency and output dc voltage versus input power are shown in Fig. 13. When the input power is 10 W, and gate dc bias is −3.4 V, the measured output dc power is 7.08 W, and the rectification efficiency is 70.8%. The maximum efficiency of 71.4% is recorded for a 7.6 W power input. The measured efficiency can be kept higher than 68% when input power is higher than 3.5 W. High rectification efficiency at input back-off region was well explained in [29]. However, if the input power is further decreased and the gate bias is kept constant, this self-driving rectifier cannot operate due to insufficient gate drive. In Fig. 13, the absolute maximal output power and the efficiency errors are 0.16 W and 4.4%, respectively.

The measured rectification efficiency and output dc voltage are also given for different load resistances as shown in Fig. 14. It shows that an RF-DC rectifier can accommodate certain load variations. In this example, higher than 54% rectification efficiency is recorded for the load resistance range from 35 to 100 Ω. The maximal rectification is 74.5% for a 35 Ω load. In Fig. 14, the maximal output power and efficiency errors are

TABLE VII
RELATIVE RESULTS OF SELF-DRIVING TRANSISTOR RECTIFIER

Ref.	Freq.	RF power	Efficiency	Device	Gate Tuning
2017 [15]	1.8 GHz	10 W	77%	GaN	Tunable phase shifter
2015 [30]	1.85 GHz	10 W	83.6%	GaN	Fixed gate-load
2015 [31]	0.91 GHz	11.9 W	85%	GaN	Tunable phase shifter
2012 [9]	2.14 GHz	10 W	85%	GaN	Gate impedance tuner
2016 [29]	1.05 GHz	10 W	72%	GaN	Tunable phase shifter
This work	2.8 GHz	10 W	70.8%	GaN	Not required

0.69 W and 6.9%, respectively, recorded at 35 Ω load compared to simulations. In general, the simulation results are close to the measurements, and the performance discrepancy is mainly related to modeling inaccuracy.

Some reported results for self-driving transistor rectifier are listed in Table VII for comparisons. And our work has offered relatively good performance at 2.8 GHz without any external gate tuning support.

VI. CONCLUSION

An RF-DC rectifier was usually designed after a power amplifier prototype according to waveform duality relation, and the synchronous gate driving was achieved by an adjustable phase shifter. In this paper, a waveform-guided coupling and matching network design method are proposed. With the aid of a large-signal analysis including transistor's package parasitics, nonlinear capacitances, and dc I-V curves, *Z*-parameters of the passive network can be directly calculated to satisfy the synchronous phase relation and waveform requirements. A 2.8 GHz class-E RF-DC rectifier is demonstrated as a design example. Quasi-class-E waveforms can be generated without a PA prototype support, and the self-driving rectification efficiency of 70.8% is measured at a 10 W RF input.

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