Analysis and Experimental Evaluation of Middle-Point Inductance's Effect on Switching Transients for Multiple-Chip Power Module Package

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***Abstract*—Middle-point inductance L_{middle} can be introduced in multiple-chip power module package designs. In this paper, the effect of middle-point inductance on switching transients is analyzed first using a frequency-domain analysis. Then a dedicated multiple-chip power module is fabricated with the capability of varying L_{middle}, and extensive switching tests are conducted to evaluate the middle-point inductance's impact. Experiment result shows that the active MOSFET's turn-on loss decreases at higher values of L_{middle}, while its turn-off loss increases. Detailed analysis of this loss variation is presented. In addition to the switching loss variation, it is also observed that different peak voltage stresses are imposed on the active switch and antiparallel diode during the switching transients. Specifically, in the case of lower MOSFET's turn-off, the maximum voltage of the lower MOSFET increases as L_{middle} goes up; however, the peak voltage of the antiparallel diode decreases significantly. The induced voltage spikes during upper MOSFET turn-on process is also evaluated, and an opposite trend is observed experimentally. Analysis of the voltage overshoot variation is discussed. Based on the experimental evaluation and analysis, a multiple-chip power module package design guideline is summarized considering the middle-point inductance's effect.**

***Index Terms*—Middle-point parasitic inductance, power module package, silicon carbide (SiC) MOSFETs, switching transients, split converter.**

Manuscript received May 8, 2018; revised August 15, 2018; accepted October 7, 2018. Date of publication October 21, 2018; date of current version May 2, 2019. This work was supported by the Electric Drive Technologies Program, DOE Vehicle Technologies Office, under Contract DE-AC05-00OR22725 with UT-Battelle, LLC, by the Engineering Research Center Program of the National Science Foundation and the Department of Energy under NSF Award EEC-1041877, and by the CURENT Industry Partnership Program. Recommended for publication by Associate Editor W. Cao. *(Corresponding authors: Fei Yang and Zhiqiang Wang.)*

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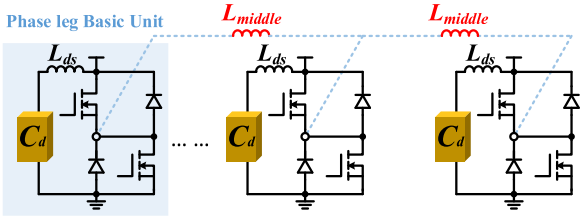

Fig. 1. Package design with identical scaling.

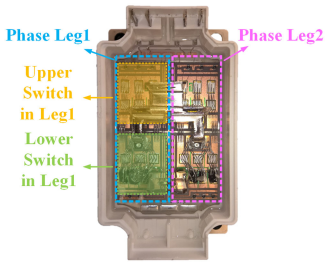

Fig. 2. Commercial SiC open module from Wolfspeed.

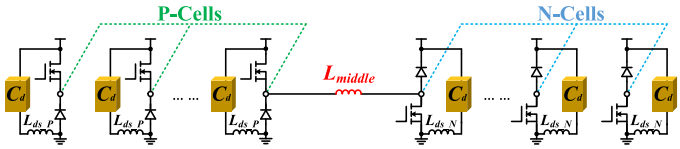

Fig. 3. Package design with split scaling.

It is observed that for both split scaling and identical scaling methods, the output or middle point of each cell needs to be connected. This is realized either through direct bonded copper (DBC) level copper trace or external connections. Correspondingly, a new parasitic inductance parameter L_{middle} is introduced. In this paper, the effect of middle-point inductance L_{middle} on the device's switching transients is investigated.

Previous studies have evaluated three main parasitic parameters' effect on the switching transient of a phase leg configuration, namely, they are the gate loop parasitic inductance L_g, the common source parasitic inductance L_{cm}, and the power loop inductance L_{ds}. The gate loop parasitic inductance L_g can cause gate voltage swings during the switching transients, which can potentially exceed the maximum voltage rating of the gate oxide [15], [16]. The common source inductance L_{cm} is the inductance shared by power loop and gate loop [17], and it can slow down the switching transient [18] or cause false turn-on [19]. As discussed earlier, the power loop inductance L_{ds} can lead to large voltage spikes during the switching transient [18]. However, none of these studies investigated the middle-point inductance's effect.

Some of the split-converter designs discussed the role of middle-point inductance L_{middle} [20], [21]. Both pointed out that the turn-on loss is reduced in split converter designs. In [21], the benefits of reduced dv/dt at the output terminal and decreased crosstalk effect are observed. The author also points out the turn-off loss will increase at larger values of L_{middle}.

However, the value of L_{middle} in those split converters are large: usually in the range of tens of μH. For multichip power modules with P-N-cell split scaling design, L_{middle} is formed by the thick copper trace on the DBC with short connections. Therefore, the middle-point inductance value is normally within several hundreds nH. With a small value, the middle-point inductance will affect the switching transients more actively. Moreover, none of the previous studies exploits the influence of L_{middle} on the device's voltage spikes during switching transients. Since the voltage overshoot is an important factor determining the maximum load current and switching speed of switching devices, it is meaningful to have a more comprehensive understanding of the effect of L_{middle} on device's operation stress.

In the following sections, detailed analysis and experimental results are provided to evaluate the middle-point inductance's effect. The paper is organized as follows. In Section II, a multiple-frequency ringing phenomenon is observed in an SiC power module with multiple chips. The explanation is given based on a frequency-domain analysis, and it is discovered that the middle-point inductance can affect the switching transients actively. To investigate the influence of L_{middle}, in Section III, a dedicated module is packaged with the capability of altering the values of middle-point inductance. Extensive tests are carried out under different cases to study the middle-point inductance's effect. Following the experiment result, conclusions are given in Section IV and a design guideline is provided for package layout with multiple chips.

II. Frequency-Domain Analysis of the Multiple-Frequency Ringing Phenomenon in an SiC Multichip Power Module

The motivation to study the middle-point inductance's effect arises from an experimental observation of multifrequency ringing in the switching waveforms of a multiple-chips SiC power module. The power module in the experiment has a phase leg configuration, and its circuit diagram and physical layout are illustrated in Fig. 4. P-cell/N-cell design methodology is adopted, and the middle points of the P-cell and N-cell are connected through the DBC-level copper trace, which forms L_{middle}, as illustrated in Fig. 4(b). For each switch, six 1200-V SiC Trench MOSFETs are used as paralleled diodes and three 1200-V SiC Schottky diodes are used as antiparallel diodes. To minimize the dynamic current sharing issue among paralleled devices, the MOSFETs with similar static characteristics (mainly threshold voltage, on-resistance, and transconductance) are selected in parallel and the package is also accommodated to minimize the power loop inductance difference among paralleled devices. In addition, the real voltage of each device can be measured through the Kelvin connections, and details about this package have been discussed in [22]–[25].

The gate drive board is mounted on top of the power module, and the driving capability for these paralleled devices is ensured by using a buffer chip with 30 A peak source/sink capability. A double pulse test (DPT) bench is built, as shown in Fig. 5, and it is configured such that the lower MOSFETs are the active switching devices. The drain current is measured through an on-board 15 mΩ coaxial shunt (SSDN-015 from T&M Research). Short coaxial cable is used to mitigate the cable parasitic inductance's

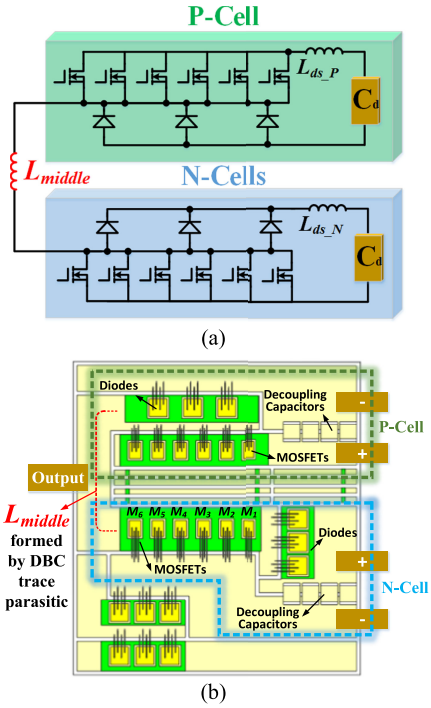

Fig. 4. Illustration of the SiC multichip power module. (a) Circuit diagram. (b) Physical layout.

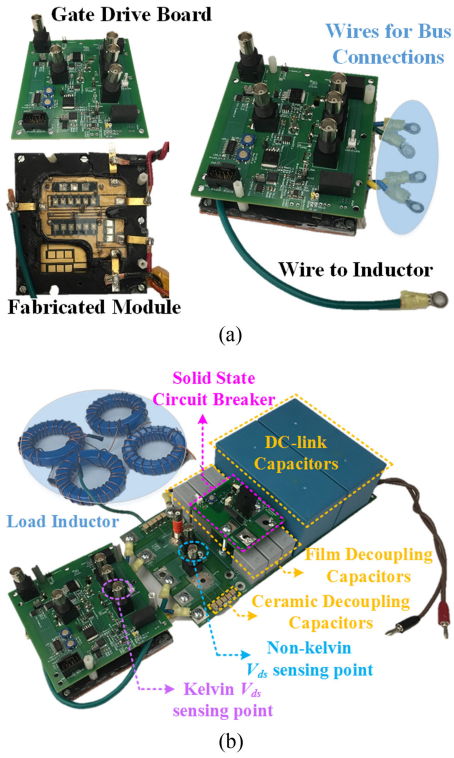

Fig. 5. Illustration of the experiment setup. (a) Real power module with a gate drive board. (b) DPT setup for the power module.

effect on the measurement accuracy. Considering the parasitics, the circuit diagram of the DPT is shown in Fig. 6.

A. Multiple-Frequency Ringing Phenomenon in SiC Power Module with Multiple Chips

At first, only the N-cells are connected to the dc-link for switching performance evaluation. The experimental turn-off switching waveforms of low-side MOSFET's Kelvin drain-to-source voltage, drain current, and the gate voltage are shown in Fig. 7. The load current is 100 A, dc-link voltage is 600 V, and the external turn-off gate resistor's value is 5 Ω. As expected, only one resonant frequency (22 MHz) is observed during the ringing period, which is determined by the junction capacitance of the paralleled MOSFETs and the lumped power loop inductance. With a junction capacitance value of 644.9 pF at 600 V from the static characterization, the power loop inductance is calculated to be

$$L_{ds\_N} = \frac{1}{4 \cdot \pi^2 \cdot f_0^2 \cdot C_{\mathrm{ds}}} = 81.15\,\mathrm{nH}\,. \tag{1}$$

In the next step, both P-cells and N-cells are connected to the power stage board for DPT. The experiment condition is the same as the N-cell test. The turn-off waveforms are shown in Fig. 8. The Kelvin voltage waveform of the lower antiparallel diode is illustrated in the orange line. As can be seen, the voltage of the lower MOSFET and lower antiparallel diodes are different. Meanwhile, two resonant frequencies are observed for both voltages. One is around 24.27 MHz, and the other is around 2 MHz.

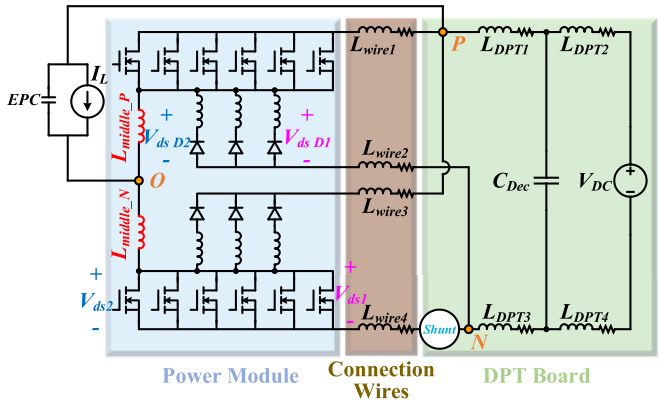

Fig. 6. Circuit diagram of the whole DPT setup.

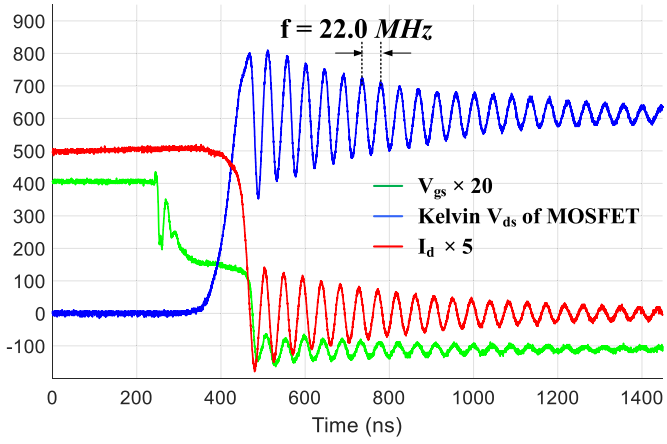

Fig. 7. Turn-off waveforms of lower MOSFET with N-cell.

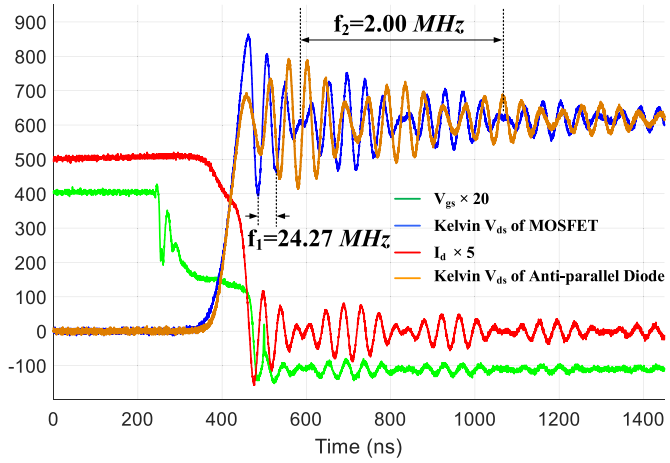

Fig. 8. Turn-off waveforms with the P-cell and the N-cell connected.

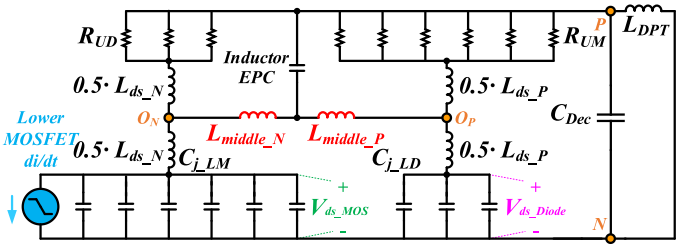

Fig. 9. High-frequency equivalent circuit of the DPT during turn-off ringing period with the P-cell and the N-cell connected.

B. Frequency-Domain Analysis of Multifrequency Ringing

To determine the cause of this multiple frequency ringing, the high-frequency equivalent circuit diagram of the circuit during the ringing period is shown in Fig. 9. On the load inductor side, its equivalent parallel capacitor is considered. Both the low-side MOSFETs and antiparallel diodes are modeled as a capacitor with a single value. The high-side MOSFETs and antiparallel diodes are modeled as resistors at high frequency since both are conducting the load current during the ringing period. The decoupling capacitor is also considered in the circuit diagram. The dc-link capacitor is shorted at high frequency. Meanwhile, the middle-point inductance is shown in red.

During the ringing period, the excitation for this impedance network is the low-side MOSFET channel's di/dt. It generates excitations at various frequencies. Correspondingly, these excitations cause voltage ringing of various frequencies on both the lower MOSFETs and lower antiparallel diodes. The ringing frequencies are determined by the network's impedance [26]. Therefore, the impedance of V_{ds_MOS} over i_{channel} is studied.

1) Parameter Extraction for Key Parameters: To implement the frequency-domain analysis, accurate values of the circuit parameters are needed. Previously, the power loop inductance of the N-cell L_{ds_N} is extracted to be 81.15 nH based on the N-cell switching test. Similarly, the lumped power loop inductance value in the P-cell can be obtained from the P-cell switching, and a value of 81.60 nH is extracted experimentally. The

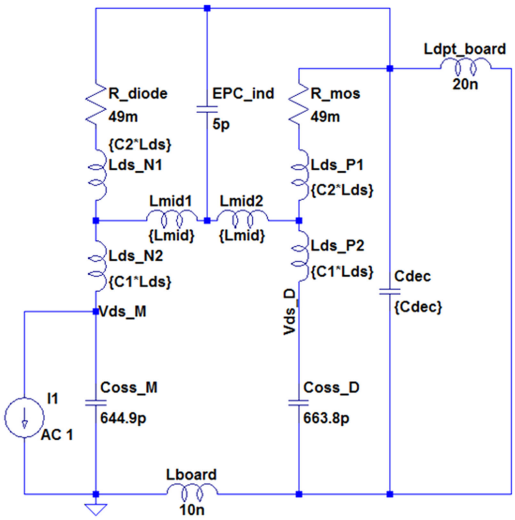

Fig. 10. LTspice simulation schematics.

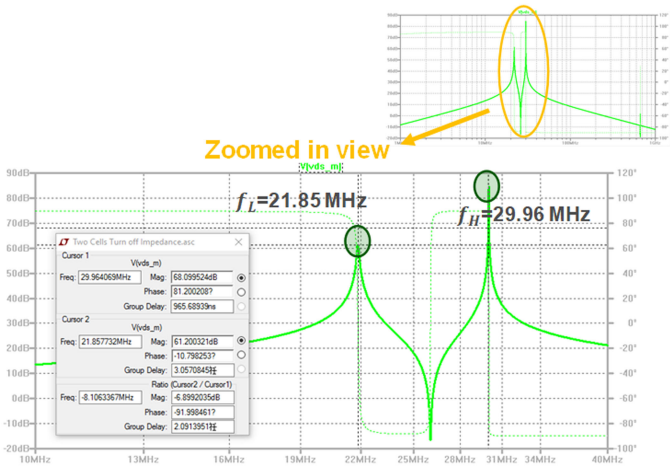

Fig. 11. Impedance of V_{ds_MOS} over i_{channel}.

equivalent parallel capacitance value of the load inductor is measured to be 3.5 pF from the impedance analyzer. The middle-point inductance is formed by the DBC-level copper trace, and the value of the middle-point parasitic inductance is extracted in Ansys Q3D based on its geometry [27]. At high frequency, the extracted value of L_{middle} is 5.47 nH. The parasitic inductance in between the on-board decoupling capacitor and dc-link capacitor is simulated to be 20.15 nH.

With all the values of circuit parameters at hand, the impedance network is built in LTspice as shown in Fig. 10. To mimic the channel di/dt, an ac current excitation is in parallel with the junction capacitor of the lower MOSFET. The impedances of $Z_{\mathrm{Mos}} = V_{ds\_\mathrm{MOS}}/i_{\mathrm{channel}}$ is obtained, as shown in Fig. 11.

As can be seen, two resonant frequencies are observed. One is at $f_L = 21.85\,\mathrm{MHz}$; the other one is $f_H = 29.96\,\mathrm{MHz}$. The amplitude of each signal is assumed to be A_L and A_H, and the

resulting signals are indicated in (2).

$$\begin{aligned} V_{ds\_\mathrm{ringing}} &= V_{\mathrm{dc}} + A_L \cdot \cos(2\pi f_L t) + A_H \cdot \cos(2\pi f_H t) \\ &= V_{\mathrm{dc}} + A_L \cdot \cos(2\pi f_L t) + A_L \cdot \cos(2\pi f_H t) \\ &\quad + (A_H - A_L) \cdot \cos(2\pi f_H t) \\ &= V_{\mathrm{dc}} + 2A_L \cdot \cos\left[2\pi \frac{f_L + f_H}{2} t\right] \\ &\quad \cdot \cos\left[2\pi \frac{f_H - f_L}{2}\right] + (A_H - A_L) \cdot \cos(2\pi f_H t). \end{aligned} \tag{2}$$

The characteristics of the active device, gate drive capability, board layout, and temperature in the turn-off periods together determine A_L and A_H, and the exact values of A_L and A_H cannot be readily derived from analytical equations. Instead, numerical solution or simulation is required with an accurate model of the devices and circuit parasitic parameters [28]. However, from the experimental ringing waveforms shown in Fig. 8, the voltage across the device has two different frequencies of zero-crossing with an offset of dc-link voltage. Therefore, it can be inferred that the values of A_L and A_H are close such that the third term in (2) can be ignored, and it can be simplified to (3).

$$\begin{aligned} V_{ds\_\mathrm{ringing}} &= V_{\mathrm{dc}} + 2A_L \cdot \cos\left[2\pi \frac{f_L + f_H}{2} t\right] \\ &\quad \cdot \cos\left[2\pi \frac{f_H - f_L}{2}\right]. \end{aligned} \tag{3}$$

The ringing term in (3) can cause multifrequency ringing in the time domain, with 2 zero-crossing frequencies of f_{Z_D} and f_{Z_C} expressed as

$$\frac{f_{Z\_D}}{2} = f_D = \frac{f_H - f_L}{2} = \frac{29.96 - 21.85}{2} = 4.06\ \mathrm{MHz} \tag{4}$$

$$\frac{f_{Z\_C}}{2} = f_C = \frac{f_H + f_L}{2} = \frac{29.96 + 21.85}{2} = 25.91\ \mathrm{MHz} \tag{5}$$

where f_C and f_D are the resulting multiple ringing frequencies in the time domain, and the simulated values are approximate to the observed two ringing frequencies ($f_1 \approx 25\,\mathrm{MHz}$ and $f_2 \approx 2\,\mathrm{MHz}$) in experiment. However, the simulated values f_C and f_D are larger than the experimental values f_1 and f_2. The difference can be explained by the discrepancy of the distribution of power loop inductance in simulation and experiment. To be specific, define C_1 (C_2) to be the percentage of inductance from the middle point to the negative bus (positive bus) over the total power loop inductance. Therefore, we have:

$$C_1 + C_2 = 1. \tag{6}$$

In the simulation, an even distribution of the power loop inductance is assumed from the middle point; therefore, C_1 and C_2 are both assigned to 0.5. However, this even distribution does not necessarily represent the real experiment setup. Take the N-cell module layout for example, the distance from the middle point to the negative bus is longer the than the distance from the middle point to the positive bus as shown in Fig. 4(b).

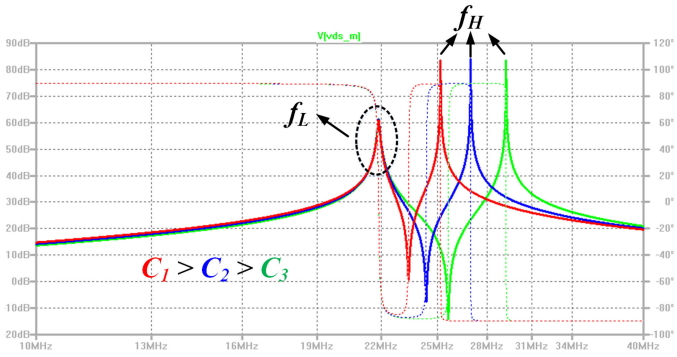

Fig. 12. Impedance of Z_{Mos} at different values of C_1.

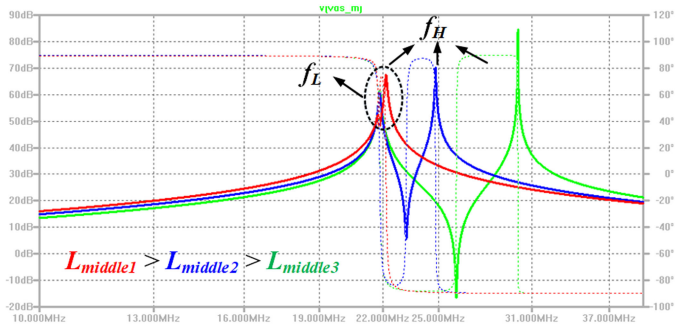

Fig. 13. Impedance of Z_{Mos} at different L_{middle}.

Therefore, C_1 is larger than C_2. Fig. 12 illustrates the simulation result at different values of C_1. As C_1 increases, f_H decreases and f_L is unchanged. Correspondingly, both f_D and f_c are smaller according to (4) and (5). This explains the fact that the observed two frequencies in experiment f_1, f_2 are smaller than the simulated f_C and f_D, respectively.

2) Analysis of Middle-Point Inductance's Effect in Frequency Domain: From the impedance network analysis, it is concluded that the middle-point inductance L_{middle} is the cause of the multiple-frequency ringing in the drain-to-source voltage. To evaluate L_{middle}'s effect on the switching transients, Fig. 13 shows another simulation of Z_{Mos} at various values of L_{middle}. As L_{middle} increases, f_H decreases but f_L is almost unchanged. According to (4), f_D will always decrease. Equivalently, the lower ringing frequency in experiment f_2 is expected to decrease as well. When L_{middle} is above a certain value, f_H and f_L overlap and a single frequency is obtained as indicated by the red line in Fig. 13. This can be interpreted from the circuit analysis as well. Considering the large L_{middle} case, the current in L_{middle} remains constant during the switching transients. Accordingly, L_{middle} can be treated as an open circuit at high frequency. Then a single ringing frequency is obtained, which is determined by the power loop inductance and the junction capacitance of the MOSFETs in the N-cells.

From the frequency-domain analysis and simulation result, L_{middle} can potential affect the device's switching transient. Therefore, experimental evaluation is needed to discover its effect in the time domain.

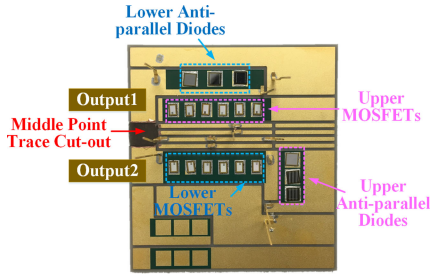

Fig. 14. Dedicated DBC substrate for evaluating L_{middle}'s effect.

Fig. 15. Fabricated module with a gate drive board.

III. Experimental Evaluation of Middle-Point Inductance's Effect

In this section, the effect of L_{middle} on switching transients is studied experimentally in a DPT. To conduct the study, a dedicated module is built with the capability of varying the values of middle-point inductance. Fig. 14 demonstrates the dedicated DBC substrate. The copper trace connecting the two middle points are cut out. Afterward, two output pins are soldered to the middle point of each cell. The middle-point inductance is connected externally for easy variation of L_{middle}'s value. Specifically, the middle-point inductance is realized by the parasitic inductance of the connection wires, and its value can be varied simply by changing the length of the wires. The remaining layout and components are the same as discussed previously. The final assembled module is shown in Fig. 15 with the gate drive board installed.

In the following sections, the switching performance is evaluated at different values middle-point inductance (10 nH, 50 nH, 160 nH, 650 nH, and 1.6 μH). The value of the middle-point inductance is measured with the Agilent 4294A impedance analyzer, and the high frequency value is used. The gate resistor values are varied at 5, 7.5, and 10 Ω. Meanwhile, both the large power loop inductance case ($L_{ds} \approx 80\,\mathrm{nH}$) and small loop inductance ($L_{ds} \approx 7\,\mathrm{nH}$) case are studied. The large power loop inductance circumstance represents the traditional package or the converter design with multiple TO-packaged devices in parallel. It is realized by connecting the power module to the DPT using twisted wires without placing decoupling capacitors. In the small loop inductance case, decoupling capacitors are directly embedded inside the power module. The small L_{ds} condition represents the state-of-the-art power module designs with low power loop inductance.

As mentioned previously, the low-side MOSFETs and antiparallel diodes have excessive voltage stress during the low-side MOSFETs' turn-off. Similarly, voltage spikes are also induced on the low-side devices during the upper MOSFETs' turn-on process. For both low-side MOSFET turn-off and high-side MOSFET turn-on transients, the voltage spikes of the lower devices are recorded at different values of L_{middle}, R_g and L_{ds}. Meanwhile, the switching loss of lower MOSFETs is compared in the large power loop inductance case at different values of L_{middle} and R_g. The switching loss in the small L_{ds} case is not calculated because the drain current is not accessible from the shunt resistor with the decoupling capacitors embedded inside the package. Table I summarizes the various specifications to be evaluated under different cases.

A. Evaluation of Middle-Point Inductance's Effect at Large L_{ds}

The case with a large value of power loop inductance is studied first. Fig. 16(a) to (c) exhibits the experimental turn-off waveforms of low-side MOSFET's gate voltage, Kelvin V_{ds}, drain current, and low-side antiparallel diode's voltage at different values of L_{middle} with $R_{g,\mathrm{off}} = 7.5\ \Omega$.

As expected from the frequency-domain analysis, the lower ringing frequency of f_2 does change with the value of L_{middle}: f_2 drops from 1.79 to 0.72 MHz as L_{middle} increases from 50 to 650 nH. At $L_{\mathrm{middle}} = 1.6\,\mu\mathrm{H}$, a single resonant frequency of 20.45 MHz is observed, which indicates a decouple of P-cell with the N-cell. Both the switching loss and voltage spikes are changed at different values of L_{middle}.

1) Middle-Point Inductance's Effect on Turn-on Switching Loss: The turn-on switching loss variation of the lower MOSFET is shown in Fig. 17 at different load current, gate resistor and L_{middle}. Regardless of the external gate resistor's value, the turn-on switching loss always decreases as the value of L_{middle} goes up over a wide range of load current.

Several factors contribute to the reduced turn-on loss at elevated values of L_{middle}. Fig. 18 illustrates the turn-on waveforms of the lower MOSFET and lower antiparallel diode at $L_{\mathrm{middle}} = 50\mathrm{nH}$ and $L_{\mathrm{middle}} = 1.6\mu\mathrm{H}$ with all other conditions the same. It can be observed that the drain-to-source voltage falls more quickly in the case with a larger value of middle-point inductance. This can be explained by the fact that the effective output capacitance to be charged or discharged is smaller because of the decoupling effect at larger values of L_{middle}. Correspondingly, with the same gate drive circuit, V_{ds} drops more quickly thus reducing the overlap switching loss. Another reason is that the peak drain current of lower MOSFET is smaller with a higher value of L_{middle}. If L_{middle} is small, the measured drain current is composed of the load current (in red), the charge current (in blue) of the upper antiparallel diode, the upper MOSFET plus equivalent parallel capacitance (EPC) of the load inductor, and the discharge current (in green) of the lower antiparallel diode, as indicated in Fig. 19(a). All this charge or discharge currents will cause excessive overlap losses since the voltage of the active switching device has not reached zero. Note that the discharge current of lower MOSFET cannot be measured from the shunt resistor.

TABLE I
SPECIFICATIONS TO BE EVALUATED AT DIFFERENT CONDITIONS

Power Loop Inductance L_{ds}	Switching Conditions	
	Lower MOSFET Turn-off	Upper MOSFET Turn-on
Case A: Large	• Switching loss of low-side MOSFETs • Voltage spikes of low-side devices	• Voltage spikes of low-side devices
Case B: Small	• Voltage spikes of low-side devices	• Voltage spikes of low-side devices

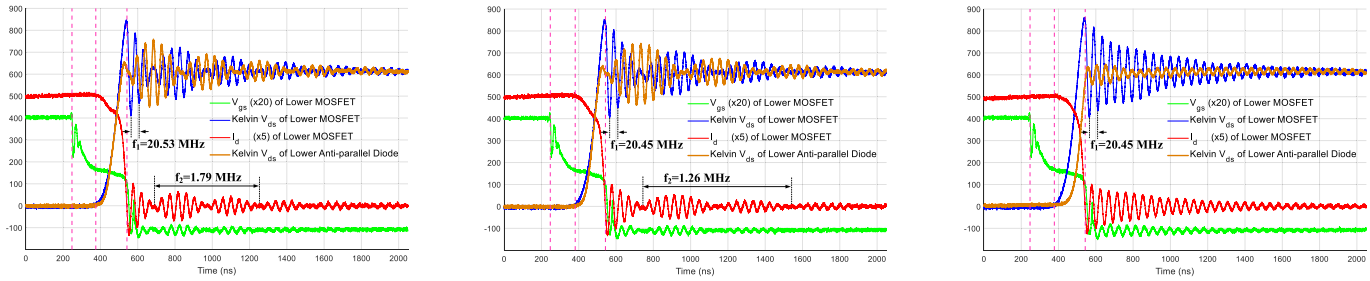

Fig. 16. Turn-off switching waveforms of lower devices at different values of L_{middle} with $R_{g,\text{off}} = 7.5\ \Omega$. (a) $L_{\text{middle}} = 50\,\text{nH}$. (b) $L_{\text{middle}} = 160\,\text{nH}$. (c) $L_{\text{middle}} = 1.6\,\mu\text{H}$.

On the contrary, when the value of L_{middle} is large, the drain-to-source voltage of the low-side antiparallel diode is not falling together with V_{ds} of the lower MOSFET. Consequently, the discharge current of lower antiparallel diode and the charge current of upper MOSFET will not introduce extra overlap losses on the lower MOSFET, as indicated in Fig. 19(b). Compared with the case of a small value of L_{middle}, the overlap loss is smaller at a large value of L_{middle}. In other words, large L_{middle} effectively decouples the P-cell with the N-cell and prevents the overlap losses due to the other phase leg.

This decoupled effect at large L_{middle} can also be observed from the fact that turn-on switching loss at 0 A is decreasing as L_{middle} goes up. The 0 A turn-on loss includes three parts: the C_{oss} charge of the upper antiparallel diode, the C_{oss} charge of upper MOSFETs, EPC charge of the load inductor, and the C_{oss} discharge of the lower antiparallel diode. The C_{oss} discharge of the lower MOSFET is not measurable. If L_{middle} is large, only the charge of the upper antiparallel diode's C_{oss} will be measured because of its decoupling effect. Consequently, the 0 A turn-on loss converges to a lower value, which is verified experimentally as indicated in Fig. 17.

2) Middle-Point Inductance's Effect on Turn-off Switching Loss: The turn-off loss result at different values of L_{middle} is summarized, as shown in Fig. 20. As can be seen, the turn-off loss is always increasing as L_{middle} goes up. Two reasons contribute to the increased turn-off loss. First, because of the reduced equivalent output capacitance at large value of L_{middle}, the drain-to-source voltage is increasing more quickly. This is verified through the comparison of the experimental turn-off waveforms at $L_{\text{middle}} = 50\,\text{nH}$ and $L_{\text{middle}} = 1.6\,\mu\text{H}$ shown in Fig. 21. Thus, more overlap loss is obtained at a given drain current.

Second, at higher L_{middle}, more current remains to flow through the lower MOSFET in the dv/dt period. Specifically,

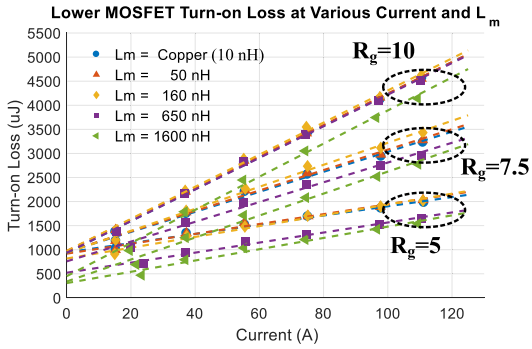

Fig. 17. Turn-on loss variation with L_{middle} at different load currents and R_g.

the switch node voltages of both N-cell and P-cell experience a rising edge dv/dt. With low L_{middle}, the measured drain current of the lower MOSFET can be expressed as

$$I_{d,L\_\text{MOS}} = I_L - (I_{C_{j\_UD}} + I_{C_{j\_UM}} + I_{C_{\text{EPC}}}) - I_{C_{j\_LD}} \quad (7)$$

where $I_{C_{j\_UD}}$, $I_{C_{j\_UM}}$, and $I_{C_{\text{EPC}}}$ are the discharge currents (in green) of the upper antiparallel diode, the upper MOSFET, and the load inductor's EPC, respectively. $I_{C_{j\_LD}}$ represents the charge current (in blue) of the lower antiparallel diode. Note that the charge current of the lower MOSFET cannot be measured with the external shunt resistor. All the charge and discharge currents are shown in Fig. 22(a) for the small L_{middle} case.

On the contrary, the increase of the switch node voltage of P-cell is small because of the decoupling effect at a large value of L_{middle}. Therefore, for the measured drain current I_{d,L_MOS}, only the discharge current of upper antiparallel diode is deducted from the load current according to (7). Correspondingly, more current remains in the lower MOSFET at a higher value of L_{middle}, as indicated in Fig. 22(b). Combining the higher V_{ds} and the

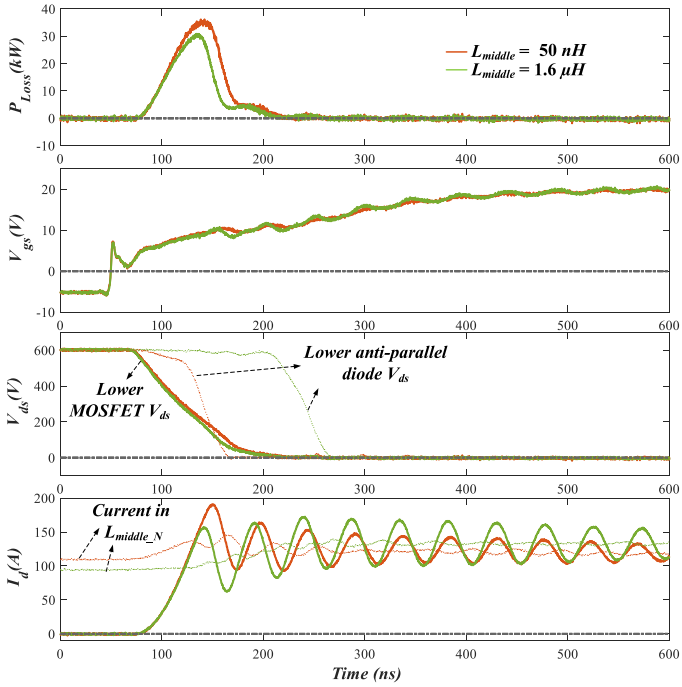

Fig. 18. Turn-on waveforms at $R_{g,\mathrm{on}} = 5\ \Omega, I_{\mathrm{load}} = 110\,\mathrm{A}$, with $L_{\mathrm{middle}} = 50\,\mathrm{nH}$ and $L_{\mathrm{middle}} = 1.6\,\mu\mathrm{H}$, respectively.

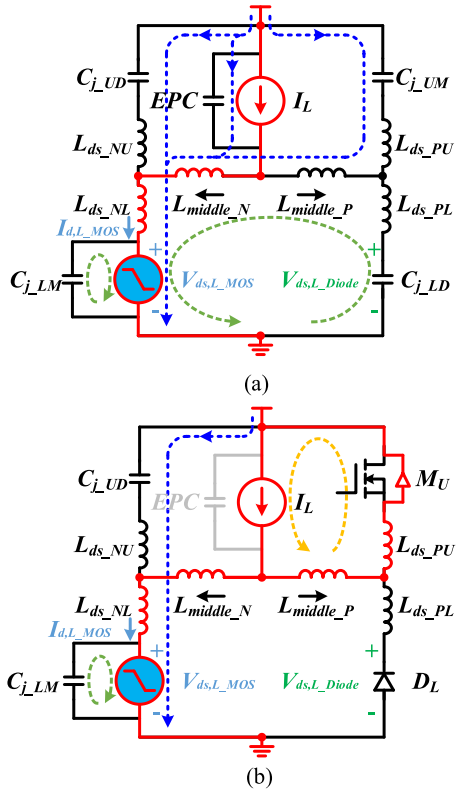

Fig. 19. Composition of measured drain current during lower MOSFET turn-on dv/dt period with different L_{middle}. (a) Small L_{middle}. (b) Large L_{middle}.

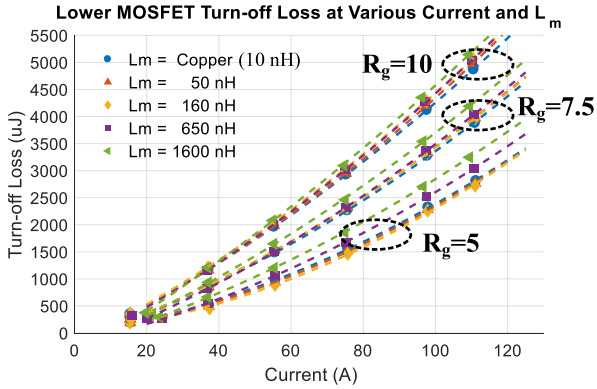

Fig. 20. Turn-off loss variation with L_{middle} at different load currents and R_g.

drain current, the overlap loss is larger as the value of L_{middle} increases.

3) Middle-Point Inductance's Effect on Voltage Spikes during Lower MOSFET's Turn-off: At different values of gate resistors and L_{middle}, the peak voltage values of lower MOSFET and lower antiparallel diode during the turn-off of lower MOSFETs are summarized in Figs. 23 and 24 with the values of L_{middle} varying.

As can be observed, the lower MOSFET and lower antiparallel diode have different overvoltage stress because of the middle-point inductance. Meanwhile, as L_{middle} increases, the maximum voltage of the MOSFET keeps increasing while the maximum voltage of the antiparallel diode drops significantly. At $R_{g,\mathrm{ext}} = 10\Omega$ and $I_{\mathrm{load}} = 110\,\mathrm{A}$, the lower MOSFET's voltage overshoot increases by 17% when L_{middle} is increased from 10 NH to 1.6 μH. At the same condition, 80% reduction of voltage overshoot is observed for the lower antiparallel diode.

The increased voltage overshoot on the low-side MOSFETs can be explained by the fact large L_{middle} effectively decouples the P-cell thus reducing the equivalent junction capacitance of the phase leg during the lower MOSFET's turn-off. Accordingly, at the same gate drive circuit and circuit layout, the overshoot voltage rises as the value of equivalent junction capacitance decreases. Similarly, the middle-point inductance also contributes to the reduced voltage spike of lower antiparallel diode at large L_{middle}. Explicitly, with large L_{middle}, the switch node voltage of the P-cell is still zero when the N-cell's switch node voltage first reaches the dc-link voltage. Therefore, the middle-point inductance plus the parasitic inductance in the P-cell $(L_{\mathrm{middle}} + L_{ds\_PL})$ starts to resonate with the junction capacitor of the P-cell's switch node (C_{j_P}) under the dc-link voltage's bias. This resonant period ends after a quarter cycle when the switch node voltage of the P-cell reaches the dc-link voltage, and is clamped by the body diode of the upper MOSFETs. Selecting the voltage base to be the dc-link voltage, the end value of the current in the P-cell's parasitic inductance is derived in (8).

The ringing period starts afterward, where the parasitic inductance in the P-cell is resonating with the junction capacitance of the lower antiparallel diodes. According to (8), the current in the parasitic inductance is smaller with a higher value of L_{middle}. Correspondingly, given the same junction capacitance and parasitic inductance, the voltage spike on the lower antiparallel diode drops as L_{middle} increases.

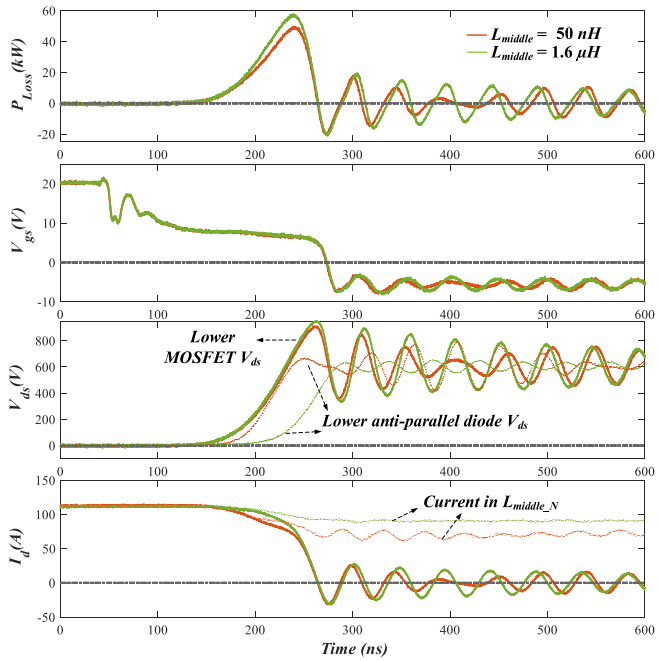

Fig. 21. Turn-off waveforms at $R_{g,\mathrm{on}} = 5\ \Omega, I_{\mathrm{load}} = 110\,\mathrm{A}$, with $L_{\mathrm{middle}} = 50\,\mathrm{nH}$ and $L_{\mathrm{middle}} = 1.6\,\mu\mathrm{H}$, respectively.

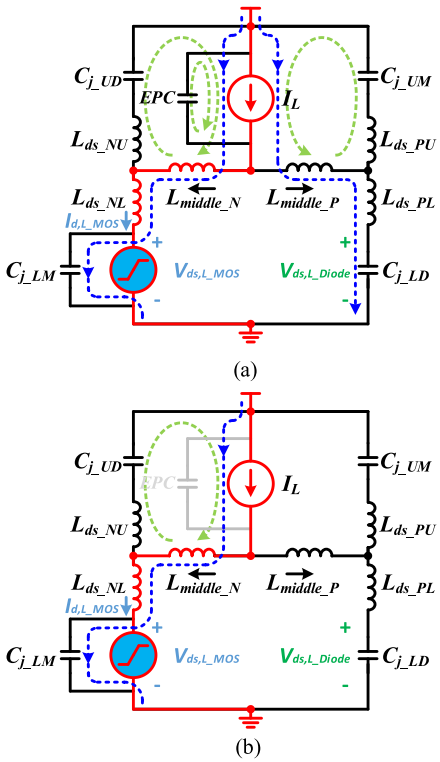

Fig. 22. Composition of measured drain current during lower MOSFET turn-off dv/dt period with different L_{middle}. (a) Small L_{middle}. (b) Large L_{middle}.

4) Middle-Point Inductance's Effect on Voltage Spikes During Upper MOSFET's Turn-on: Another group of tests is implemented where both the maximum voltage of lower MOSFETs and lower antiparallel diodes are measured during the turn-on time of the upper MOSFET. The results are exhibited in Figs. 25 and 26 at different values of gate resistors.

Like the case of lower MOSFET's turn-off, the voltage spikes of the lower MOSFET and the antiparallel diode are different. However, compared to the lower MOSFET's turn-off case, an opposite trend of voltage spike variation is observed. To be specific, as L_{middle} increases, the lower MOSFET's voltage decreases while the antiparallel diode's voltage builds up. Considering the turn-on condition at $R_{g,\mathrm{ext}} = 10\ \Omega$ and $I_{\mathrm{load}} = 110$ A, the induced voltage overshoot on lower MOSFET is reduced by 56% as L_{middle} changes from 10 nH to 1.6 μH. On the other hand, the lower antiparallel diode's overshoot is increased by 40%.

To explain this phenomenon, the circuit operation before the turn-on of upper MOSFETs needs to be analyzed first. Fig. 27 demonstrates the simplified circuit diagram of the DPT for upper MOSFETs considering some of the key parasitic parameters.

In the first pulse, the upper MOSFETs are on and the load current reaches the desired value. Then the upper MOSFETs are turned off, and the switch node of the P-cell experiences a falling edge dv/dt. This negative dv/dt forces the switch node voltage of the N-cell to drop, and a resonance between the junction capacitance of the N-cell's switch node and the middle-point inductance is initiated. This resonance ends after a quarter cycle when $V_{ds,\ L\_\mathrm{MOS}}$ reaches a negative value and is clamped by the body diode of low-side MOSFETs. The developed current in $L_{\mathrm{middle\_}N}$ is positive, as defined in Fig. 27, and the load current conducts through both the body diode of the lower MOSFETs and the antiparallel diode, as indicated in Fig. 28. Since the voltage drop on the body diode is larger than that of the antiparalleled Schottky diode, the current in $L_{\mathrm{middle\_}N}$ gradually decreases toward zero while the current in $L_{\mathrm{middle\_}P}$ rises to the load current. Ignoring the power loop parasitic inductances L_{ds_NL} and L_{ds_PL}, the rate of change of the current is determined by

$$\frac{di}{dt} = \frac{V_{\mathrm{on,bdiode}} - V_{\mathrm{on,}L\_\mathrm{Diode}}}{L_{\mathrm{middle\_}N} + L_{\mathrm{middle\_}P}}. \tag{9}$$

With a large value of middle-point inductance, the current commutation is slow. Consequently, before the upper MOSFETs are switched on in the second pulse, the current in $L_{\mathrm{middle\_}N}$ can still be positive and the current in $L_{\mathrm{middle\_}P}$ is less than the load current. Fig. 29 shows the experimental verification of this analysis. The upper MOSFETs are turned on at $L_{\mathrm{middle}} = 50$ nH and $L_{\mathrm{middle}} = 1.6\,\mu$H, respectively. As can be seen from the last row in Fig. 29, the measured current of $L_{\mathrm{middle\_}P}$ is indeed lower than the load current when the middle-point inductance is large.

The upper MOSFETs are turned on in the second pulse, and the current in the lower antiparallel diodes starts to commutate to

$$I_{L_{ds\_PL}} = 1 \cdot I_{\mathrm{base}} = \frac{V_{\mathrm{base}}}{R_0} = V_{\mathrm{dc}} \cdot \sqrt{\frac{C_{j\_P}}{L_{\mathrm{middle}} + L_{ds\_PL}}} \approx V_{\mathrm{dc}} \cdot \sqrt{\frac{C_{j\_P}}{L_{\mathrm{middle}}}} \tag{8}$$

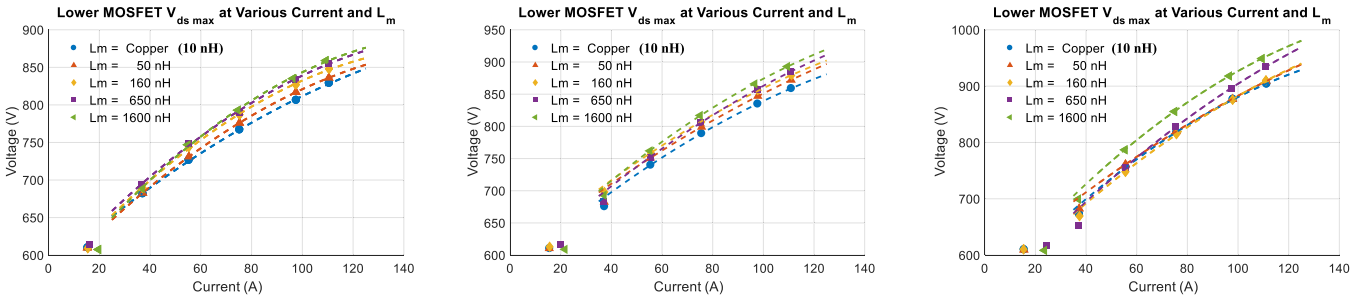

Fig. 23. Maximum voltage of low-side MOSFETs at different L_{middle} during lower MOSFET turn-off. (a) $R_{g,\mathrm{off}} = 10\ \Omega$. (b) $R_{g,\mathrm{off}} = 7.5\ \Omega$. (c) $R_{g,\mathrm{off}} = 5\ \Omega$.

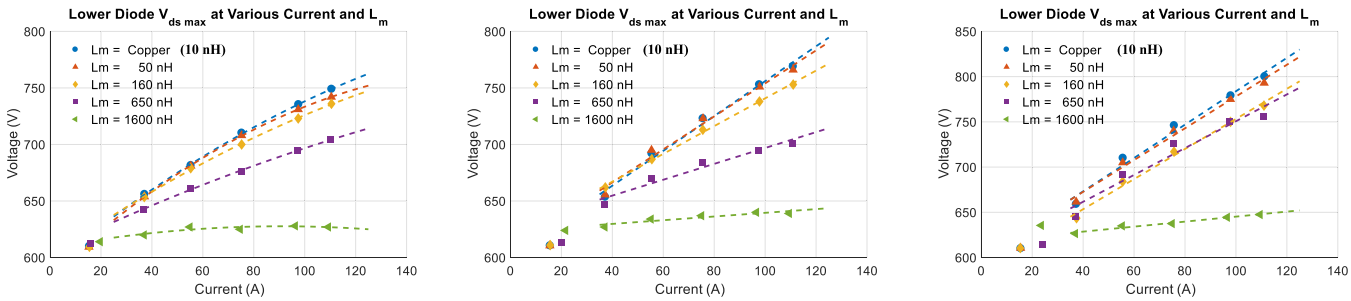

Fig. 24. Maximum voltage of low-side antiparallel diodes at different L_{middle} during lower MOSFET turn-off. (a) $R_{g,\mathrm{off}} = 10\ \Omega$. (b) $R_{g,\mathrm{off}} = 7.5\ \Omega$. (c) $R_{g,\mathrm{off}} = 5\ \Omega$.

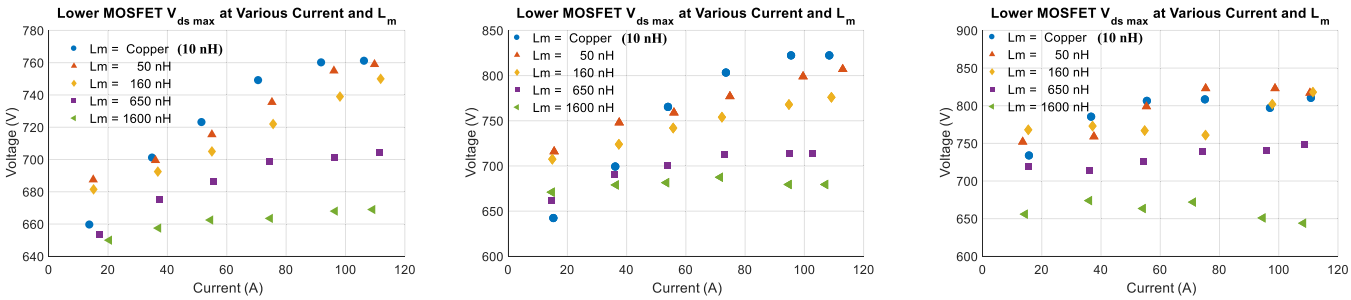

Fig. 25. Maximum voltage of low-side MOSFETs at different L_{middle} during upper MOSFET turn-on. (a) $R_{g,\mathrm{on}} = 10\ \Omega$. (b) $R_{g,\mathrm{on}} = 7.5\ \Omega$. (c) $R_{g,\mathrm{on}} = 5\ \Omega$.

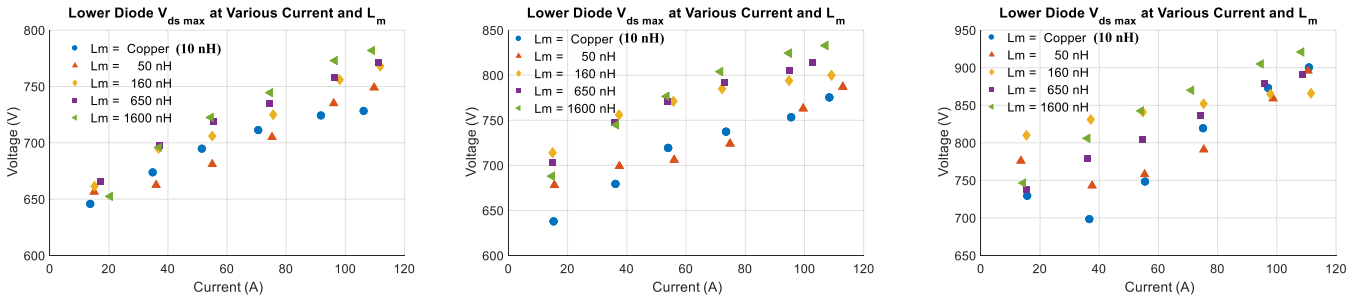

Fig. 26. Maximum voltage of low-side antiparallel diodes at different L_{middle} during upper MOSFET turn-on. (a) $R_{g,\mathrm{on}} = 10\ \Omega$. (b) $R_{g,\mathrm{on}} = 7.5\ \Omega$. (c) $R_{g,\mathrm{on}} = 5\ \Omega$.

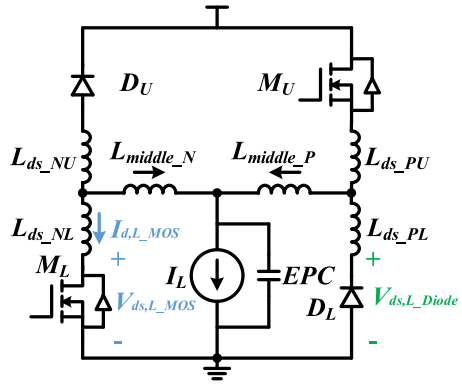

Fig. 27. Simplified circuit diagram for upper MOSFET DPT.

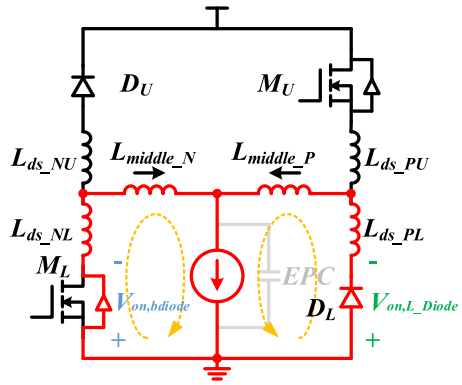

Fig. 28. Circuit after upper MOSFETs turn-off.

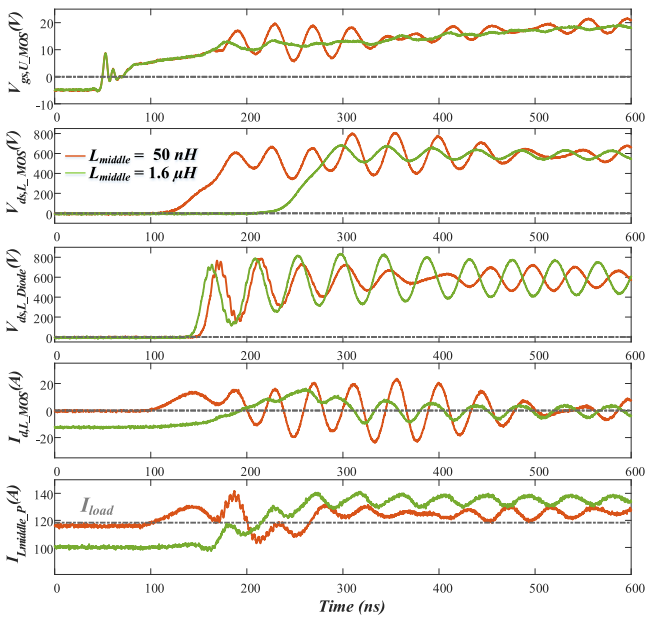

Fig. 29. Experiment waveforms during upper MOSFET turn-on at $R_{g,\mathrm{on}} = 7.5\,\Omega, I_{\mathrm{load}} = 110\,\mathrm{A}$, with $L_{\mathrm{middle}} = 50\,\mathrm{nH}, 1.6\,\mu\mathrm{H}$.

the upper MOSFETs. Afterward, the drain-to-source voltage of the upper MOSFETs collapses to its on-state voltage. Consequently, a rising edge is observed at the switch node voltage of P-cell, and it quickly reaches the dc-link voltage.

With a small value of middle-point inductance, the switch node voltage of the N-cell follows the P-cell's voltage instantaneously, and the junction capacitance of each device is charged or discharged, as shown in Fig. 30(a). The green and blue lines indicate the discharge and charge current, respectively. The load current path is shown in red. Once both switch node voltages reach the dc-link voltage, the ringing period starts where the power loop inductance resonates with the junction capacitance formed by the lower MOSFETs, lower antiparallel diodes, and the equivalent parallel capacitance of the load inductor. It can be seen that before it starts ringing, the current in the parasitic inductance L_{ds_PU} is the load current if the high frequency charge or discharge current is ignored.

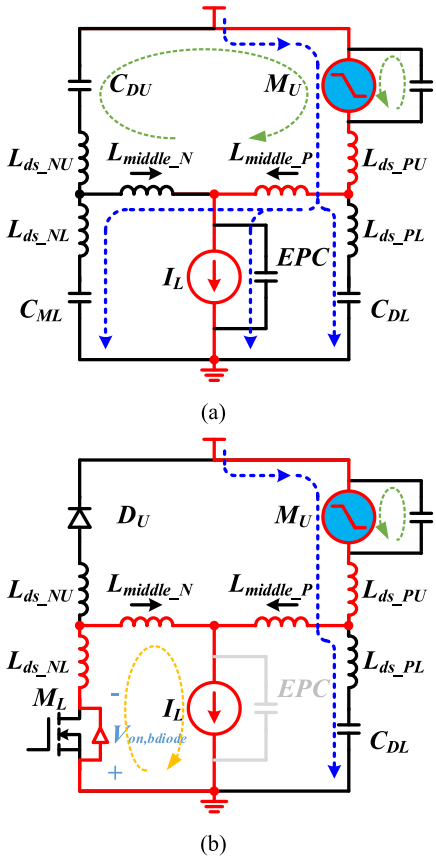

Fig. 30. Equivalent circuit diagram during upper MOSFET turn-on dv/dt period at different L_{middle}. (a) Small L_{middle}. (b) Large L_{middle}.

However, if a large middle-point inductance is considered, the current of $L_{\mathrm{middle\_}N}$ is still positive before the upper MOSFETs are turned on. Therefore, the switch node voltage of the N-cell is clamped by the body diode, as shown in Fig. 30(b). Since the P-cell's switch node voltage is the dc-link voltage, the current in $L_{\mathrm{middle\_}N}$ is forced to drop. When the current in $L_{\mathrm{middle\_}N}$ reaches zero, the lower MOSFET can be modeled as a junction capacitor, and a new period initiates where the middle-point inductance plus the parasitic inductance in N-cell $(L_{\mathrm{middle}} + L_{ds\_NL})$ starts to resonate with the junction capacitance of the N-cell's switch node (C_{j_N}), as illustrated in Fig. 31. The initial voltage on the junction capacitance is zero, and the dc-bias is the dc-link voltage at the P-cell's switch node. This resonant period lasts for a quarter cycle when the switch node voltage of the N-cell reaches the dc-link voltage and is clamped by the upper diodes. Selecting the voltage base to be the dc-link

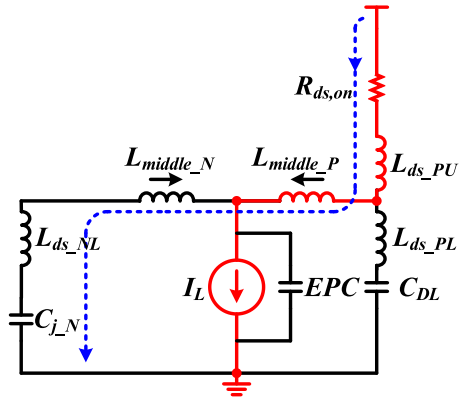

Fig. 31. Equivalent circuit at resonant period of upper MOSFET turn-on with large L_{middle}.

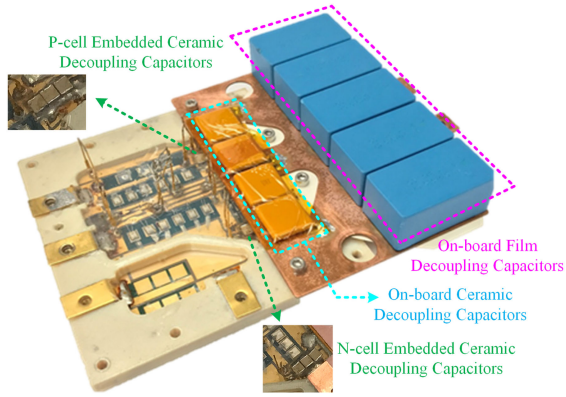

Fig. 32. Fabricated low L_{ds} power module with embedded ceramic decoupling capacitors.

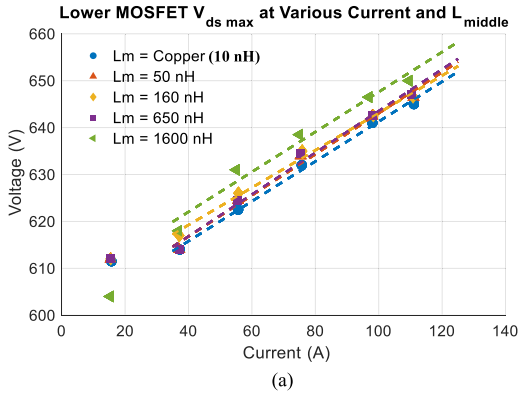

Fig. 33. Maximum voltage of lower devices during lower MOSFET turn-off at different L_{middle} with $R_{g,\mathrm{off}} = 5\,\Omega$ and small L_{ds}. (a) Lower MOSFETs. (b) Lower antiparallel diodes.

voltage, the end value of the current in the N-cell's parasitic inductance derived in (10), which is indicated at the bottom of this page.

Then the ringing period starts. For the N-cell side, the parasitic inductance in the N-cell is ringing with the junction capacitance of the lower MOSFETs. Similar to the previous analysis, the initial current in the N-cell's parasitic inductance is smaller at a higher value of L_{middle} according to (10). Correspondingly, given the same values of junction capacitance and parasitic inductance, the voltage overshoot on the lower MOSFETs is smaller at larger L_{middle}. This explains the experimental variation of lower MOSFETs' peak voltage over different values of middle-point inductance shown in Fig. 25.

For the P-cell with large L_{middle}, the current in $L_{\mathrm{middle\_}P}$ reaches a value higher than the load current after this quarter-cycle resonant transition, as verified experimentally in Fig. 29. Ignoring the high-frequency ringing current in the junction capacitor of the lower antiparallel diodes, the current in L_{ds_PU} is the same as that in $L_{\mathrm{middle\_}P}$. Thus, the current in the P-cell's parasitic inductance is increased with a large value of middle-point inductance. Compared to the small L_{middle} case, the junction capacitance is also smaller because of the decouple effect. Combining the higher current in the power loop inductance and lower value of junction capacitance, a larger voltage overshoot is induced on the lower antiparallel diodes. This explains the observed increase of lower antiparallel diodes' voltage at elevated values of L_{middle} shown in Fig. 26.

B. Evaluation of Middle-Point Inductance's Effect at Small L_{ds}

The low inductance package is realized by embedding ceramic decoupling capacitors inside the power module, as shown in Fig. 32.

For the small power loop inductance case, the peak voltage variations of the lower MOSFET and lower antiparallel diode are investigated at different values of middle-point inductance. Similar to the large L_{ds} case, both the turn-off of lower MOSFET and turn-on of upper MOSFET are studied at a dc-link voltage of 600 V.

1) Middle-Point Inductance's Effect on Voltage Spikes During Lower MOSFET's Turn-off: Fig. 33 illustrates the peak voltage of the lower MOSFET and lower antiparallel diode during

$$I_{L_{ds\_NL}} = 1 \cdot I_{\mathrm{base}} = \frac{V_{base}}{R_0} = V_{\mathrm{dc}} \cdot \sqrt{\frac{C_{j\_N}}{L_{\mathrm{middle}} + L_{ds\_NL}}} \approx V_{\mathrm{dc}} \cdot \sqrt{\frac{C_{j\_N}}{L_{\mathrm{middle}}}} \tag{10}$$

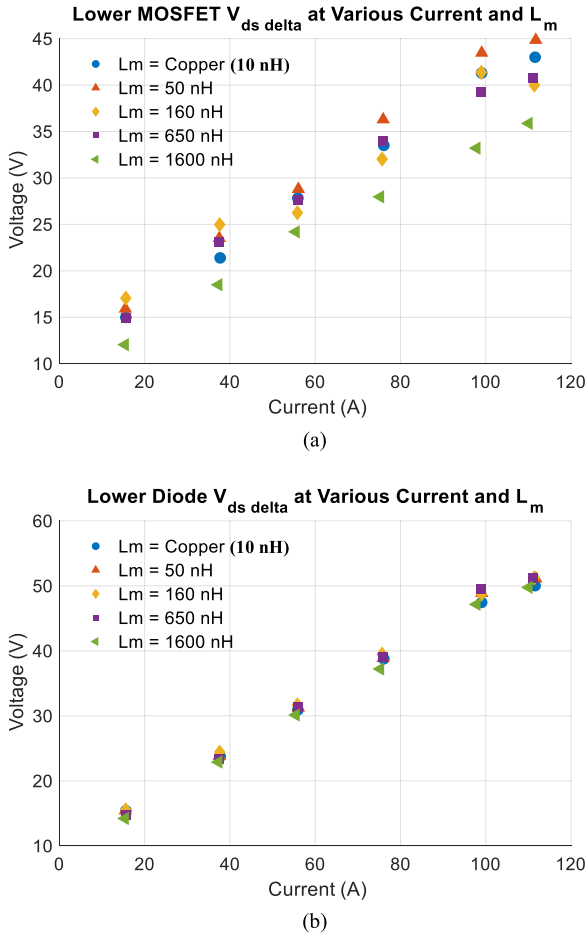

Fig. 34. Voltage overshoot of lower devices during upper MOSFET turn-on at different L_{middle} with $R_{g,\mathrm{on}} = 5\,\Omega$ and small L_{ds}. (a) Lower MOSFETs. (b) Lower antiparallel diodes.

lower MOSFET's turn-off at different values of L_{middle} and load current with $R_g = 5\ \Omega$.

The voltage spike variation trend shows a similar result as the case of large L_{ds}: the MOSFET's peak voltage increases at higher L_{middle} while the antiparallel diode's voltage overshoot drops. However, compared to the large L_{ds} case, the absolute value of the voltage spike is significantly reduced.

2) Middle-Point Inductance's Effect on Voltage Spikes During Upper MOSFET's Turn-on: More experiments are implemented at small L_{ds} considering the case of upper MOSFET turn-on. The voltage overshoot variations of the lower MOSFET at different values of gate resistors are demonstrated in Fig. 34(a). As can be seen, the lower MOSFET's voltage overshoot drops slightly as L_{middle} increases. This coincides with the variation trend at large L_{ds}. However, the voltage overshoots are less than 60 V at all conditions over the tested load current range with a dc-link voltage of 600 V.

At different L_{middle}, almost no voltage overshoot variation in the lower antiparallel diode is observed with small L_{ds}, as indicated in Fig. 34(b). In fact, when L_{ds} is low, the initial energy stored in the stray inductance is also small. Though the current value changes because of the variation of middle-point inductance, this current change cannot cause significant variations in the stray inductance's energy. As a result, the voltage spike variation is small in experiment. As can be seen, at small values of power loop inductance, the effect of middle-point inductance is attenuated in terms of the voltage spike variation.

IV. Conclusion and Future Work

In this paper, the phenomenon of multiple-frequency ringing in a multiple-chip split-scaled SiC power module is explained by frequency-domain analysis. It is found that a new parasitic parameter, middle-point inductance L_{middle}, can affect the switching transients actively. To evaluate the middle-point inductance's effect, a dedicated DPT setup is designed, and the power module is built with the capability of varying L_{middle}. Both the lower MOSFET and upper MOSFET switching tests are carried out extensively at different values of middle-point inductance, gate resistor, and load condition.

The key findings from the experiment are summarized as follows:

1) In terms of the active switch's switching loss, the turn-on loss will decrease as L_{middle} increases. At the same time, the turn-off loss increases and an overall decrease of switching loss is observed from the experimental result. Detailed loss reduction or increase due to the variation of middle-point inductance is analyzed in this paper considering the switching transients.
2) In the large power loop inductance case, the experiment results indicate that L_{middle} will stress the active switch and antiparallel diode differently in terms of voltage spikes. Considering lower MOSFET's turn-off, the voltage overshoot on the lower MOSFETs increases by 17% in experiment as L_{middle} goes up. However, the overvoltage on the lower antiparallel diode decreases, and more than 80% reduction is observed. Considering the voltage spikes during upper MOSFET's turn-on, an opposite trend is obtained: the peak voltage on lower MOSFET will decrease as L_{middle} increases while the diode's maximum voltage builds up.

- Therefore, in designing a multichip package layout with large power loop inductance, the value of middle-point inductance is important and should be controlled to make sure all the devices are operating within the device's maximum voltage rating under different operating conditions. In the real layout design, a case-to-case study is required, and a detailed circuit simulation based on the real device behavior model and extracted physical layout parasitic parameter is recommended to evaluate different L_{middle}'s effect at various operating conditions.

3) In the small L_{ds} case, the voltage spike variation trend shows a similar result as the case of large L_{ds}. However, compared to the large L_{ds} case, the absolute value of the voltage spike and the voltage spike variation are reduced significantly. Therefore, the middle-point inductance's effects on active switch and antiparallel diode's voltage overshoot are less concerned with small value of L_{ds}. Consequently, in a multichip package layout

design with a small power loop inductance, the selection of the middle-point inductance's value is more flexible without worrying about the voltage stress variation due to L_{middle}. Considering the benefits of reduced switching loss at higher value of L_{middle}, it is possible to purposely increase the middle-point inductance value in a low-inductance package to improve the converter's efficiency. Nevertheless, considering the conduction loss in L_{middle} and increased diode conduction loss during the commutation period at higher L_{middle} discussed in [20] and [21], a comprehensive evaluation in the converter level at different operating conditions is needed to manifest the efficiency improvement with proper selection of L_{middle} in the package design stage. Further evaluation is to be presented in the future.

In terms of future work, the analytical relationship between the voltage spike and the middle-point inductance is to be explored. Based on these analytical expressions, the middle-point inductance's effect can be readily modeled in a package design tool without implementing the time-consuming circuit simulations.

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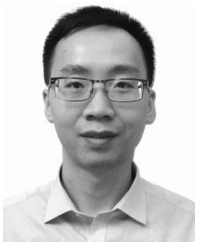

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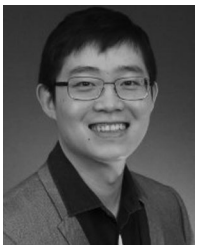

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