An SiC MOSFET and Si Diode Hybrid Three-Phase High-Power Three-Level Rectifier

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***Abstract*—The utilization of wide bandgap devices such as silicon carbide (SiC) diode and MOSFET can significantly increase the power density and the efficiency of rectifier circuits. However, SiC-based circuits always suffer from the high cost of their power stage. In this paper, a highly efficient low-cost hybrid three-phase three-level rectifier is proposed. Instead of using SiC diode and Si IGBT, it consists of SiC MOSFET and Si diode. It presents extremely low switching losses because the reverse recovery losses of all the Si diodes are eliminated. At the same time, the total device cost of this rectifier is much lower than the all-SiC-based rectifiers. Furthermore, half-bridge modules can be used to comprise the rectifier circuit, which makes it suitable for high-power applications. In this paper, the circuit operational analysis, simulation, and experimental results are given. A comparison is given to show the advantages of the proposed rectifier.**

***Index Terms*—Hybrid power stage, silicon carbide (SiC), three-level rectifier.**

I. Introduction

AFTER many years' development, the performance of conventional Si-based devices such as Si IGBT has approached their theoretical limitation. In order to further improve the performance of a power converter, wide bandgap semiconductor materials such as silicon carbide (SiC) are investigated intensely. As illustrated in [2], compared to Si material, SiC material shows higher critical electrical field, higher

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SiC switches keeps the same for both two-level and three-level converters, which means that the comparison is not fair enough. Better performance of the three-level converter is expected, especially in a higher switching frequency range.

However, for the SiC-based multilevel rectifier, price issue becomes more significant since more devices are required for each phase circuit. In order to address this problem, hybrid rectifiers, which consist of Si IGBT/MOSFET and SiC diode, have been intensely investigated in the research. In Section II, a review of hybrid active rectifier solutions for high-power applications is given. The review of existing solutions shows that in most solutions, Si devices such as IGBT or MOSFET are still switched under the same frequency as the SiC devices. Therefore, the Si devices still have large switching losses. On the other hand, the application of the SiC diode has been fully explored, while the potential of the combined usage of SiC MOSFET and Si device has not been investigated.

In this paper, a highly efficient low-cost hybrid three-phase three-level rectifier is proposed. This rectifier applies SiC MOSFET and Si diode instead of SiC diode and Si IGBT. It presents low switching losses because the reverse recovery losses of all the Si devices are eliminated. At the same time, the total device cost of this rectifier is lower than the all-SiC-based rectifiers. In this paper, a review of high-power hybrid rectifier topologies is given in Section II. The circuit operational analysis is given in Section III. The simulation and experimental results are given in Section IV. A comparison between several classic solutions and the proposed rectifier is carried out in Section V. Section VI concludes the paper.

II. Review of Hybrid High-Power Active Front-End Topologies

There are a great many topologies that are suitable for AFE applications. However, when it comes to a high-power system, which has a three-phase input and high-voltage dc link, many single-phase rectifier topologies such as conventional boost type rectifiers in [13] and [14] and bridgeless boost-type rectifiers in [15] and [16] become less attractive since three large dc-link capacitors are required under this situation. On the other hand, soft-switching schemes with too many additional components are not preferred in the high-power area. As a result, fewer possible rectifiers are considered in this section.

In the high-power hard-switching Si-based rectifier circuit, a large portion of switching losses is caused by the reverse recovery of the Si diode. As a result, in most of the hybrid circuit structure, an SiC Schottky diode is applied to replace the Si fast recovery diode and paired with the Si IGBT or MOSFET.

Among all these hybrid structures, the classic two-level active rectifier is the most common one whose per-phase circuit is shown in Fig. 1(a), where S_1, S_2 are Si IGBTs and D_1, D_2 are SiC Schottky diodes. Investigation in Fig. 1 shows that by applying this, the turn-ON energy losses $E_{\rm on}$ can be reduced by 55%, and the reverse recovery losses in the SiC Schottky diode can be almost completely eliminated [17]. However, the disadvantage of this circuit is that large ac-side filters and higher voltage rating devices are required by the two-level rectifier. These will increase the total cost as well as the total losses.

On the other hand, three-level rectifiers can further decrease the size of the filters and switching losses. The per-phase circuits of different three-level rectifiers are shown in Fig. 1(b)–(f). A total of three types of three-level neutral point clamped (NPC) rectifiers are demonstrated in Fig. 1(b)–(d). Among these three types, type I shown in Fig. 1(b) is the most common one in the industry. It requires two fast switching diodes D_1 and D_4 where reverse recovery always takes place. In applications where high performance is required, D_1 and D_4 may be replaced by SiC Schottky diodes [18]. Type II shown in Fig. 1(c) is proposed in [19] and [20] where active switches S_1 and S_2 have changed their positions. Another type III NPC circuit with more diodes and fewer switches is shown in Fig. 1(d). Although these two types of the circuit are slightly different than type I, the position and the number of the fast switching SiC diodes are kept the same. A total of two types of three-level T-type rectifiers are shown in Fig. 1(e) and (f) [21], [22]. Compared to the hybrid NPC rectifiers, these hybrid T-Type rectifiers use higher voltage-rating SiC diodes for D_1 and D_2. But much lower conduction losses are expected with T-type rectifier circuits.

By summarizing the hybrid topology solutions given above, it can be found that in all SiC diode and Si switch hybrid circuits, the switching transient commutation is always between one Si active switch and one SiC diode. It means that the switching frequency of the Si device is always the same as the SiC diode [even higher in Fig. 1(d) and (f)]. From the loss distribution given in [17] and [22], it is obvious that the Si devices still have high switching losses. The further improvement of the power density based on these hybrid configurations is thus limited by their thermal constraint.

Following the maturing of SiC MOSFET manufacture technology, the combined usage of SiC MOSFET and Si device becomes attractive. Initial research works can be found on the device level, where one SiC MOSFET and one Si IGBT are packed together to form a new hybrid switch [23]. On a circuit level, hybrid structures like the one shown in Fig. 1(g) have utilized the similar idea that the SiC diode and Si switch hybrid circuits have [24]. The problem is that the switching frequency of the Si switches is still the same as that of their SiC paired parts. The switching losses are too high for the Si devices, while the potential of SiC MOSFETs has not been fully explored.

In conclusion, the review of existing hybrid high-power active rectifiers shows that the problem that limits the further improvement of the switching frequency and power density is the high switching losses on Si devices. Advanced circuit topology is yet to be investigated.

III. Analysis of the Proposed SiC MOSFET and Si Diode Hybrid Three-Phase Three-Level Rectifier

In this paper, a novel three-phase three-level hybrid rectifier is proposed whose per-phase circuit is shown in Fig. 2(a). The circuit is derived from the classic NPC-type three-level rectifier. The major difference between the proposed circuit and three-level NPC rectifier type II shown in Fig. 1(c) is that for the proposed rectifier, Q_2 and Q_3 are using SiC MOSFET instead of Si devices, while D_1 and D_4 are using a low-speed Si diode instead of a high-speed diode such as the SiC Schottky diode. In this

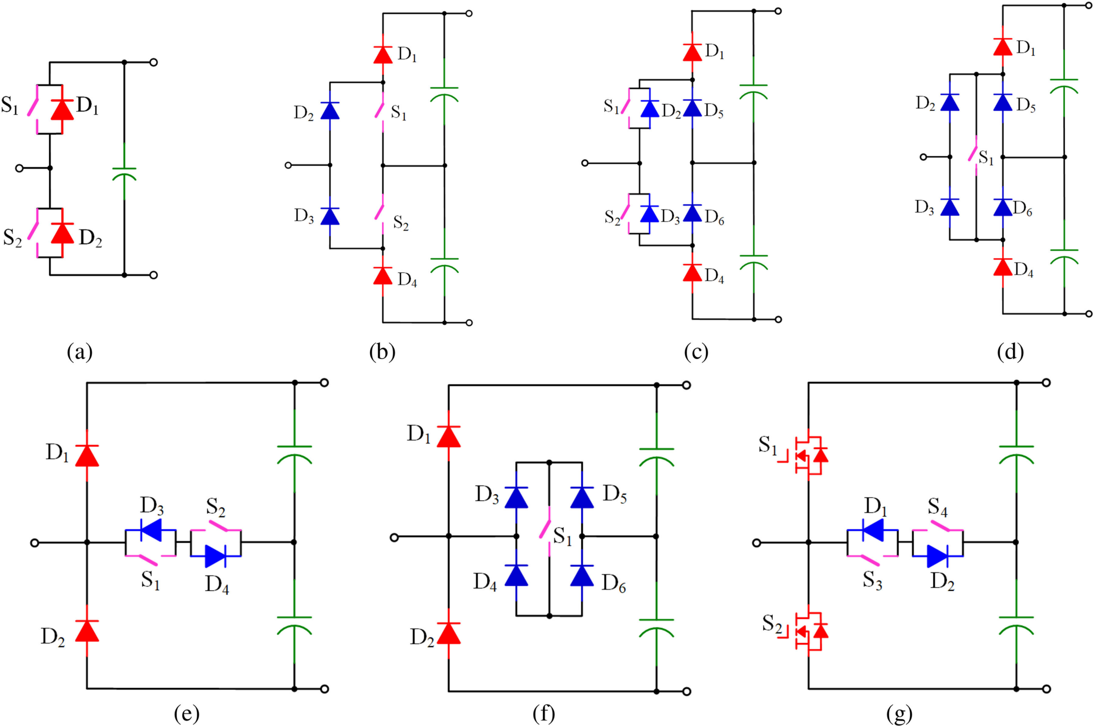

Fig. 1. Per-phase circuit of existing hybrid PFC boost rectifiers: Diodes in blue: slow speed diode; Diodes in red: fast-switching diode using the SiC Schottky diode. (a) Two-level rectifier. (b) Three-level NPC rectifier type I. (c) Three-level NPC rectifier type II. (d) Three-level NPC rectifier type III. (e) Three-level T-type rectifier type I. (f) Three-level T-type rectifier type II. (g) SiC MOSFET and Si switch bi-directional rectifier.

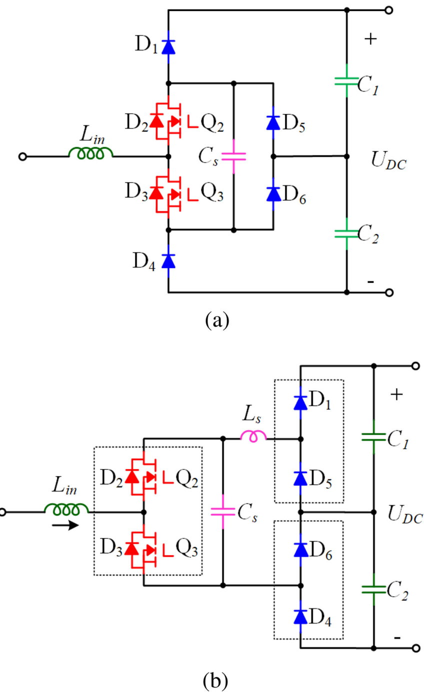

Fig. 2. Per-phase circuit of the proposed hybrid three-level rectifier. (a) Schematic of the proposed rectifier. (b) Real implementation in the high-power application.

way, each phase circuit consists of four low-speed Si diodes and two SiC MOSFETs. Furthermore, an additional snubber capacitor C_s is added. This capacitor is critical for the proposed rectifier, especially when applying to the high-power area where typically power modules are adopted instead of discrete devices. The equivalent circuit of the proposed rectifier, which consists of SiC and Si power modules, is shown in Fig. 2(b). The two SiC MOSFETs form one half-bridge module, while the four Si diodes form two Si diode half-bridge modules. Whatever it uses, the copper bar or laminated busbar to connect the SiC and Si modules, inevitable large stray inductance L_s exists between these two parts. C_s is required to absorb the energy in L_s when Q_2 or Q_3 is forcibly turned OFF. On the other hand, even if no L_s exists, the original dc-link capacitors C_1 and C_2 still cannot realize the voltage clamping for Q_2 and Q_3 during their turning OFF, since D_5 and D_6 block the transient current. In the later section, theoretical analysis and simulation is given to demonstrate the function of C_s.

In the following part, the operational principle of the circuit is demonstrated to show how to realize low switching losses by eliminating the reverse recovery losses on those Si diodes. The key waveforms are shown in Fig. 3. The equivalent circuits during the operation are shown in Fig. 4(a)–(f). The gating strategy to generate each voltage level is given in Table I. Since there are only two active switches per one phase circuit, the output voltage level is not only depended on the switching patterns but also highly related to the polarity of the input ac voltage, or in other words, it is decided by the input ac current since the ac voltage and ac current are always in phase with each other if the unity power factor is realized.

One switching period when the input voltage is positive is given as an example to show the operational principle. During

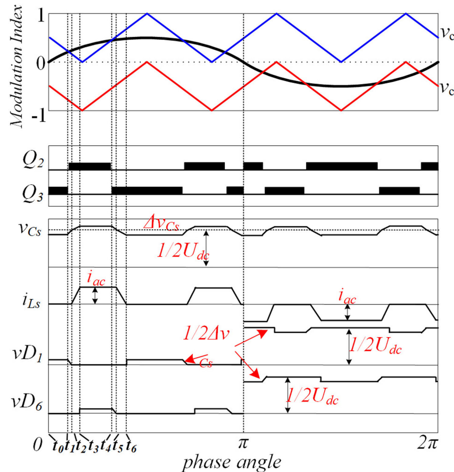

Fig. 3. Key waveforms of the proposed rectifier.

TABLE I
RELATIONSHIP AMONG INPUT VOLTAGE, VOLTAGE LEVELS, AND SWITCHING PATTERNS

Input Voltage or Input Current	Voltage Level	Q_2	Q_3
"-"	-1	0	1
	-0	1	0
"+"	+0	0	1
	+1	1	0

this one switching period, Si diodes D_5 and D_4 are always in the off-state. Their voltages are always equal to half of the dc-link voltage minus the voltage drop on their complimentary diodes D_1 and D_6.

[t_0–t_1]: The analysis starts from the interval when the circuit output is the voltage level "+0." At the moment, Q_3 is ON, Q_2 is OFF, and the ac current goes through Q_3 and D_6 as the equivalent circuit in Fig. 4(a) shows.

[t_1–t_2]: At the time t_1, Q_3 is turned OFF and the ac current is forced to commutate to Q_2's body diode D_2. At this time, the C_s voltage v_{Cs} is still lower than the voltage on C_1, which is $1/2U_{\rm dc}$. Therefore, D_1 does not enter into the conduction mode immediately. Instead, the D_1 voltage decreases gradually. The ac current charges C_s and continues to go through D_6. The turn-OFF losses on Q_3 can thus be lower due to the voltage clamping. The equivalent circuit is shown in Fig. 4(b). During this interval, the voltage on D_1 is equal to the voltage difference between v_{Cs} and v_{C1}. After a period of short deadtime, Q_2 can be turned ON and make the current go back to its MOS channel.

[t_2–t_3]: At the time t_2, v_{Cs} becomes higher than v_{C1} and D_1 begins to conduct. The equivalent circuit of this interval is shown in Fig. 4(c). However, the rising rate of i_{Ls} is limited. During this interval, C_s still acts as a snubber capacitor that resonates with L_s and the voltage on C_s continues to increase. v_{Cs} and i_{Ls} can be calculated by (1) and (2), respectively. $I_{\rm ac}$ represents the instantaneous ac current during this switching period:

$$i_{Ls} = I_{\rm ac}\left[1 - \cos\frac{1}{\sqrt{L_s C_s}}(t - t_2)\right] \tag{1}$$

$$v_{Cs} = \sqrt{\frac{L_s}{C_s}} I_{\rm ac} \sin\frac{1}{\sqrt{L_s C_s}}(t - t_2) + \frac{1}{2}U_{\rm dc}. \tag{2}$$

[t_3–t_4]: At the time t_3, i_{Ls} becomes equal to the ac current. The voltage on Si diode D_6 increases and the resonance between v_{Cs} and i_{Ls} soon stops. v_{Cs} becomes its maximum value, which is higher than v_{C1}. This part of voltage drops on D_6. It can be found that the OFF-state voltage on D_6 is much lower than $1/2U_{\rm dc}$, which is almost equal to zero if the volume of C_s is large enough. At the same time, its reverse recovery current is limited by L_s. Thus, its reverse recovery losses can be neglected. On the other hand, the maximum voltage of C_s is also the maximum voltage on all SiC devices. As a result, a reasonable volume should be chosen to minimize the system voltage stress. During this interval, the circuit output is the voltage level "+1." The ac current goes through Q_2 and D_1, as shown in Fig. 4(d).

[t_4–t_5]: At the time t_4, Q_2 is turned OFF. After a short deadtime, Q_3 is turned ON. The equivalent circuit during this interval is shown in Fig. 4(e). The input inductor current is commutated from $Q_2(D_2)$ to Q_3. C_s begins to be discharged through L_s and D_1. The voltage of D_6 begins to decrease.

[t_5–t_6]: As soon as v_{Cs} becomes equal to v_{C1}, its resonance with L_s starts again. The expressions for v_{Cs} and i_{Ls} are similar to (1) and (2). The equivalent circuit during this interval is shown in Fig. 4(f). At the time t_6, i_{Ls} becomes zero and the resonance stops. v_{Cs} becomes its minimum value, which is lower than v_{C1}. This part of voltage drops on D_1. Theoretically, D_1 should have experienced the reverse recovery process. However, the changing rate of the current through D_1 is limited by L_s. Moreover, the blocking voltage on D_1 is only the voltage difference between v_{Cs} and v_{C1}. Thus, its reverse recovery losses can also be neglected just like D_6. After this interval, the equivalent circuit becomes the same as Fig. 4(a) shows where a new switching period begins.

The operational principle when the input voltage is negative is similar to when the input voltage is positive, and will not go in details here. After the analysis, it is soon found that the Si diodes D_4 and D_5 have the similar situation as D_1 and D_6, which is that the reverse recovery losses are minimized and the entire off-state voltage is undertaken by Q_3 (D_3) after the commutation. Under this mechanism, the reverse recovery losses and turn-ON losses of the rectifier circuit can be minimized, since all the losses are shifted from Si diodes to SiC MOSFETs or their body diodes. The switching frequency of all the Si diodes can be considered as equal to the line frequency. As a result, even general purpose diodes used in bridge rectifiers are also applicable for D_1, D_4, D_5, and D_6.

The commutation of the proposed circuit when the ac current is crossing zero is slightly different. When the ac current is crossing zero, the current is reversely blocked by the Si diodes. During this time, the ac current charges or discharges the junction capacitor of all Si diodes. All these capacitors added together resonate with the ac inductor $L_{\rm in}$. Nevertheless, since the amplitude of the current is very low during this interval, all Si diodes can still be considered as under the zero-current-switching (ZCS) condition and the switching losses are still minimized.

There is another benefit of applying this hybrid configuration. Compared with the NPC rectifier type I in Fig. 1(b) and the NPC

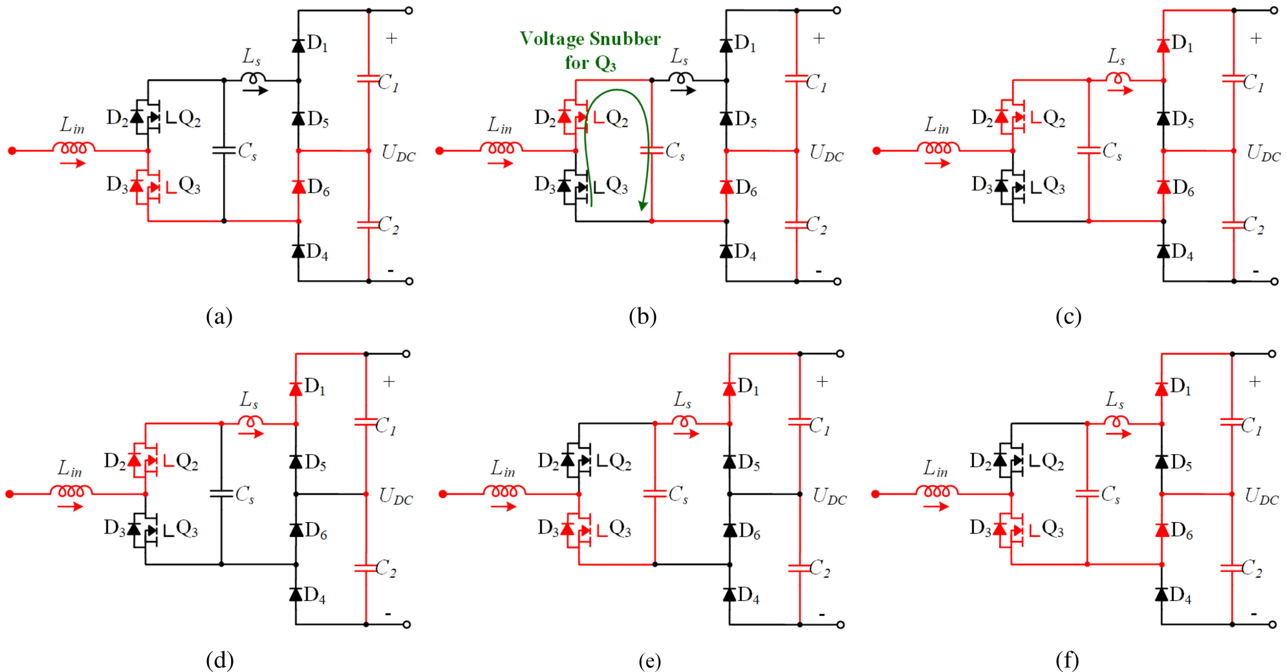

Fig. 4. Equivalent circuit of intervals when the input voltage is positive. (a) $[t_0–t_1]$. (b) $[t_1–t_2]$. (c) $[t_2–t_3]$. (d) $[t_3–t_4]$. (e) $[t_4–t_5]$. (f) $[t_5–t_6]$.

rectifier type II in Fig. 1(c) where two discrete SiC diodes are implemented, the proposed circuit can be realized by implementing two Si diode half-bridges and one SiC MOSFET half-bridge. It is convenient for those high-power applications where power modules are usually adopted. No customized power module with Si IGBT-SiC diode pair or Si MOSFET-SiC diode pair is required. Also, from the above-mentioned analysis, it can also be inferred that the essence of the proposed rectifier is still an NPC-type three-level rectifier. Therefore, the modulation and control of the circuit are fully compatible with many well-developed strategies for other NPC-type three-level rectifiers.

TABLE II
SIMULATION, CONVERTER PROTOTYPE SPECIFICATIONS, AND DEVICE SELECTION

	Experimental Prototype	Simulation
Configuration	Single-Phase	Three-Phase
Rated Output Power P_{max}	4.2 kW	500 kW
DC link Voltage U_{dc}	650 V	1500 V
Switching Frequency f_{sw}	20 kHz, 30 kHz, 40 kHz	30 kHz
Grid Voltage V_{ac}	208 V_{ac}/60 Hz	870 V_{ac}/60 Hz
Grid AC Current I_{ac}	21 A	330 A
Grid Inductor L_f	870 μH (0.0286 p.u.)	116 μH (0.0286 p.u.)
DC Capacitance C_{dc}	9 mF each	1 mF each
Snubber Capacitor C_s	1 μF	25 μF
Stray Inductance L_s	N/A	100 nH
SiC MOSFET	ROHM-SCT3022AL-E (650 V, 65 A)	
Si Diode	Infineon-IKW75N65ES5 (Anti-parallel diode 650 V, 75 A)	

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to demonstrate the functionality of the circuit as well as the efficiency performance, simulation and experiment are both carried out. The specification of the simulation and experiment is given in Table II. Aiming to the high-power application, the simulation is carried out with the specification where the power rating of the rectifier is 500 kW and the dc-link voltage is 1500 V. With such a high power range, three-level topologies are always desired to minimize the power loss and increase the power density. The circuit diagram for simulation is shown in Fig. 5(a). On the other hand, in order to simplify the experimental set, a scaled down single-phase prototype is assembled. The neutral point of the dc link of the prototype is connected to the neutral of the ac grid to make this circuit work. The operational principle of the single-phase simplified set is the same as the three-phase version if using the same p.u. value of the grid-side inductor and the modulation index. Also, large dc-link capacitors are applied to minimize the double line frequency dc-link voltage ripple. The circuit diagram for the experiment is shown in Fig. 5(b) and the power stage picture of the developed prototype is shown in Fig. 5(c).

Based on the specification of the prototype, 650 V series semiconductors including SiC MOSFETs and Si diodes are selected. As a result, the prototype can operate with 650–800 V dc link and 208 V ac grid system. It is difficult to find a slow speed general purpose diode with suitable package and voltage rating, since typically those diodes are not designed for the switching mode power supply. Therefore, the Si diodes selected for D_1, D_4, D_5, and D_6 are using the integrated antiparallel diode of one IGBT. Thus, they are all fast recovery diodes instead of slow speed general purpose diodes. Since all these diodes can be considered as switching under the line frequency, irrespective of which type is adopted, there will be little influence on the switching loss performance.

In order to evaluate the function of C_s, a 100 nH stray inductance L_s is added to the simulation. Based on (2), the maximum

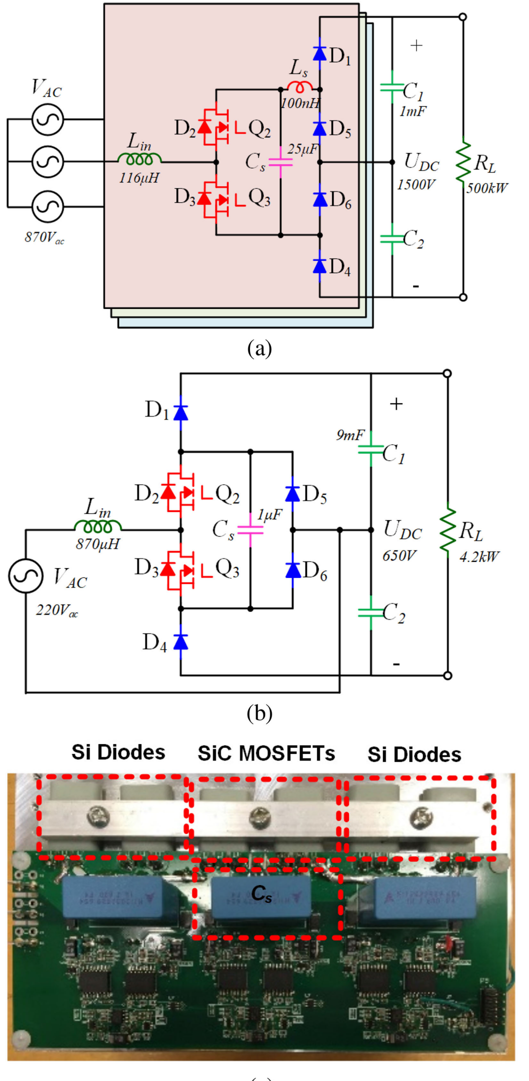

Fig. 5. Simulation and experimental setup for the proposed hybrid three-level rectifier. (a) Three-phase circuit diagram used for simulation. (b) Single-phase circuit diagram used for the experiment. (c) Power stage of a developed 4.2 kW single-phase prototype.

v_{Cs} can be calculated with

$$v_{Cs_\max} = \frac{1}{2}U_{\rm dc} + \sqrt{\frac{L_s}{C_s}} I_{\rm ac_max}. \tag{3}$$

According to the specification of the simulation, the maximum ac current $I_{\rm ac_max}$ is around 500 A. With 25 μF snubber capacitor C_s, the maximum voltage is around 780 V with respect to 750 V half-dc-link voltage. During the experiment, however, multilayer printed circuit board (PCB) and careful layout design lead to very small stray inductance. At the same time, the output ac current is also small. As a result, a 1 μF capacitor can make the over-voltage problem become negligible.

As mentioned in the previous section, the control of this rectifier can be exactly the same as that of other three-phase three-level rectifiers. Algorithms such as space vector modulation (SVM) and neutral point voltage control, which have been already addressed in several papers [25], [26], are directly applied in the control scheme of this converter. The steady-state three-phase rectifier operation is demonstrated in Fig. 6(a). It can be found that a purely sinusoidal ac current input is realized. On the other hand, two dc-link capacitor voltages are balanced with the applied SVM and neutral point voltage control.

The waveforms on devices in half of the circuit are shown in Fig. 6(b). It can be found that the waveforms when the ac current is at its peak are exactly the same as the theoretical analysis. The voltage ripple on C_s is about 60 V, which meets the result calculated by (3). Thus, the maximum voltage on C_s as well as other SiC MOSFETs is all equal to 780 V. At the same time, the OFF-state voltages on D_1 and D_5 during the positive cycle are also only 30 V, which is much lower than 750 V half-dc voltage. It means that only the SiC MOSFET pairs Q_2 and Q_3 have high-frequency hard-switching. On the other hand, the voltage waveforms on D_1 and D_5 when the ac current is crossing zero become different. Resonance takes place between the ac inductor and the output capacitance of D_1 and D_5. ZCS switching is realized for D_1 and D_5. The simulation results have proved that the proposed circuit should have low switching losses since the reverse recovery losses on all Si diodes are minimized.

The experimental results are shown in Figs. 7 and 8. The detailed voltage waveforms on all devices are shown in Fig. 7. According to Fig. 7(a) and (b), when the input ac voltage is positive, the equivalent circuits of the rectifier are the same as Fig. 4 shows. Furthermore, since the stray inductance L_s and the ac current are small, the voltage ripple on C_s can be neglected. Therefore, according to the waveforms, the voltage on D_1 and D_6 is equal to zero, while the voltage on D_4 and D_5 is equal to half of the dc-link voltage 325 V. Reverse recovery losses are minimized on those diodes. On the other hand, two SiC MOSFETs are complimentarily fast switching. The turning OFF of Q_3 changes the voltage level of the circuit from "+0" to "+1." Q_2 is turned ON after a short deadtime to provide synchronous rectification. In Fig. 7(c), the low-speed switching of all diodes and fast switching of SiC MOSFET are demonstrated more clearly. It can be found that D_1 and D_5 are switching under 60 Hz. High efficiency can thus be achieved since only SiC devices are under high-frequency switching.

The waveforms on ac input and dc output are shown in Fig. 8. power factor correction (PFC) functions are realized. The total harmonics distortion (THD) of the ac current is 4.341% according to the measurement. Because the input grid-side voltage contains significant contents of voltage harmonics, the ac side current also includes current harmonics. Better input voltage and advanced control scheme may decrease these current harmonics.

The efficiency of the prototype operating under rated input voltage 220 Vac and rated dc voltage 650 V is evaluated. The result of the test, which includes all parts of losses, is shown in Fig. 9. It can be found that, under 40 kHz switching frequency, the overall efficiency can be over 98.4%. The peak efficiency of the prototype can reach up to 99.2% under 20 kHz switching.

V. Comparison and Discussion

In this section, a comprehensive comparison is made between the proposed rectifier and other popular hybrid and all SiC-based

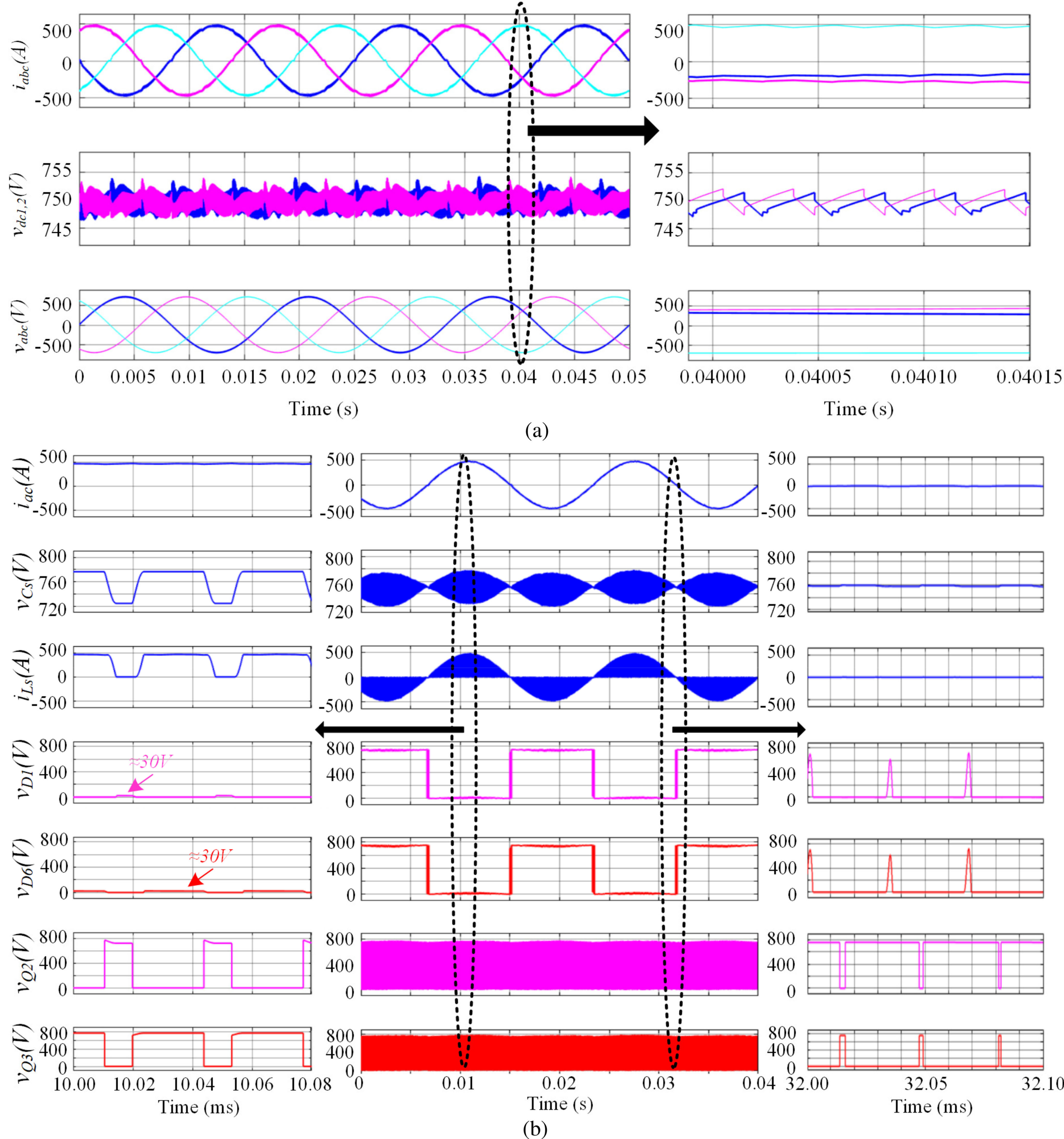

Fig. 6. Simulation results of the proposed rectifier. (a) Steady-state three-phase operational waveforms. (b) Waveforms on devices in half of the one-phase circuit.

rectifier circuits in terms of cost and efficiency. As the proposed rectifier topology is targeting the high-power applications, the comparison is carried out based on the assumed specification shown in the simulation where a 1500 V dc-link voltage and 500 kW power rating are selected. However, currently, there is no SiC diode in the market that is designed for the high-power application. In order for fair comparison, only 1200 V/1700 V SiC and Si devices with the TO-247 package are selected. Their key characteristics and price used for comparison are listed in Table III. In order to take the high current, ten pieces of each type are connected in parallel. The 1700 V SiC diode requires 20 pieces in parallel since it has a lower current rating and smaller die size. Within all analyses, it is assumed that the main current will be evenly distributed to each device.

A total of five different rectifier configurations are considered to be compared, which are listed in Table IV. They are (a) hybrid T-type three-level rectifier, (b) SiC T-type three-level rectifier, (c) hybrid NPC three-level rectifier, (d) SiC NPC three-level rectifier, and (e) the proposed rectifier. The selection of devices for each configuration is also listed in Table IV.

The loss comparison is carried out first with the help of simulation based on *PLECS block* in *MATLAB/Simulink*. The switch-

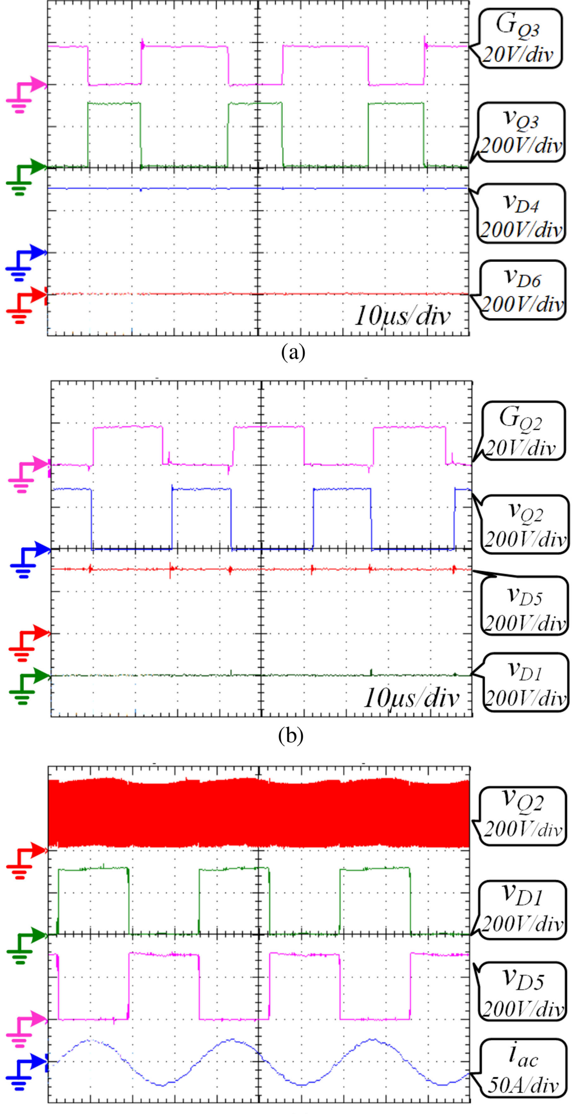

Fig. 7. Demonstration of voltage on all devices. (a) Voltage waveforms on Q_3, D_4, D_6 when the ac voltage is positive. (b) Voltage waveforms on Q_2, D_1, D_5, when the ac voltage is positive. (c) Voltage waveforms in several line periods.

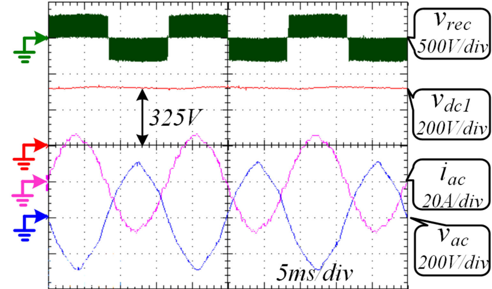

Fig. 8. Experimental waveforms of the proposed rectifier: rectifier side voltage, dc capacitor voltage, ac input voltage, and ac input current.

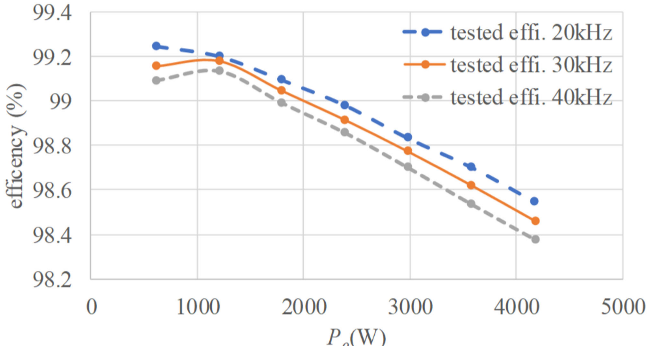

Fig. 9. Efficiency performance under different switching frequencies and 220 Vac input.

ing loss data and the ON-state characteristic of each device are extracted from its datasheet and logged into the software thermal library. The results of each part of power losses are calculated automatically. One difficult thing is that for the Si IGBT/SiC diode hybrid switching pair, the turn-ON loss data are not the same as the datasheet shows, since, with the elimination of diode's reverse recovery losses, the turn-ON losses of Si IGBT should also be decreased significantly. In our calculation, the turn-ON losses in this situation are considered to be decreased by around 50%. This number can be referred to in different papers such as [17] and [27].

For the cost comparison, only the components in the power stage can have the price number from the website. Another issue is that, apparently, the switching loss of the Si IGBT/SiC diode hybrid pair is much higher than that of the pure SiC pair. In order to make the loss performance comparable, the switching frequency of the Si IGBT/SiC diode hybrid pair is set to be only 1/3 of the frequency used for the pure SiC pair. In this way, a larger filter design is required to achieve a similar THD performance for the hybrid pair. Therefore, the cost comparison is carried out according to the price of the power stage and the volume of the grid-side inductor. All these results are given in Table IV. The analyses of the results are given in the following parts.

A. Conduction Loss Comparison

The calculated results based on PLECS for the five topologies are given in Table IV. From the results, it can be found that the T-type rectifiers have lower conduction losses than other NPC-type rectifiers due to fewer devices when the voltage level is "+1" or "–1." However, this advantage is not as significant as the Si-based T-type converter has. The reason is that the SiC diodes here are all Schottky type, which does not have the conductivity modulation effect. So higher voltage 1700 V SiC diodes have distinct higher conduction losses than the 1200 V SiC diodes.

On the other hand, the conduction loss comparison between three NPC-type rectifiers (c)–(e) becomes the comparison of voltage drop under the same current among SiC diode, SiC MOSFET, and Si IGBT. In Table III, the die size of SiC devices can be derived. In order to have a fair comparison, the ON-state characteristic of all devices is scaled to the same die size 30 mm^2 and then plotted in Fig. 10. And a 100 W constant power curve is also plotted to indicate the conduction loss limitation applied to the die. In fact, the theoretical maximum power dissipation of a 30 mm^2 die should be higher than this number. But after considering the switching losses and nonideal heat transfer condition, it is hard to let the conduction losses of the die be

TABLE III
CHARACTERISTICS AND PRICE OF SiC AND Si DEVICES IN COMPARISON

	Voltage rating (V)	*Continuous current at T_c>100°C (A)*	*Die Size (mm²)*	*E_{off} (mJ) U_{dc}=600 V, I_c=60 A*	*Unit price (USD) (Buy more than 100 pcs @www.digikey.com)*
Si Diode (Vishay-VS-60EPF12PBF)	1200	60	N/A		5.45
SiC Diode (CREE-C4D40120D)	1200	54	18.97		37.5
SiC Diode (CREE-C3D25170H)	1700	26.3	16.83		63.6
Si IGBT (Infineon IKQ50N120)	1200	50	N/A	5	9.52
SiC MOSFET (CREE-C2M0025120D)	1200	60	26.02	0.5	73.29
SiC MOSFET (CREE-C2M0045170D)	1700	48	29.98	0.5	91.56

TABLE IV
SUMMARY OF COMPARISON BETWEEN TOPOLOGIES

	(a) Hybrid T-type Three Level Rectifier	**(b) SiC T-type Three-Level Rectifier**	**(c) Hybrid NPC Three Level Rectifier**	**(d) SiC NPC Three-Level Rectifier**	**(e) Proposed Rectifier**
Topology	Fig. 1(e)	Fig. 1(e)	Fig. 1 (b) or (c)	Fig. 1 (b)	Fig. 2
SiC Diode	1700 V SiC Diode × 40	1700 V SiC Diode × 20	1200 V SiC Diode × 20	1200 V SiC Diode × 20	0
Slow speed Diode	0	0	1200 V Si Diode × 20	1200 V Si Diode × 20	1200 V Si Diode × 40
Active Switch	1200 V Si IGBT × 20	1200 V SiC MOSFET × 20	1200 V Si IGBT × 20	1200 V SiC MOSFET × 20	1200 V SiC MOSFET × 20
Price per each phase (USD)	2734.4	4009.8	1049.4	2324.8	1683.8+14.31
Switching Frequency (Hz)	10 kHz	30 kHz	10 kHz	30 kHz	30 kHz
Conduction Loss(W)	2208	2190	2670	2592	2376
Switching Loss(W)	1488	1074	1488	1068	1080
AC inductor Volume (μH)	348 μH	116 μH	348 μH	116 μH	116 μH
Current THD	1.80%	1.58%	1.74%	1.60%	1.63%

higher than this number. According to the results, in most of the design case, the SiC MOSFET should have a lower ON-state voltage drop compared to the SiC diode, especially for the 1200 V type. A similar conclusion can be derived for the comparison between SiC MOSFET and Si IGBT. By investigating the topology of the proposed rectifier, each voltage level is formed by series connecting the SiC MOSFET and Si diode, while in the other NPC topologies, the voltage levels are formed by connecting the SiC diode and Si diode or Si IGBT and Si diode. This is the reason that the proposed rectifier has the lowest conduction losses among all three NPC-type rectifiers.

B. Switching Loss Comparison

The difference in switching losses comes from different switching pairs. In (a) and (c), the switching actions are between SiC Schottky diode and Si IGBT, while in other configurations, the switching actions are between SiC diode and SiC MOSFET. Although with the help of SiC diodes, the reverse re-

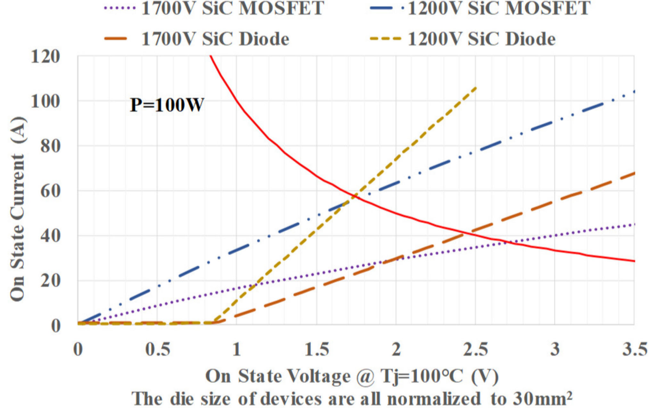

Fig. 10. On-state I–V curve comparison for SiC MOSFET and SiC diode.

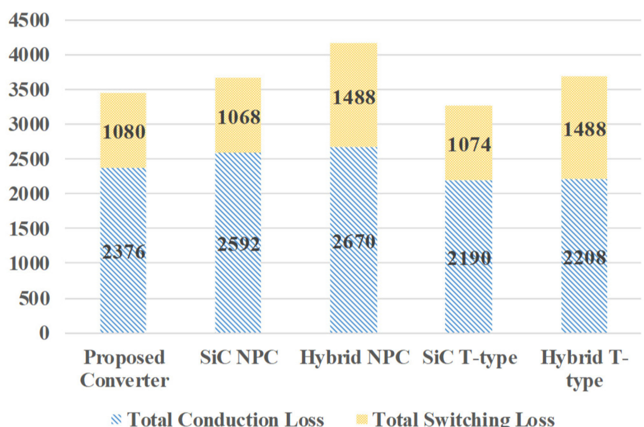

Fig. 11. Total loss comparison results among five topologies.

covery current is minimized, the turn-OFF loss E_{off} is still high in the 1200 V IGBT. Therefore, (a) and (c) should still have much higher switching losses compared to the others. According to the results, even though the switching frequency of (a) and (e) has decreased to 10 kHz, the switching losses are still higher than the others. On the other hand, for the proposed rectifier, the switching actions are always between the SiC MOSFET and its body diode instead of between SiC MOSFET and individual SiC Schottky diode in (b) and (d). Comparative research in [28] shows that, based on nowadays manufacturing technology, the reverse recovery losses on the body diode of SiC MOSFET have now become similar to the SiC Schottky diode. This makes the switching loss performance of (b), (d), and (e) become similar. The analyses are well supported by the calculated results, where the proposed rectifier shows a superior switching loss performance among all these circuits.

The results of total losses for each topology are shown in Fig. 11 as well as in Table IV. It can be found that the proposed converter has the second lowest total power losses among all topologies.

C. Cost Comparison

In Table III, it can be found that Si diode and IGBT can almost be considered as a no-cost device compared to SiC diode and MOSFET. Although compared to the SiC diode, SiC MOSFET is still more expensive, but the price gap is not so significant. Especially for the 1700 V SiC diode, it has a small current rating and much higher price than the 1200 V one. It means that, for the T-type converter, in order to have lower conduction losses, more 1700 V SiC diodes should be used per each phase. The results in Table IV show that both SiC rectifiers and the hybrid T-type rectifier have higher total cost than the proposed rectifier. On the other hand, compared to the hybrid NPC rectifier, although the proposed rectifier has higher total cost, it requires only 1/3 of the inductor volume, which leads to further decreasing of total cost and higher power density. The additional 25 μF/1100 V film capacitor only costs $14.31 on digikey.com, which can be neglected.

In summary, the proposed rectifier has reasonably low cost and lower switching losses under over 1000 V dc bus specification compared to the other hybrid and all-SiC based solutions. It has achieved an optimized performance between the total cost and the power losses. It can potentially become an attractive solution for the high-power high-end rectifier applications.

VI. Conclusion

In this paper, a highly efficient three-phase three-level rectifier comprising SiC MOSFET and Si diode hybrid power stage is proposed. It presents reasonably low cost in high-power high-voltage applications and, at the same time, achieves low switching losses because the reverse recovery losses on all Si diodes have been eliminated. Furthermore, this topology is easy to be configured as high-power type since all devices can use the half-bridge module.

The proposed rectifier is targeting the high-power rectifier area where the dc bus voltage is over 1000 V. Limited by the ac source voltage in the laboratory, it is tested with 650 V dc and 650 V devices. According to the experimental results, the proposed rectifier can achieve over 99% high efficiency within a wide power range. In order to fully explore its advantages, a comparison is carried out under the specification where the dc bus is over 1000 V. The results show that the proposed rectifier has the reasonable cost, and the switching losses and conduction losses are both lower compared to other hybrid or all SiC-based NPC-type rectifiers. Thus, this circuit is favorable for high power density, high dc voltage three-phase ac–dc applications such as EV charging station or AFE for the medium-voltage drive system.

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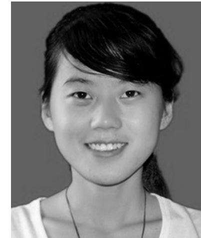

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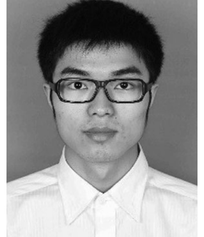

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