An SiC MOSFET Based Three-Phase ZVS Inverter Employing Variable Switching Frequency Space Vector PWM Control

Jianliang Chen, *Student Member, IEEE*, Deshang Sha, *Senior Member, IEEE*, Jiankun Zhang, and Xiaozhong Liao, *Member, IEEE*

***Abstract*—In this paper, a variable switching frequency space vector pulsewidth modulation control is proposed. It is used to achieve zero voltage switching (ZVS) for a three-phase grid-connected voltage source inverter with unity power factor. A wide range of ZVS can be realized without any additional sensors, auxiliary circuits, or current zero crossing detection circuits. The switching frequency can be easily calculated by a digital controller. The frequency variation range in a line cycle is only about 1.5 times at any specific load. An *LCL* filter is used to attenuate the high current ripples at the inverter side, and active damping is adopted to avoid the resonance and reduce the filter power loss. The switching loss can be significantly reduced by using silicon carbide MOSFETs so that the conversion efficiency is high. The power density can also be improved due to the high switching frequency and the low inductance value of the filter. The operating principle, design considerations, and loss analyses are discussed in detail. A 3.5-kW simulation and experimental prototype interfacing a 350–400-V dc with a three-phase 110-V ac grid is developed to verify the performance of the proposed control strategy.**

***Index Terms*—Space vector pulsewidth modulation (SVPWM), three-phase voltage source inverter (VSI), variable switching frequency control, zero voltage switching (ZVS).**

I. Introduction

OWING to its simple structure and bidirectional power flow capability, the three-phase voltage source inverter (VSI) has been used extensively in all kinds of applications, such as electric vehicle chargers, active power filters, and renewable energy systems [1]–[3]. Although the VSI has been developed for decades of years, the demands on higher conversion efficiency and higher power density never stop.

The emerging wide bandgap (WBG) devices, including gallium nitride (GaN) and silicon carbide (SiC) transistors, offer a

Manuscript received January 8, 2018; revised May 10, 2018 and July 31, 2018; accepted September 20, 2018. Date of publication October 3, 2018; date of current version May 2, 2019. This work was supported in part by the National Natural Science Foundation of China under Grant 51577012, in part by the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources under Grant LATS17019, and in part by the Key Laboratory of Solar Thermal Energy and Photovoltaic System of the Chinese Academy of Sciences. Recommended for publication by Associate Editor J. Wang. *(Corresponding author: Deshang Sha.)*

The authors are with the Advanced Power Conversion Center, School of Automation, Beijing Institute of Technology, Beijing 100081, China (e-mail:

both positive and negative in one switching cycle. The idea was implemented in boost power factor correction (PFC) [19], totem-pole bridgeless PFC rectifiers [20], and single-phase ZVS inverters [21]. A zero crossing detection (ZCD) circuit is usually used to limit the unnecessary current ripples and circulation loss, leading to a variable switching frequency. It can also distribute the conducted EMI spectrum and effectively reduce the EMI filter size [22]. Interleaving and coupled inductor techniques are also integrated to reduce the current ripples with the critical current mode (CRM) [23] or the triangular current mode [24]. A four phase-leg single-phase inverter is also proposed in the Google Little Box Challenge to achieve high power density [25].

However, this method has only been widely discussed in single-phase inverters/rectifiers. The ZVS method of three-phase inverters has not been thoroughly investigated because the three-phase currents are coupled. It is difficult to guarantee that all the three-phase inductor currents flow in the appropriate directions when the corresponding switch is turned-ON. In [26], the neutral point of the filter capacitors in the *LCL* filter is connected to the middle point of the dc-bus. Thus, the inductor current of each phase is decoupled and can be controlled similarly as in the single-phase inverter. However, the switching frequency range is too wide in a line cycle due to a large variation of the inductor voltage amplitude. A combination of the CRM and discontinuous pulsewidth modulation (DPWM) soft switching three-phase inverter was recently proposed in [27]. ZCD circuits are used for each phase current; hence, switching frequency synchronization is needed. Although high efficiency and high power density are achieved, a detailed analysis of the ZVS range has not been done.

In this paper, a ZVS three-phase inverter without any auxiliary circuits or additional sensors is proposed. The conventional continuous five-segment space vector PWM (SVPWM) is used. The switching frequency can be simply calculated, and the frequency variation range is narrow. The ZVS can be achieved within a wide range. An *LCL* filter and active damping are used to attenuate the high current ripples at the inverter side. This paper is organized as follows. The modulation scheme, ZVS condition, and the proposed control are explained in Section II. The design considerations of the filter parameters and the active damping method are analyzed in Section III. The simulation and experimental verification are presented in Section IV. The power loss analysis is discussed in Section V. Finally, Section VI gives the conclusion.

II. Operation Principle

The three-phase grid-connected VSI with an *LCL* filter configuration is shown in Fig. 1. L_1 is the inverter-side inductor and L_2 is the grid-side inductor. C is the filter capacitor. The inductor currents on both sides are i_{x1} ($x = a, b, c$) and i_{x2}, respectively. v_x is the grid phase voltage and $V_{\rm dc}$ is the dc voltage. Q_1–Q_6 are the six switches. The gate signals of two switches in a phase-leg are complementary.

The inverter-side inductor currents i_{x1} should be specifically designed to achieve ZVS. Note that i_{x1} is affected by the switching states of all the three phase-legs. In addition, the summation

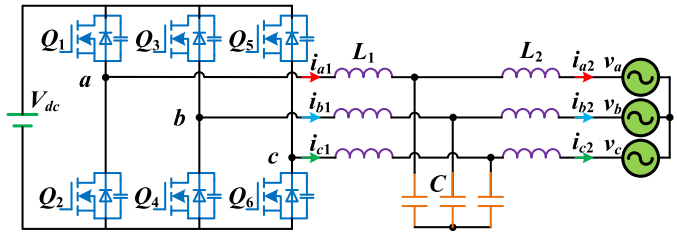

Fig. 1. Three-phase grid-connected VSI with *LCL* filter.

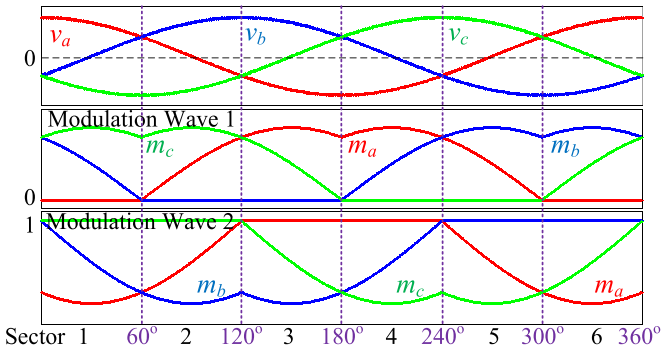

Fig. 2. Modulation waveforms of continuous five-segment SVPWM.

of the three-phase currents i_{x1} must be zero at any time instant. Due to these two constraints, a possible solution is to keep the switching state of one phase-leg constant during a certain time period and realize ZVS for the other two phase-legs. Therefore, an appropriate modulation strategy is necessary.

A. Analysis of Continuous Five-Segment SVPWM

Space vector modulation is used extensively in three-phase VSIs [28]. According to the distribution of the freewheeling switching states (zero vectors) in a switching cycle, the SVPWM has a couple of variations, including seven segments, continuous five segments, and DPWM. The seven-segment SVPWM is widely used because of its symmetry and low harmonics. However, all the switches are kept switching, which makes it hard for the ZVS realization of all the switches. In addition, the current distortion for the DPWM is too high to be adopted, especially for small inductance case. Therefore, the continuous five-segment SVPWM is used in this paper because only two phase-legs are switching at any time. Assuming the carrier wave is a triangle wave from 0 to 1, the modulation waves m_x are as shown in Fig. 2. The upper switch is ON when the corresponding modulation wave is lower than the carrier wave. There are two kinds of modulation waves for the five-segment SVPWM. The first one only uses the 111 (all top switches ON) vector as the zero vector. Whichever phase voltage is the highest among the three, the switching state of that phase-leg remains constant at 1. It is on the contrary for the second modulation wave. Actually, the two modulation waves have the same operating principle in view of the ZVS realization. In this paper, the first one is used.

Fig. 3 shows the PWM and phase currents i_{x1} and i_{x2} in sector 1 as an example. Since m_a is always zero, the top switch of phase a (Q_1) remains ON in sector 1; thus, ZVS is to be

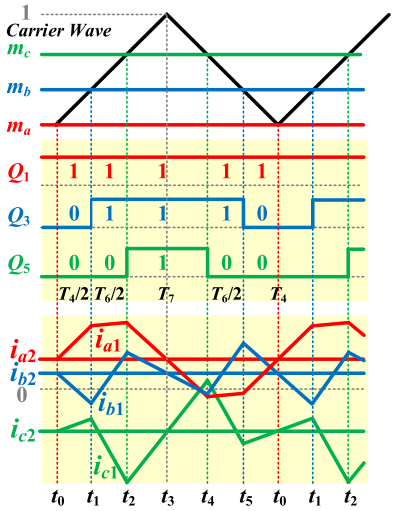

Fig. 3. Gate signals and inductor currents in sector 1.

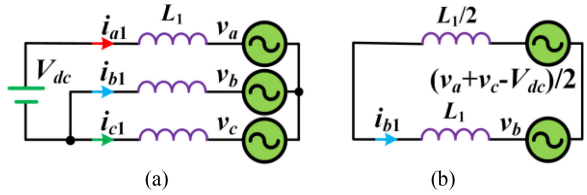

Fig. 4. (a) Equivalent circuit for the interval from t_5 to t_1 (100 switching state). (b) Thevenin's equivalent circuit.

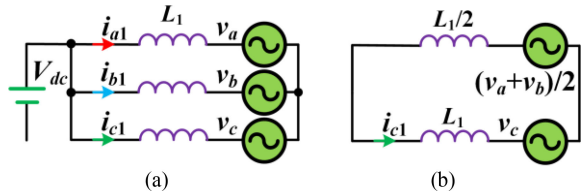

Fig. 5. (a) Equivalent circuit for the interval from t_2 to t_4 (111 switching state). (b) Thevenin's equivalent circuit.

achieved only for the switches in phases *b* and *c*. It can be seen from Fig. 2 that the modulation wave m_c is greater than m_b; thus, the five-segment vector sequence is $T_4/2$ (100), $T_6/2$ (110), T_7 (111), $T_6/2$, and $T_4/2$. The currents are shown at the bottom. The three straight lines represent the grid-side inductor current i_{x2}. Since the inductance of L_{x1} is designed to be small, the currents i_{x1} have high current ripples.

B. Inductor Current Ripple and ZVS Analysis

Three assumptions for the following analysis are given here. First, in a switching cycle, the grid voltages v_x can be treated as constant. Second, the voltage of *C* is equal to the corresponding grid voltage v_x. Third, the average current of i_{x1} in a switching cycle is equal to the instantaneous grid current i_{x2}.

Owing to the symmetry of the carrier wave, the relationships between i_{x1} and i_{x2} are as follows:

$$\begin{cases} i_{x1}(t_0) = i_{x2}, i_{x1}(t_0 - \Delta t) + i_{x1}(t_0 + \Delta t) = 2i_{x2} \\ i_{x1}(t_3) = i_{x2}, i_{x1}(t_3 - \Delta t) + i_{x1}(t_3 + \Delta t) = 2i_{x2}. \end{cases} \tag{1}$$

The requirements to achieve ZVS for phases *b* and *c* are as follows:

$$\begin{cases} i_{b1}(t_1) < -I_{\text{bias}} \\ i_{b1}(t_5) > I_{\text{bias}}; \end{cases} \quad \begin{cases} i_{c1}(t_2) < -I_{\text{bias}} \\ i_{c1}(t_4) > I_{\text{bias}} \end{cases} \tag{2}$$

where I_{bias} is the minimum current to charge/discharge the output capacitors C_{oss} of switching devices. It is a small current, especially for WBG devices. The specific design consideration is discussed in Section III.

Since i_{c2} is always lower than zero in sector 1, according to (1), if $i_{c1}(t_4)$ is greater than I_{bias}, then $i_{c1}(t_2)$ must be lower than $-I_{\text{bias}}$. However, the average current of phase *b* changes its polarity in sector 1. Therefore, the requirements to achieve ZVS can be rewritten as follows:

$$\begin{cases} i_{b1}(t_5) - i_{b1}(t_1) > 2(|i_{b2}| + I_{\text{bias}}) \\ i_{c1}(t_4) - i_{c1}(t_2) > 2(|i_{c2}| + I_{\text{bias}}). \end{cases} \tag{3}$$

The average voltage drops across L_2 are small; hence, the second assumption is true. The equivalent circuit from t_5 to t_1 is shown in Fig. 4. Based on Thevenin's theorem, the inductor current i_{b1} can be calculated as follows:

$$L_1 \frac{\Delta i_{b1}}{\Delta t} = \frac{v_a + v_c - 2v_b - V_{\text{dc}}}{3} = \frac{-3v_b - V_{\text{dc}}}{3} \tag{4}$$

$$\begin{cases} i_{b1}(t_5) = i_{b2} + (t_0 - t_5)(3v_b + V_{\text{dc}})/3L_1 \\ i_{b1}(t_1) = i_{b2} - (t_1 - t_0)(3v_b + V_{\text{dc}})/3L_1. \end{cases} \tag{5}$$

For phase *c*, the time interval between t_2 and t_4 should be studied. The equivalent circuit is shown in Fig. 5. Based on Thevenin's theorem, the inductor current i_{c1} can be expressed as follows:

$$L_1 \frac{\Delta i_{c1}}{\Delta t} = \frac{v_a + v_b - 2v_c}{3} = -v_c \tag{6}$$

$$\begin{cases} i_{c1}(t_2) = i_{c2} + (t_3 - t_2)\, v_c/L_1 \\ i_{c1}(t_4) = i_{c2} - (t_4 - t_3)\, v_c/L_1. \end{cases} \tag{7}$$

C. Variable Switching Frequency Control

Any of the above-mentioned time intervals can be easily expressed by the modulation wave, i.e.,

$$\begin{cases} t_0 - t_5 = t_1 - t_0 = m_b/2f_s \\ t_4 - t_3 = (1 - m_c)/2f_s \end{cases} \tag{8}$$

where f_s is the switching frequency.

Substituting (5), (7), and (8) into (3), the boundary switching frequency f_{sx} to achieve ZVS is given by

$$\begin{cases} f_{\text{sb}} < \dfrac{m_b(3v_b + V_{\text{dc}})}{6L_1(|i_{b2}| + I_{\text{bias}})} \\ f_{\text{sc}} < \dfrac{(m_c - 1)\, v_c}{2L_1(|i_{c2}| + I_{\text{bias}})}. \end{cases} \tag{9}$$

Assuming that the circuit parameters are given as listed in Table I, the boundary switching frequency variation in sector

TABLE I
CIRCUIT PARAMETERS TO CALCULATE BOUNDARY FREQUENCY

Item	Parameter
Grid phase voltage v_x	110 V RMS
DC voltage V_{dc}	350~400 V
Rated Power P_{max}	3.5 kW
Inductance L_1	10 μH
Power factor PF	1
Bias current I_{bias}	2 A

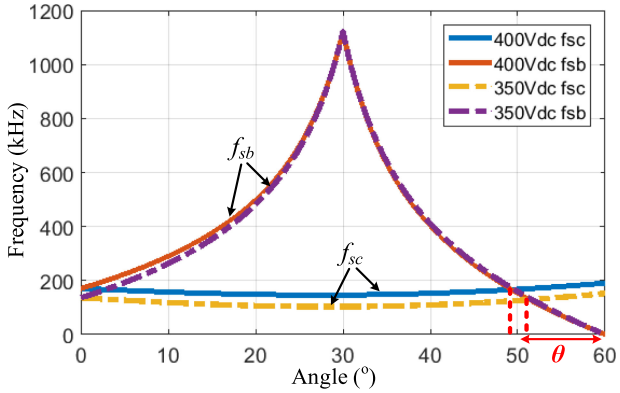

Fig. 6. Boundary frequency for phases b and c in sector 1.

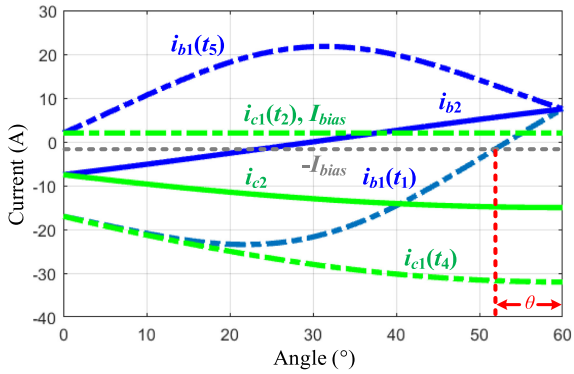

Fig. 7. Current ripple envelop line of i_{b1} and i_{c1} in sector 1.

1 can be plotted, as shown in Fig. 6. f_{sb} starts at the same value as f_{sc} but becomes much higher afterward for most of the time. During the last θ° (from around 50° to 60°), f_{sb} drops below f_{sc} and becomes zero at 60°. The reason is that both the modulation wave m_b and the time interval from t_5 to t_1 decrease to zero. To achieve ZVS for both phases, the lower boundary switching frequency should be chosen. However, when the angle is close to 60°, f_{sb} changes too much and approaches zero, which is unfeasible in practice. Therefore, regardless of the ZVS realization of phase b during the last θ°, only f_{sc} is chosen as the boundary switching frequency in sector 1.

By setting f_{sc} as the switching frequency, the current ripple envelop lines at 350-V dc are illustrated in Fig. 7. The bottom switch can achieve ZVS if the maximum current of i_{x1} is higher than I_{bias}, and the top switch can achieve ZVS if the minimum

TABLE II
THREE PHASE-LEGS' SWITCHING STATES IN A LINE CYCLE

Sector	1	2	3	4	5	6
Fixed switching state phase-leg	a	b	b	c	c	a
Non-ZVS switch in inverter mode	Q_3	Q_1	Q_5	Q_3	Q_1	Q_5
Non-ZVS angle	60-θ ~60	60~ 60+θ	180-θ ~180	180~ 180+θ	300-θ ~300	300~ 300+θ
f_s based on phase	c		a		b	
f_s equation	$\frac{(m_c-1)v_c}{2L_1(\lvert i_{c2}\rvert+I_{bias})}$		$\frac{(m_a-1)v_a}{2L_1(\lvert i_{a2}\rvert+I_{bias})}$		$\frac{(m_b-1)v_b}{2L_1(\lvert i_{b2}\rvert+I_{bias})}$	

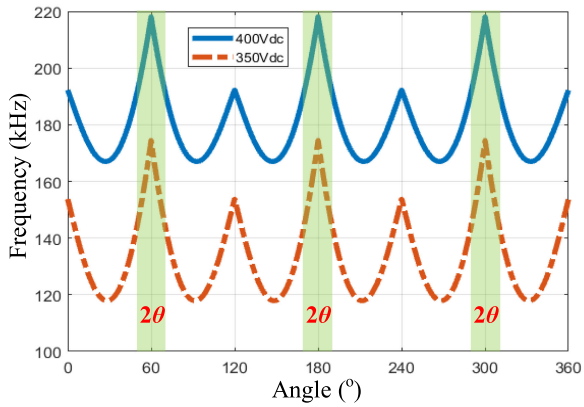

Fig. 8. Switching frequency variation in a line cycle.

current is lower than $-I_{\text{bias}}$. However, this is not a necessary condition because I_{bias} is designed to leave some margin. It can be seen that $i_{c1}(t_2)$ is kept constant as I_{bias} and $i_{c1}(t_4)$ are lower than $-I_{\text{bias}}$. Therefore, both switches in phase c can achieve ZVS. From about 52° to 60° (θ°), $i_{b1}(t_1)$ is greater than $-I_{\text{bias}}$; hence, the top switch Q_3 cannot achieve ZVS.

Sector 2 is symmetrical to sector 1, except that v_a and v_b exchange their roles. The voltage v_c is still the lowest among the three phase voltages. Therefore, the switching state of phase b remains constant, and the boundary switching frequency is still f_{sc} in (9). Similarly, ZVS cannot be fully achieved for phase a (Q_1) during the first θ° in sector 2. For the following sectors from 3 to 6, the three phase voltages keep exchanging positions, but the frequency calculation method is the same. It can be concluded as given in Table II.

Fig. 8 illustrates the switching frequency variation in a line cycle at different dc voltages. It can be seen that the frequency is continuous and symmetrical at each sector break. The maximum frequency occurs at 60°, 180°, and 300°. In the meantime, one of the switches cannot realize ZVS during the θ° on both sides of these angles.

The maximum and minimum switching frequencies in a line cycle at different dc voltages and powers are shown in Fig. 9. A lower dc voltage and a higher power lead to a lower frequency. The switching frequency variation ratio in a line cycle is around 1.5 times at any dc voltage or load condition. This is favorable compared with other wide frequency range methods

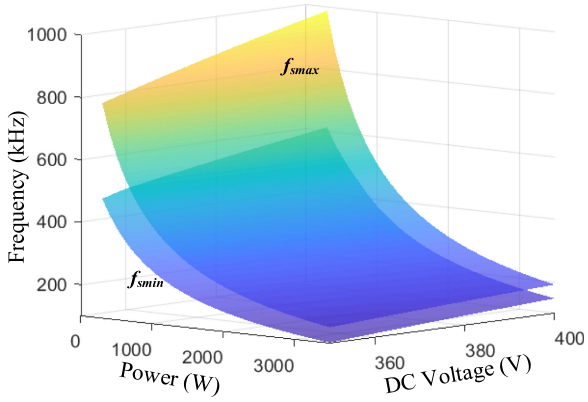

Fig. 9. Maximum and minimum switching frequencies at different dc voltages and powers.

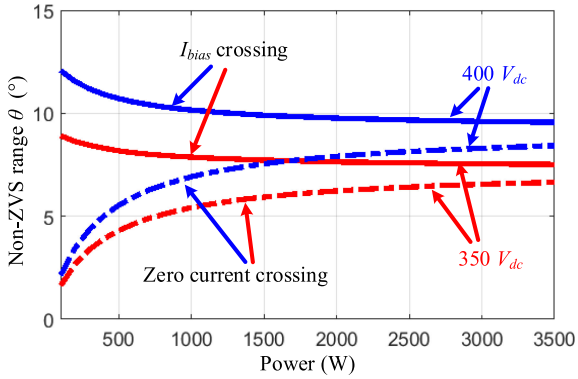

Fig. 10. Non-ZVS range in a sector at different powers and dc voltages.

whose driving circuits are difficult to be designed in practice. It should be noted that the actual non-ZVS range is smaller than θ because θ is defined at I_{bias} crossing. This is only a sufficient condition but not a necessary condition for ZVS. The relationship between ZVS current and power at different dc voltages is shown in Fig. 10. Only one switch cannot achieve ZVS during the $\theta°$ in any sector. A higher power and a lower dc voltage result in a smaller θ or a wider ZVS range. At a lower power and a higher dc voltage, the switching frequency becomes higher and the current ripple becomes lower; thus, the ZVS range decreases a little.

According to the switching frequency calculation equation, three-phase grid voltages and currents, as well as the modulation ratio information, are needed. For the conventional fixed switching frequency grid-connected inverter, grid voltages are also sampled to obtain the phase angle, and currents are needed for the closed-loop control. The modulation ratios can be acquired by the digital controller itself. Therefore, no additional sensor is needed to achieve the proposed variable frequency control. Both the modulation wave generation method and the closed-loop control are the same as the fixed frequency control. Only the carrier wave frequency or period is to be updated at the same time. The only limitation of this control strategy is that it is not suitable for non-unity power factor. The switching frequency variation becomes discontinuous when the current is not in phase with the modulation wave. However, it can also work

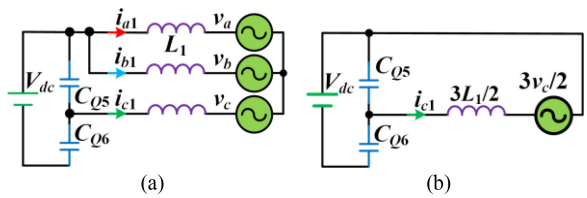

Fig. 11. (a) Equivalent circuit to achieve ZVS of Q_6 at t_4. (b) Thevenin's equivalent circuit.

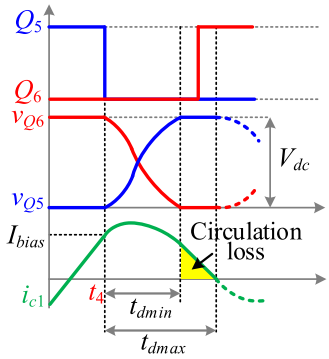

Fig. 12. Resonant waveform of the ZVS realization process.

in the PFC converter. The operation principle and the switching frequency calculation method are the same. Only the non-ZVS switches become the bottom ones.

III. Design Considerations

This section introduces a design example of a 3.5-kW inverter interfacing a 350–400-V dc with a 110-V ac grid. The minimum switching frequency is set at 100 kHz.

A. Bias Current and Inverter-Side Inductance Design

The inductance L_1 not only has an influence on the switching frequency but also affects I_{bias} and the dead time t_d selection. Thus, they should be designed together. The ZVS resonant process of Q_6 in sector 1 around t_4 is analyzed as an example. The equivalent circuit is shown in Fig. 11. C_{Q5} and C_{Q6} are the output capacitors of the switches Q_5 and Q_6. According to the equivalent circuit, the resonant process can be written as follows:

$$\begin{cases} v_{Q5}+v_{Q6}=V_{\text{dc}}, v_{Q6}\left(t_4\right)=V_{\text{dc}}, i_{c1}\left(t_4\right)=I_{\text{bias}} \\ i_{c1}=C_{\text{oss}}\left(\frac{dv_{Q5}}{dt}-\frac{dv_{Q6}}{dt}\right), \frac{3L_1 di_c}{2dt}+v_{Q5}+\frac{3v_c}{2}=0 \end{cases} \tag{10}$$

where v_{Qn} is its drain–source voltage. Thus, v_{Q6} and i_{c1} are given by

$$\begin{cases} i_{c1}=I_{\text{bias}}\cos\omega\left(t-t_4\right)+3C_{\text{oss}}v_c\omega\sin\omega\left(t-t_4\right) \\ v_{Q6}=V_{\text{dc}}-\dfrac{3v_c}{2}+\dfrac{3v_c}{2}\cos\omega\left(t-t_4\right) \\ \quad -\dfrac{3L_1 I_{\text{bias}}}{2}\omega\sin\omega\left(t-t_4\right). \end{cases} \tag{11}$$

The resonant process is shown in Fig. 12. At t_4, if i_{c1} is positive and large enough to fully charge and discharge the

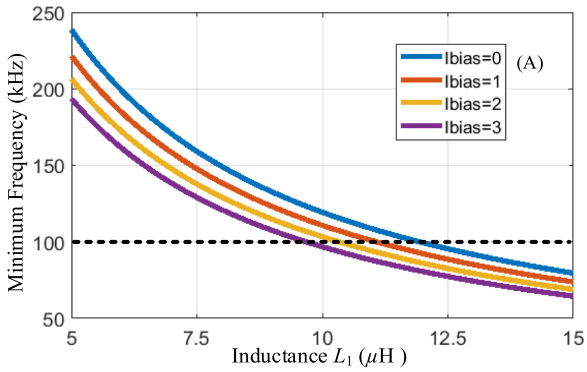

Fig. 13. Relationship between L_1 and $f_{s\min}$.

TABLE III
DEAD TIME SELECTION WITH DIFFERENT BIAS CURRENTS

I_{bias} (A)	L_1 (μH)	$t_{d\min}$ (ns)	$t_{d\max}$ (ns)
0	12	N/A	N/A
1	11.1	50	93
2	10.3	24	126
3	9.7	16	165

output capacitors of Q_5 and Q_6, the body diode of Q_6 can be turned-ON. Then, the current i_{c1} keeps decreasing linearly after the resonant process and becomes zero at $t_{d\max}$. The ZVS for Q_6 can be achieved if the driving signal is applied between $t_{d\min}$ and $t_{d\max}$. Otherwise, the output capacitors can be reversely charged and discharged after that. However, this time interval should be as short as possible to reduce the circulation loss; hence, I_{bias} should be carefully designed. On the other hand, to guarantee that the minimum switching frequency is 100 kHz, the relationship between L_1 and $f_{s\min}$ at different bias currents should be figured out. The frequency calculation equation uses 350-V dc voltage, 110-V ac voltage, and 3.5-kW power. The relationship is illustrated in Fig. 13. At 100 kHz, the higher the bias current is, the lower the inductance needs to be.

In this design example, an SiC MOSFET is used, whose C_{oss} is 60 pF. The worst case to achieve ZVS for Q_6 in sector 1 is when V_{dc} is 400 V and v_c is at its maximum voltage (angle is 0°). By substituting the parameters obtained from Fig. 13 into (11), the dead time range can be calculated as given in Table III. For WBG devices, a high switching speed may lead to voltage overshoot and cross-talk phenomena. Therefore, the switching speed should be limited by adjusting the driving circuit parameters. Meanwhile, the power loop parasitic inductance should be reduced, and a negative driving voltage is needed. The rise and fall times and the turn-ON and turn-OFF delays can be obtained from the device datasheet. Considering the propagation delay of the driving circuits and the tolerance of L_1, I_{bias} is designed as 2 A, and L_1 is 10.3 μH. The dead time is set to 100 ns.

B. LCL Filter and Active Damping Design

In order to attenuate the high current ripples and improve the grid current quality, an *LCL* filter is necessary. However, the design methodology is not the same as the conventional one. The reason why the switching frequency can be calculated according to the voltage and current sensor information is based on the assumptions used in the previous analysis. According to the assumptions, the voltage drop across the inductors L_2 should be low, and the reactive current generated by the capacitors C should be small. Since the impedance of inductors L_2 at line frequency f_g is generally small, the voltage drop compared with the grid voltage can always be ignored. The reactive current through L_2 is designed to be less than 2% of the active current so that the phase error can be neglected. The capacitance C can be calculated as follows:

$$v_x^2 2\pi f_g C < 2\% P_{\max}/3. \tag{12}$$

The capacitance is designed as 4.7 μF in this example. The current ripple attenuation is related to C and L_2. It is a second-order low-pass filter and can be expressed as follows:

$$\frac{i_{x2}(s)}{i_{x1}(s)} = \frac{1}{L_2 C s^2 + 1}. \tag{13}$$

The higher the frequency of the current ripple, the better it attenuates. The worst case in a line cycle occurs at the minimum switching frequency $f_{s\min}$. It can be seen from Fig. 7 that in sector 1, i_{b1} has the highest current ripple of about 40 A at $f_{s\min}$. If a maximum current ripple of 1 A is required, then the attenuation factor at $f_{s\min}$ should be 1/40 (or -32 dB). Therefore, the inductance L_2 is designed as 20 μH. Under other operating conditions, the grid-side current ripple is much lower because of a higher switching frequency.

Since the high current ripple component of i_{x1} is filtered out by the capacitors C, the conventional method of using damping resistors to eliminate the *LCL* resonance may cause an enormous amount of power loss. In this paper, a filter-based active damping is adopted [29]. It applies a notch filter to the modulation wave in order to cancel the resonant peak. It does not need any additional sensors, which is more cost-effective and flexible. The resonant angular frequency of the *LCL* filter can be expressed as follows:

$$\omega_{\text{res}} = \sqrt{(L_1 + L_2)/L_1 L_2 C}. \tag{14}$$

The transfer function of the notch filter in the s-domain can be written as follows:

$$N(s) = \frac{s^2 + \omega_{\text{res}}^2}{s^2 + k\omega_{\text{res}} s + \omega_{\text{res}}^2} \tag{15}$$

where k determines the width of the band-stop region. Considering the tolerances of the inductances, the capacitance, as well as the parasitic grid impedance, k can be chosen between 2 and 5. In this example, the resonant frequency is 28 kHz and k is designed as 3.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

To verify the parameter design and the performance of the inverter, simulation and experimental results are discussed in this section. The specification and the parameters are obtained from Section III and are given in Table IV.

Fig. 14 shows the simulation waveform in a line cycle at full load when the dc voltage is 350 V. In sector 1, phase a is not

TABLE IV
SPECIFICATIONS AND THE PARAMETERS OF THE INVERTER

Item	Parameter	Item	Parameter
V_{dc}	350~400 V	v_x	110 V RMS
P_{max}	3.5 kW	PF	1
L_1	10.3 μH	L_2	20 μH
C	4.7 μF	I_{bias}	2 A
f_{smin}	100 kHz	t_d	100 ns

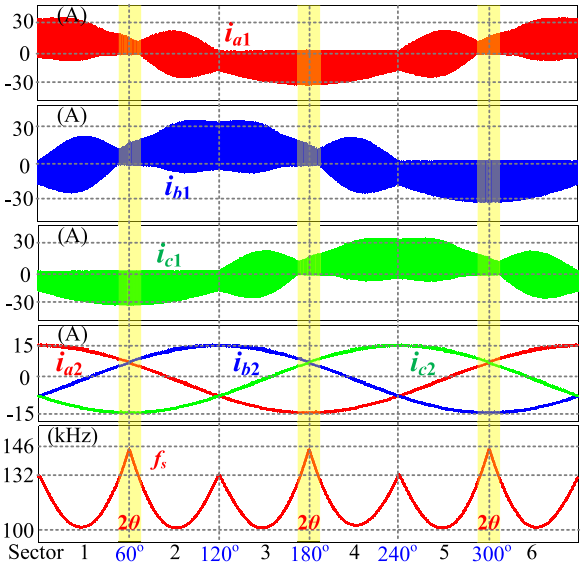

Fig. 14. Simulation waveform in a line cycle at 350-V dc full load.

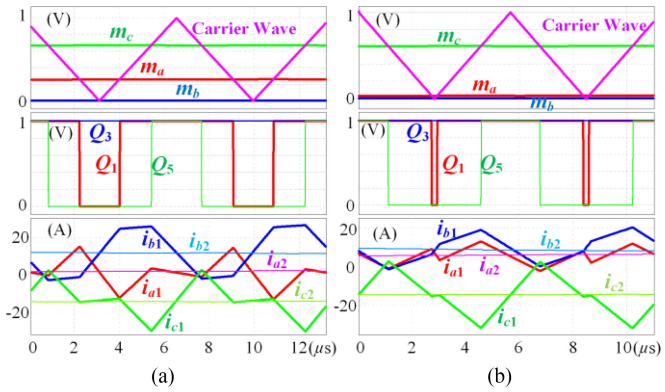

Fig. 15. Simulation waveform of a switching cycle in sector 2. (a) Around 90°. (b) Around 65°.

switching; hence, the shape of i_{a1} is not important. The envelop lines of i_{b1} and i_{c1} are almost the same as the prediction in Fig. 7. The small difference in i_{b1} at the end of sector 1 is depicted in Fig. 15(b). For the following sectors, the envelop lines of i_{x1} are just a duplication or mirror image of sector 1. For example, i_{a1} in sector 2 is a mirror image of i_{b1} in sector 1. It can be clearly seen that the peak current of i_{c1} is kept well at 2 A in sectors 1 and 2. i_{a1} in sectors 3 and 4, along with i_{b1} in sectors 5 and 6, is the same. Therefore, ZVS can be achieved

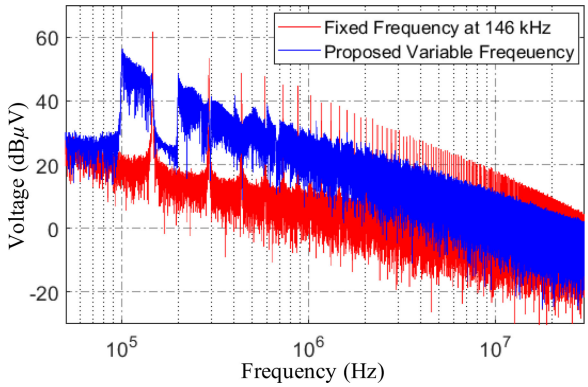

Fig. 16. EMI simulation results comparison between fixed frequency control and proposed control.

for all the switches, except in the shadowed region based on the aforementioned analysis. Although the current ripple is very high at the inverter side, the total harmonic distortion (THD) measured from the grid current i_{x2} is only 2.3% owing to high frequency attenuation. The minimum switching frequency is 100 kHz, and the maximum frequency is 146 kHz.

Fig. 15(a) shows the simulation waveforms in a switching cycle in the middle of sector 2, which are similar to that shown in Fig. 3. In sector 2, Q_3 is ON; thus, the current waveform of i_{b1} does not affect the ZVS realization. Only the switches in phases a and c are switching. At the turn-ON and turn-OFF instants of Q_1, i_{a1} is negative and positive, respectively. At the turn-OFF instant of Q_5, i_{c1} reaches its peak value of 2 A (I_{bias}). Therefore, ZVS can be achieved for all the switches in phases a and c. The waveforms in other sectors are similar, except the exchange of the three-phase sequence.

As depicted in Figs. 8 and 14, during the $\theta°$ on both sides of 60°, 180°, and 300°, one of the switches loses ZVS. Fig. 15(b) shows an example at around 65° in sector 2. During this interval, the modulation wave m_a is still low; hence, the pulsewidth for Q_2 is too short to generate a high current ripple for i_{a1}. Therefore, i_{a1} cannot become negative before Q_1 is turned-ON. Thus, Q_1 cannot achieve ZVS. However, as m_a increases, the current ripple of i_{a1} becomes higher. The ZVS for Q_1 can be achieved after $\theta°$. In a line cycle, the top switch of each phase loses ZVS for $\theta°$ twice ($2\theta°$). It should be noted that under this condition, although the minimum current of i_{a1} is still lower than zero, it does not occur at the turn-ON instant of Q_1. Therefore, the envelop line is a little different from the analysis depicted in Fig. 7.

The conducted EMI simulation follows the CISPR 22 standard. A comparison between the conventional fixed switching frequency control and the proposed control is made for the same circuit parameters. The fixed frequency is set as the maximum of the variable switching frequency at 146 kHz. A 10-pF capacitor is added between the drain of each device and the ground to simulate the capacitor between the thermal pad and the heatsink. Fig. 16 shows the simulation results at full load and 350-V dc. The EMI peak value occurs at the integral multiple of the switching frequency. For the conventional fixed switching frequency

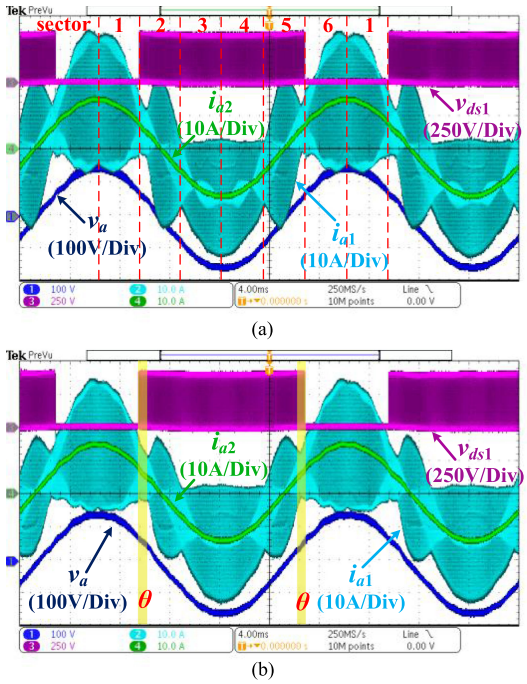

Fig. 17. Experiment waveforms of phase *a* in full load at 350- and 400-V dc. (a) At 350-V dc. (b) At 400-V dc.

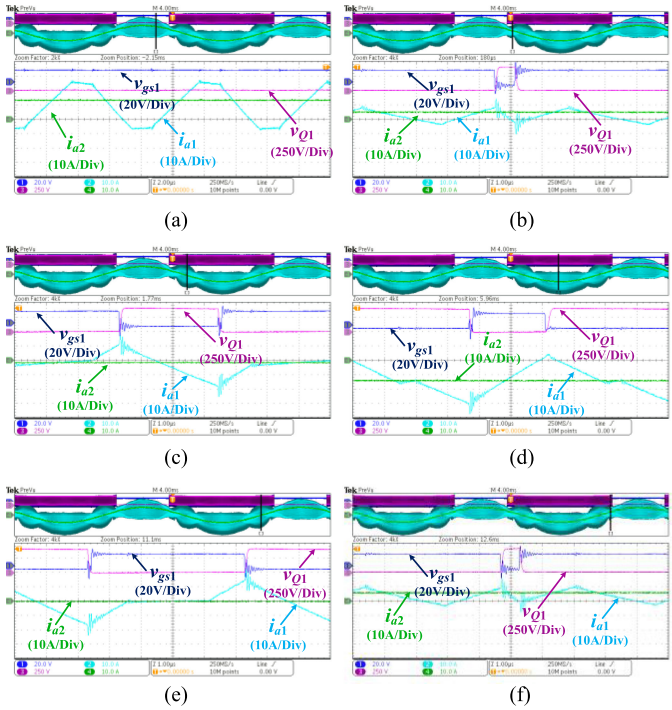

Fig. 18. ZVS and non-ZVS waveforms of top switch Q_1. (a) Not switching, (b) and (f) Non-ZVS, (c), (d) and (e) ZVS.

control, the noise concentrates on several specific frequencies. However, the proposed variable switching frequency can effectively distribute the noise spectrum and decrease the noise peak value. Therefore, a lower noise attenuation is needed, and the EMI filter size and cost can be reduced.

The experimental prototype is fabricated by using the SiC MOSFET C3M0065090J (900 V, 65 mΩ) as the switching device. DSP TMS320F28335 is the digital controller. The maximum switching frequency is set to 500 kHz to limit the switching loss when the load is lower than 20%. The sampling and control frequencies are constant and set to be 100 kHz.

The steady-state operating waveforms of phase *a* at 350- and 400-V dc full load are illustrated in Fig. 17. For phases *b* and *c*, the waveforms are almost the same. The grid current i_{a2} is in phase with the phase voltage v_a, and it is always the average of i_{a1}, which satisfies the third assumption. Compared with 350-V dc, the switching frequency at 400-V dc is higher; thus, the current ripple is smaller. The sector numbers are shown in Fig. 17(a). In sectors 3 and 4, when the phase current is the lowest, the bias current is well kept at 2 A. A small ripple is caused by the accuracy of the voltage- and current-sensing. Therefore, the ZVS of Q_1 and Q_2 can always be achieved in these two sectors. In sectors 1 and 6, when the phase current is the highest, the top switch Q_1 remains ON; hence, the ZVS is not a concern. In sectors 2 and 5, the envelop lines of i_{a1} are similar to that of i_{b1} in sector 1, as shown in Fig. 7. The current ripple of i_{a1} is mostly large enough to realize ZVS. However, at the beginning of sector 2 and at the end of sector 5, as shown in Fig. 17(b), the bottom envelop line is greater than -2 A. Thus, the top switch Q_1 may lose ZVS for about 10° in both sectors. It is the same with phases *b* and *c*.

The ZVS and non-ZVS waveforms of the top switch Q_1 at full load 400-V dc are shown in Fig. 18. The driving signal v_{gs1} and the drain–source voltage v_{Q1} are illustrated together to show the ZVS realization. The inverter-side current i_{a1} should be lower than -2 A at the turn-ON instant to achieve ZVS. It can be seen that ZVS cannot be achieved only in Fig. 18(b) and (f) because the modulation ratio is too small to produce enough current ripples. The non-ZVS range accounts for approximately 10° in each of the two sectors. From Fig. 18(c)–(e), ZVS can always be realized because i_{a1} is much lower than -2 A. The drain–source voltage v_{Q1} decreases to zero before the driving signal v_{gs1} is higher than the gate threshold (2 V). This can also be justified from v_{Q1} that it decreases to zero smoothly. However, from Fig. 18(c)–(e), since the turn-ON current i_{a1} is high, the junction capacitor is still discharged fast. From Fig. 18(b) and (f), it can be seen that v_{Q1} drops to zero sharply because the junction capacitor is shorted when the device is turned-ON. It should be noted that due to the assembly of the power stage, it is difficult to connect the probe directly to the gate pin of the device; hence, the driving signal before the gate resistor is measured. Therefore, it shows obvious ringing and resonance.

The bottom switch can achieve ZVS at any time in a line cycle using the proposed control. Fig. 19 shows the ZVS waveforms of the bottom switch in phase *a*. ZVS can be achieved on the condition that i_{a1} is greater than 2 A at the turn-ON instant. In Fig. 19(c) and (d), the peak current of i_{a1} is kept as 2 A on purpose to realize ZVS. The voltage v_{Q2} always decreases to zero before the driving signal v_{gs2} becomes higher than the gate threshold. In Fig. 19(a), (b), (e), and (f), i_{a1} is much higher than 2 A at the turn-ON instant so that the ZVS condition is fully met.

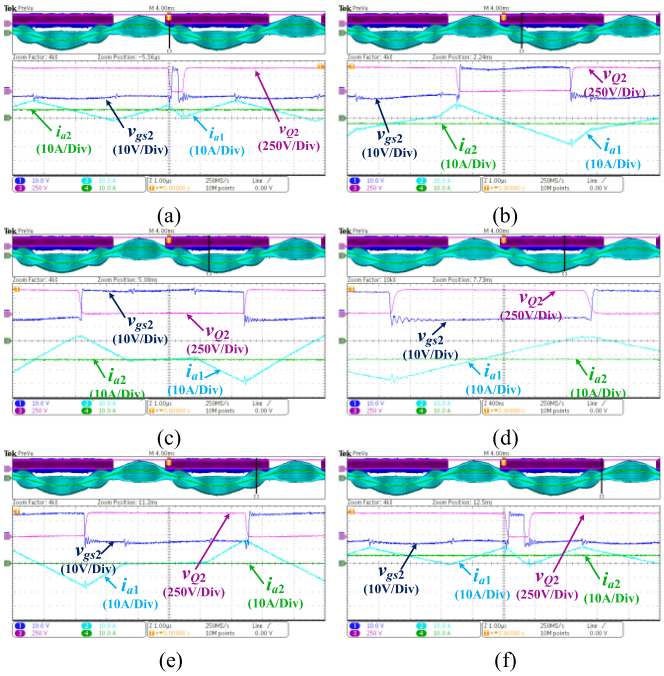

Fig. 19. ZVS waveforms of bottom switch Q_2. (a) to (f) ZVS waveform.

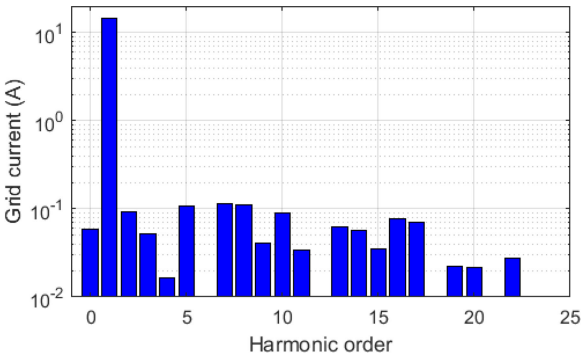

Fig. 20. Harmonic analysis of the grid current.

Due to the use of an autotransformer, the three-phase voltages are not exactly the same. The THD measured from the experimental waveform of i_{a2} is 3.2% at 350-V full load. The harmonics calculated from the waveform data are shown in Fig. 20. It can be seen that the current at the fundamental frequency is 15 A, and the harmonics are all lower than 0.12 A. If a lower THD is required, L_2 can be designed to be larger, without affecting the operation of the inverter and the proposed control strategy.

The dynamic response of the inverter is verified and shown in Fig. 21. The grid current step increases from 30% to full power. The grid current i_{a2} has a fast dynamic response and is always in phase with the grid voltage v_a. On the other hand, the switching frequency calculation also has a good performance. The bias current can be maintained well as 2 A before and after the transition. Therefore, ZVS can always be achieved, even in transients. The dynamic response proves that the conventional inverter closed-loop control combined with the proposed variable switching frequency technique has good stability.

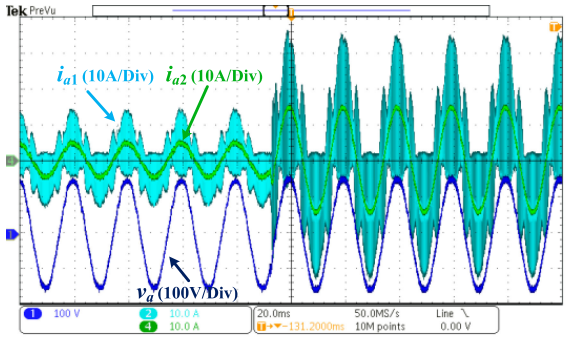

Fig. 21. Dynamic response of the grid current step-up change.

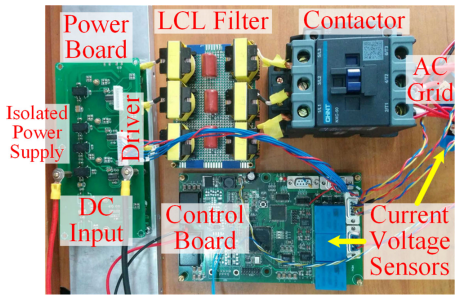

Fig. 22. Experiment prototype.

Fig. 22 shows the prototype photo. Since the thermal design of the surface-mounted device is difficult for the conventional printed circuit board (PCB), a single-layer metal-core PCB is adopted. It has a thin inner insulation layer. It can, therefore, be directly attached to the heatsink only with thermal grease. The surface-mounted SiC MOSFET and the decoupling capacitors can be simply soldered on the metal-core PCB. However, the driving circuit layout is difficult to implement on the single-layer PCB. Therefore, the driver board is designed on the conventional PCB mounted on top of the power stage through connectors. EI-33 ferrite core is used for all the inductors. It can be seen that the *LCL* filter size is much smaller compared with a conventional inverter having the same current rating.

With the help of the proposed control, a power density of approximately 3 kW/L can be achieved. Compared with the commercial inverter products that generally have a power density of 0.5 kW/L, the power density increases several times.

V. Power Loss Analysis

The total power loss includes switching devices' conduction and switching losses, inductors' core and copper losses, filter capacitors' losses, and the driving loss.

The device loss is analyzed first. Owing to the symmetrical structure, the conduction loss generated in any phase-leg is the same as in a line cycle. In addition, only one switch in a phase-leg conducts the phase current at any time. The total conduction loss can, thus, be simply calculated as follows:

$$P_{\text{cond}} = 3I_{x1,\text{rms}}^2 R_{ds(\text{ON})}. \tag{16}$$

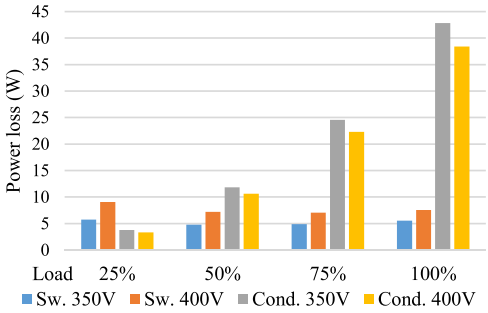

Fig. 23. Device losses breakdown.

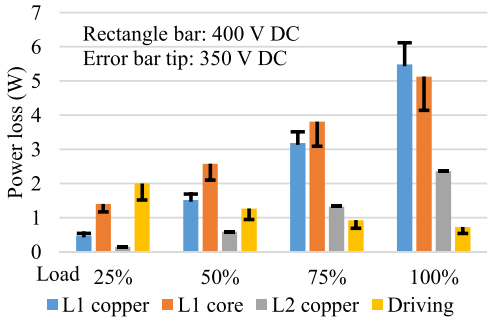

Fig. 24. Other major losses breakdown.

Here, $R_{ds(\mathrm{on})}$ is the device ON resistance and $I_{x1,\mathrm{rms}}$ is the rms value of the inverter-side inductor current i_{x1}. For a triangle current waveform, the rms current can be directly calculated based on its mean value and bias current. However, for the method discussed in this paper, the inverter-side current has four segments in a switching cycle, and the envelop lines in a line cycle are irregular. Therefore, it is very difficult to obtain an analytical expression between the inductor rms current and the grid current. The simplest and the most accurate way to calculate the conduction loss is to acquire the rms value directly from the simulation or experimental waveform data.

The total switching loss is the same in any sector. Thus, sector 1 is taken as an example. The switching state of phase *a* is constant; hence, it has no switching loss. Both switches of phases *b* and *c* have turn-OFF loss. The top switch of phase *b* also has turn-ON loss during the last several degrees. The turn-ON and turn-OFF switching energies versus different drain currents are obtained from the datasheet and curve-fitted in MATLAB. The variable switching frequency f_s and the envelop lines of i_{b1} and i_{c1} in sector 1 can also be calculated, which have been discussed in Section II. The current envelop lines are actually the turn-ON and turn-OFF currents. Therefore, substituting the envelop lines into the curve-fitting equation leads to the switching energy at different times. After it is multiplied by the corresponding switching frequency, the total switching loss can be acquired by the summation of the results.

The device loss breakdown at different dc voltages and load conditions is shown in Fig. 23. At 400-V dc, the current ripple of i_{x1} is smaller than that at 350 V; thus, the conduction loss at 400 V is lower. Although the switching frequency at light load is much higher than that at full load, the turn-OFF current is also lower. Therefore, the switching loss at different loads does not have a large difference. Compared with 350 V, the switching frequency at 400 V is higher and the turn-OFF voltage is also higher; thus, the total switching loss is always higher. At light load, the switching loss is a little higher than the conduction loss, but as the power goes up, the switching loss decreases gradually, and the conduction loss increases dramatically.

Since the grid-side current i_{x2} has tiny current ripples and the filter capacitors also have a very low equivalent series resistance (ESR), the core loss of L_2 and the capacitors' loss can be neglected for the analysis. The loss calculations for the core and copper loss of L_1, the copper loss of L_2, and the driving loss are discussed in the following. Fig. 24 illustrates other major losses' breakdown at different loads and dc voltage conditions. The rectangular bars represent the power loss at 400-V DC, and the error bars represent the loss differences between 350 and 400 V. The current i_{x1} has high-frequency components; hence, the copper loss of L_1 should be calculated at different frequencies due to the skin effect. It can be expressed as follows:

$$P_{L1,\mathrm{copper}} = \sum_f I_{x1,f}^2 R_{L1,f} \tag{17}$$

where $I_{x1,f}$ is from the Fourier transformation of i_{x1}. It mainly contains line frequency and switching frequency components. The ESR at different frequencies $R_{L1,f}$ can be measured with an impedance analyzer. However, the copper loss of L_2 is much easier to calculate because i_{x2} almost only contains the line frequency component. The copper loss of L_2 is the same at 350- and 400-V dc.

The core loss of L_1 is calculated using the generalized Steinmetz equation [30] due to the irregular current. The simulation data of i_{x1} as well as the core loss parameters are taken as the input of the code. It uses the difference of the inductor current and the step time to calculate the core loss. Although the current ripple is high, ferrite material is used as the core. The core loss is, therefore, relatively low.

The driving loss can be easily calculated because at any time only four devices are switching. It is given by

$$P_{\mathrm{drv}} = 4\left(V_{\mathrm{drv}+} - V_{\mathrm{drv}-}\right) Q_g \overline{f_s} \tag{18}$$

where $V_{\mathrm{drv}+}$ and $V_{\mathrm{drv}-}$ are the positive and negative voltages of the driving voltage, respectively, Q_g is the total gate charge of each device at a given driving voltage, and $\overline{f_s}$ is the average of the variable switching frequency in a line cycle. Owing to the low Q_g of the SiC mosfet, although the switching frequency is up to 450 kHz at 25% load, the total driving loss is still only 2 W.

The conversion efficiency measured with a power analyzer is shown in Fig. 25. The control power is not added to the power loss. The calculated efficiency is included as comparison. The loss difference is a little higher at heavy load possibly due to the device temperature rise. The peak efficiency is 98.7% at around

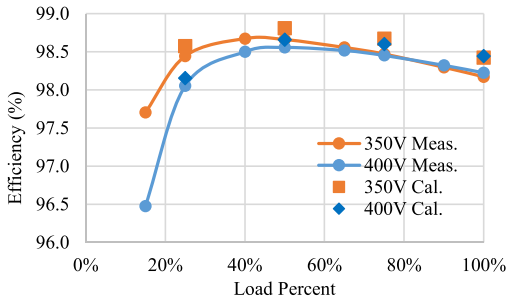

Fig. 25. Measured and calculated efficiency curves at different voltages.

50% load. The efficiency at light load is lower at 400-V dc than that at 350-V dc because of a higher switching loss, but when the load is higher than 80%, the efficiency at 400 V becomes a little higher owing to a lower conduction loss. It should be noted that for commercial products, such as solar inverters and battery storage inverters, the California Energy Commission (CEC) or European efficiency can also achieve 97%, and some are even 98%. Therefore, the efficiency only increases a little, but the switching frequency and the power density are greatly improved.

VI. Conclusion

This paper proposes a variable switching frequency SVPWM control for a three-phase grid-connected inverter. The operating principle, the inductor current ripple, and the ZVS condition are analyzed in detail. Due to the high current ripples at the inverter side, an *LCL* filter is needed. To avoid the resonance of the filter and to reduce the losses, the active damping technique is adopted. The design considerations of the filter and the active damping parameters are discussed. The simulation and experimental results of a 3.5-kW prototype using SiC MOSFETs are shown to verify the proposed control method. The major advantages are as follows.

1) The frequency variation range in a line cycle is only about 1.5 times under any operating condition, in facing load and voltage variations.
2) ZVS can be obtained over a wide range without using any additional sensors, auxiliary circuits, or current ZCD circuits.
3) The power density is high owing to the high switching frequency and low inductance of the filter.
4) The conversion efficiency is high.
5) A good dynamic response can be achieved with the proposed method.

References

[1] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.
[2] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep.–Oct. 2005.
[3] X. Liu, P. Wang, and P. C. Loh, "A hybrid AC/DC microgrid and its coordination control," *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 278–286, Jun. 2011.
[4] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sep. 2016.
[5] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 799–807, Sep. 2016.
[6] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2208–2219, May 2014.
[7] J. A. Anderson, C. Gammeter, L. Schrittwieser, and J. W. Kolar, "Accurate calorimetric switching loss measurement for 900 V 10 mΩ SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 8963–8968, Dec. 2017.
[8] C. M. Wang, C. H. Su, M. C. Jiang, and Y. C. Lin, "A ZVS-PWM single-phase inverter using a simple ZVS-PWM commutation cell," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 758–766, Feb. 2008.
[9] X. Yuan and I. Barbi, "Analysis, designing, and experimentation of a transformer-assisted PWM zero-voltage switching pole inverter," *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 72–82, Jan. 2000.
[10] J. L. Russi, M. L. da Silva Martins, and H. L. Hey, "Coupled-filter-inductor soft-switching techniques: Principles and topologies," *IEEE Trans. Ind. Electron.*, vol. 55, no. 9, pp. 3361–3373, Sep. 2008.
[11] W. Yu, J. S. Lai, and S. Y. Park, "An improved zero-voltage switching inverter using two coupled magnetics in one resonant pole," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 952–961, Apr. 2010.
[12] C. M. de Oliveira Stein, H. A. Grundling, H. Pinheiro, J. R. Pinheiro, and H. L. Hey, "Zero-current and zero-voltage soft-transition commutation cell for PWM inverters," *IEEE Trans. Power Electron.*, vol. 19 no. 2, pp. 396–403, Mar. 2004.
[13] R. C. Beltrame, J. R. Zientarski, M. L. Martins, and J. R. Pinheiro, "Simplified zero-voltage-transition circuits applied to bidirectional poles: Concept and synthesis methodology," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1765–1776, Jun. 2011.
[14] D. M. Divan, "The resonant DC link converter—A new concept in static power conversion," *IEEE Trans. Ind. Appl.*, vol. 25, no. 2, pp. 317–325, Mar./Apr. 1989.
[15] R. Gurunathan and A. K. S. Bhat, "Zero-voltage switching DC link single-phase pulsewidth-modulated voltage source inverter," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1610–1618, Sep. 2007.
[16] C. Du, D. Xu, N. He, and N. Zhu, "Modeling and optimization of a zero-voltage switching inverter for high efficiency and miniaturization," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 150–163, Jan. 2017.
[17] Y. Chen *et al.*, "A ZVS grid-connected full-bridge inverter with a novel ZVS SPWM scheme," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3626–3638, May 2016.
[18] R. Li and D. Xu, "A zero-voltage switching three-phase inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1200–1210, Mar. 2014.
[19] J. W. Kim, S. M. Choi, and K. T. Kim, "Variable on-time control of the critical conduction mode boost power factor correction converter to improve zero-crossing distortion," in *Proc. Int. Conf. Power Electron. Drive Syst.*, Nov. 2005, pp. 1542–1546.
[20] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.
[21] Q. Zhang, H. Hu, D. Zhang, X. Fang, Z. J. Shen, and I. Bartarseh, "A controlled-type ZVS technique without auxiliary components for the low power DC/AC inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3287–3296, Jul. 2013.
[22] D. Jiang and F. Wang, "Variable switching frequency PWM for three-phase converters based on current ripple prediction," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4951–4961, Nov. 2013.
[23] Z. Liu, Z. Huang, F. C. Lee, and Q. Li, "Digital-based interleaving control for GaN-based MHz CRM totem-pole PFC," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 808–814, Sep. 2016.
[24] C. Marxgut, F. Krismer, D. Bortis, and J. W. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[25] D. Bortis, D. Neumayr, and J. W. Kolar, "$\eta\rho$-Pareto optimization and comparative evaluation of inverter concepts considered for the Google Little Box Challenge," in *Proc. IEEE 17th Workshop Control Model. Power Electron.*, 2016, pp. 1–5.

[26] D. Zhang, Q. Zhang, H. Hu, A. Grishina, J. Shen, and I. Batarseh, "High efficiency current mode control for three-phase micro-inverters," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 892–897.
[27] Z. Huang, Z. Liu, F. C. Lee, Q. Li, and F. Xiao, "Critical-mode-based soft-switching modulation for three-phase inverters," in *Proc. IEEE Conf. Energy Convers. Congr. Expo.*, Oct. 2017, pp. 167–174.
[28] E. R. C. da Silva, E. C. dos Santos, and B. Jacobina, "Pulsewidth modulation strategies," *IEEE Ind. Electron. Mag.*, vol. 5, no. 2, pp. 37–45, Jun. 2011.
[29] J. Dannehl, M. Liserre, and F. W. Fuchs, "Filter-based active damping of voltage source converters with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3623–3633, Aug. 2011.
[30] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, 2002, pp. 36–41.

Jianliang Chen (S'15) received the B.S. degree in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2014, where he is currently working toward the Ph.D. degree.

From 2017 to 2018, he was a Visiting Student with CURENT, University of Tennessee, Knoxville, TN, USA. His research interest includes high power density converters.

Deshang Sha (M'09–SM'17) received the M.S. degree from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2001, and the Ph.D. degree from the Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, China, in 2005.

Since 2008, he has been with the Beijing Institute of Technology, Beijing, where he is currently an Associate Professor with Tenure. From 2012 to 2013, he was a Visiting Professor with VT FEEC, Blacksburg, VA, USA. He has authored over 100 papers and two books in the field of power electronics. His research interests include high-efficiency power conversion.

Jiankun Zhang received the B.S. and M.S. degrees, both in electrical engineering, from the Beijing Institute of Technology, Beijing, China, in 2014 and 2016, respectively, where he is currently working toward the Ph.D. degree in power electronics.

His research interest includes power electronic conversion.

Xiaozhong Liao (M'09) received the B.S. and M.S. degrees in electrical engineering from Tianjin University, Tianjin, China, in 1982 and 1984, respectively, and the Ph.D. degree from the Beijing Institute of Technology (BIT), Beijing, China, in 2004.

She is currently a Professor with BIT. Her research interest includes power electronics control.