Letters

A Self-Balancing Five-Level Boosting Inverter With Reduced Components

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***Abstract*—Two-Stage boosting multilevel inverters (MLIs), which are highly suitable for photovoltaic power plants, are known to suffer because of the high voltage stress on the switches of second stage. One of the ways to confront this issue is through eliminating the front-end booster. However, this leads to increased structural and control complexity of the resulting integrated boosting MLI. This letter presents a single-stage boosting MLI requiring lesser number of switches, diodes, and capacitors for renewable power generation applications. It requires nine switches and only one capacitor for five-level voltage generation. The topology has inherent self-balancing capability, thereby does not need additional balancing circuitry. The proposed topology has a uniform peak inverse voltage stress on the switches of value equal to the input dc voltage. A less complicated logic-form-equations-based gating pulse generation scheme is designed for enabling the proposed MLI to maintain its capacitor voltage. Further, a comparative study with state-of-the-art topologies is carried out to demonstrate the superior performance of the proposed topology. Finally, the feasibility of the proposed topology is validated through experimental tests and the corresponding results are elucidated.**

***Index Terms*—Multilevel inverter (MLI), power quality, single stage, step up.**

I. Introduction

THE key drivers behind the increasing concern toward generating green power from renewable sources such as photovoltaics and wind farms are the depleting fossil fuels and increased environmental concern. Furthermore, it is imperative to employ power electronic converters in order to efficiently harness such green power. Among the many varieties of converters, multilevel inverters (MLIs) are widespread due to their attractive features of reduced dv/dt, improved waveform quality, and reduced power losses [1], [2]. A few of the classic topologies that are majorly used are cascaded H-bridge (CHB), neutral point clamped, and flying capacitor converters. However, as the number of voltage level increases, these topologies suffer from several drawbacks, such as dc-link capacitor voltage imbalance,

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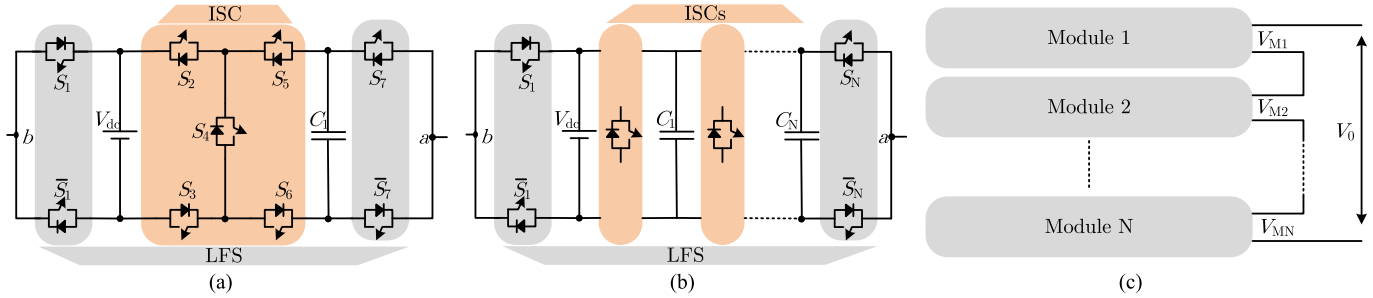


Fig. 1. (a) Proposed 5L boosting MLI. (b) Proposed extension M1. (c) Proposed extension M2.

5) four out of nine switches operate at fundamental frequency (50 Hz) and thereby leads to reduced switching losses.

The operation of the proposed topology is validated through experiments and the results are presented. And its pertinent characteristics are illustrated through a detailed component count based comparative study and cost analysis.

II. Proposed Step-Up Inverter Topology

A. Circuit Description

The proposed single-phase five-level (5L) boosting inverter is shown in Fig. 1(a). It consists of nine power switches, one SC, and a single dc source of magnitude $V_{\rm dc}$. The arrangement of switches S_2, S_3, S_4, S_5, and S_6 interconnecting the dc source and SC is referred to as an intermediate switching cell (ISC). The remaining four switches ($S_1, \bar{S}_1, S_7$, and $\bar{S}_7$) operate only once in every half-cycle of the fundamental voltage and thus are termed as line frequency switches (LFSs). It is evident that only one dc supply is employed for the 5L voltage generation. A photovoltaic cell/array, EV battery, or fuel cell can act as such dc supply. Besides, the proposed circuit arrangement exhibits a uniform blocking voltage across all the switches and has a voltage boosting factor (VBF) of two. Unlike many other structures wherein an H-bridge is used for the polarity generation, the proposed architecture has an inherent voltage reversal capability. The voltage across the SC is balanced around a voltage of magnitude $V_{\rm dc}$ without any need for sensors, and thus, makes the proposed topology cost-effective.

Further, with the proposed 5L basic unit, the number of voltage levels ($N_{\rm L}$) can be increased in two ways. First, by appending additional ISCs and SCs referred to as Method-1 (M1) [refer Fig. 1(b)]. Second, by cascading a number of 5L units referred to as Method-2 (M2) [refer Fig. 1(c)], the resulting configuration has a higher $N_{\rm L}$ and VBF. Such an arrangement is highly suitable for the interconnection of multiple dc supplies (renewable sources). The relation between number of switches ($N_{\rm sw}$), number of SCs ($N_{\rm cap}$), $N_{\rm L}$, VBF, number of modules ($N_{\rm M}$), and number of ISCs ($N_{\rm ISC}$) is given as

$$\text{M1} \Rightarrow \begin{cases} N_{\rm L} = 3 + 2N_{\rm ISC} \\ N_{\rm sw} = 4 + 5N_{\rm ISC} \\ N_{\rm cap} = N_{\rm ISC} \\ \text{VBF} = 1 + N_{\rm ISC} \end{cases} \quad \text{M2} \Rightarrow \begin{cases} N_{\rm L} = 1 + 4N_{\rm M} \\ N_{\rm sw} = 9N_{\rm M} \\ N_{\rm cap} = N_{\rm M} \\ \text{VBF} = 1 + N_{\rm M}. \end{cases} \tag{1}$$

TABLE I
Switching States for the Proposed 5L Inverter

$v_{\rm ab}$	S_1	S_2	S_3	S_4	S_5	S_6	S_7	C_1
$2V_{\rm dc}$	0	1	0	1	0	1	1	Discharging
$V_{\rm dc}$	0	1	1	0	1	1	1	Charging
0	0	0	1	0	0	1	0	No Effect
0	1	1	0	0	1	0	1	No Effect
$-V_{\rm dc}$	1	1	1	0	1	1	0	Charging
$-2V_{\rm dc}$	1	0	1	1	1	0	0	Discharging

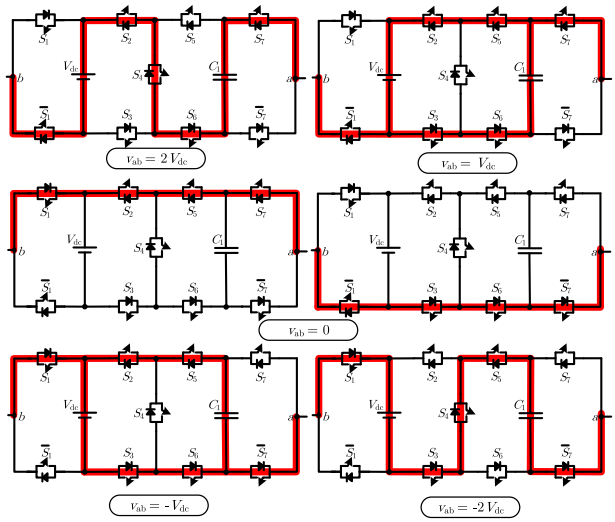


Fig. 2. Active switches for each of the output voltage levels.

B. Pulsewidth Modulation Strategy

The switching combination required for the generation of a 5L output voltage is listed in Table I. The entry "1" indicates that a particular switch is ON and "0" indicates the OFF condition. The table also indicates the effect of each of the voltage levels on the SC voltage. The current path and the active switches for each level are shown in Fig. 2. It is essential to produce appropriate gating signals in order to synthesize the output voltage with the desired steps. For this, two level-shifted high-frequency carriers ($v_{\rm cr1}$ and $v_{\rm cr2}$) and a single fully rectified signal of the sinusoidal reference ($v_{\rm ref} = V_{\rm m} \sin \omega t$) are employed [refer Fig. 3]. For the derivation of switching functions (SFs), suitable logic operations are performed on the comparator outputs $v_{\rm comp1}$ and $v_{\rm comp2}$. A zero crossing detector ($Z_{\rm c}$) defined as $Z_{\rm c} = 1$ for $v_{\rm ref} > 0$ is required for the construction of the SFs. The derived SFs are

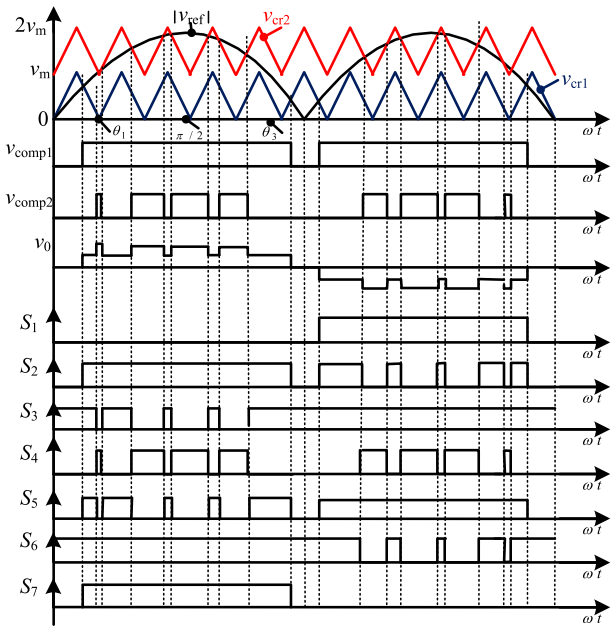


Fig. 3. Gating pulse generation process.

as follows:

$$\begin{aligned} S_1 &= v_{\text{comp1}} \times \bar{Z}_{\text{c}} \\ S_2 &= v_{\text{comp1}} \times Z_{\text{c}} + \bar{v}_{\text{comp2}} \times \bar{Z}_{\text{c}} \\ S_3 &= \bar{v}_{\text{comp2}} \times Z_{\text{c}} + \bar{Z}_{\text{c}} \\ S_4 &= v_{\text{comp2}} \\ S_5 &= \bar{v}_{\text{comp2}} \times Z_{\text{c}} + v_{\text{comp1}} \times \bar{Z}_{\text{c}} \\ S_6 &= Z_{\text{c}} + \bar{v}_{\text{comp2}} \times \bar{Z}_{\text{c}} \\ S_7 &= v_{\text{comp1}} \times Z_{\text{c}}. \end{aligned} \tag{2}$$

C. Capacitor Voltage Balancing

As evident from Fig. 2, during levels $\pm V_{\text{dc}}$, the dc source and the SC are connected in parallel. Considering the parasitics of the switches involved in the charging path to be low, the SC can be assumed to instantaneously charge up to the value of the input dc source, whereas for levels $\pm 2V_{\text{dc}}$, the SC is connected in series with the dc source across the load. Therefore, the energy supplied by the SC during these intervals results in the discharge of the SC. The minimum value of the capacitance required to permit an acceptable voltage ripple (ΔV) for a given load resistance (R_0) and fundamental output voltage frequency (ω_0) is as follows:

$$C_{\text{min}} = \frac{2V_{\text{dc}}}{\omega_0 R_0 \Delta V} \times (\theta_3 - \theta_1). \tag{3}$$

III. Comparative Assessment of the Proposed 5L Boosting Inverter

In order to comprehensively attest the illustrious features of the proposed topology, it has been compared against various other classic benchmarked circuits and recent state-of-the-art topologies. The comparison is performed in terms of N_{sw}, number of gate drivers (N_{driver}), number of diodes (N_{diode}), number of dc sources (N_{source}), number of capacitors (N_{cap}), and total blocking voltage (TBV) in per unit (p.u.)

TABLE II
Component Count Comparison of the Proposed MLI With Other Boosting Topologies

MLI type	N_{L}	N_{sw}	N_{driver}	N_{diode}	N_{source}	N_{cap}	TBV (p.u.)	PIV (p.u.)	Efficiency
[12]	5	12	12	12	1	2	20	1	96.7
[13]	7	16	14	16	1	2	16	2	93.1
[14]	5	6	6	8	1	2	8	1	97.01
[15]	5	7	7	10	1	2	9	1	96.8
[16]	5	9	8	10	1	1	9	1	97.4
[17]	5	6	6	8	1	1	12	2	95.8
[18]	5	6	6	7	1	1	11	2	98.1
[19]	5	8	8	8	2	-	12	2	97
Proposed	5	9	9	9	1	1	9	1	97.91

As can be seen from Table II, topology in [19] requires two isolated dc sources to generate a 5L output voltage, whereas the proposed circuit requires only one dc source. It can be observed that the proposed topology requires only one capacitor, which is the least among all, and thus, resulting in higher reliability and lower stored energy as well. The TBV of the proposed topology, that in [15] and [16], is the second least in comparison with others. Overall, the proposed topology requires a lesser number of switches and zero diodes, whereas a majority of rest of the topologies employ additional diodes.

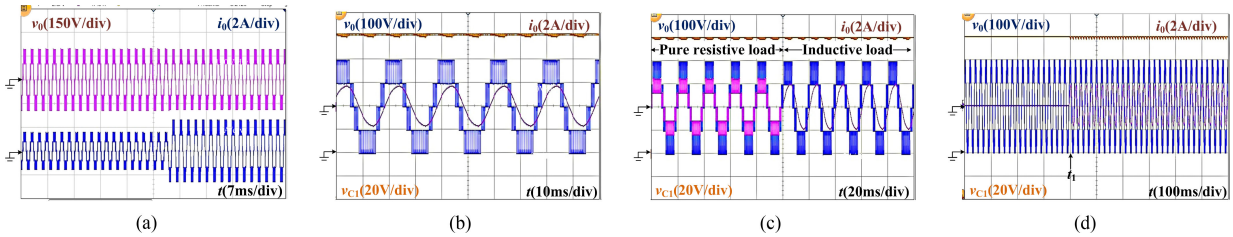
It is worth mentioning that, except for the proposed topology and that in [16], the rest of the boosting topologies in Table II exhibit non-uniform blocking voltages. In other words, the PIV of few of the switches in these circuits is equal to voltage gain times the input dc voltage. Therefore, in order to employ identical voltage rated switches, two or more such devices are to be connected in series due to their structural constraints unlike the proposed topology and that in [16], wherein the PIV of all the switches is only V_{dc}. However, the usage of a bipolar switching device in [16] limits its regenerative capability. Using the method described in [20], the theoretical efficiency of the topologies is evaluated. Owing to the lesser component count and voltage stresses, the proposed topology's efficiency value is comparable with other recent topologies.

Needless to say that the distinctive merits of an MLI topology cannot be assessed adequately only through the part count comparison. This is due to the overlooking of various cost influencing factors, which profoundly dictates the overall cost of the inverter. Therefore, it is essential to evaluate and thereby attest the merits of the MLI through a comprehensive cost analysis. In order to demonstrate the lucrative merits of the proposed topology, a case study example of a 2 kW, with 200 V input voltage is considered. The generic rating of the switches, capacitors, and diodes is chosen in accordance with the structure of the various boosting topologies under consideration. The resulting cost for each of the topologies is enlisted in Table III. It is to be noted here that the above-mentioned cost evaluation assigns an equal importance to number of components, TBV and PIV while considering no voltage rating margins. Although the cost

TABLE III
PRICE COMPARISON OF THE PROPOSED MLI WITH OTHER RECENT SINGLE DC SOURCE BASED BOOSTING TOPOLOGIES

Part	Part number	Ratings	Unit price*($)	[12]	[13]	[14]	[15]	[16]	[17]	[18]	Proposed
MOSFETs	IRFP240PBF	200 V, 20 A	2.1	10	14	4	5	9	2	2	9
	IRFP350PBF	400 V, 20 A	2.97	2	2	2	2	-	4	4	-
Diodes	STPS20M200ST	200 V, 20 A	3.9	-	-	2	4	1	2	1	-
Capacitor	LLG2D222MELCM0	200 V, 2.2 mF	6	2	2	2	2	1	1	1	1
Gate driver	IR2110	-	1.8	12	14	6	7	9	6	6	9
Total cost ($)				60.54	72.54	44.9	56.6	45	40.68	36.78	41.1

Courtesy: www.digikey.in, www.galco.com: * The prices may vary based on market growth.



(a) (b) (c) (d)

Fig. 4. Experimental results. (a) Output voltage and current waveforms for step change in pure resistive load from 50 to 30 Ω. (b) Output with resistive inductive load of 50 Ω and 70 mH. (c) Output for dynamic change in load PF. (d) Output for step change in load.

of the proposed topology is lower than most of the other circuits, it is slightly higher than the topologies in [17] and [18] for 5L operation. On the other side, for higher voltage levels, the PIV of circuit in [17] limits the selection of an appropriate power switches due to the usage of an H-bridge, and hence is not well-suited for high-voltage applications. Further, the asymmetric dc source based circuit in [18] has inherent bipolar voltage level generation capability and is recommended for higher number of levels. Nevertheless, it still needs two switches (interconnecting the left and right SC units) to be rated for total load voltage. As a result, it has a higher TBV than the proposed topology. For example, the TBV of circuit in [18] and the proposed topology [see Fig. 1(c)] is 44 and 36, respectively, for 17L operation. Therefore, for higher level operation and/or for high input voltage, the proposed topology has an upper hand over its counterparts and surpasses the competent topologies in [17] and [18].

Owing to the floating nature of the dc source in the proposed topology, a solid connection between the PV module and the grid is not possible (the same is equally applicable for motor drives). This may generate variable common mode voltage and in turn leading to leakage current in the system, which needs to be confronted through a suitable modulation technique or special consideration (additional switching devices or switching sequence).

IV. EXPERIMENTAL RESULTS

A laboratory prototype was fabricated in order to verify the operability of the proposed topology. The Semikron insulated gate bipolar transistors SKM75GB063D switches with SKYPER-32-PRO-R gate drivers were used. The dc input voltage was set to 100 V. A 3300 μF capacitor was used as C_1. The dSPACE 1104 generated the gating pulses with a switching frequency of 2.5 kHz. A suitable dead band of 2 μs is provided between the complimentary switches. The experimental waveforms are shown in Fig. 4(a)–(d). It is evident from Fig. 4(a) that the output voltage is composed of five levels with a peak value of 200 V, confirming the boosting ability. The inductive-loading ability is validated in Fig. 4(b). Fig. 4(c) corresponds to the dynamic change in load power factor (PF). A step change in load is applied at time t_1 and corresponding waveforms are shown in Fig. 4(d). From all the above cases, it is confirmed that the proposed topology is able to maintain its SC voltage irrespective of PF and has the ability to operate satisfactorily during the dynamic conditions as well.

V. CONCLUSION

This letter proposed a 5L MLI with the features of voltage boosting, self-voltage balancing, reduced components, inductive-loading ability, and uniform blocking voltage across the switches. The detailed component-based and cost-based comparison has fortified the superiority of the proposed topology against other recent boosting topologies for different conditions. Finally, the presented experimental results validated the operation and confirmed the feasibility of the developed topology and its control scheme.

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