# Letters

## A Constant Frequency ZVS Control System for the Four-Switch Buck–Boost DC–DC Converter With Reduced Inductor Current

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***Abstract*—A constant frequency zero-voltage-switching (ZVS) control strategy with a minimum root mean square (rms) value of inductor current is proposed in this letter for the four-switch buck–boost (FSBB) dc–dc converter that is used as a 48 V intermediate bus pre-regulator in distributed power systems. The quadrilateral inductor current modulation is adopted to achieve ZVS operation. The four control time intervals are optimally selected such that the inductor current rms value is minimized, thus reducing the conduction loss. The proposed closed-loop ZVS control scheme can be implemented without sensing the load current, although the rms minimum current algorithm needs the input and output voltages and load current at given a steady-state condition. The control scheme is verified in a 300 W dc–dc prototype of the ZVS FSBB converter. The input voltage and load transition tests are provided to verify the closed-loop characteristics without sensing load current.**

***Index Terms*—Closed loop, four-switch buck–boost (FSBB), high frequency, ZVS.**

### I. Introduction

With the development of the telecommunications industry in recent years, distributed power systems (DPS) have been widely used in telecom power supply systems [1]–[3]. In order to achieve high efficiency and high power density, 48 V intermediate bus pre-regulator in DPS is required since the voltage of the bus paralleled with batteries varies within a wide range (from 36 to 72 V). The four-switch buck–boost (FSBB) converter, as shown in Fig. 1, is a very promising candidate for the bus pre-regulator because of its ability to step-up and step-down. Furthermore, it is featuring less current and volt-second stresses for the inductor when compared to conventional buck–boost and other dc–dc converters [4].

Different from conventional buck and boost converters, there exists three degrees of control freedom in the FSBB converter, i.e., the duty cycles $d_1$ and $d_2$ of the two switching legs and the phase shift angle between the two duty cycles illustrated in Fig. 1. Although the multi-control freedoms lead to the complexity of the control, it brings the flexibility of the converter, which provides more possibilities for the current and conduction loss optimization. A lot of efforts have been made to explore the control methods for the FSBB in recent years.

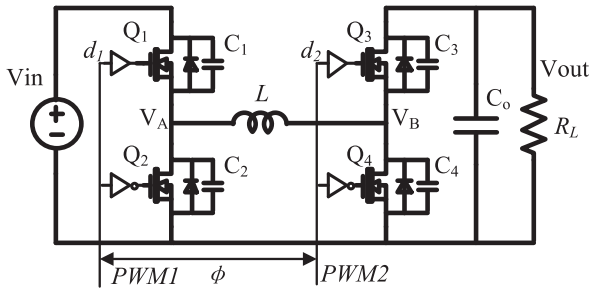


Fig. 1. Topology and control signals of the ZVS FSBB converter.

In order to improve the efficiency, some control methods for the FSBB converter have been presented in the publications [4]–[6] with hard switching. However, with the higher and higher requirements for the power density and frequency, the hard switching controls suffer from large switching losses. A few soft-switching control methods [7]–[11] have been proposed recently aiming at high frequency and high efficiency. In [7], a triangular current mode soft-switching control for the FSBB was addressed with a critical conduction mode (CRM) control strategy. The peak and root mean square (rms) values of inductor current are both too high, especially in the CRM buck–boost mode, which results in high switching OFF loss and conduction loss. A unified quadrilateral inductor current mode zero-voltage-switching (ZVS) modulation was introduced in [8] and [9] shown in Fig. 2. But only the steady-state modulation concept was presented and the current optimization principle and algorithm were missing. Under the quadrilateral inductor current modulation, the inductor current waveform is divided into four segments to generate a reverse flowing current to realize ZVS. With this control concept, the rms value of the inductor current can be reduced with ZVS ON for all switches. A low-loss ZVS modulation scheme for FSBB, which is the same to the above-mentioned control concept, is used to minimize the

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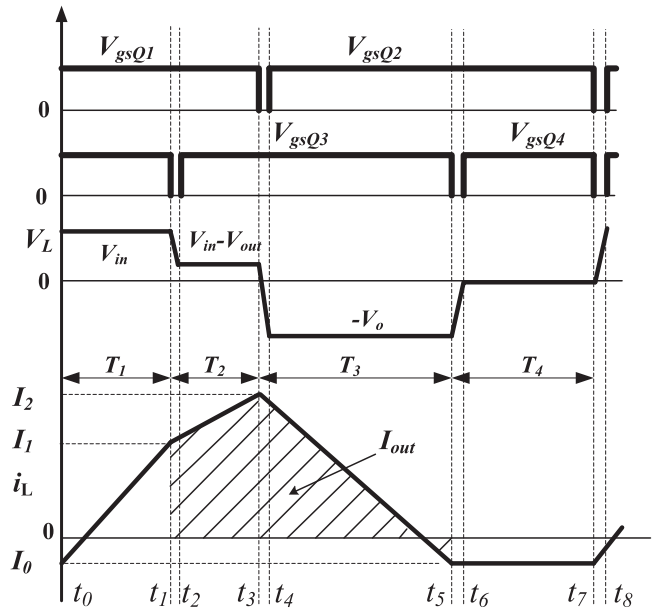



Fig. 2. Key waveforms of the ZVS FSBB converter.

rms value of the inductor current by sensing the input and output voltages and output current at the same time [10]. However, the theoretical analysis of the algorithm of guaranteeing the minimum rms current is missing. A simpler modulation scheme in [11] maintained ZVS operation when the operating points change. However, the inductor current rms value is not the minimum because the duty cycles of the two switching legs are kept complementary.

Besides the theoretical analysis for the rms current minimization, the closed-loop control scheme for output voltage has not been discussed in the current literature. In order to reduce the inductor current rms value with ZVS operation and achieve output tight regulation, this letter proposes a closed-loop constant frequency ZVS control scheme for the FSBB converter without load current sensing.

## II. Proposed ZVS Control With Minimum RMS Inductor Current

### A. ZVS Conditions

The proposed control scheme for the FSBB is based on quadrilateral inductor current mode ZVS modulation shown in Fig. 2, whose operating modes have been descripted in detail in [8]–[11]. The switching period is divided into four segments, $T_1$, $T_2$, $T_3$, and $T_4$. The ZVS conditions are rewritten as follows:

$$I_1 t_{\rm dead} \geq 2C_{\rm oss}V_{\rm out} \tag{1}$$

$$I_2 t_{\rm dead} \geq 2C_{\rm oss}V_{\rm in} \tag{2}$$

$$|I_0|\, t_{\rm dead} \geq 2C_{\rm oss}\max(V_{\rm out}, V_{\rm in}) \tag{3}$$

where $C_{\rm oss}$ is the MOSFET output capacitance, and it is assumed that $C_{\rm oss} = C_1 = C_2 = C_3 = C_4$. The $t_{\rm dead}$ is the dead time in switching legs. $I_0$, $I_1$, and $I_2$ are inductor current values, respectively, at different switching instant $t_5$, $t_1$, and $t_3$.

At interval $T_4$, the inductor current is freewheeling with a value of $I_0$. Since larger $I_0$ will lead to more conduction loss, $I_0$ should be as small as possible under the limitation of (3).

It should be noted that (1)–(3) is an approximation for ZVS conditions, since $C_{\rm oss}$ exhibits a nonlinear, voltage-dependent characteristic.

For simplification, the ZVS conditions are expressed as

$$|I_0|\,,\ I_1, I_2 \geq I_{\rm ZVS} \tag{4}$$

where $I_{\rm ZVS} = \frac{2C_{\rm oss}\max\{V_{\rm out}, V_{\rm in}\}}{t_{\rm dead}}$.

### B. Modulation Scheme for Minimal Inductor Current RMS Value

From the above-mentioned ZVS condition analysis, the interval $T_3$ is determined by the negative current value detection at $t_5$ in each switching cycle. In consideration of low conduction loss and ZVS conditions, $I_0$ is equal to $-I_{\rm ZVS}$. During the time interval $T_4$, the voltage across the inductor is almost zero and the inductor current maintains $I_0$ with freewheeling. So, $T_4$ can be a flexible control variable to keep the constant switching frequency operating. Consequently, the $T_1$ and $T_2$ are utilized to regulate the output voltage. As shown in Fig. 3, the current waveforms vary with load current at given input and output voltages. At light load, the $T_4$ interval is inserted into a switching period to keep the constant frequency. When the load current increases, the $T_4$ becomes shorter until it decreases to zero. After $T_4$ becomes zero, $T_1$ increases with the growing of load. However, from the operating modes and ZVS condition, there are many options for $T_1$ and $T_2$ at a given output power and input/output voltages. In order to reduce the conduction loss, another constraint for $T_1$ and $T_2$, namely the minimum rms inductor current value, is utilized. Fortunately, there is unique interval for $T_1$ and $T_2$, respectively, when the rms value of the inductor current is achieved at given load current and voltages $V_{\rm in}$ and $V_{\rm out}$. The derivation for this unique pare of intervals ($T_1$, $T_2$) under a minimal rms current value are provided in the following.

Some necessary assumptions are made to simplify the following analysis.

1. The dead time is small enough that it can be ignored during the switching cycle.
2. The inductance and other parasitic parameters are linear during switching transitions.
3. The input and output voltages are constant during one switching cycle. Based on these assumptions, the optimal variables $T_1$ and $T_2$ are discussed as follows:

$$T_s = T_1 + T_2 + T_3 + T_4 \tag{5}$$

$$I_1 - I_0 = \frac{V_{\rm in}}{L}T_1 \tag{6}$$

$$I_2 - I_1 = \frac{V_{\rm in} - V_{\rm out}}{L}T_2 \tag{7}$$

$$I_{\rm out} = \frac{1}{T_s}\left[\frac{T_2}{2}(I_1 + I_2) + \frac{T_3}{2}(I_0 + I_2)\right] \tag{8}$$

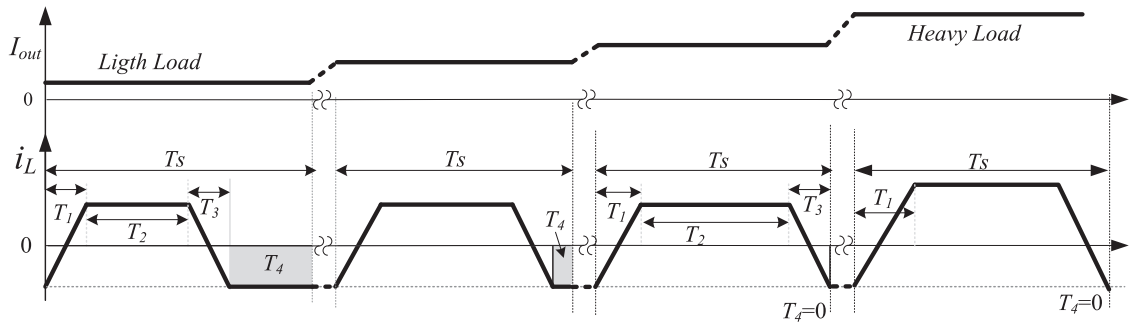



Fig. 3. Control time interval vary with increasing load ($V_{\rm in} = V_{\rm out}$).

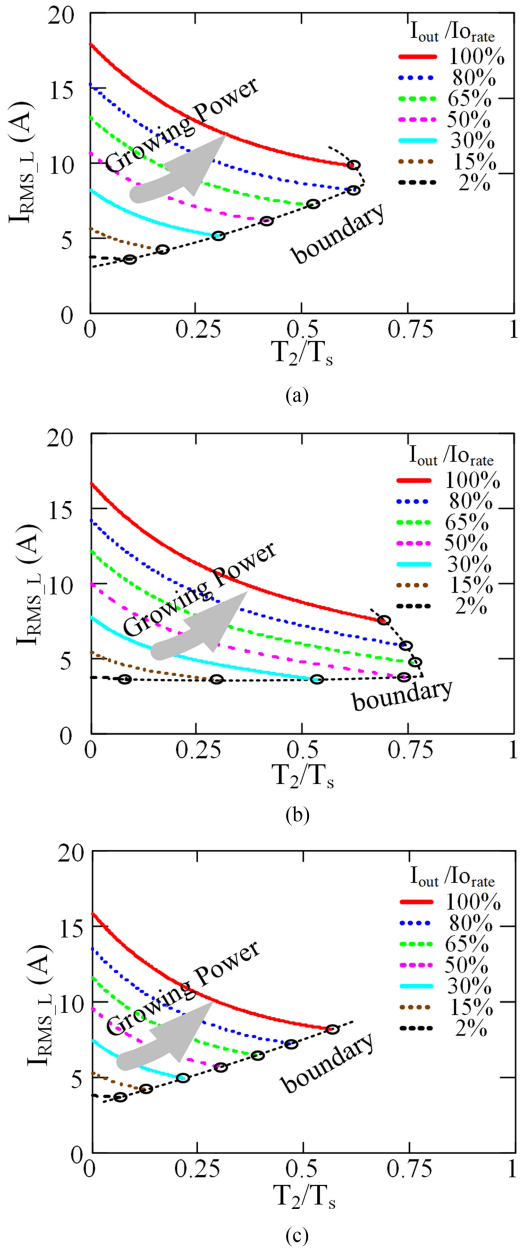



Fig. 4. Curves of $I_{\rm RMS\_L}$ versus $T_2$ under different $V_{\rm in}$ and $I_{\rm out}$ with $V_{\rm out}$ = 48 V. (a) $I_{\rm RMS\_L}$ versus $T_2$ at $V_{\rm in}$ = 36 V. (b) $I_{\rm RMS\_L}$ versus $T_2$ at $V_{\rm in}$ = 48 V. (c) $I_{\rm RMS\_L}$ versus $T_2$ at $V_{\rm in}$ = 60 V.

where $I_{\rm out}$ is the output current. According to the volt-second balance of the inductance, we obtain the following:

$$V_{\rm in} \cdot (T_1 + T_2) = V_{\rm out} \cdot (T_2 + T_3) \tag{9}$$

after the elimination of variables $I_1$, $I_2$, $T_3$, $T_4$ in (5)–(9), and the relationship between $T_1$ and $T_2$ is obtained in

$$T_1 = \frac{-I_0 L - T_2 V_{\rm in} + \sqrt{I_0^2 L^2 + 2 I_{\rm out} T_s V_{\rm out} L + V_{\rm in} V_{\rm out} T_2^2}}{V_{\rm in}}. \tag{10}$$

On the other hand, the inductor current rms value is expressed, in terms of $T_1$ and $T_2$, in following equation, and the detailed expression is given in the Appendix:

$$I_{\rm RMS\_L} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_L^2(t)\,dt} = I_{\rm RMS\_L}(T_1, T_2) \tag{11}$$

where $i_L(t)$ is the inductor current in a switching period shown as

$$i_L(t) = \begin{cases} I_0 + \frac{V_{\rm in}}{L} t, \ 0 \le t \le T_1 \\ i_L(T_1) + \frac{V_{\rm in} - V_{\rm out}}{L}(t - T_1), \ T_1 < t \le T_1 + T_2 \\ i_L(T_1 + T_2) + \frac{-V_{\rm out}}{L}(t - T_1 - T_2), \ T_1 + T_2 < t \\ \quad \le T_1 + T_2 + T_3 \\ I_0, \ T_1 + T_2 + T_3 < t \le T_s. \end{cases} \tag{12}$$

By substituting (10) into (11), the rms value of inductor current is a function of $T_2$. From (11) and (12), the rms current value of inductor versus $T_2/T_S$ under different input voltages and load conditions can be plotted in Fig. 4. The detailed parameters of the FSBB converter are presented in Table I.

Because the ZVS operating must be guaranteed, there is a limitation for the $T_2$ interval. The boundary (black dash line) in Fig. 4 is the constraints for $T_2$ that are determined by ZVS condition provided in (4) and (5). The time interval $T_2$ does not exceed the boundary.

In order to achieve the minimum rms value of inductor current and reduce the conduction loss, the time interval $T_2$ can be selected according to Fig. 4. The minimum $I_{\rm RMS\_L}$ value marked by circle points in Fig. 4 can be found by means of derivative in (13). Otherwise, if $I_{\rm RMS\_L}$ is a monotonic function with respect to $T_2$, the minimum value is found at the boundary of the feasible

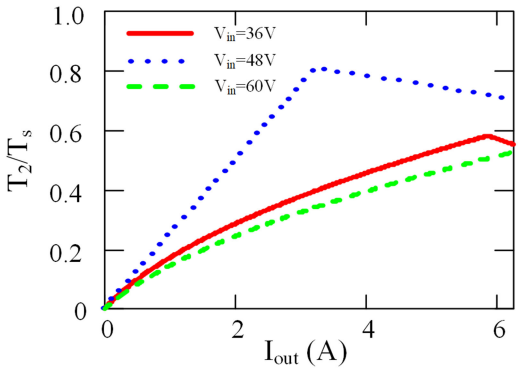



Fig. 5. Optimal $T_2$ (normalized) under different $V_{\rm in}$ and $I_{\rm out}$.

region as

$$\frac{dI_{\rm RMS\text{-}L}}{dT_2} = 0. \tag{13}$$

Then, the solutions of $T_2$ under different power and input voltages are shown in Fig. 5, which can be utilized to minimize the rms value of inductor current.

In fact, the solution $T_2$ can be expressed under given $V_{\rm in}$, $V_{\rm out}$, $I_{\rm out}$, $T_s$, and $L$ in a certain prototype. Consequently, the time interval $T_1$ can also be derived by (10). Then, the intervals $T_1$ and $T_2$ are reorganized as

$$[T_1, T_2]_{\rm optimal} = f_{L,T_s}(V_{\rm in}, V_{\rm out}, I_{\rm out}). \tag{14}$$

According to (10), by applying a pair of ($T_1$, $T_2$) to a certain FSBB with given input and output voltages, the load current $I_{\rm out}$ has definitely a unique solution. Hence, the operating intervals $T_1$ and $T_2$ contain the load current information. If $T_1$ and $T_2$ are optimally selected according to function (14), with sensed $V_{\rm in}$ and $V_{\rm out}$, the output current must follow the input variable $I_{\rm out}$ in function (14). Otherwise, the output voltage will deviate from the $V_{\rm ref}$. Therefore, this principle can be utilized to control the output voltage in the closed-loop control strategy for the FSBB converter.

### C. Proposed Closed-Loop Control System

With the proposed current rms optimization algorithm, the closed-loop control system for the FSBB can be developed. From the above-mentioned optimal inductor current control scheme, there is a unique pare of time intervals ($T_1$, $T_2$) under given $V_{\rm in}$, $V_{\rm out}$, $I_{\rm out}$, and $T_s$. The duty cycles for the switches can be derived from the $T_1$ and $T_2$ according to (14) as follows:

$$d_1 = \frac{T_1 + T_2}{T_s} \tag{15}$$

$$d_2 = \frac{T_2 + T_3}{T_s}. \tag{16}$$

In (14), there are three inputs $V_{\rm in}$, $V_{\rm out}$, and $I_{\rm out}$ to the minimum rms value of inductor current optimization algorithm. Among them, the input and output voltages $V_{\rm in}$ and $V_{\rm out}$ are easily sampled. The sensing for the load current $I_{\rm out}$ will cause additional loss and needs auxiliary analog amplifier. In order to simplify the circuit and reduce the sensing loss, the input parameter ($I_{\rm out}$) in (14) is utilized as a control variable. Additionally, the output of PI regulator is utilized instead of the load current to construct the negative feedback closed-loop system.

The control system blocks are shown in Fig. 6(a), where Min. RMS represents the function (14). The sampled input and output voltages $V_{\rm in}$ and $V_{\rm out}$, and PI's output are three inputs of the Min. RMS block to calculate the optimal control time intervals $T_1$ and $T_2$. Due to the computational complexity, the calculation is implemented by a lookup table and linear interpolation. $T_3$ is determined by hardware current detection to insure ZVS cycle by cycle. As shown in Fig. 3(b), during $T_3$ interval, the current flowing through $Q_2$ is sensed by resistor $R_s$ and compared with $I_{\rm ZVS}$. Once the absolute value of the negative current is larger than $I_{\rm ZVS}$, $Q_3$ turns OFF and $T_3$ terminates. Therefore, the negative current $I_0$ is naturally controlled and is equal to $-I_{\rm ZVS}$. $T_4$ is automatically inserted by pulsewidth modulation (PWM) modulation to maintain constant frequency operation. Fig. 6(c) shows the simplified closed-loop diagram, where the output of PI determines the average output current of the switch network. The average output current is determined by $T_1$ and $T_2$, which are optimally selected by Min. RMS algorithm according to "$I_{\rm out}$" input, which can be given by the PI controller. Therefore, the system can be seen as controllable current source and the controller is the PI regulator. At a steady-state condition, the output of PI is determined by the voltage error between the $V_{\rm ref}$ and $V_{\rm out}$ If the output of PI does not match the load current at dynamic conditions, it will cause $V_{\rm out}$ to deviate from $V_{\rm ref}$. Then, the $V_{\rm out}$ deviation will make the output of PI, i.e., input of Min. RMS ($I_{\rm out}$), to correct the current difference owing to negative feedback control.

Fig. 7 gives the detailed PWM logic waveforms, which can be realized by digital controller (TMS320F28027). The sum of time intervals $T_1$ and $T_2$ is sent to CMP1A register while the time interval $T_2$ is sent to CMP2A register. When the counter rises from 0 to $T_s$, the CMP1A is compared with counter to generate EPWM1A. EPWM2A is set once the counter counts to CMP2A, and reset by the $T_3$end signal. EPWM1A and EPWM2A are inverted and added dead time to produce $V_{gsQ1}$–$V_{gsQ4}$ driving signals.

By eliminating the load current sensing, the control system for the ZVS-FSBB can be simplified and the efficiency can be improved.

## III. Experimental Verifications and Comments

In order to demonstrate and verify the proposed control strategy, a 300 W, 36–72 V input, 48 V output FSBB prototype has been built up, as shown in Fig. 8. The key parameters of the prototype are list in Table I. The inductance selection is calculated according to the worst case of ZVS, where the FSBB operates at maximum power and minimum input voltage [10].

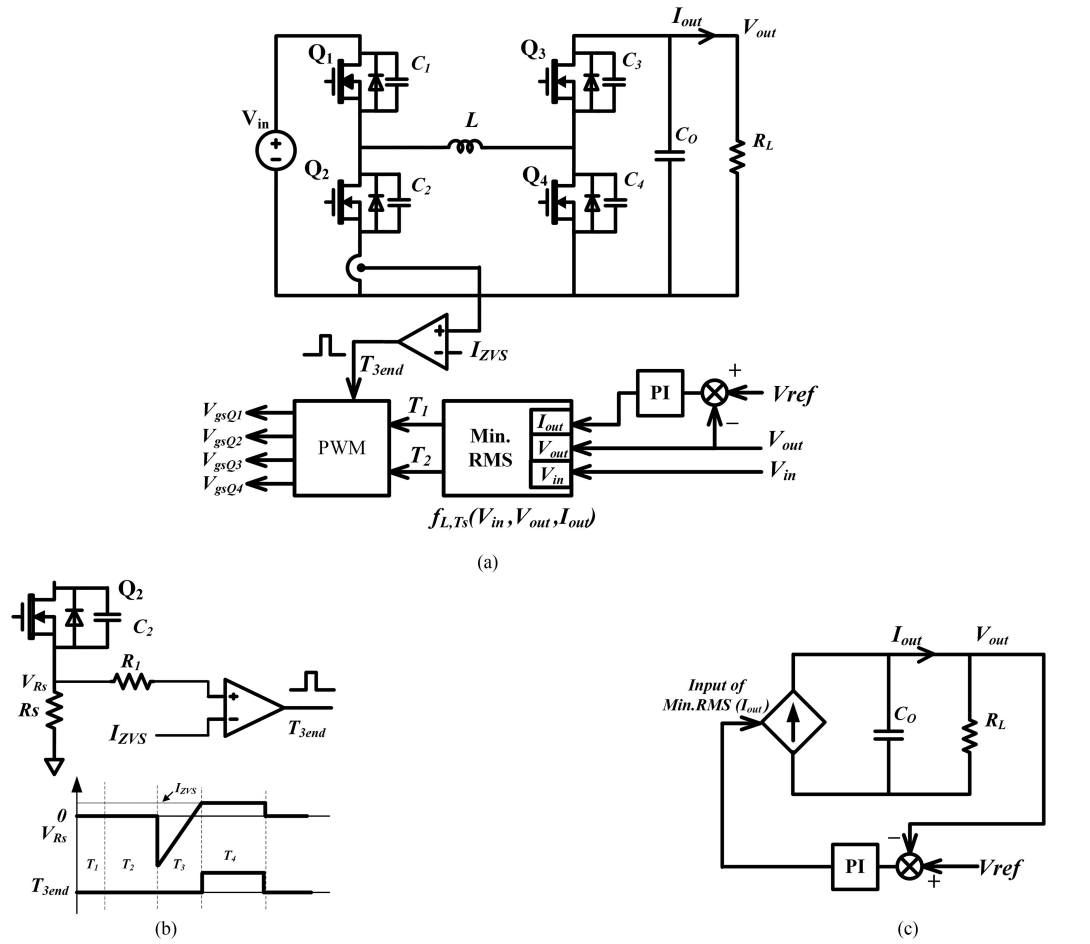



Fig. 6. Proposed Min. RMS current closed-loop control system without output current sensing. (a) Block diagram of closed-loop control. (b) $T_{3\mathrm{end}}$ signal generation. (c) Simplified closed-loop diagram.

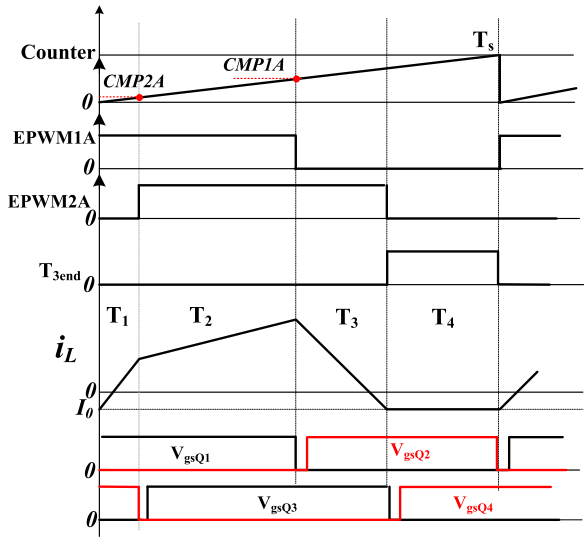



Fig. 7. Generation of four PWM driving signals for switches.

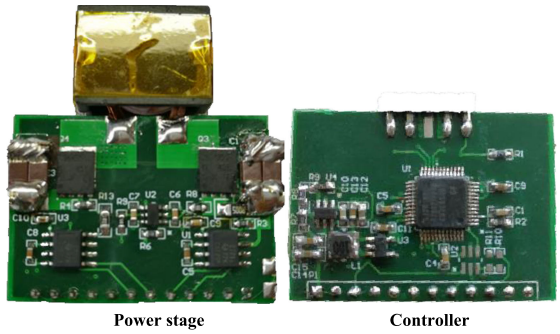


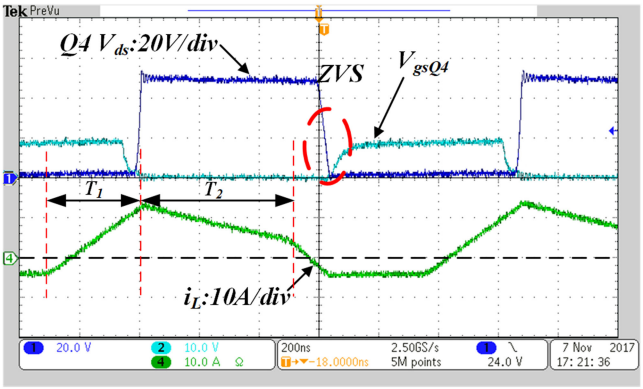

Fig. 8. Prototype photos.

The ZVS switching for $Q_4$ is guaranteed by negative current detection at $t_5$ cycle by cycle. The measured ZVS waveforms of $Q_4$ are given in Fig. 9 with different input voltages. It can be clearly seen that the gate voltage $V_{gsQ4}$ begins to turn ON after the $V_{\mathrm{ds}}$ of $Q_4$ falls to zero at different input voltage. Fig. 10 shows the ZVS waveforms of $Q_2$ at different input voltages. From the measured ZVS operations in Figs. 9 and 10, all switches of the FSBB converter can achieve ZVS operation with the proposed control strategy.

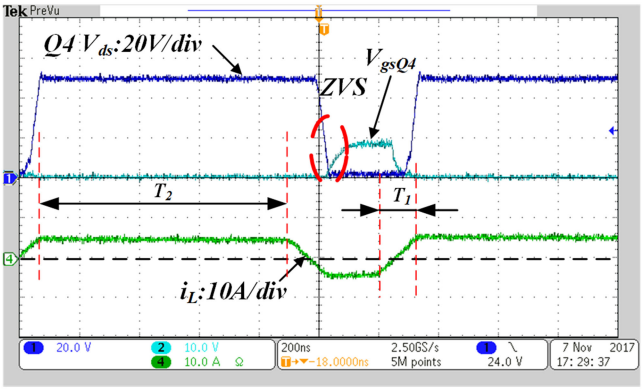
With the purpose of feasibility verification for the regulation ability by the proposed control method, input voltage and load transient tests are conducted on the prototype. In order to ver-

TABLE I
PARAMETERS OF THE PROTOTYPE

| Switches | BSC035N10S5 |
|---|---|
| L | 780nH |
| Co | 4.7uF x4 |
| Gate driving IC | UCC27211D |
| Frequency | 800kHz |
| Controller | TMS320F28027 |




(a)

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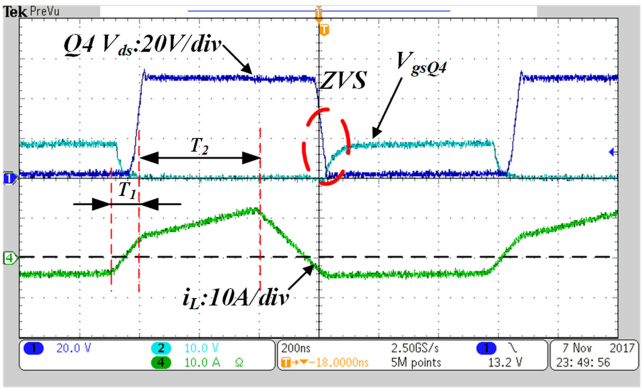
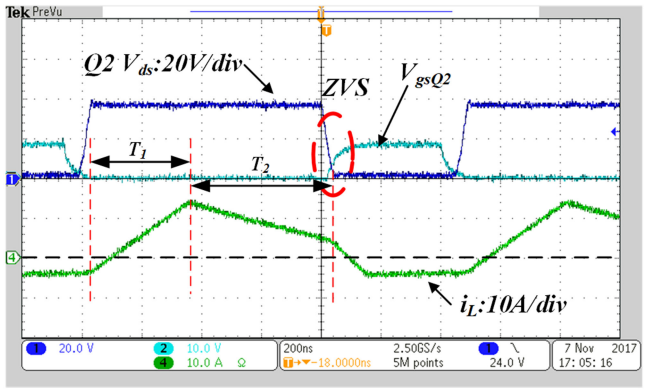



(c)

Fig. 9. ZVS waveforms of the switch $Q_4$ at different input voltages. (a) $V_{\rm in} < V_{\rm out}$. (b) $V_{\rm in} = V_{\rm out}$. (c) $V_{\rm in} > V_{\rm out}$.

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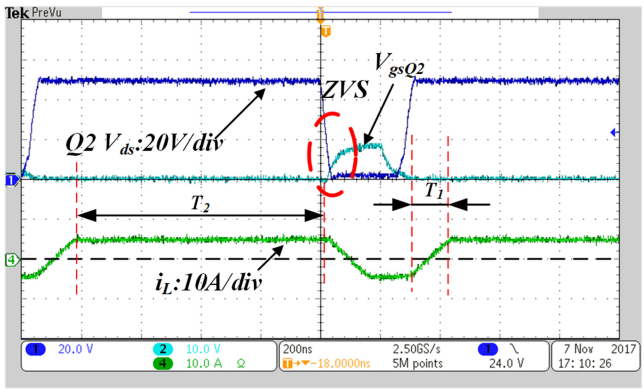


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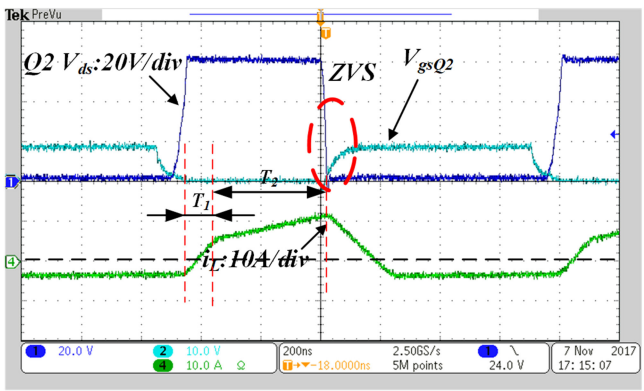
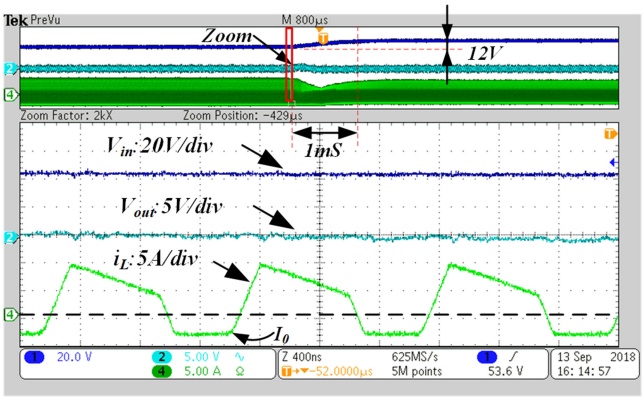



(c)

Fig. 10. ZVS waveforms of the switch $Q_2$ at different input voltages. (a) $V_{\rm in} < V_{\rm out}$. (b) $V_{\rm in} = V_{\rm out}$. (c) $V_{\rm in} > V_{\rm out}$.

ify the algorithm adaptation between modes in real time, the input voltage switches from 42 to 54 V within 1 ms with 48 V output. Fig. 11 gives the inductor current waveforms during an input voltage transition period. At different input voltage ranges ($V_{\rm in} < V_{\rm out}$, $V_{\rm in} = V_{\rm out}$, and $V_{\rm in} > V_{\rm out}$), the current waveforms are identical to Figs. 9 and 10. By the proposed algorithm, the FSBB smoothly changed between modes in real time.

Fig. 12 gives the output voltage/current and inductor current at load transitions. The settling time of the prototype is about 150 $\mu$s. The overshoot and undershoot of the prototype are both

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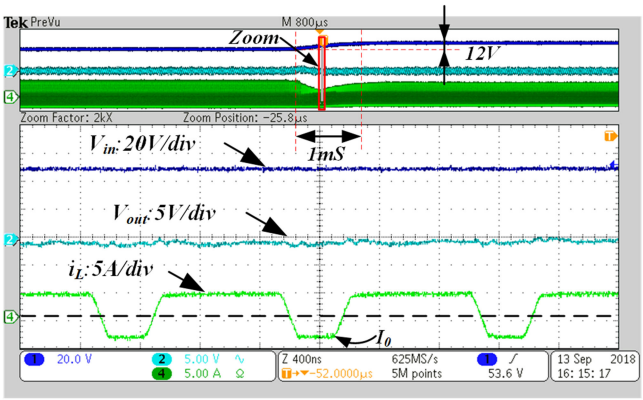


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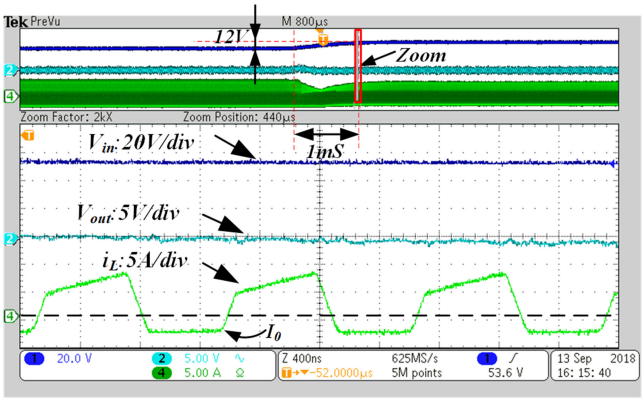
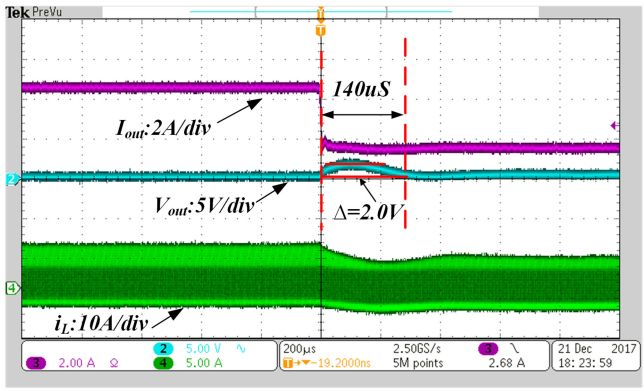
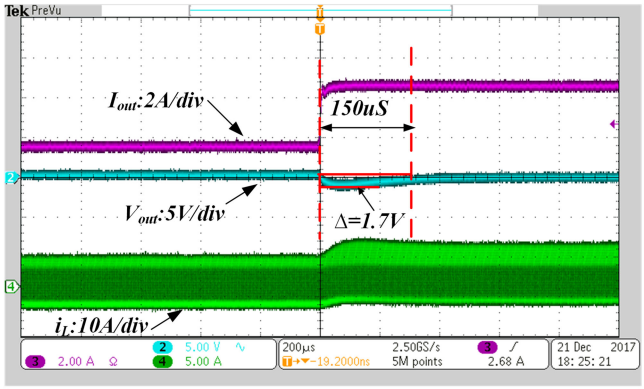



(c)

Fig. 11. Modes transition when $V_{\rm in}$ switches from 42 to 54 V. (a) $V_{\rm in} < V_{\rm out}$. (b) $V_{\rm in} = V_{\rm out}$. (c) $V_{\rm in} > V_{\rm out}$.




(a)




(b)

Fig. 12. Inductor current and output waveforms at load transients. (a) 25%–75% load transient. (b) 75%–25% load transient.

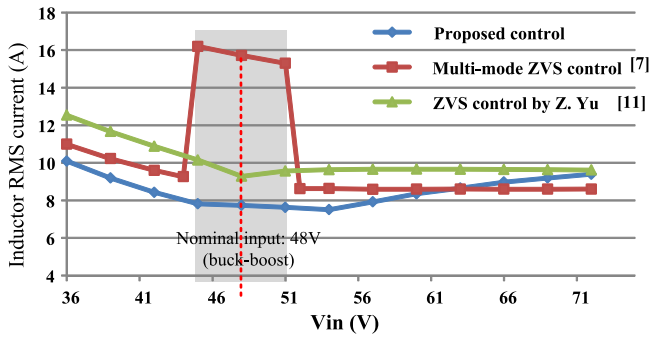



Fig. 13. Inductor current rms value under different control schemes (simulation).

within 5% of the nominal output voltage. The sampling and algorithm calculation are done every three switching cycles due to the limitation of the CPU bandwidth. Nevertheless, it can be seen that the output regulation works pretty well by the proposed control method without output current sampling.

In order to show the reduction of an inductor current rms value, Fig. 13 illustrates the inductor current rms value versus input voltage under different control schemes at full load. The triangular current multi-mode ZVS control [7] almost doubles the rms value of inductor current when operating in a buck–boost mode near the nominal input voltage (shadow area). The rms value of inductor current with the control scheme proposed by Yu *et al.* [11] is maintained at a little bit higher level than that of the proposed scheme. The proposed control scheme keeps the rms value of the inductor current at the lowest level in a wide voltage range. Therefore, the proposed control scheme has less conduction losses.

Fig. 14 shows the measured efficiency curves of the prototype at different input voltages. The peak efficiency is about 98.0% at 48 V input. As the input voltage deviates from the central

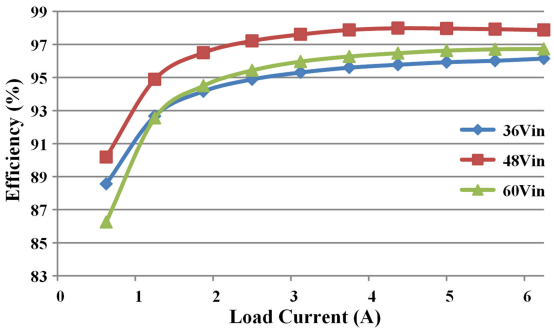



Fig. 14. Efficiencies of the prototype at different input voltages.

nominal input voltage (which is about 48 V), both the rms values of inductor current and the turn OFF current increase. Thus, the conduction loss and switching loss increase, resulting in the efficiency drop.

## IV. Conclusion

In this letter, a simple closed-loop control scheme for the constant frequency ZVS FSBB converter is proposed without sensing the load current. By the proposed current optimal control scheme, the conduction loss of the inductor is further reduced compared to conventional ZVS control schemes; and the output tight regulation can be achieved without load current sampling. A 300 W prototype of the FSBB converter is built up and tested for the verification of the proposed control method.

## Appendix

$$I_{\mathrm{RMS}}(T_1,T_2)=\frac{1}{3L^2T_sV_2}\left[3T_sI_0^2L^2V_2+3I_0LT_1^2V_1\left(V_1+V_2\right)\right.$$
$$+6I_0LT_1T_2V_1^2+3I_0LT_2^2V_1\left(V_1-V_2\right)$$
$$+T_1^3V_1^2\left(V_1+V_2\right)+3T_1T_2\left(T_1+T_2\right)V_1^3$$
$$\left.-\left(3T_1+2T_2\right)T_2^2V_1^2V_2+T_2^3V_1\left(V_1^2+V_2^2\right)\right]. \tag{A.1}$$

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