A Comprehensive Harmonic Analysis and Control Strategy for Improved Input Power Quality in a Cascaded Modular Solid State Transformer

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***Abstract*—In a three-stage cascaded modular solid state transformer (CMSST), unbalanced dc bus voltages at the output of cascaded multilevel rectifier is a common issue due to inevitable parameter mismatch in stage-2. To balance the dc bus voltages, either voltage balance control (VBC) in stage-1 or power balance control (PBC) in stage-2 is necessary. In this paper, an in-depth theoretical analysis to investigate the input power quality of the CMSST in the presence of voltage and PBC schemes is presented. The grid-side multilevel voltage of the CMSST is analyzed to highlight the limitation of using VBC in stage-1. It is then mathematically proven that the switching frequency based harmonics in the grid current are significantly reduced by using the PBC in stage-2. Simulation studies of a 3.3-kV, 50-kVA CMSST are carried out using the PLECS software to substantiate the proposed analysis. Experimental verifications are performed on a 750-VA single-phase CMSST laboratory prototype for a 20% parameter mismatch in stage-2. It is found that the grid current total harmonic distortion (THD) is reduced from 6.65% to 3.8% at 50% load by using PBC in stage-2. This paper provides guidelines for the designer to choose appropriate balance controllers for the CMSST.**

***Index Terms*—Cascaded multilevel rectifier, power balance control (PBC), power electronic transformer, smart grid, solid state transformer (SST), voltage balance control (VBC).**

I. Introduction

A LARGE penetration of intermittent renewable energy resources (RES) and fast charging electric vehicles (EV) have opened a new set of challenges in terms of voltage regulation, stability, etc., in the power distribution network with current infrastructure [1]. The future power distribution network can be divided into interconnections of small clusters of distributed sources and loads called microgrids [2], [3]. Each microgrid is connected to other microgrids or the main grid through an energy control center [4]. The basic functionalities

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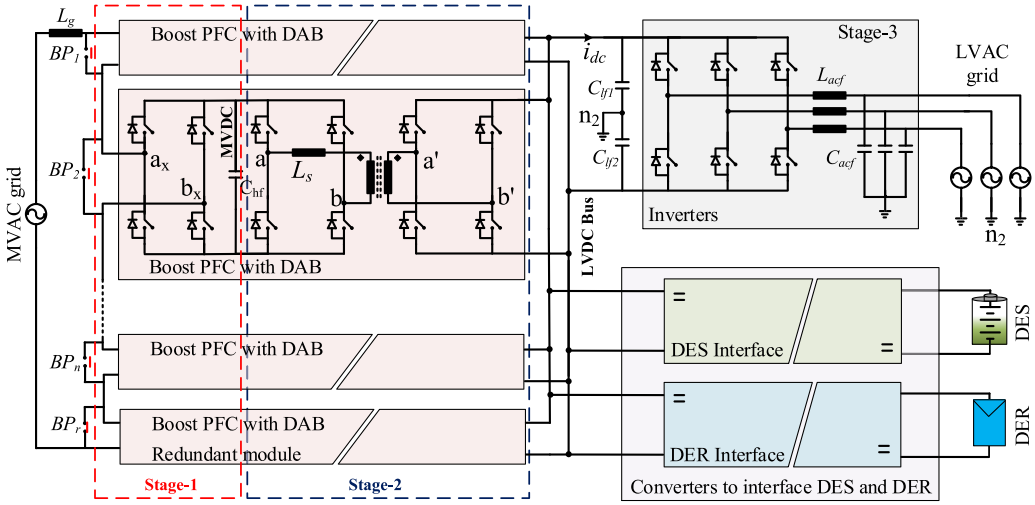

Fig. 1. Three-stage CMSST.

by using LV devices (1200/1700 V) operating at low-switching frequency ($f_s < 2$ kHz) [20], [21]. Stage-2 of the CMSST is implemented using a high-frequency isolated dual active bridge (DAB) dc–dc converter to convert the MVDC to LVDC. The advantages of DAB are its simple hardware construction and control, and minimum number of passive elements compared to other isolated dc–dc converters [22]–[25]. A B-6 two-level inverter topology is used in stage-3 to convert the LVDC to LV AC of the desired frequency [26], [27].

Even though the design and control of individual power electronic conversion stages in SST have been well researched, there are few challenges both at the component level (for e.g., design and testing of medium frequency transformer with high-voltage insulation [28]–[31]) as well as at the system level, which are control and power quality issues [32], [33]. Unlike the conventional passive transformer, an SST introduces additional switching harmonics into the MVAC grid if the SST is not modulated properly. All H-bridges in stage-1 of the SST are fed from a single MVAC grid voltage and the MVDC output voltage of each H-bridge is controlled by the input grid current and modulation index. It is difficult to design and fabricate identical high-frequency transformers and series inductors for stage-2. As a result, each isolation stage draws unequal power from each H-bridge [34]. Any load unbalance at the output of this stage can lead to unbalanced MVDC voltages across each H-bridge, which not only increases the voltage stress across the active devices, but also increases the total harmonic distortion (THD) of the grid current.

Several voltage balancing schemes have been proposed to balance the MVDC bus voltages of the SST. The individual voltage balance controllers (VBCs) [35], [36] as well as cluster balancing control (which ensures equal power in all the three phases of the cascaded H-bridge) [35] are introduced in stage-1 to ensure equal MVDC bus voltages despite the power unbalance due to parameter mismatch in the isolation stage. Moreover, a simple master-slave control has been introduced to regulate the LVDC bus voltage of the isolation stage, which alleviates the computational burden on the controller in stage-2 [35], [36]. Despite the simplicity of the above control schemes, introducing additional PI-based voltages balance controllers in stage-1 have created a compromise between the fast dynamic response and system stability. In [37], the space vector based modulation has been introduced in stage-1 to control the power factor of input current as well as balance the dc bus voltages. In summary, the control schemes presented in [35]–[39] are designed to adjust the modulation index of each H-bridge such that the output voltages are balanced despite the parameter mismatch in the isolation stage. The quoted advantage of such control is that the control complexity on stage-2 controller is reduced by implementing the VBC in stage-1. Alternatively, the power balance control (PBC) schemes can be incorporated in the isolation stage to adjust power flow through each DAB such that the load seen by each H-bridge in stage-1 is balanced [40]–[42]. It has been shown in [43] that implementing the PBC in stage-2 offers superior transient response compared to the VBCs in stage-1. However, the effect of these control schemes [35]–[43] on the harmonic performance of input current has not been analyzed in the literature. Moreover, the switching frequency is also not closer to the optimal operating points as discussed above [20], [21].

In this paper, the harmonic performance of the grid current is analyzed for various MVDC voltage balance schemes proposed in the literature for SST. Special emphasis is given to analyze various switching frequency based harmonic components in the multilevel waveform with the two approaches: 1) power balancing control implemented in stage-2 [40]–[42] and 2) voltage balancing control implemented in stage-1 [35]–[39]. The presented analysis would help the designer choose an appropriate balance controller for the CMSST. Rest of the paper is organized as follows. A brief overview of the three-stage CMSST and required average models are presented in Section II. The switching frequency based harmonic components in the multilevel waveform of the CMSST are derived for the above mentioned two cases in Section III. Simulation and experimental results are presented in Section IV to validate the analysis. Finally, Section V concludes the paper.

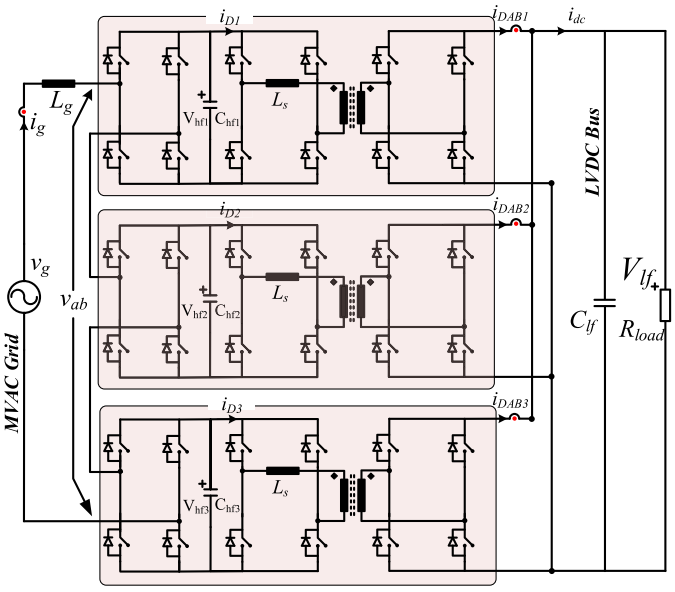

Fig. 2. First and second stages (i.e., cascaded multilevel rectifier stage and isolation stage) of the three-stage CMSST.

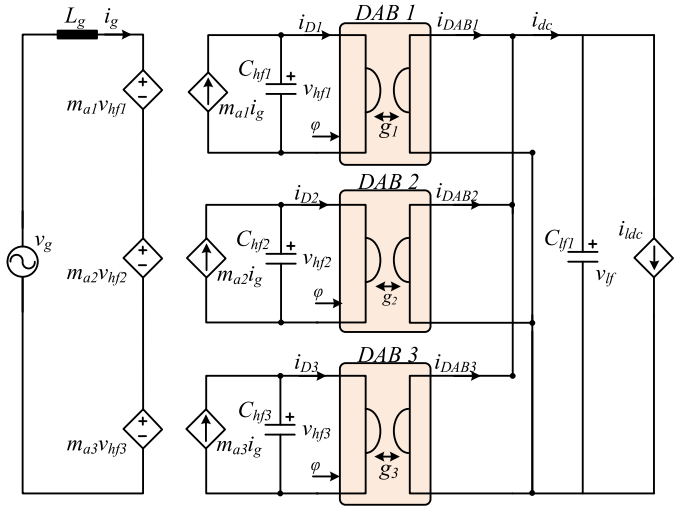

Fig. 3. Simplified average model of the first and second stages (i.e., cascaded multilevel rectifier and isolation stages) of the CMSST.

II. Three-Stage CMSST

The three-stage CMSST is the most suitable architecture for distribution grid applications as it has not only a stiff dc port to integrate DES and DER, but also the capability to regulate real and reactive power flows at the MV grid and the LV grid. Additionally, the stiff dc ports act as an energy buffer to decouple the effect of MV side disturbances on the LV side and vice versa. It consists of a cascaded multilevel rectifier in stage-1, followed by an isolation stage, and finally an inverter stage to convert dc to three phase ac. The third stage of the CMSST is omitted in the discussions from now on as it does not affect the analysis presented in this paper. The first and second stages of a three-stage seven level CMSST is shown in Fig. 2.

Balancing dc bus voltages at the output of stage-1 is one of the major challenges in the CMSST topology. To understand the voltage balancing issues in this topology, it is necessary to understand how the average power is being shared at the isolation stage. For better understanding of power sharing at the isolation stage and its effects on stage-1, the average model of the CMSST as shown in Fig. 3 is considered, and various factors that affect the power sharing are analyzed. Assuming that the cascaded multilevel rectifier is operated with a modulation index m_{an}, where $n = 1, 2,$ and 3, for a particular grid current (i_g), the rectifier output current is $m_{an}i_g$. Under steady-state operation, the rectifier output current ($m_{an}i_g$) is equal to the DAB input current (i_{Dn}). For any given input current, i_g, the dc voltage at the output of stage-1 (V_{hfn}) is decided by the difference in the rectifier current $m_{an}i_g$ and DAB input current i_{Dn}

$$v_{hfn}(t) = \left[\frac{m_{an}i_g - i_{Dn}}{C_{hfn}}\right]t + < V_{hf} >$$
$$\text{where,} \quad < V_{hf} >= \frac{v_{hf1} + v_{hf2} + v_{hf3}}{3}. \tag{1}$$

When the currents drawn by the isolation stages (i_{D1}, i_{D2}, and i_{D3}) are equal, the dc voltages at the output of stage-1 (v_{hf1}, v_{hf2}, and v_{hf3}) are equal, assuming C_{hfn} are equal. This scenario is possible only when all the isolation stages are perfectly identical, which is not feasible in practice especially due to the mismatch in series inductor values and high-frequency isolation transformers. The isolation stage (DAB) can be modeled using gyrator model as follows [44]:

$$\begin{pmatrix} i_{Dn} \\ i_{\text{DAB}n} \end{pmatrix} = \begin{pmatrix} 0 & g \\ g & 0 \end{pmatrix} \begin{pmatrix} v_{hfn} \\ v_{lf} \end{pmatrix}$$
$$\text{where,} \quad g = \frac{n\phi(\pi - \phi)}{2\pi^2 f_{sd} L_s} \tag{2}$$

where L_s is the series inductor of the transformer; f_{sd} is the switching frequency of the DAB; ϕ is the phase shift between the primary and secondary voltages of the DAB that acts as a control parameter to adjust the power transfer in DAB; and g is the gyrator constant. The power transferred by the DAB is given as follows [44]:

$$P = gV_{hfn}V_{lf} = \frac{nV_{hfn}V_{lf}\phi(\pi - \phi)}{2\pi^2 f_{sd} L_s}. \tag{3}$$

Considering ϵ as the magnitude of uncertainties in the parameters of the isolation stage (i.e., series inductors and leakage inductance of high-frequency transformers), power delivered by the DAB stage for such parameter mismatch is given as follows:

$$\begin{aligned} P &= \frac{nV_{hfn}V_{lf}\phi(\pi - \phi)}{2\pi^2 f_{sd}(L_s \pm \epsilon)} \\ &\approx \frac{nV_{hfn}V_{lf}\phi(\pi - \phi)}{2\pi^2 f_{sd} L_s}(1 \mp \frac{\epsilon}{L_s} \pm \frac{\epsilon^2}{L_s^2}). \end{aligned} \tag{4}$$

Assuming other parameters as constant, the normalized power delivered by the DAB for a maximum parameter mismatch of 20% is shown in Fig. 4

$$[\epsilon_{\min}, \epsilon_{\max}] \in [-0.2L_s, 0.2L_s].$$

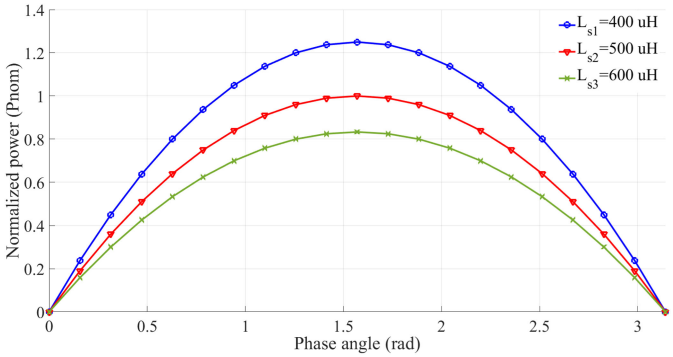

Fig. 4. Normalized power transferred by DAB for three inductance values.

When all the DABs are controlled with the same phase shift (ϕ), the DAB with the highest series inductance value [i.e., $(L_s + \epsilon_{\max})$] transfers less power from the MVDC bus (V_{hfn}) to the LVDC bus (V_{lf}) compared to the other DABs. In the case considered in Fig. 4, DAB3 transfers less power compared to DAB2 and DAB1 at any phase shift (ϕ). As a result, the current drawn by DAB3 (i_{D3}) from the dc bus capacitor C_{hf3} also decreases. The output voltages of the H-bridges in stage-1 are as follows:

$$v_{hf1}(t) = \left[\frac{m_{a1} i_g - i_{D1}}{C_{hf1}}\right] t + < V_{hf} >$$
$$v_{hf2}(t) = \left[\frac{m_{a2} i_g - i_{D2}}{C_{hf2}}\right] t + < V_{hf} > \quad (5)$$
$$v_{hf3}(t) = \left[\frac{m_{a3} i_g - i_{D3}}{C_{hf3}}\right] t + < V_{hf} > .$$

Under steady-state operation, as $i_{D3} < i_{D2} < i_{D1}$ in Fig. 4, for any given input current (i_g) and modulation index of stage-1 ($m_{a1} = m_{a2} = m_{a3} = m_a$), dc bus voltages are having the relationship: $V_{hf3} > V_{hf2} > V_{hf1}$.

The unbalanced voltage not only increases the voltage stress across the active devices, but also it may eventually cause the device failure if the voltage increases above the absolute maximum rating of the devices. Also, equal power sharing between various DABs is desirable especially in SST applications as it results in uniform thermal loading on all active devices. Nonuniform thermal loading may cause the active devices to age faster or fail even before the maintenance period. Keeping in mind the high reliability requirements for SST at distribution level for grid applications, the device failure in any case should be avoided. In this regard, the voltage and PBCs for the three-stage CMSST have been proposed to balance the individual dc bus voltages and detailed analysis is presented in Section III.

III. Voltage and PBCs for Three-Stage CMSST

As discussed in Section II, a balance controller is necessary to balance the dc output voltages of each H-bridge in the first stage of the three-stage CMSST. Such a balance controller can be incorporated either in stage-1, i.e., cascaded multilevel rectifier (referred to as the VBC) or in stage-2, i.e., isolation stage

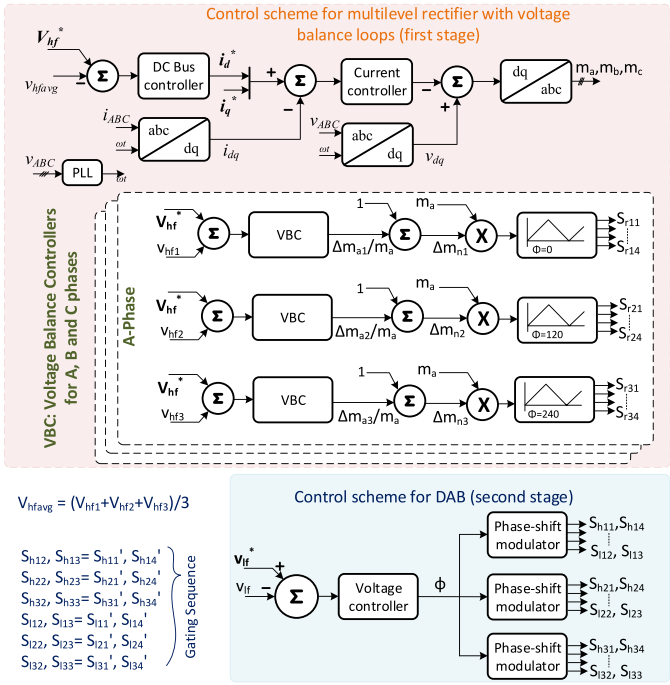

Fig. 5. VBC incorporated in stage-1 of SST.

(referred to as the PBC). In this section, the pros and cons of implementing the balance control in both the stages are studied to standardize the control objectives.

A. VBC in Stage-1

VBC can be incorporated in stage-1 as shown in Fig. 5. The dc bus controller for multilevel rectifier generates necessary active power reference to maintain the average of all capacitors voltages, i.e., $((v_{hf1}+v_{hf2}+v_{hf3})/3)$ as close as possible to the reference voltage (V^*_{hf}), whereas the reactive power reference (i^*_q) is provided by the grid operator. However, this does not guarantee equal voltages across all capacitors. Therefore, additional terms (Δm_{a1}, Δm_{a2}, and Δm_{a3}) from the individual VBCs are added to the common modulation index (m_a) generated by the current controller to maintain each capacitor voltage at the reference value [35]–[38]

$$v_{hf1}(t) = \left[\frac{(m_a + \Delta m_{a1}) i_g - i_{D1}}{C_{hf1}}\right] t + < V_{hf} >$$
$$v_{hf2}(t) = \left[\frac{(m_a + \Delta m_{a2}) i_g - i_{D2}}{C_{hf2}}\right] t + < V_{hf} > \quad (6)$$
$$v_{hf3}(t) = \left[\frac{(m_a + \Delta m_{a3}) i_g - i_{D3}}{C_{hf3}}\right] t + < V_{hf} > .$$

The additional modulation terms ($\Delta m_{a1}, \Delta m_{a2}$, and Δm_{a3}) are adjusted by the VBC as shown in Fig. 5 such that the following are satisfied

$$m_{a1} i_g - i_{D1} = (m_a + \Delta m_{a1}) i_g - i_{D1} \approx 0$$
$$m_{a2} i_g - i_{D2} = (m_a + \Delta m_{a2}) i_g - i_{D2} \approx 0 \quad (7)$$
$$m_{a3} i_g - i_{D3} = (m_a + \Delta m_{a3}) i_g - i_{D3} \approx 0.$$

When (7) is ensured, all the MVDC bus voltages converge to V_{hf}^*, i.e., $v_{hf1} \approx v_{hf2} \approx v_{hf3} \approx V_{hf}^*$. In Fig. 5, $\Delta m_{n1}, \Delta m_{n2}$, and Δm_{n3} are given as follows:

$$\Delta m_{n1} = 1 + \frac{\Delta m_{a1}}{m_a};\ \Delta m_{n2} = 1 + \frac{\Delta m_{a2}}{m_a};$$
$$\Delta m_{n3} = 1 + \frac{\Delta m_{a3}}{m_a}. \tag{8}$$

According to [35]–[39], the major advantage with the VBC in stage-1 is that it reduces the control complexity in stage-2. As shown in Fig. 5, a simple voltage controller can control the phase shift (ϕ) for all the dc–dc converters. However, the effect of balance controller on the harmonic profile is neglected. Therefore, special emphasis is given to the individual switching harmonics in this section.

1) Harmonic Analysis: The effect of VBC on the grid current can be understood by analyzing the Fourier transform of the pole-to-pole voltage (v_{ab}) of stage-1 of the CMSST. The approach followed here for deriving the Fourier transform is as follows: first the Fourier transform of pole-to-pole voltage of individual H-Bridges is obtained, and later the individual Fourier transforms are added to find the Fourier transform of multilevel converter. In this case, the modulation signals are modeled as follows:

$$m_{a1} = M_1 \cos(\omega_f t);\ m_{a2} = M_2 \cos(\omega_f t);$$
$$m_{a3} = M_3 \cos(\omega_f t) \tag{9}$$

where ω_f is the grid fundamental angular frequency in rad/sec. In a unipolar sinusoidal PWM, the odd-order switching harmonics along with the respective sidebands are zero. The switching frequency based harmonic component of a $(2N+1)$-level cascaded H-bridge (N-modules cascaded) is as follows [45]

$$v_{2msh}(t) = \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{l=-\infty}^{\infty} \frac{1}{2m} \cos[(m+l-1)\pi] \sum_{s=1}^{N} J_{(2l-1)}(m\pi M_s) \times \cos\left[2m\omega_c t + (2l-1)\omega_f t + \frac{2m(s-1)\pi}{N}\right] \tag{10}$$

where *m* is the carrier frequency index; *l* is the side-band index; and *J* is the Bessel function, which can be evaluated using MATLAB. For a seven-level cascaded H-bridge, i.e., $N = 3$, the second-, fourth-, and sixth-order switching harmonics along with their side bands (viz., $v_{2sh}(t)$, $v_{4sh}(t)$, and $v_{6sh}(t)$) can be obtained by evaluating (10) for $m = 1, 2,$ and 3, respectively

$$v_{2sh}(t) = \frac{2V_{dc}}{\pi} \sum_{l=-\infty}^{\infty} \cos(l\pi) \Big\{ J_{-1}(\pi M_1) \cos\left[2\omega_c t + (2l-1)\omega_f t\right] + J_{-1}(\pi M_2) \cos\left[2\omega_c t + (2l-1)\omega_f t + \frac{2\pi}{3}\right] + J_{-1}(\pi M_3) \times \cos\left[2\omega_c t + (2l-1)\omega_f t + \frac{4\pi}{3}\right] \Big\} \tag{11}$$

$$v_{4sh}(t) = \frac{V_{dc}}{\pi} \sum_{l=-\infty}^{\infty} \cos[(l+1)\pi] \Big\{ J_{-1}(2\pi M_1) \cos\left[4\omega_c t + (2l-1)\omega_f t\right] + J_{-1}(2\pi M_2) \cos\left[4\omega_c t + (2l-1)\omega_f t + \frac{4\pi}{3}\right] + J_{-1}(2\pi M_3) \times \cos\left[4\omega_c t + (2l-1)\omega_f t + \frac{2\pi}{3}\right] \Big\} \tag{12}$$

$$v_{6sh}(t) = \frac{4V_{dc}}{6\pi} \sum_{l=-\infty}^{\infty} \cos[(l+2)\pi] \cos\left[6\omega_c t + (2l-1)\omega_f t\right] \times \left\{ J_{-1}(3\pi M_1) + J_{-1}(3\pi M_2) + J_{-1}(3\pi M_3) \right\}. \tag{13}$$

In an ideal seven-level multilevel converter with phase-shifted carrier modulation

$$v_{msh}(t) = \begin{cases} 0, & \text{if } m < 3 \\ \dfrac{2V_{dc}}{\pi} \sum_{l=-\infty}^{\infty} \cos[(l+2)\pi] \times \cos\left[6\omega_c t + (2l-1)\omega_f t\right] J_{-1}(3\pi M), & \text{if } m = 3. \end{cases} \tag{14}$$

To generalize, for an ideal multilevel rectifier with N cascaded H-bridges, i.e., $(2N+1)$ levels, the first switching frequency based harmonics are centered at $(2N)$ times the switching frequency of each H-bridge when a phase-shifted carrier modulation is adopted.

In case of the seven-level converter shown in Fig. 2, ideally, the first switching frequency based harmonic component should be centered at six times the switching frequency of each H-bridge, given by (13). However, in a three-stage CMSST, when the VBCs are implemented in stage-1, the modulation indices of all H-bridges are not equal (i.e., $M_1 \neq M_2 \neq M_3$). As a result, the second and fourth switching frequency based harmonics given by (11) and (12) are nonzero. For a seven-level CMSST

$$v_{\text{msh}}(t) = \begin{cases} \text{non-zero}, & \text{if } m < 3 \\ \dfrac{4V_{dc}}{6\pi} \sum_{l=-\infty}^{\infty} \cos[(l+2)\pi] \times \cos\left[6\omega_c t + (2l-1)\omega_f t\right] \times \Big\{ J_{-1}(3\pi M_1) + J_{-1}(3\pi M_2) + J_{-1}(3\pi M_3) \Big\}, & \text{if } m = 3. \end{cases} \tag{15}$$

It can be understood from (14) and (15) that additional switching harmonics are visible in the harmonic spectrum when the VBCs are implemented in stage-1 of the CMSST. Therefore, the VBC in stage-1 nullifies the advantages of multilevel converter by introducing additional switching harmonics up to $(2N)$th switching harmonic.

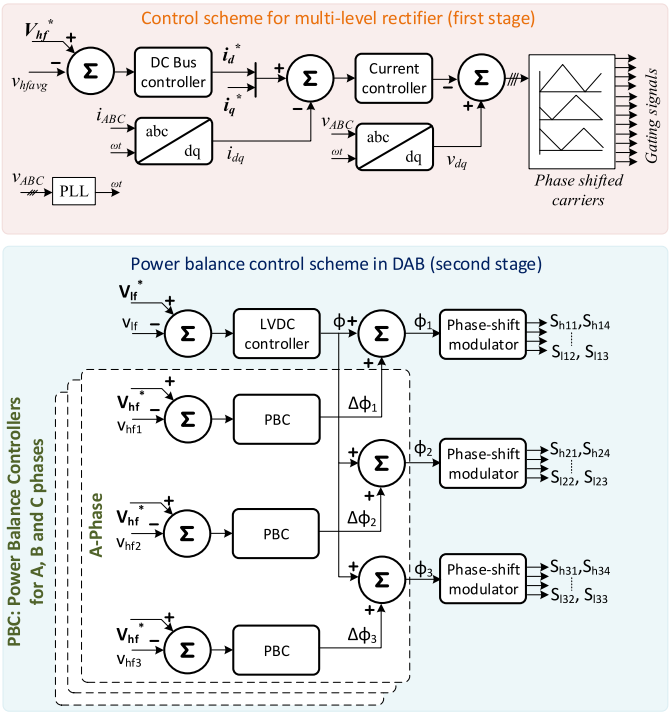

Fig. 6. PBC incorporated in stage-2 of SST.

B. PBC in Stage-2

PBC can be incorporated in stage-2 of the CMSST, i.e., DAB stage as shown in Fig. 6. As mentioned earlier and as shown in Fig. 6, the dc bus controller in stage-1 generates the necessary active power reference (i_d^*), to maintain the average of all the capacitors voltages as close as possible to the reference voltage (V_{hf}^*). But, this does not guarantee equal voltages across all capacitors. As shown in Fig. 6, the dc bus voltages at the output of stage-1 are balanced by introducing PBCs in stage-2 [40]–[42]. The PBCs add additional terms, viz., $\Delta\phi_1$, $\Delta\phi_2$, and $\Delta\phi_3$ to the phase shift (ϕ) generated by the LVDC controller.

$$P_n = \frac{nV_{hfn}V_{lf}\phi_{kn}(\pi-\phi_{kn})}{2\pi^2 f_{sd}L_s}\left(1 \mp \frac{\epsilon}{L_s} \pm \frac{\epsilon^2}{L_s^2}\right); \quad \text{where } \phi_{kn} = \phi + \Delta\phi_n. \tag{16}$$

These additional terms ($\Delta\phi_1$, $\Delta\phi_2$, and $\Delta\phi_3$) help to maintain equal power transfer through all DABs, which in turn ensures equal DAB input currents, i.e., $i_{D1} \approx i_{D2} \approx i_{D3} \approx i_D$ as shown in Fig. 3. Hence, (5) becomes

$$v_{hf1} = v_{hf2} = v_{hf3} = \left[\frac{m_a i_g - i_D}{C_{hf}}\right]t + < V_{hf} > . \tag{17}$$

Therefore, for any given modulation index (m_a) and grid current (i_g), all dc bus voltages converge to the same average value (V_{hf}^*).

1) Harmonic Analysis: All the H-bridges in stage-1 have the same modulation index, m_a, as shown in Fig. 6, and it can be modeled as follows:

$$m_a = M\cos(\omega_f t). \tag{18}$$

In this case, the second-, fourth-, and sixth-order switching harmonics (viz., $v_{2sh}(t)$, $v_{4sh}(t)$, and $v_{6sh}(t)$) can be obtained by substituting M_1, M_2, and M_3 as M in (11), (12), and (13)

$$v_{2sh}(t) = 0; \quad v_{4sh}(t) = 0 \tag{19}$$

$$v_{6sh}(t) = \frac{2V_{dc}}{\pi}\sum_{l=-\infty}^{\infty}\cos[(l+2)\pi] \cos\times\left[6\omega_c t + (2l-1)\omega_f t\right]J_{-1}(3\pi M). \tag{20}$$

It can be seen from (19) and (20) that when the PBCs are implemented in stage-2, the second and fourth switching frequency based harmonics can be eliminated. For a seven-level CMSST with PBCs

$$v_{msh}(t) = \begin{cases} 0, & \text{if } m < 3 \\ \dfrac{2V_{\text{dc}}}{\pi}\sum_{l=-\infty}^{\infty}\cos[(l+2)\pi] \\ \cos\times\left[6\omega_c t + (2l-1)\omega_f t\right]J_{-1}(3\pi M), & \text{if } m = 3. \end{cases} \tag{21}$$

The first harmonic frequency in the harmonic spectrum of the pole voltage of the CMSST (v_{ab}) in this case is centered at the $(2N)$th switching frequency based harmonic component. Equation (21) is similar to the ideal multilevel case, i.e., (14). This is due to the fact that the modulation indices of all the H-bridges in stage-1 are equal. Implementing the PBC in stage-2 is equivalent to operating the cascaded H-bridge as an ideal multilevel converter.

C. Grid-Side Filter Design

In an ideal multilevel rectifier, the MVAC grid-side filter (L_g) is designed to mitigate the $(2N)$th switching frequency based harmonic component and above [46]. However, when the VBCs are implemented in stage-1, switching frequency based harmonics starting from second switching frequency component exist in the pole voltage of multilevel rectifier as mentioned earlier. Hence, L_g must be designed to mitigate second switching frequency component instead of $(2N)$th component. As a result, the designer is forced to choose a higher value of L_g than normally required. This is a major drawback that needs to be considered while implementing the voltage balancing controller in stage-1 of the three-stage CMSST.

To illustrate the intensity of the problem, the value of L_g for a *3-ph* 3.3 kV, 50 kVA, seven-level CMSST (specifications in Table II) is compared for two cases: 1) VBC implemented in the first stage and 2) PBC implemented in the second stage. The approach followed to design L_g for the above specifications is as follows.

1) Modulation indices of stage-1: In case of VBC implemented in stage-1, the modulation indices of the multilevel rectifier (M_1, M_2, M_3) due to the mismatch in the series inductance of the isolation stage (L_s) are calculated from (7). In case of PBC implemented in stage-2, the modulation indices of stage-1 are equal to $\dfrac{V_g}{V_{hf}^*}$.

TABLE I
SUMMARY OF ANALYSIS PRESENTED IN SECTION III

Voltage balance control in	Modulation indices for stage-1	Phase shift for stage-2	Input current THD
stage-1	Unequal	Equal	High
stage-2	Equal	Unequal	Low

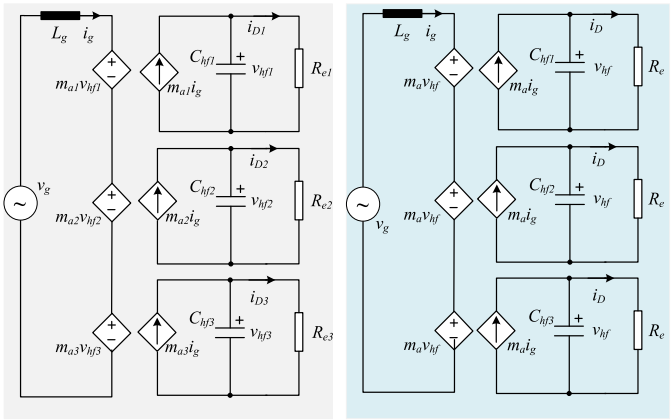

Fig. 7. Equivalent circuit model of multilevel rectifier. (a) When the VBCs are implemented in stage-1. (b) When the PBCs are implemented in stage-2.

2) The switching frequency related harmonics (along with their side bands) of V_{ab} are calculated using (11), (12), and (13).
3) The minimum value of L_g required to maintain the THD of grid current within 5% is calculated through iterations.

For a 10% mismatch in the series inductance value in the isolation stage, the L_g value required to maintain the THD of grid current below 5% is 90 mH if the VBCs are implemented in stage-1, whereas only 60 mH is sufficient in case of PBCs implemented in stage-2 for the considered specifications. It can be observed from this design that at least 50% higher inductance is required in case of VBCs implemented in the first stage to maintain the grid current THD below 5% compared to the PBCs in stage-2.

Some of the key take away points from the analysis presented in this section are summarized in Table I. The analysis is validated using simulation and experimental results in the subsequent sections.

D. Equivalent Circuit Models for Balance Controllers

It can be understood from (7) that when the VBCs are implemented in stage-1, the unbalance in the DAB converters input currents (i.e., i_{D1}, i_{D2}, and i_{D3}) is counteracted by creating an additional unbalance in stage-1 (i.e., $\Delta m_{a1} i_g$, $\Delta m_{a2} i_g$, and $\Delta m_{a3} i_g$) corresponding to each DAB converter. Therefore, this can be modeled as the cascaded H-bridge supplying an unbalanced load as shown in Fig. 7(a). Hence, the effect of VBCs on the grid current harmonics can be studied by connecting an unbalanced load to each H-bridge and implementing a VBC in stage-1.

TABLE II
SIMULATION PARAMETERS

Parameter name	Symbol	Value
Grid voltage	V_g	3.3 kV
Grid frequency	f_g	50 Hz
Nominal power	P_n	50 kVA
Specification of stage-1		
Grid side inductor	L_g	60 mH
DC link capacitor (individual)	C_{hf}	3.3 mF
Individual DC link voltage	V_{hf}	1260 V
No. of H-bridges	N	3
No. of levels	N_l	$(2N+1)$=7
Switching frequency of each H-bridge	f_s	0.5 kHz
Phase shift between carriers	ϕ_c	$2\pi/3$
Specification of stage-2		
Series inductor	L_s	63 μH
Switching frequency	f_{sd}	100 kHz
Filter capacitor	C_{lf}	300 μF

When the PBCs are implemented in stage-2, it is understood from (17) that the unbalance in the DAB converters input currents (i.e., i_{D1}, i_{D2}, and i_{D3}) is counteracted by having additional phase shift terms for each DAB (i.e., $\Delta\phi_1$, $\Delta\phi_2$, and $\Delta\phi_3$). Therefore, stage-2 always resembles a balanced load to the multilevel rectifier (i.e., stage-1). It can be modeled as the cascaded H-bridge supplying a balanced load as shown in Fig. 7(b). Hence, the effect of PBC on the grid current harmonics can be studied by connecting a balanced load to each H-bridge in stage-1.

IV. RESULTS AND DISCUSSIONS

The theoretical analysis presented in Section III is validated using simulations and experimental results in this section.

A. Simulation Results

A 3.3 kV, V_{L-L}, *3-ph* three-stage CMSST with the specifications shown in Table II was simulated using PLECS simulation software. Simulation results are presented in Figs. 8, 9, 10, and 11 for the two cases. Case 1): PBC implemented in stage-2 with 10% parameter mismatch (series inductance) in stage-2 and case 2): VBC implemented in stage-1 with 10% parameter mismatch (series inductance) in stage-2. The following are some of the inferences from the simulation results.

1) Grid voltage (v_g), grid current (i_g), dc bus voltages at the output of stage-1 (V_{hfn}, where $n = 1, 2,$ and 3), output current of the isolation stage ($i_{\text{DAB}n}$, where $n = 1, 2,$ and 3), modulation signals for first and second stages (i.e., m_{an}, where $n = 1, 2,$ and 3 and ϕ_{DAB}, respectively) when VBCs are implemented in stage-1 are shown in Fig. 8.
   Before activating the VBCs in stage-1 (i.e., $t < 2$ s in Fig. 8), the currents through the isolation stages (i_{DAB1}, i_{DAB2}, and i_{DAB3}) are unequal due to parameter mismatch (series inductance (L_s) value). As a result, the dc bus voltages at the output of stage-1 (viz., V_{hf1}, V_{hf2}, and V_{hf3}) settle at unequal voltages as shown in Fig. 8.
   After activating the VBCs in stage-1 (i.e., $t > 2$ s in Fig. 8), the modulation signals (m_{a1}, m_{a2}, and m_{a3}) to

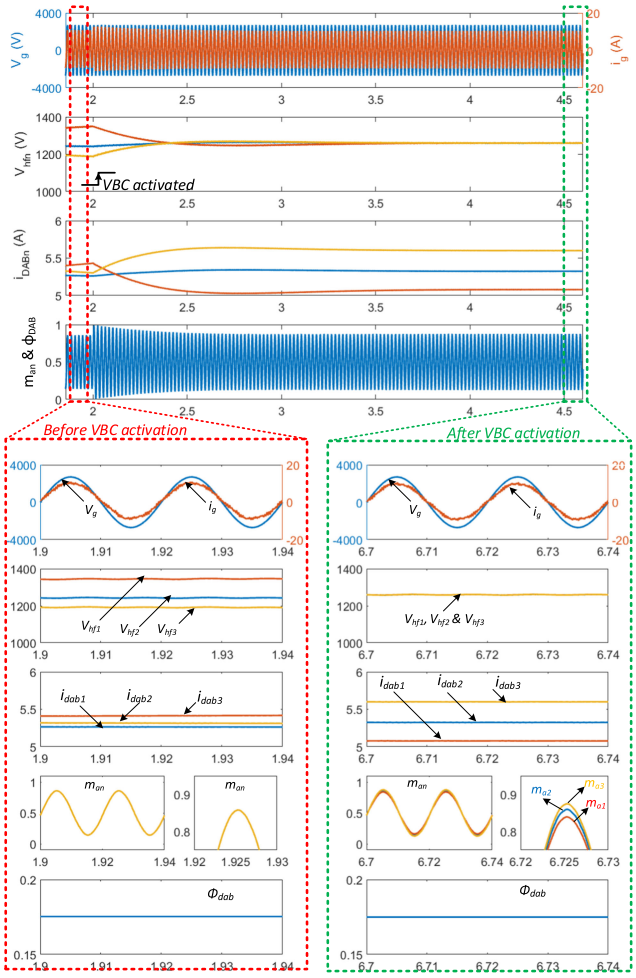

Fig. 8. Grid voltage (V_g), grid current (i_g), dc bus voltages at the output of stage-1 (V_{hfn}, where $n = 1, 2,$ and 3), output currents of isolation stage ($i_{\text{DAB}n}$, where $n = 1, 2,$ and 3), modulation signals to the cascaded H-bridge (m_{an}, where $n = 1, 2,$ and 3), and phase-shift control signal to the isolation stage (ϕ_{DAB}) before and after activating the VBC in stage-1.

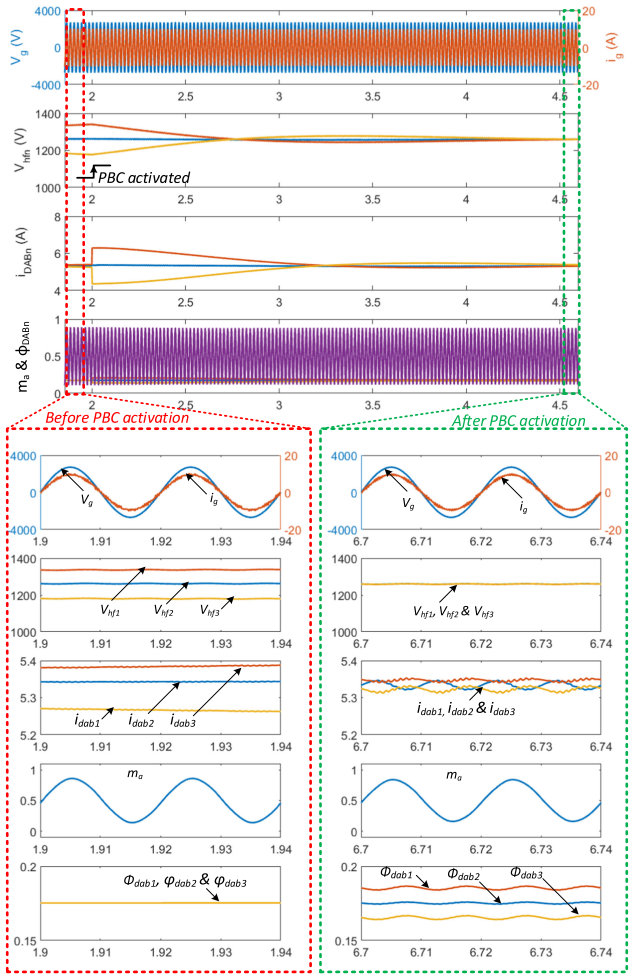

Fig. 9. Grid voltage (V_g), grid current (i_g), dc bus voltages at the output of stage-1 (V_{hfn}, where $n = 1, 2,$ and 3), output currents of isolation stage ($i_{\text{DAB}n}$, where $n = 1, 2,$ and 3), modulation signal to the cascaded H-bridge (m_a) and phase-shift control signals to the isolation stage ($\phi_{\text{DAB}n}$, where $n = 1, 2, and 3$) before and after activating the PBC in stage-2.

the cascaded H-bridge (stage-1) are adjusted such that all the output voltages of stage-1 (V_{hf1}, V_{hf2}, and V_{hf3}) converge to the reference voltage (1260 V). Since the power unbalance in the isolation stage is counteracted by creating an additional unbalance in the control signals to stage-1 ($m_{a1} \neq m_{a2} \neq m_{a3}$), the output currents of the isolation stage ($i_{\text{DAB}n}$) remain unbalanced as shown in Fig. 8.

2) Grid voltage (v_g), grid current (i_g), dc bus voltages at the output of stage-1 (V_{hfn}, where $n = 1, 2,$ and 3), output currents of the isolation stage ($i_{\text{DAB}n}$, where $n = 1, 2,$ and 3), modulation signals for first and second stages (i.e., m_a and $\phi_{\text{DAB}n}$, where $n = 1, 2,$ and 3) when PBCs are implemented in the isolation stage are shown in Fig. 9. Before activating the PBCs in the isolation stage (i.e., $t <$ 2 s in Fig. 9), the isolation stages draw unequal currents due to the parameter mismatch as mentioned in Section II. As a result, the dc bus voltages at the output of stage-1 settle at unequal voltages, i.e., $V_{hf1} \neq V_{hf2} \neq V_{hf3}$. However, their average value ($0.33 * (V_{hf1} + V_{hf2} + V_{hf3})$) equals to the reference value, i.e., 1260 V due to the average voltage controller in stage-1.

After activating the PBCs in stage-2 (i.e., $t >$ 2 s in Fig. 9), the control signals to the isolation stage (ϕ_{DAB1}, ϕ_{DAB2}, and ϕ_{DAB3}) are adjusted such that all the output voltages of stage-1 (V_{hf1}, V_{hf2}, and V_{hf3}) converge to the reference voltage (1260 V). The power unbalance due to the parameter mismatch in the isolation stage is corrected by varying the control signals to the isolation stage (ϕ_{DAB1}, ϕ_{DAB2}, and ϕ_{DAB3}) keeping equal modulation signal (m_a) to all H-bridges in stage-1. Therefore, all the output currents of isolation stage become equal after activating the PBCs in stage-2.

It can be clearly seen from Figs. 8 and 9 that both the voltage and PBCs balance the dc bus voltages at the output of stage-1. However, the unbalance created in the modulation index of stage-1 due to VBC (i.e., $m_{a1} \neq m_{a2} \neq m_{a3}$ as shown in Fig. 8) can cause additional switching frequency based harmonics in stage-1. To illustrate this clearly, the grid current (i_g) and grid-side multilevel voltage of stage-1 (V_{ab}) for both the cases

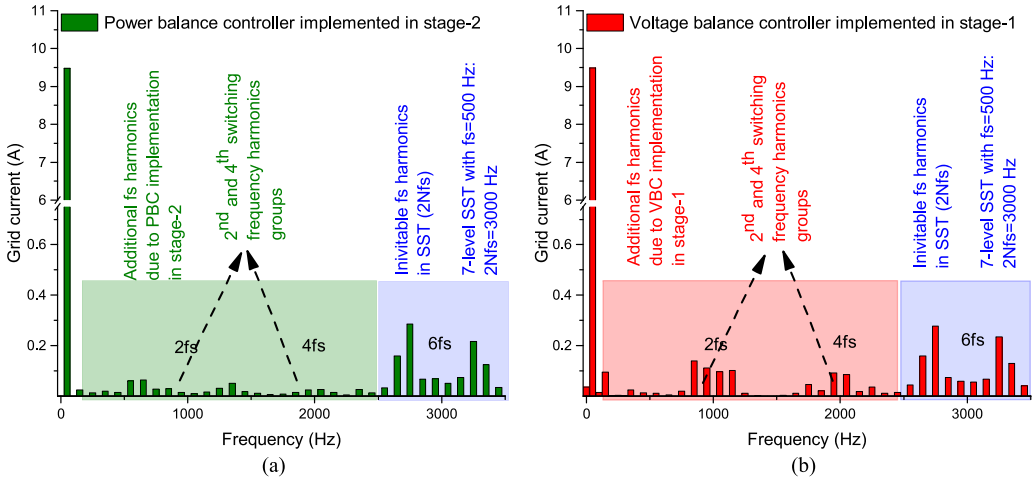

Fig. 10. (a) PBC implemented in stage-2 with 10% parameter mismatch (series inductance) in stage-2 [case 1)]; THD of grid current is 5.0%. (b) VBC implemented in stage-1 with 10% parameter mismatch (series inductance) in stage-2 [case 2)]; THD of grid current is 6.5%.

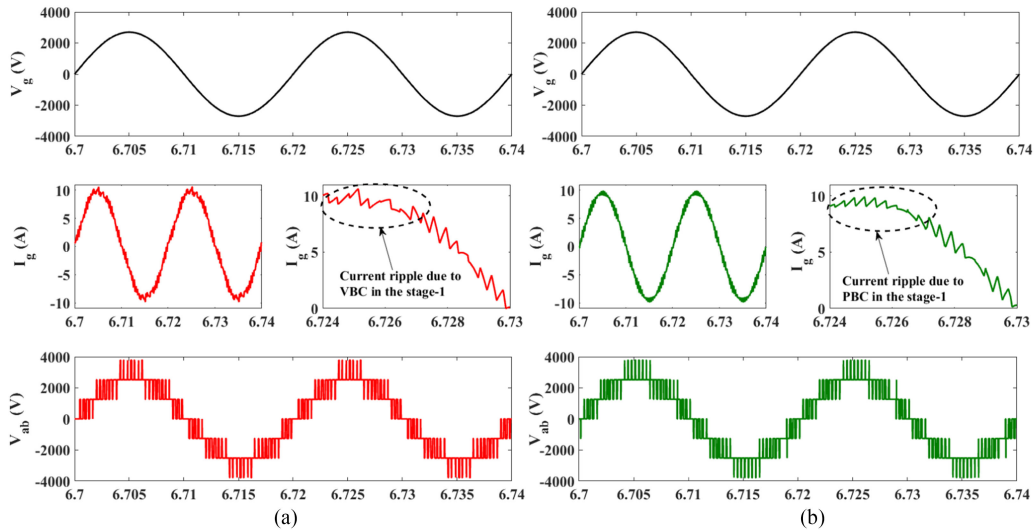

Fig. 11. Grid voltage (V_g), grid current (i_g), and the grid-side multilevel voltage (V_{ab}) when VBCs [case 2)] and PBCs [case 1)] are activated.

(case 1): PBCs implemented in the isolation stage and case 2): VBCs implemented in stage-1) are shown in Fig. 11. Also, the THD of grid current for case 1) and case 2) are shown in Fig. 10. The following are some of the inferences.

1) The grid current (i_g) for both case 1) and case 2) are shown in Fig. 11. It can be seen from this figure that the current ripple after activating the VBC in stage-1 is erratic [as shown in Fig. 11(a)] due to the presence of lower-order switching frequency based harmonic components in the grid current. As mentioned earlier, the VBCs in stage-1 introduce an unbalance in the modulation signals to each H-bridge ($m_{a1} \neq m_{a2} \neq m_{a3}$) to balance the dc bus voltages at the output of stage-1. On the contrary, the PBCs in stage-2 achieve equal voltages at the output of stage-1 by introducing an unbalance in the control signals to each converter in the isolation stage, i.e., $\phi_{\text{DAB1}} \neq \phi_{\text{DAB2}} \neq \phi_{\text{DAB3}}$, keeping the modulation signal in stage-1 equal, i.e., ($m_{a1} = m_{a2} = m_{a3}$). Equal modulation signals and dc bus voltages in stage-1 cancels the lower-order switching frequency based harmonics in cascaded multilevel converter resulting in a uniform high-frequency ripple as shown in Fig. 11(b).
2) The harmonic components of grid current for case 1) and case 2) are shown in Fig. 10. In an ideal multilevel converter case, the harmonics should be centered around (2N) times the switching frequency (i.e., $2Nf_s$, where N is the number of cascaded H-bridges). Therefore, for the presented simulation case with three H-bridge in stage-1, the switching frequency based harmonic components should be centered around $6f_s$ and the harmonic frequencies less than $6f_s$ should be absent. It can be seen from Fig. 10 that the harmonics less than $6f_s$ are dominant when the VBCs are implemented in stage-1 [case 2)] than its counterpart [case 1)]. The additional harmonics have increased the THD of grid current from 5.0% to 6.5%.

The simulation results confirmed the theory presented in Section III. The analysis is further substantiated with experimental results in the next section.

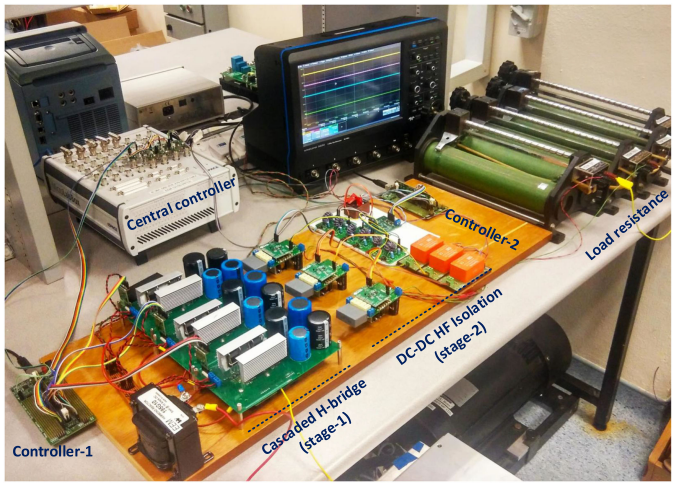

Fig. 12. Scale down hardware prototype stage-1 and stage-2 of single-phase three-stage CMSST. A centralized controller implemented in dSPACE MicroLabBox communicates appropriate voltage references to controller-1 and controller-2.

TABLE III
PARAMETERS OF THE TEST SETUP

Parameter name	Symbol	Value
Grid voltage	V_g	115 $Vrms$
Grid frequency	f_g	50 Hz
Nominal power	P_n	750 VA
Grid side inductor	L_g	5 mH
DC link capacitor (individual)	C_{hf}	3.3 mF
Individual DC link voltage	V_{hf}	70 V
No. of H-bridges	N	3
No. of levels	N_l	$(2N+1)$=7
Switching frequency of each H-bridge	f_s	0.5 kHz
Phase shift between carriers	ϕ_c	$2\pi/3$
LVDC bus voltage	V_{LVDC}	200 V
Switching frequency of isolation stage	f_{sd}	100 kHz
Controller sampling frequency	f_c	50 kHz

B. Experimental Results

A scale down hardware prototype of single-phase cascaded H-bridge, as shown in Fig. 12, is built with the specifications shown in Table III to validate the analysis presented in Section III. The conventional two-loop *d–q* control for stage-1 and voltage mode control for stage-2 are implemented in two TMS320f28335 TI DSPs (controller-1 and controller-2 in Fig. 12). The reactive power reference is kept as zero throughout the experiment. The experimental waveforms of grid voltage (v_g), grid current (i_g), and grid-side rectifier voltage (V_{ab}) for 50% and 100% load conditions are shown in Fig. 13(a) and (b), respectively. It can be clearly seen from these figures that the grid voltage (v_g) and grid current (i_g) are in phase irrespective of load.

As mentioned earlier, the parameters of all converters in the isolation stages are not same which results in unequal voltages at the output of stage-1.

In such cases, either VBC in stage-1 or PBC in stage-2 is required to balance the output dc bus voltages of stage-1. The dc bus voltages of three H-bridges along with the grid current before and after enabling the VBCs in stage-1 are shown in Fig. 14(a) and (b), respectively.

1) Before enabling the VBCs, the dc bus voltage of the first H-bridge is higher compared to second and third H-bridges ($V_{hf1} > V_{hf2}$ and $V_{hf1} > V_{hf3}$). This is due to the fact that the first isolation stage is delivering lower power compared to the other two isolation stages. This can be clearly observed from the output currents of isolation stage ($i_{\text{DAB1}} < i_{\text{DAB2}}$ and $i_{\text{DAB1}} < i_{\text{DAB3}}$).
2) After enabling the VBCs in stage-1, as shown in Fig. 14(b), all dc bus voltages at the output of stage-1 (V_{hf1}, V_{hf2}, and V_{hf3}) have converged to the same reference. This is due to the fact that the VBCs implemented in stage-1 adjust the modulation indices of each H-bridge such that (7) is satisfied.

The dc bus voltages of three H-bridges (V_{hf1}, V_{hf2}, and V_{hf3}) along with the grid current before and after enabling the PBCs in stage-2 are shown in Fig. 15(a) and (b), respectively.

1) It can be seen from Fig. 15(a) that before enabling the PBCs, the dc bus voltages of three H-bridges (V_{hf1}, V_{hf2}, and V_{hf3}) are not same because of unequal powers drawn by stage-2.
2) When the PBCs are enabled, as shown in Fig. 15(b), the individual control signals for the isolation stages are adjusted such that equal power are drawn from each H-bridge in stage-1.

Even though both voltage and PBCs can ensure equal dc bus voltages at the outputs of stage-1, the VBCs in stage-1 increase the THD of grid current by introducing additional switching harmonics. To illustrate these effects, the harmonic spectra of the grid current for 50% and 100% loads are measured experimentally using a Yokogawa WT3000 precision power analyzer and the results are presented in Fig. 16. Following are some of the inferences.

1) The harmonic spectrum of the grid current for the case where the PBCs are implemented in stage-2 is shown in case 1) of Fig. 16(a) and (b). It can be seen from these figures that the first and second switching frequency based harmonic components, i.e., $2f_s$ and $4f_s$, and their side bands are absent. This is due to the fact that the modulation indices of the three H-bridges in stage-1 are equal, i.e., $m_{a1} = m_{a2} = m_{a3}$. In such a scenario, the right-hand side terms of (11) and (12) get canceled, yielding an overall reduction in the grid current THD. In this case, the advantages quoted for cascaded H-bridge converters such as low grid-side filter inductance and low grid current THD are fully justified.
2) The harmonic spectrum of the grid current when the VBCs are implemented in stage-1 of SST with 10% and 20% parameter mismatch (series inductance) in stage-2 are shown in case 2) and case 3) of Fig. 16(a) and (b), respectively. Any power mismatch in the isolation stage result in an unequal load on each H-bridges in stage-1. The VBCs in stage-1 adjust the modulation indices, i.e., $m_{a1} \neq m_{a2} \neq m_{a3}$ such that all the dc bus voltages at the output of stage-1 are equal. As a result, the first and second switching frequency based harmonic components and their side bands appear in the harmonic spectrum, which

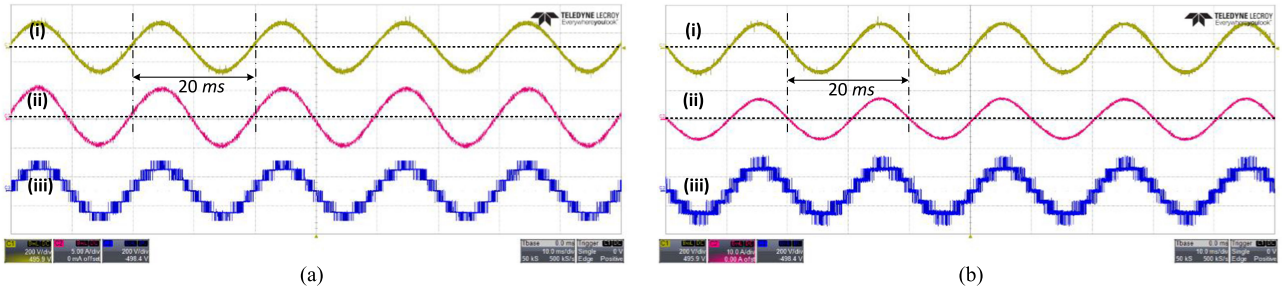

Fig. 13. Grid voltage, current, and gird side multilevel voltage waveform of stage-1 for 50% and 100% load cases. (a) (i) v_g: Grid voltage (scale: 200 V/div), (ii) i_g: Grid current (scale: 5 A/div), and (iii) v_{ab}: Grid-side rectifier voltage (scale: 200 V/div) at 50% load. Time scale: 10 ms/div. (b) (i) v_g: Grid voltage (scale: 200 V/div), (ii) i_g: Grid current (scale: 10 A/div), and (iii) v_{ab}: Grid-side rectifier voltage (scale: 200 V/div) at 100% load. Time scale: 10 ms/div.

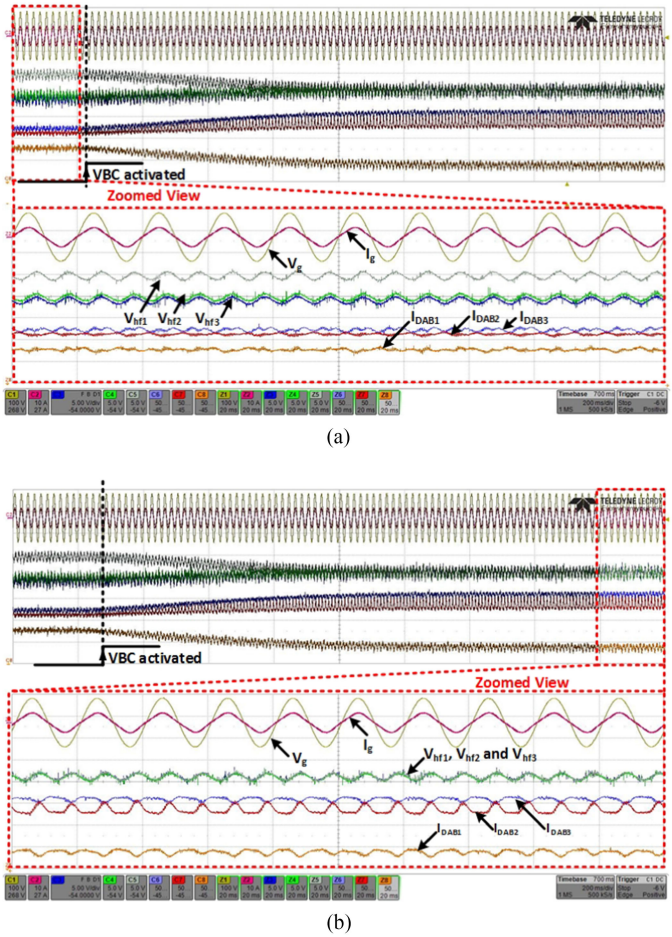

Fig. 14. V_g: Grid voltage (scale: 100 V/div), i_g: Grid current (scale: 10 A/div), V_{hf1}, V_{hf2} and V_{hf3}: DC bus voltage of first, second and third H-bridges, respectively (scale: 5 V/div), i_{dab1}, i_{dab2} and i_{dab3}: Output currents of first, second and third isolation stages, respectively (scale: 0.5 A/div); Time scale: 200 ms/div. (a) Zoomed view: Before activating the VBCs in stage-1. (b) Zoomed view: After activating the VBCs in stage-1.

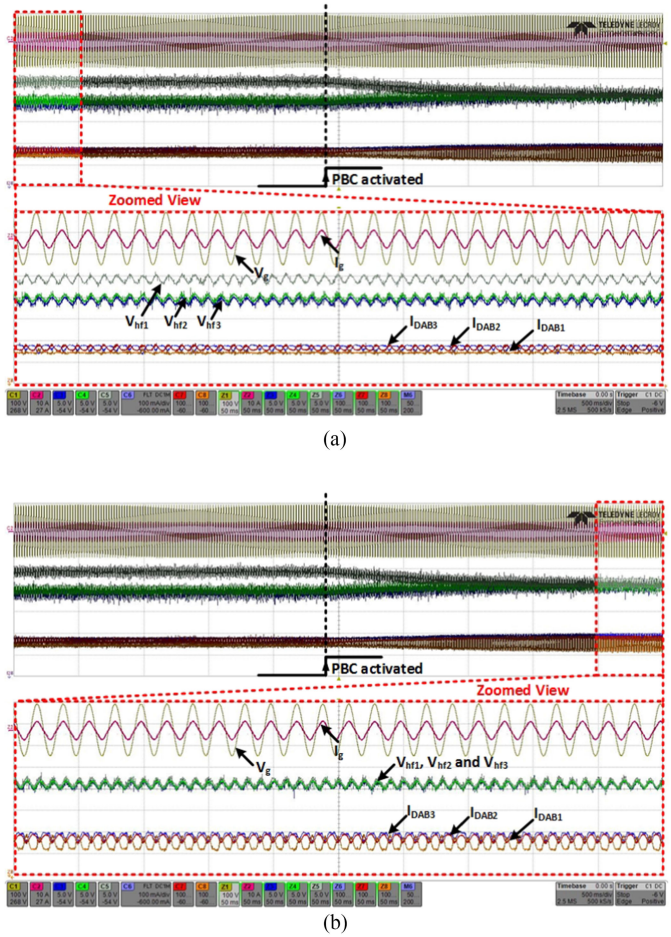

Fig. 15. V_g: Grid voltage (scale: 100 V/div), i_g: Grid current (scale: 10 A/div), V_{hf1}, V_{hf2}, and V_{hf3}: DC bus voltage of first, second, and third H-bridges, respectively (scale: 5 V/div), i_{dab1}, i_{dab2}, and i_{dab3}: Output currents of first, second, and third isolation stages, respectively (scale: 0.5 A/div); Time scale: 500 ms/div. (a) Zoomed view: Before activating the PBCs in stage-2. (b) Zoomed view: After activating the PBCs in stage-2.

can be seen clearly in Fig. 16(a) and (b). The unequal modulation indices result in a nonzero right-hand side terms in (11) and (12), yielding an overall increment in the grid current THD. In this case, the quoted advantages of multilevel converters are not completely realized.

3) As shown in Fig. 16(a), the measured THD of the grid current for case 2) and case 3) are 5.85% and 6.68%, respectively. It can be seen clearly from these results that the THD of the grid current has crossed the 5% current THD standards. To reduce the grid current THD below 5%, the value of grid-side filter inductor (L_g) has to be increased, which offsets the advantages of multilevel converters. Since anything higher than 20% parameter mismatch (series inductance) is not practical, the results are

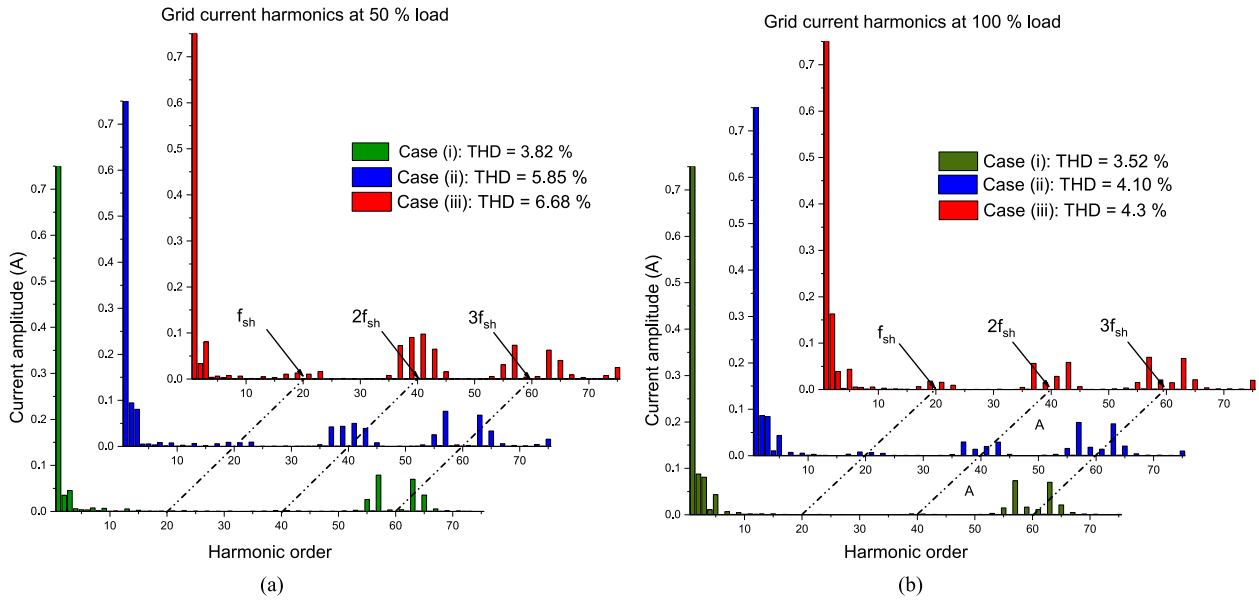

Fig. 16. Experimentally measured harmonic spectrum of MV side grid current for various cases. Case 1): PBC implemented in stage-2 with 20% parameter mismatch (series inductance) in stage-2. Case 2): VBC implemented in stage-1 with 10% unbalance in stage-2. Case 3): VBC implemented in stage-1 with 20% unbalance in stage-2. (a) 50% load case. (b) 100% load case.

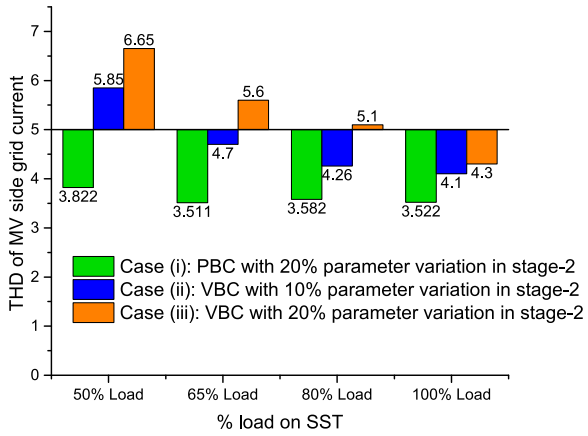

Fig. 17. THD of MV side grid current for various loads. Case 1): PBC implemented in the isolation stage with 20% parameter mismatch (series inductance) in isolation stage, case 2): VBC implemented in stage-1 with 10% parameter mismatch (series inductance) in isolation stage, and case 3): VBC implemented in stage-1 with 20% parameter mismatch (series inductance) in stage-2.

shown at 20% parameter mismatch (series inductance) case to bring out the intensity of this issue.

The overall THD profile of the grid current for 50% to 100% load conditions for all the three cases are shown in Fig. 17. It can be seen from these results that there is an overall increment in the THD of grid current when the VBCs are implemented in stage-1. The THD of the grid current is worst at light load with VBCs in stage-1. Hence, it is advisable to implement the PBCs in the isolation stage rather than the VBCs in the cascaded H-bridge stage.

V. Conclusion

In this paper, the effect of balance controllers on the THD of the grid current in a three-stage CMSST is studied. It is known that the balance controllers can be implemented either in the cascaded multilevel rectifier stage (stage-1) or the isolation stage (stage-2) in a three-stage CMSST. The Fourier series of the grid-side voltage of multilevel rectifier revealed that implementing VBCs in stage-1 introduces additional switching harmonics apart from the inevitable switching harmonics in a multilevel rectifier ($2N$ times the switching frequency of each H-bridge). Also, it is proven mathematically that stage-2 behaves like a balanced load to stage-1 if the PBCs are implemented in stage-2. With equal modulation indices and balanced load, the harmonics in the grid current are centered only at $2N f_s$. The same has been proven using the PLECS simulations and hardware results. Experiments on the hardware prototype revealed that the THD of the grid current has decreased from 6.65% to 3.8% at 50% load when PBC is implemented in stage-2 instead of having VBC in stage-1 with a 20% parameter mismatch (series inductance); and from 5.85% to 3.8% for the same case with 10% parameter mismatch (series inductance). When the VBC scheme is implemented in stage-1, the grid current THD followed an increasing trend as the load decreases and unbalance increases.

Therefore, it is advisable to implement the PBC scheme in the isolation stage rather than VBC scheme in stage-1 to have minimum THD with optimal grid-side filter inductor in a three-stage CMSST.

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