A -20 to 30 dBm Input Power Range Wireless Power System With a MPPT-Based Reconfigurable 48% Efficient RF Energy Harvester and 82% Efficient A4WP Wireless Power Receiver With Open-Loop Delay Compensation

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***Abstract*—This paper presents a reconfigurable wide input power range radio frequency (RF) energy harvester (EH) with alliance for wireless power (A4WP) wireless power receiver (WPR). A reconfigurable RF-DC converter for RF EH and maximum power point tracking algorithm are proposed to maintain high efficiency over a wide input power range –20 to +20 dBm. The A4WP WPR is designed and merged with the EH to receive power higher than +20 dBm. In order to improve the power conversion efficiency (PCE), the delay between the ac input voltage and current is compensated by the proposed open-loop delay compensation method. The chip is implemented in 0.18 μm bipolar-CMOS-double-diffused metal-oxide-semiconductor process (DMOS). The die area of the chip is 4.3 mm $\times$ 3.2 mm, including the pads. The proposed EH with WPR achieves a measured peak PCE of 48.19% with respect to the input power of 0 dBm at 900 MHz. It also has a peak PCE of 82.14% with respect to the input power of 30 dBm in an A4WP mode operation at 6.78 MHz.**

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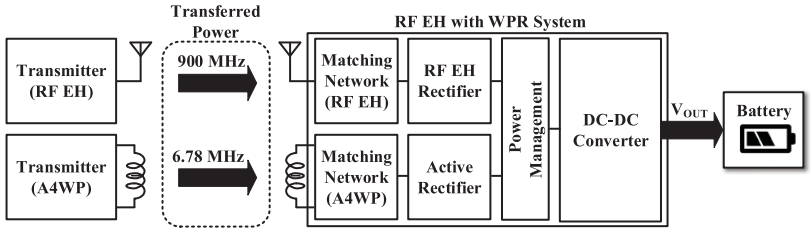


Fig. 1. Block diagram of the RF EH with WPR system.

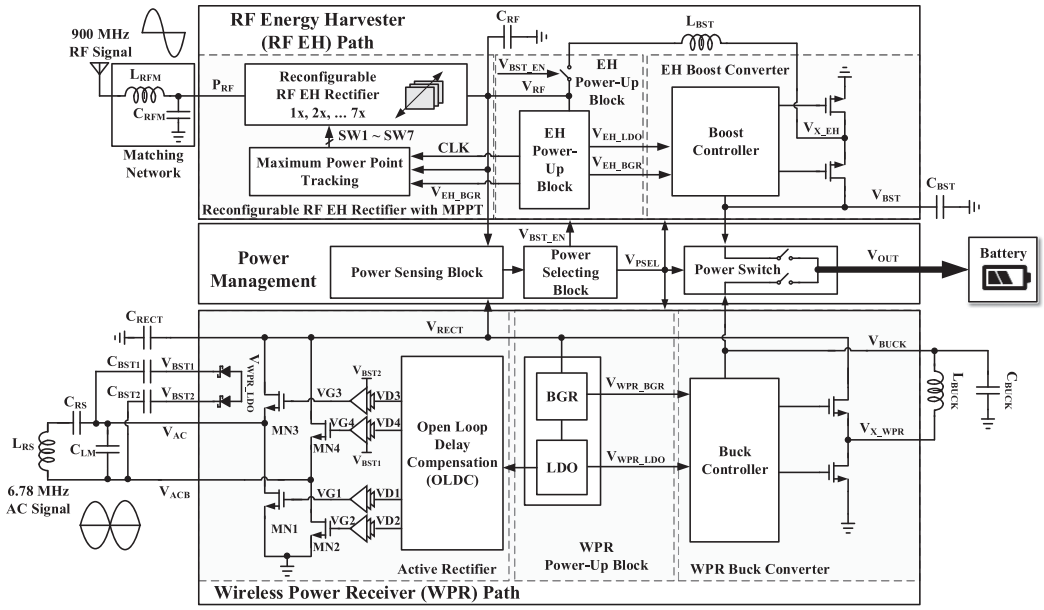


Fig. 2. Block diagram of the proposed RF EH with WPR.

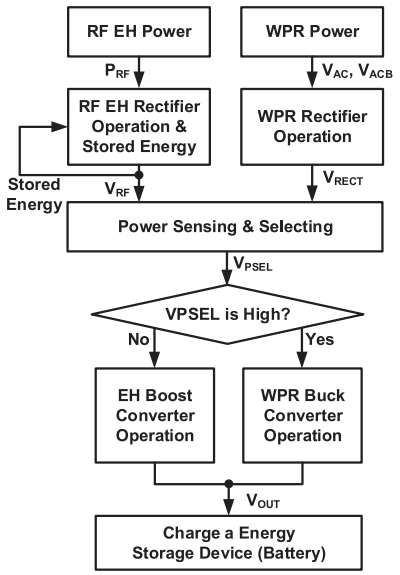
Thus, this paper proposes that RF EH needs to be merged with the WPR system to increase the charging distance and power levels at the same time, as shown in Fig. 1. Combining the WPR system with the EH not only slightly increases the area but also has a large burden. In the environment where the A4WP transmitter is configured, it is possible to receive high power using the WPR system, and when the distance to the transmitter is far, transfer power using the EH. Therefore, these systems can get great effect in terms of power delivery according to the distance. Furthermore, efficient power management needs to be proposed to efficiently control the optimum power sources.

This paper presents a reconfigurable wide input power range RF EH with A4WP WPR. A reconfigurable RF-DC converter for RF EH and maximum power point tracking (MPPT) algorithm are proposed to maintain high efficiency over a wide input power range by automatically selecting the optimum configuration. The A4WP WPR is designed and merged with the EH to receive power higher than 20 dBm when the A4WP power source is available. In order to compensate for the reverse leakage current of the rectifier, and to enhance the power conversion efficiency (PCE), an open-loop delay compensation (OLDC) block is proposed in the A4WP rectifier.

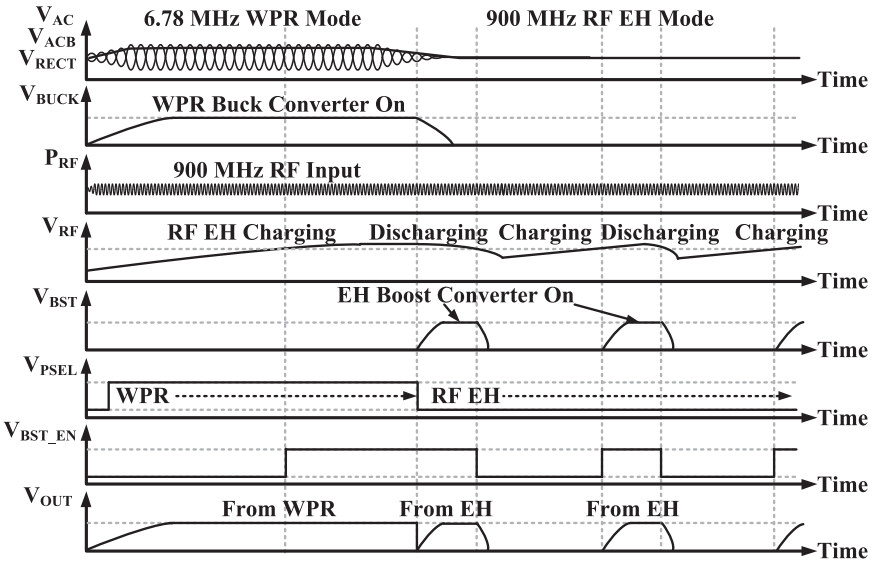
Section II describes the proposed EH with WPR. Section III presents the building block, while Section IV describes the experimental measurements that are taken on a test chip from the 0.18 μm bipolar-CMOS-double-diffused metal-oxide-semiconductor (BCD) implementation. Section V concludes the paper.

II. Architecture of the RF Energy Harvester With Wireless Power Receiver

Fig. 2 shows a block diagram of the proposed RF EH with WPR, which is comprised of two power paths (the RF EH path and the WPR path), and power management. The RF EH path is composed of the reconfigurable RF-DC converter for RF EH with MPPT, EH power-up block, and EH boost converter. The reconfigurable RF-DC converter for RF EH with MPPT converts the RF input signal power (P_{RF}) into dc power with high PCE. The reconfigurable RF-DC converter for RF EH, which is composed of a seven-stage RF-DC converter for RF EH unit, continuously stores the energy in the storage capacitor (C_{RF}). If the V_{RF} is in the input range that can drive the EH boost converter, the V_{RF} is connected to the EH boost converter by the $V_{\mathrm{BST\_EN}}$ signal from the power management. Therefore, it can convert ac power to dc power with high PCE and without wasting energy. The output of the EH boost converter (V_{BST}) is connected to the battery through the power switch.



(a)



(b)

Fig. 3. (a) Flowchart and (b) timing diagram of the RF EH with WPR system.

In addition to the RF EH path, the WPR path is composed of an active rectifier, WPR power-up block, and WPR buck converter. The active rectifier converts the power from the receiver coil (L_{RS}) into dc power with high PCE. The conventional active rectifier has reverse leakage current flows through the power NMOS transistors from the driver's delay, which degrades the overall efficiency [5]. An OLDC in the active rectifier is proposed to compensate for the reverse leakage current caused by the fast switching frequency of the A4WP standard, and to enhance the PCE. The output of the WPR buck converter (V_{BUCK}) is connected to the battery through the power switch.

The power management is composed of a power sensing block, power selecting block, and power switch. This efficiently manages the system by selecting the path connected to the battery. The signal levels (V_{RF} and V_{RECT}) of the two paths are compared in the power sensing block, and the power selecting block controls the power path using the V_{BST_EN} and V_{PSEL} signals. The V_{PSEL} signal selects the power switch between the RF EH path and the WPR path to the battery.

Fig. 3(a) and (b) shows the flowchart and timing diagram of the RF EH with the WPR system, respectively. Fig. 3(a) shows that it selects the optimum power path to the battery. The V_{PSEL} signal from the power selecting block selects the path to the battery between the RF EH path and the WPR path. The WPR path has higher priority over the RF EH path, since the power level of the WPR path is larger than that of the RF EH path. Fig. 3(b) shows that when the power is supplied to the WPR path by the wireless power transmitter (WPT), the V_{PSEL} signal

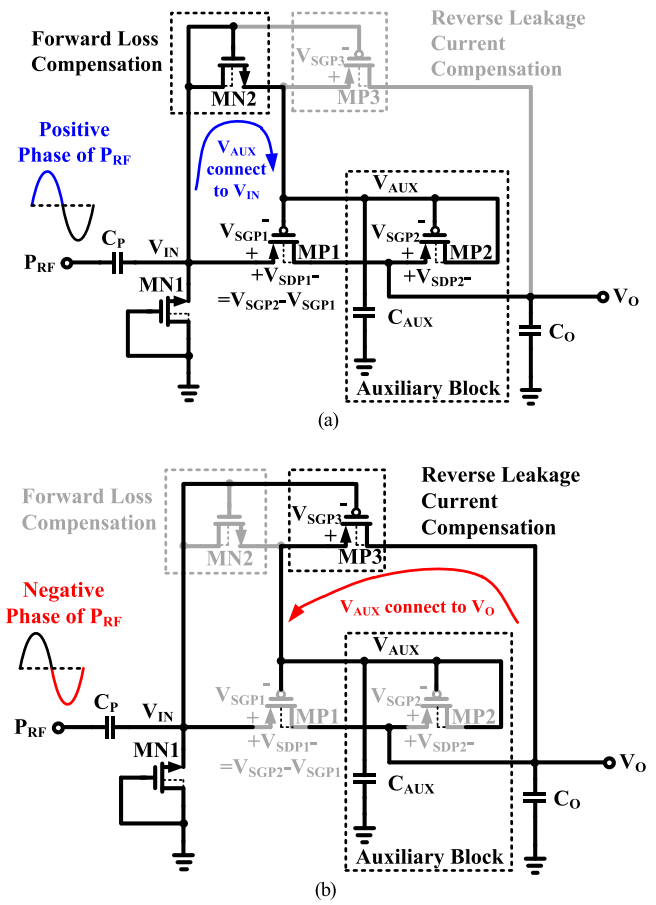


Fig. 4. Proposed RF-DC converter for RF EH with IVC and loss compensation in (a) positive phase and (b) negative phase of P_{RF}.

becomes high. At the same time, if the P_{RF} is available, the RF EH path continuously stores the energy to the C_{RF}. If the input of the WPR path is not available, the V_{PSEL} signal becomes low and the power is supplied to the battery through the RF EH path. By supplying the stored energy to the battery in this way, energy can be managed efficiently.

III. Building Blocks

A. RF-DC Converter for RF EH

The conventional Dickson charge pump architecture is widely used in rectifiers for RF EH applications [7], [8]. When switching metal-oxide-semiconductor field-effect transistors (MOSFETs) are turned ON or OFF, respectively, the efficiency of a rectifier is degraded by conduction loss and reverse leakage current. The threshold voltage of MOSFET is the main cause of conduction loss, which can be solved through some techniques that are presented in [9]–[11]. However, these architectures have limitations in terms of efficiency, since the maximum efficiency cannot be achieved with respect to variable input power levels, because the number of rectifier stages is fixed.

Fig. 4(a) and (b) shows the proposed RF-DC converter for RF EH with internal threshold voltage cancelation (IVC) and loss compensation in the positive phase and negative phase, respectively. NMOS (MN2) and PMOS (MP3) transistors dynamically control V_{SGP1}. This can achieve forward loss and reverse leakage current loss compensation. Fig. 4(a) shows that during the positive phase of the P_{RF} with respect to the ground, the MP1 and MP2 are forward-biased and forward loss is compensated by transistor MN2. This results in the reduction of the threshold voltage of transistors MP1 and MP2 increasing the forward current, since V_{AUX} is connected to V_{IN} through the MN2.

The V_{SGP3} transistor lies below the threshold voltage and it remains turned OFF. Fig. 4(b) shows that during the negative phase of the P_{RF} with respect to the ground, the transistors MP1 and MP2 are reversed-biased, which makes the V_{SGP3} of MP3 large enough to turn it ON while reducing V_{SGP1} and V_{SGP2} to zero. This results in reduced leakage current, since V_{AUX} is connected to V_O through the MP3. The minimum number of transistors is used to implement this loss compensation scheme, so those additional blocks do not cause considerable power loss. In the positive phase, the source and gate (through the MN2) of MP1 are connected to V_{IN}. Gate–source voltage is much greater than the threshold voltage $V_{\mathrm{GS}} > V_{\mathrm{TH}}$, so MP1 is "ON." In the negative phase, the MP1 is reversed biased and this makes V_{SGP3} large enough to turn it ON while reducing V_{SGP1}. Thus, the gate–source voltage of MP1 is less than the threshold voltage $V_{\mathrm{GS}} < V_{\mathrm{TH}}$, so MP1 is "OFF."

During the positive phase of P_{RF}, as the V_O is increased, V_{SGP2} increases continuously, because the source voltage of the MP2 is connected to V_O. When V_{SGP2} is equal to the threshold voltage of the MP1 ($|V_{THP1}|$), the MP2 drives the adjacent MP1 into the saturation region. During the negative phase of P_{RF}, the purpose of the C_{AUX} capacitor is to preserve some part of the charge lost during the reverse-conduction in the RF-DC converter for RF EH. Equations (1)–(3) describe the V_O as a function of $V_{\mathrm{IN}}, V_{SDP1}, V_{SDP2}$, and V_{AUX}

$$V_O = V_{\mathrm{IN}} - V_{\mathrm{SDP1}} \tag{1}$$

$$V_O = V_{\mathrm{SDP2}} + V_{\mathrm{AUX}}. \tag{2}$$

By adding (1) and (2), V_O can be represented as the following equation:

$$V_O = 1/2\ (V_{\mathrm{IN}} - V_{\mathrm{SDP1}} + V_{\mathrm{SDP2}} + V_{\mathrm{AUX}}) \tag{3}$$

where V_{SDP1} and V_{SDP2} are the voltage drops across the MP1 and MP2, respectively. When MP1 and MP2 are in the saturation region, V_{SDP1} and V_{SDP2} are the threshold voltages of MP1 and MP2, respectively. Similarly, the V_O can be represented by V_{SG} and V_{SD} of the MP1 and MP2 as (4)–(6)

$$V_{\mathrm{IN}} = V_{\mathrm{SGP1}} + V_{\mathrm{AUX}}. \tag{4}$$

Substituting (4) into (1), we obtain the following:

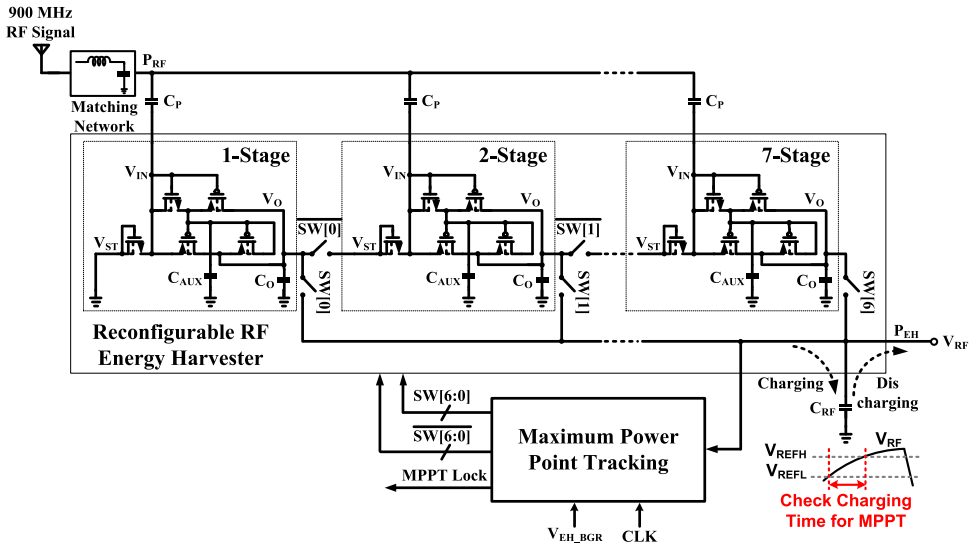
$$V_O = -V_{\mathrm{SDP1}} + V_{\mathrm{SGP1}} + V_{\mathrm{AUX}} \tag{5}$$

$$V_O = V_{\mathrm{SGP2}} + V_{\mathrm{AUX}}. \tag{6}$$

By subtracting (5) from (6), the following equation can be obtained:

$$V_{\mathrm{SDP1}} = V_{\mathrm{SGP1}} - V_{\mathrm{SGP2}}. \tag{7}$$

Equation (6) clearly shows that the value of V_{SGP2} increases proportionally with V_O. When V_{SGP2} equals the threshold



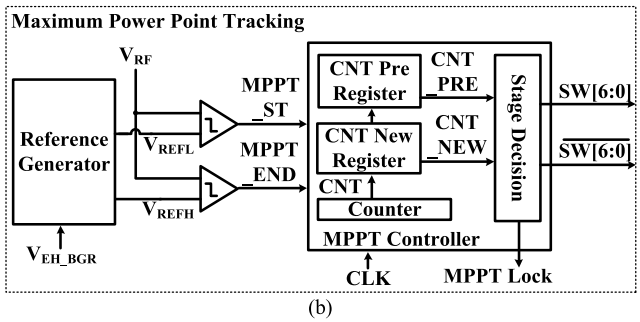


Fig. 5. Block diagram of (a) the proposed reconfigurable RF-DC converter for RF EH with MPPT and (b) maximum power point tracking.

voltage, MP1 enters the saturation region. Through (3) and (7), V_O can be derived as follows:

$$V_O = 1/2\ (V_{\rm IN} - V_{\rm SG1} + |V_{\rm THP1}| + V_{\rm SG2} - |V_{\rm THP2}| + V_{\rm AUX}),\ V_{\rm SG1} \sim V_{\rm SG2} = V_{\rm TH} \quad (8)$$

$$V_O = 1/2\ (V_{\rm IN} + |V_{\rm THP1}| - |V_{\rm THP2}| + V_{\rm AUX}). \quad (9)$$

Thus, the effect of the threshold voltage on the dc output voltage is minimized.

B. Reconfigurable RF EH With MPPT

Fig. 5(a) shows a block diagram of the proposed reconfigurable RF-DC converter for RF EH with the MPPT. In order to achieve the peak PCE with respect to the wide input range, a reconfigurable RF-DC converter for RF EH with MPPT is proposed to adjust the number of stages, by adding and controlling the switches. The basic structure of each stage is the proposed RF-DC converter for RF EH with IVC and loss compensation in Fig. 4. This is merged with stage control switches (SW[6:0]) to control the stage. After the external matching network, the $P_{\rm RF}$ charges the output capacitors of each stage, and is transferred to the following stages. Finally, the energy from the RF input signal is stored in $C_{\rm RF}$.

To analyze the reconfigurable RF-DC converter for RF EH with the MPPT, analysis of a basic one-stage RF-DC converter for RF EH can be used in [13]. If the output voltage (V_O) of one-stage RF-DC converter for RF EH is calculated through the supply charge and the lost charge, the following equation can be obtained as in [13]:

$$V_O = V_a - V_{\rm th} - \left(\frac{15\,\pi I_o\sqrt{2V_a}}{8\,\mu_n C_{\rm OX}\left(\frac{W}{L}\right)}\right)^{2/5}. \quad (10)$$

As a result, when V_a decreases in the one-stage rectifier, it is difficult to generate output voltage due to $V_{\rm th}$. Therefore, a series multistage rectifier structure should be used for operation with low input power.

The N multistage RF-DC converter for RF EH total charges in different regions are accounted for by

$$N \cdot \Delta\, Q_{\rm OUT} = \Delta Q_{\rm load} + N \cdot \Delta Q_{\rm leak} \quad (11)$$

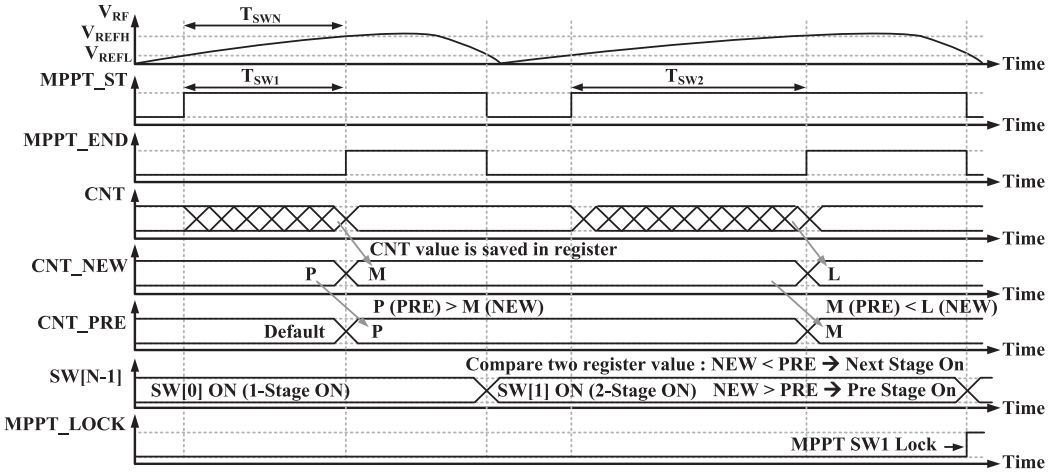


Fig. 6. Timing diagram of the proposed MPPT.

where V_{boost} is the incremental voltage of each stage. Using (10), V_{boost} is given by the following:

$$V_{\text{boost}} = V_a - V_{\text{th}} - N \cdot \left(\frac{1}{N} \frac{15\,\pi I_o \sqrt{2V_a}}{8\,\mu_n C_{\text{OX}} \left(\frac{W}{L}\right)} \right)^{2/5}. \quad (12)$$

If the body effect is ignored, (12) becomes

$$V_{\text{boost}} = V_a - V_{\text{th}} - N^{3/5} \cdot V_{ov} \quad (13)$$

where V_{boost} is the voltage increment per stage with no body effect, and V'_{ov} is defined as follows:

$$V_{ov} = \left(\frac{15\,\pi \sqrt{2v_a}}{8\,\mu_n C_{\text{OX}} \left(\frac{W}{L}\right)} \right)^{2/5}. \quad (14)$$

The output voltage of the *N*-stage rectifier is thus

$$\begin{aligned} V_{oN} &= N \cdot V_{\text{boost}} \\ &= N \cdot \left[V_a - V_{\text{th}} - N^{3/5} \cdot V_{ov} \right]. \end{aligned} \quad (15)$$

The output power of the *N* multistage RF-DC converter for RF EH is thus

$$\begin{aligned} P_{\text{out}} &= V_{oN} \cdot I_o \\ &= I_o \cdot \left[\text{N} \left(V_a - V_{\text{th}} \right) - N^{8/5} \cdot V_{ov} \right]. \end{aligned} \quad (16)$$

The efficiency of the *N* multistage RF-DC converter for RF EH is thus

$$\begin{aligned} \eta &= \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{oN} \cdot I_o}{P_{\text{in}}} \\ &= \frac{I_o}{P_{\text{in}}} \cdot \left[N \left(V_a - V_{\text{th}} \right) - N^{8/5} \cdot V_{ov} \right] \end{aligned} \quad (17)$$

when differentiating for *N* in order to determine *N* at which η becomes maximum

$$\begin{aligned} \eta' (N) &= \frac{d}{dN} \left\{ \frac{I_o}{P_{\text{in}}} \cdot \left[N \left(V_a - V_{\text{th}} \right) - N^{8/5} \cdot V_{ov} \right] \right\} \\ &= \frac{I_o \cdot (V_a - V_{\text{th}})}{P_{\text{in}}} - \frac{8}{5} V_{ov} \cdot N^{3/5}. \end{aligned} \quad (18)$$

In (19), $\eta'(N)$ is set to 0 in order to confirm *N* at which η becomes maximum

$$N = \left(\frac{I_o \cdot (V_a - V_{\text{th}})}{P_{\text{in}}} - \frac{5}{8 \cdot V_{ov}} \right)^{5/3}. \quad (19)$$

In (19), I_o is the load current, V_{th} is the characteristic of the device, and P_{in}, V_a, and V_{ov} are determined according to the input power. As a result, the *N* of the multistage RF-DC converter for RF EH having maximum efficiency is determined according to the input power and load current. For example, when the input power is 0 dBm, and the load impedance is 1 MΩ, the *N* of the multistage RF-DC converter for RF EH having maximum efficiency is the two-stage by (19). When the input power is –20 dBm, and load impedance is 1 MΩ, the *N* of the multistage RF-DC converter for RF EH having the maximum efficiency is the four-stage by (19).

In the conventional MPPT methods, the maximum power is found by placing storage capacitors as an array, and using the relative value of the output power integrated into the capacitor [15]–[17]. In that case, the PCE is degraded, and additional chip size is needed, due to the capacitor array. In this paper, only one storage capacitor is used to generate the dc voltage in EH. Fig. 5(b) shows that the proposed MPPT is composed of the MPPT controller, comparators, and reference generator. In the proposed MPPT, the output power is calculated by the charging time of the C_{RF}. The stage decision of the MPPT controller determines the optimum switch control signals, SW[6:0], to select the number of stages for the reconfigurable RF-DC converter for RF EH based on the charging times.

Fig. 6 shows a timing diagram of the proposed MPPT. The proposed MPPT selects the optimum stage by calculating the output power in terms of the time (T_{SWN}). As the output power is increased, the charging time is decreased when the storage capacitor and the reference voltages (V_{REFH} and V_{REFL}) are the same. The proposed MPPT measures the charging time of V_{RF} from V_{REFL} to V_{REFH} by the digital counter. Fig. 6 shows that when the one-stage is turned ON (SW[0] ON), the charging time of V_{RF} is counted and saved as *M* by the internal counter.

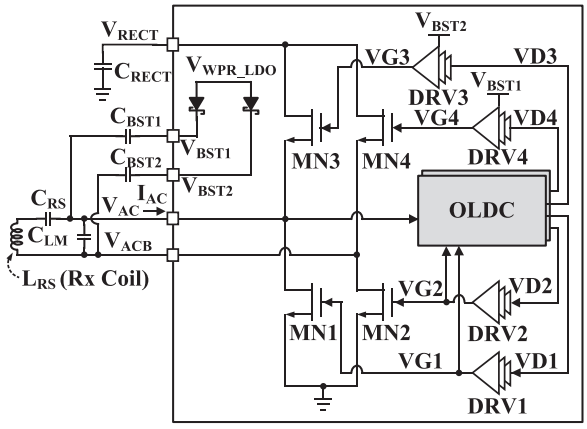


Fig. 7. Block diagram of active rectifier for A4WP WPR.

In a similar way, when one-stage and two-stage are turned ON (SW[0] and SW[1] ON), L becomes the new counted value corresponding to the charging time of V_{RF}. Then, after saving two consecutive counted values, the M and L are compared. By this algorithm, as the counted value is decreased continuously until the number of enabled stages is N with the rectifier switch control signal, SW[$N-1$] , and then the counted value is increased when the stage $(N+1)$ is enabled with the rectifier switch control signal, SW[N], the MPPT controller locks to the rectifier switch control signal, SW[$N-1$] . By using the proposed MPPT algorithm, additional blocks, such as capacitor array, are not needed, so that the current consumption and size can be reduced, enhancing the PCE of the RF-DC converter for RF EH.

C. Active Rectifier for A4WP Wireless Power Receiver

Fig. 7 shows a block diagram of the proposed active rectifier for the A4WP WPR. The rectifier converts the ac voltages (V_{AC} and V_{ACB}) into dc voltage (V_{RECT}). The core of the rectifier is composed of four power NMOS transistors: MN1 and MN2 for the low side, and MN3 and MN4 for the high side. For the high side core implementation, PMOS cross-coupled structure also can be used to reduce the switching loss, as they are part of the *LC* resonant tuning capacitor that do not dissipate power [8], [9]. However, the mobility of PMOS is lower than that of the NMOS transistor so that the size of the PMOS should be designed as big as possible to reduce the V_{DS} voltage drop of the PMOS. Moreover, the output of the proposed rectifier (V_{RECT}) is higher than 5 V for the WPR buck converter to generate the output voltage (V_{BUCK}) as 5 V. As a result, core transistors in the proposed rectifier are selected as high voltage lateral double-diffused metal-oxide-semiconductor (LDMOS) to guarantee the device reliability. By the reason explained above, NMOS transistors are used for implementing high-side structure to reduce the size of the core while maintaining the small V_{DS} voltage drop. Boosting voltages ($V_{\mathrm{BST1}}, V_{\mathrm{BST2}}$) are generated and used to drive the high-side NMOS (MN3, MN4) and to guarantee 5 V V_{GS} voltage of MN3 and MN4. In A4WP standard, parasitic capacitance and the internal circuit delay cause the dominant

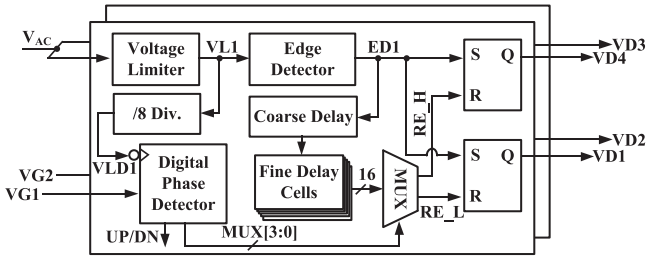


Fig. 8. Block diagram of open-loop delay compensation.

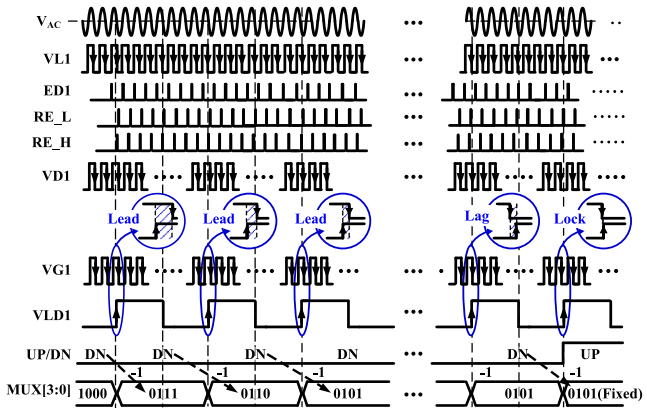


Fig. 9. Timing diagram of the OLDC.

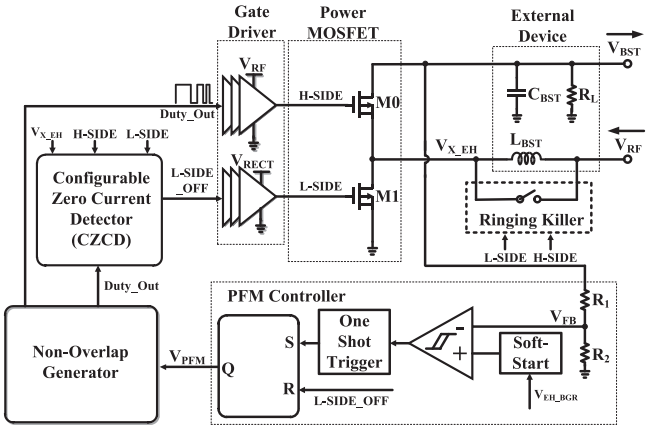


Fig. 10. Block diagram of the EH boost converter.

switching power losses, since the switching frequency of the A4WP standard is 6.78 MHz and very fast compared to other standards such as WPC and PMA. Even though the switching signals are generated from the accurate power transmitter, delays from the four drivers (i.e., DRV1–DRV4) cause delayed switching signals (i.e., VG1–VG4) for the power NMOS transistors, so that reverse leakage current flows through the power NMOS transistors, and degrades the overall efficiency [5].

The OLDC block is proposed to compensate for the reverse leakage current caused by delays of internal circuits, including drivers, and to enhance the PCE. Fig. 8 shows a block diagram of the proposed OLDC. This consists of a voltage limiter (VL),

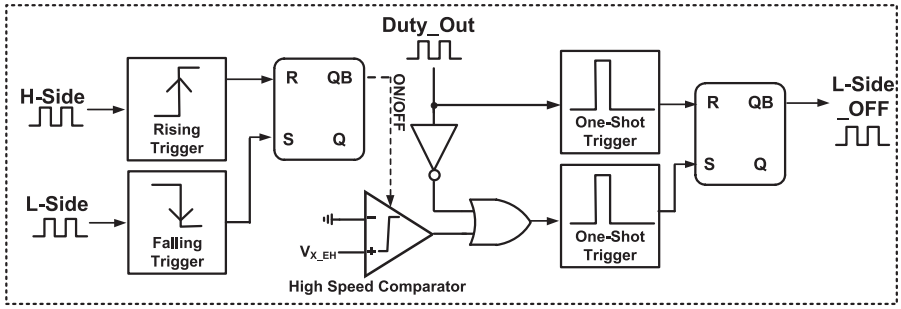


Fig. 11. Block diagram of CZCD.

edge detector (ED), digital phase detector (DPD), divided-by-8 divider (/8 Div.), coarse delay, fine delay cells, multiplexer (MUX), and SR latch. The purpose of the OLDC shown in Fig. 8 is to synchronize the falling edge of the output of the driver, VG1, with the zero-crossing point of the ac signal, $V_{\rm AC}$, so that the MN1 can be turned OFF at the exact moment that the $V_{\rm AC}$ becomes negative and $V_{\rm ACB}$ rises from negative to positive.

Fig. 9 shows that the DPD is used to compare the falling edges of VLD1 and VG1, which are the limited voltage signal of $V_{\rm AC}$ and the final gate control signal of MN1, respectively. The falling edge of VL1 is generated as RE_L, which is the delayed signal of ED1 through the coarse delay and fine delay cells. Sixteen delayed signals of coarse delay and fine delay cells are applied to the input of MUX and can be selected by MUX[3:0] from DPD, so that the falling edge of VG1 can be synchronized with that of VL1. When the duties of VD1 and VD4 are changed after the comparison, it takes time for the internal signals of the rectifier to settle down.

To guarantee stable operation, the frequency of VL1 is divided into 8, and applied as a clock of OLDC. When the falling edge of VLD1 lags that of VG1, the value of MUX[3:0] is added by 1 by the DPD, so that the delay can be increased. Otherwise, when the falling edge of VLD1 leads that of VG1, the value of MUX[3:0] is subtracted by 1 by the DPD so that the delay can be decreased. Through the SR latch, ED1 signal is used as set signal and RE_L is used as reset signal, so that VD1 is generated, and applied to the input of DRV1. For the high side, the delay of DRV4 is longer than that of DRV1, due to the level shifter inside DRV4 for making $V_{\rm GS}$ of MN4 as 5 V. Thus, the RE_H signal for the high side is selected to be less than RE_L signal for the low side by "0101," considering the delay difference between the high side and low side. The comparison of the DPD repeats for certain times and it is finished with the rising edge of LCK signal when the falling edges of VLD1 and VG1 are synchronized. Reducing the current consumption caused from forming the closed loop can additionally enhance the PCE.

D. Energy Harvesting Boost Converter

Fig. 10 shows a block diagram of the proposed EH boost converter. Since the output voltage of the RF-DC converter for RF EH is not sufficiently high to charge the battery directly, a low-power EH boost converter is designed in this paper. To maximize the PCE and reduce the power loss, a configurable zero current detector (CZCD) and ringing killer are proposed. The proposed EH boost converter is composed of a power MOSFET, gate driver, CZCD, nonoverlap generator, pulse frequency modulation (PFM) controller, and ringing killer. Typically, the target applications of an EH system operate under a light load current of less than 1 mA. Since the PFM can reduce the on-time of the power MOSFET more than can pulsewidth modulation, PFM can increase the efficiency under light load. Thus, in order to achieve high efficiency, PFM is adopted in this paper.

The ringing killer blocks the inductor resonance that can cause unnecessary power loss at the $V_{X\_{\rm EH}}$ node when both the power MOSFETs (M0, M1) are turned OFF [18]. In the discontinuous conduction mode (DCM), the low-side gate (M1) of the EH boost converter is turned ON and OFF after the operation of the high-side gate (M0). When the high-side gate and low-side gate are turned OFF simultaneously, inductor ringing is generated at the zero current of the inductor in the DCM. To block the ringing of the inductor, the ringing killer shortens $V_{\rm RF}$ and $V_{X\_{\rm EH}}$ node, and this scheme can achieve reduction of the power loss.

Fig. 11 shows a block diagram of the proposed CZCD. To optimize the current of the high-speed comparator by automatically changing the power enable signal of the high-speed comparator, the CZCD is proposed. The high-speed comparator is enabled by the proposed CZCD only when zero current is sensed. When the CZCD senses zero current using the $V_{X\_{\rm EH}}$, the inductor current becomes zero. It eventually turns OFF the low-side power MOSFET (M1). This efficiently reduces the current consumption of internal circuits, and improves the PCE more as the load current is decreased.

E. Wireless Power Receiver Buck Converter

Fig. 12 shows a block diagram of the WPR buck converter. When power MOSFETs (M0, M1) are turned ON at the same time, the proposed WPR buck converter does not need the dead-time generator to prevent leakage current. The all digital zero current detector (AD-ZCD) is proposed to replace the conventional dead-time generator. The AD-ZCD senses the duty of the high-side pulse, low-side pulse, and the $V_{X\_{\rm WPR}}$ node without using comparators to reduce the current consumption, and adjusts the duty of the gate control signal of M1.

The conventional ZCD has a large power consumption to sense the zero inductor current point using a high-performance comparator [17], [18]. Fig. 13 shows a block diagram of the

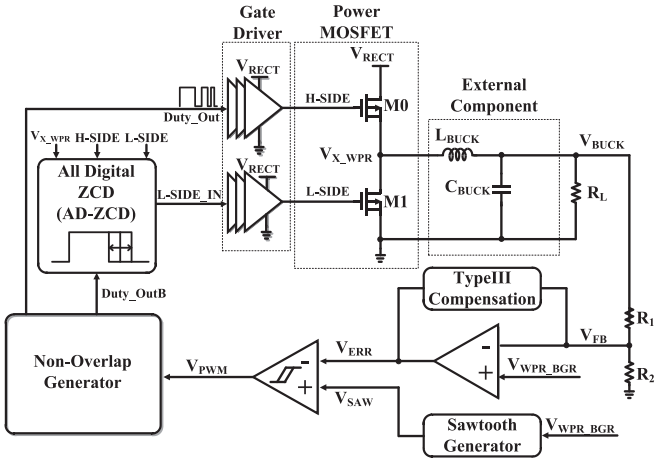


Fig. 12. Block diagram of the WPR buck converter.

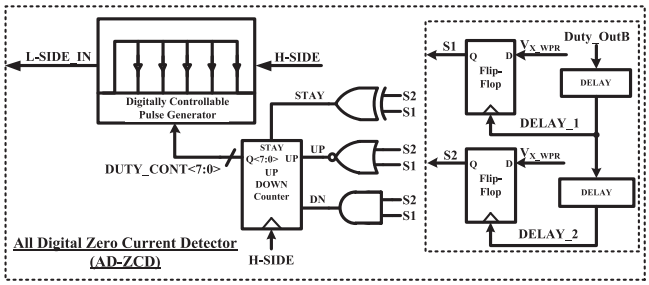


Fig. 13. Block diagram of AD-ZCD.

proposed AD-ZCD. The current consumption of the AD-ZCD is 2 μA, which is smaller than the current consumption of the conventional ZCD. Therefore, the AD-ZCD can improve the efficiency by reducing the control loss that takes a large proportion of the DCM dc–dc converter in the light load current conditions. It is also possible to prevent the efficiency reduction due to ZCD timing errors caused by the comparator offset. The proposed AD-ZCD detects the inductor current indirectly at the time of the switching off in the previous period while monitoring the voltage of V_{X_WPR} node for the switching of M1 at every cycle. The AD-ZCD continuously senses the voltage of V_{X_WPR} node with DELAY_1 and DELAY_2 signals. So, if the (S1, S2) value is changed by the load condition or PVT variations, the AD-ZCD detects the instant when the inductor current is 0 A with duty control of Duty_OutB and UP/DOWN Counter. Through the operation of the digital AD-ZCD, the digitally controllable pulse generator is thereby generating suitable pulsewidth along with flip-flop.

IV. Experimental Results

Fig. 14 shows a microphotograph of the proposed EH with WPR. The die size is 4.3 mm $\times$ 3.2 mm including electrostatic discharge designed with 1P6M 0.18 μm CMOS.

Fig. 15 shows the measurement environment of the EH with WPR. In the test board, the operations of EH and WPR are measured through the test ports at the output of the EH with WPR ($V_{\rm OUT}$), the inputs of the EH ($P_{\rm RF}$) and WPR ($V_{\rm AC}$, $V_{\rm ACB}$).

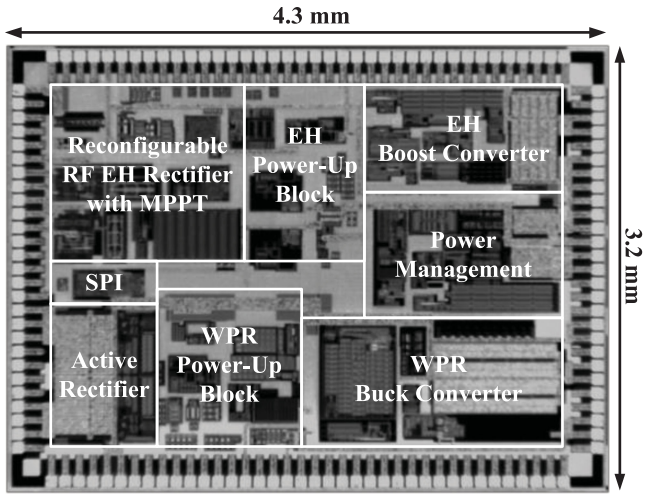


Fig. 14. Chip microphotograph.

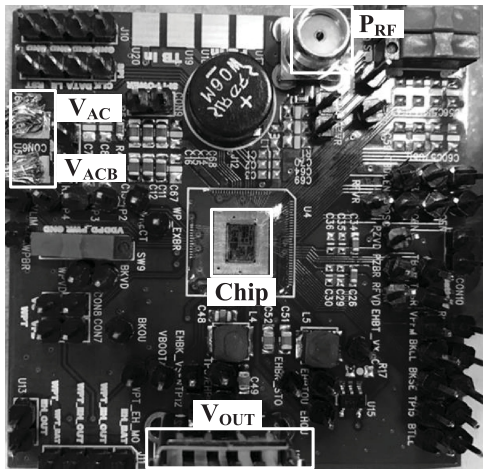


Fig. 15. Measurement environment of the RF EH with WPR.

Fig. 16 shows the measurement result of the RF EH with WPR system. Fig. 16 shows that it selects the optimum power path to the battery according to the input source. The $V_{\rm PSEL}$ signal from the power selecting block selects the path to the battery between the RF EH path and the WPR path. When the power is supplied to the WPR path by the WPT, the $V_{\rm PSEL}$ signal becomes high. If the input of the WPR path is not available, the $V_{\rm PSEL}$ signal becomes low and the power is supplied to the battery through the RF EH path. It can be seen that $V_{\rm OUT}$ is supplied with 5 V through the WPR or EH path depending on the $V_{\rm PSEL}$.

Fig. 17 shows the measurement results of the EH path including the power-up sequence. When the output of the rectifier, $V_{\rm RF}$, is 3.5 V after the settling time of EH path, the output of EH LDO, $V_{\rm EH\_LDO}$, is regulated to 1.8 V. Also, as the $V_{\rm EH\_LDO}$ and $V_{\rm RF}$ settle to 1.8 and 3.5 V, respectively, the EH boost converter is turned ON, and the output of the EH Boost Converter is regulated to 4.94 V.

Fig. 18 shows the measured initial power-up sequence of the WPR path. When the VRECT is 7 V after the settling time of WPR path, VWPR$_{\rm _BGR}$ settles to 1.2 V. Also, as the $V_{\rm WPR\_LDO}$

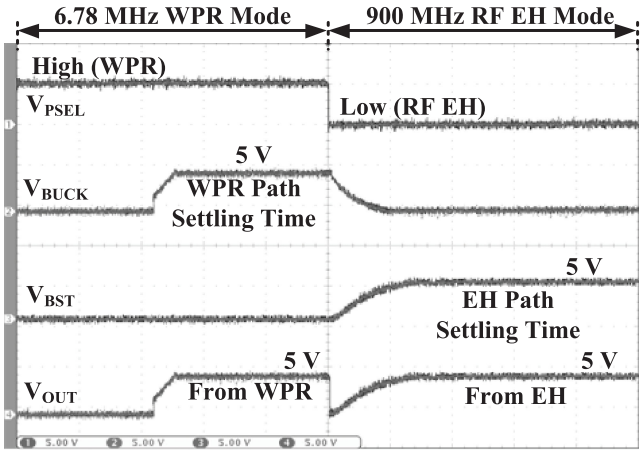


Fig. 16. Measurement result of the RF EH with WPR system.

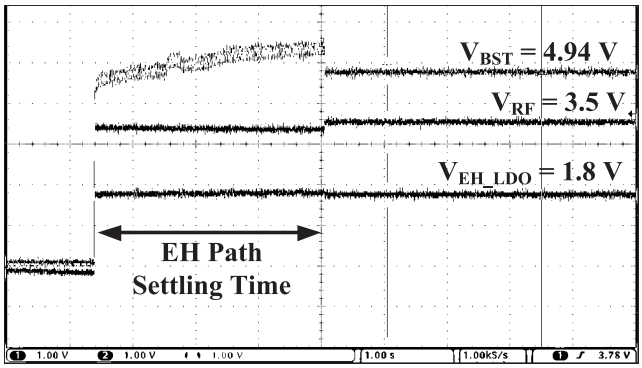


Fig. 17. Measurement result of the RF EH path.

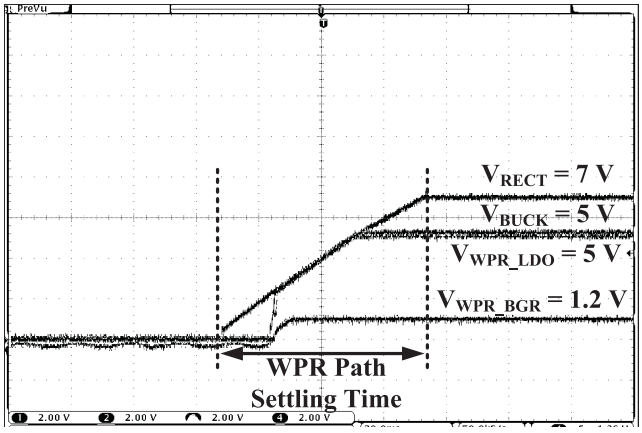


Fig. 18. Measurement result of the WPR path.

and V_{RECT} are charged to 5 and 7 V, respectively, the output of the WPR buck converter is turned ON, and the output of the WPR buck converter (V_{BUCK}) is regulated to 5 V.

Fig. 19 (a) and (b) show the simulation results of the proposed RF-DC converter V_{RECT} and efficiency for comparison with the conventional RF-DC converter structure, respectively. The result of the conventional structure is simulated using the structure in [7]. The proposed RF-DC converter for RF EH is composed of IVC and loss compensation in the positive phase and negative phase. As can be seen from the result, the proposed RF-DC converter architecture has a high power conversion efficiency of over 8% for the same input power.

Fig. 20(a) and (b) shows the measured transient waveforms and efficiencies, respectively, of the RF-DC converter for RF EH when the input power level is 0 dBm. Fig. 20(a) shows that when the input power is 0 dBm, RF-DC converter for RF EH locks to the two-stage by the MPPT operation, achieving maximum efficiency.

Fig. 20(b) shows that the RF-DC converter for RF EH has the maximum efficiency at two-stage when the input power is 0 dBm. Fig. 20(a) and (b) shows that the optimum number of stages is two for the input power level of 0 dBm, where the corresponding efficiencies are 48.19%.

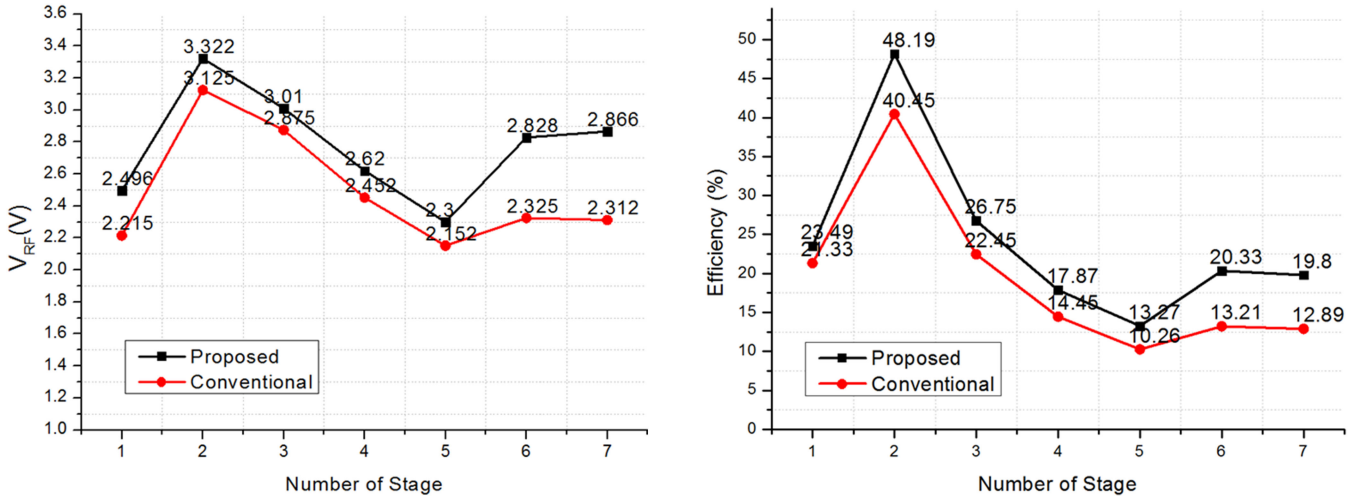
Fig. 21(a) and (b) shows the measured transient waveforms and efficiencies of the RF-DC converter for RF EH when the input power level is –20 dBm. Fig. 21(a) shows that when the input power is –20 dBm, RF-DC converter for RF EH locks to the four-stage by MPPT operation, achieving maximum efficiency. Fig. 21(b) shows that the RF-DC converter for RF EH has maximum efficiency at the four-stage when the input power level is –20 dBm. Fig. 21(a) and (b) shows that the optimum number of stages is four for the input power level of –20 dBm, where the corresponding efficiencies are 31.8%.

Fig. 22 shows the simulation result of the proposed OLDC. Since the VG1 controls MN1 being turned ON and OFF, VG1 should turn OFF with the falling edge of VL1, to prevent the reverse leakage current. DPD compares VL1 and VG1, and generates the UP/DN signal to control the MUX[3:0]. By adjusting the MUX[3:0] signal, the falling edge of VD1 is controlled to be synchronized with the falling edge of VL1. VLD1, the divided-by-8 signal of VL1, is used as the clock of DPD for the settling time of the rectifier. When the falling edge of VG1 is synchronized with that of VL1 after the certain period, LCK signal becomes high and MUX[3:0] is fixed.

Fig. 23 shows the measurement result of the A4WP rectifier with OLDC. The V_{AC} and V_{ACB} with a frequency of 6.78 MHz are received and rectified to the dc voltage, V_{RECT}. As can be seen from the result, the reverse leakage current is not generated in the waveform of ac input current (I_{AC}) since the delay is compensated by the proposed OLDC operation at the point where the power MOSFETs are turned ON and OFF by the V_{AC} and V_{ACB}. Under the load condition of 100 mA, the overall power efficiency of the designed structure is about 82.14%.

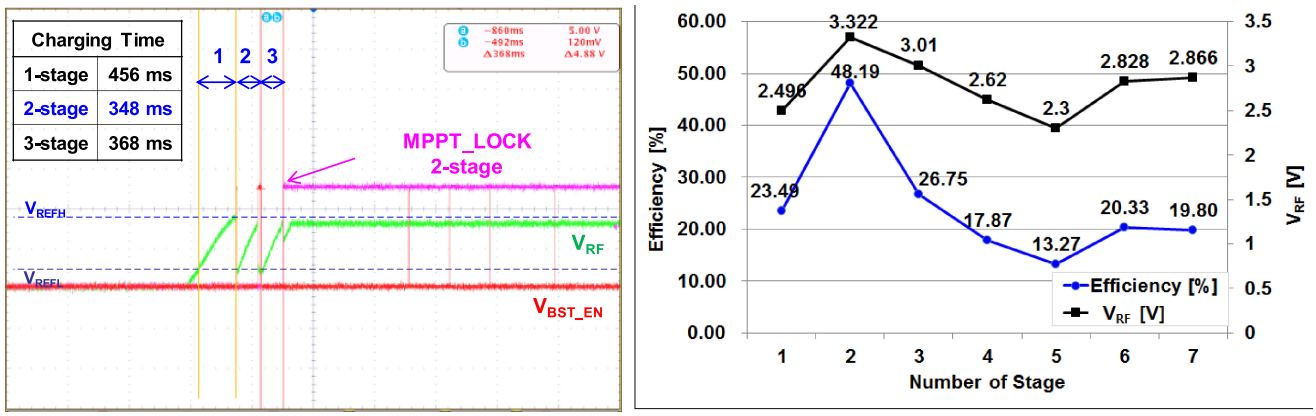
Fig. 24 shows the measured efficiency with respect to the input power of the RF EH path and WPR path. When the input power level is over 20 dBm, the WPR path shows a higher efficiency than the EH path. When the input power is 30 dBm, the peak efficiency of the WPR path is 82.14%. On the other hand, when the input power level is less than 20 dBm, the efficiency of the EH path is higher than that of the WPR path. When the input poser is 0 dBm, the peak efficiency of the EH path is 48.19%.

Table I summarizes the measured performance of the chip compared with the state-of-the-art circuits. Compared with prior works, the proposed EH with WPR achieves the measured peak



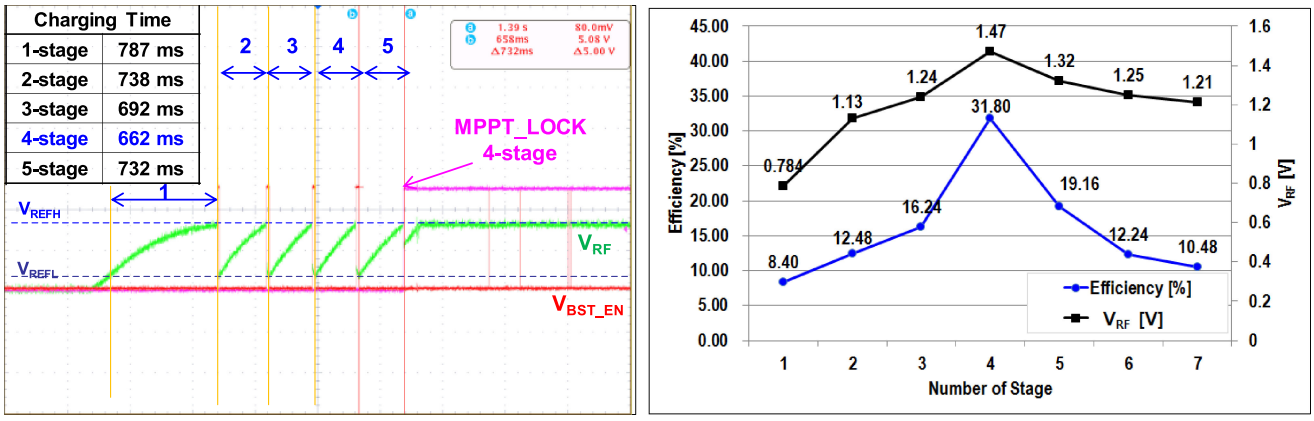
(a) (b)

Fig. 19. Simulation results of (a) the RF-DC converter V_{RF} and (b) the RF-DC converter efficiency.



(a) (b)

Fig. 20. Measured (a) transient waveforms and (b) efficiency of the reconfigurable RF-DC converter for RF EH with MPPT at input power of 0 dBm with respect to the number of stages.



(a) (b)

Fig. 21. Measured (a) transient waveforms and (b) efficiency of the reconfigurable RF-DC converter for RF EH with MPPT at input power of –20 dBm with respect to the number of stages.

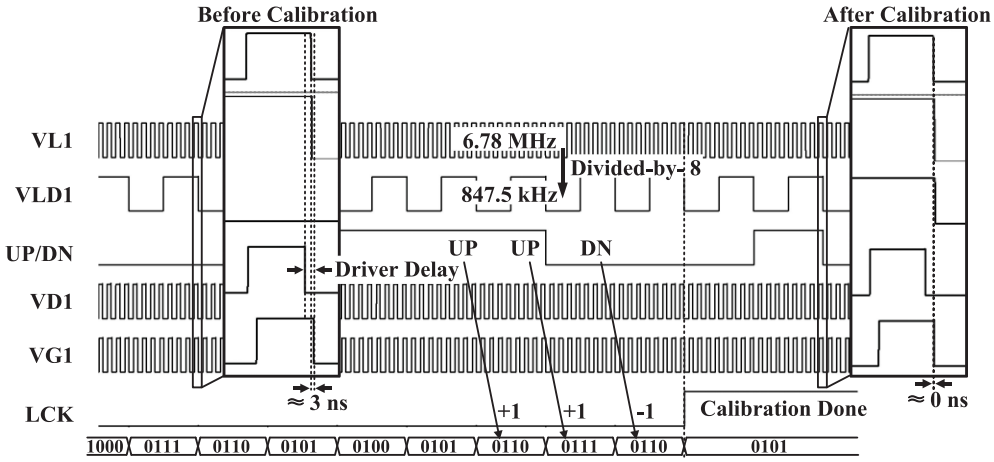


Fig. 22. Simulation result of the active rectifier with OLDC for A4WP.

TABLE I
PERFORMANCE SUMMARY

Reference	This work	JSSC 2014 [1]	ISSCC 2015 [2]	JSSC 2013 [3]	JSSC 2014 [20]	JSSC 2011 [21]
Technology	180 nm	130 nm	65 nm	130 nm	90 nm	90 nm
Frequency	900 MHz	902-928 MHz	5.8 GHz	402/433 MHz	868 MHz	915 MHz
Die area	13.76 mm^2 (EH : 0.32mm^2, WPR : 6.02mm^2)	0.4 mm^2	0.26 mm^2	8.25 mm^2	N/A	1.35 mm^2
MPPT	Yes (RC Time)	No	No	No	No	No
Reconfigurable	Yes	No	No	No	No	No
Energy Harvesting	RF	RF	RF	Thermal, RF	RF	RF
WPR	Yes	No	No	No	No	No
Sensitivity ($R_{load} = \infty$)	-20 dBm for 1 V	-20.5 dBm for 1 V	-5.9 dBm	-10 dBm	-27 dBm for 1 V	-24 dBm for 1 V
Peak PCE	31.8% @ -20 dBm 32% @ -18.83 dBm 34.7% @ -15 dBm 48.19% @ 0 dBm 42.8% @ 14.8 dBm (RF EH) 82.14% @ 30 dBm (WPR)	32% @ -15 dBm	N/A	38% @ 14.8 dBm	25% @ -20 dBm	11% @ -18.83 dBm

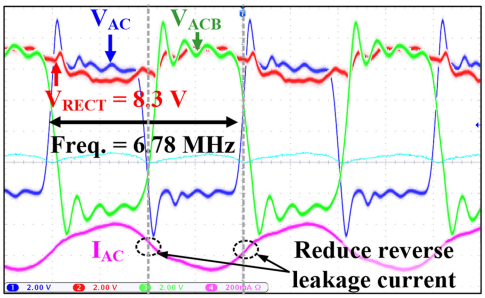


Fig. 23. Measurement result of the active rectifier with OLDC for A4WP.

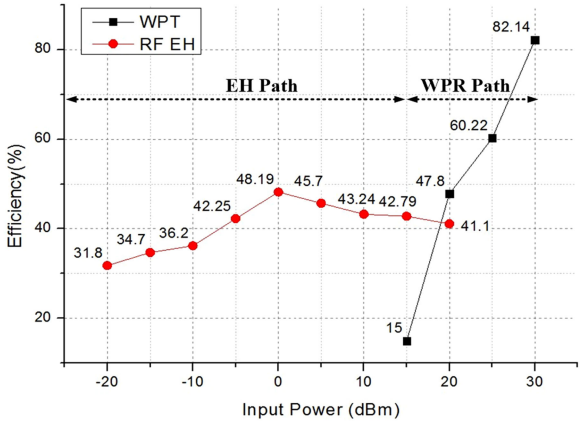


Fig. 24. PCE of the RF EH with WPR.

PCE of 48.19% with respect to the input power of 0 dBm at 900 MHz, and is the only system with reconfigurable RF-DC converter for RF EHs with MPPT and A4WP WPR mode capability. The proposed EH achieves the measured PCE of 31.8%, 32%, 34.7%, and 42.8% higher than in [1], [3], [20], and [21] with respect to the input power of −20, −18.83, −15, and 14.8 dBm, respectively. It also has a peak PCE of 82.14% with respect to the input power of 30 dBm in the A4WP mode operated at 6.78 MHz. As the WPR system is combined with EH, the overall area is slightly increased, the area of EH is 0.32 mm^2, and the area of WPR is 6.02 mm^2. The remaining areas include the power-up block, dc–dc converter and power management.

V. Conclusion

This paper presents a reconfigurable wide input power range RF EH with A4WP WPR. The reconfigurable RF-DC converter for RF EH and MPPT algorithm are proposed to maintain high efficiency over a wide input power range by automatically selecting the optimum configuration. The A4WP WPR is designed and merged with the EH to receive high power when the magnetic resonance A4WP power source is available. In order to improve the PCE, the delay between the ac input voltage and current is compensated by the proposed OLDC method. The chip is implemented in 0.18 μm BCD process. Its die area is 4.3 mm x 3.2 mm, including pads. The proposed EH with WPR achieves a measured peak PCE of 48.19% with respect to the input power of 0 dBm at 900 MHz. It also has a peak PCE of 82.14% with respect to the input power of 30 dBm in the A4WP mode operated at 6.78 MHz.

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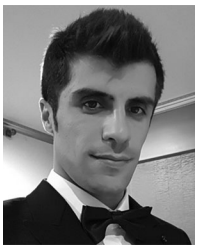

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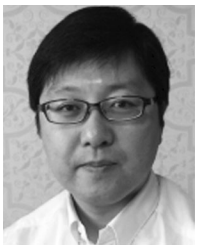

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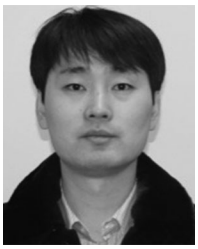

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