Letters

Wide Load Range ZVZCS Three-Level DC–DC Converter With Compact Structure

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***Abstract*—To fit the requirements of high input dc–dc power conversion, a novel zero-voltage and zero-current switching (ZVZCS) three-level dc–dc converter is proposed. Some advantages of the proposed converter are concluded as follows. The OFF voltages on the primary switches are clamped around $V_{in}/2$ by the input capacitors and the blocking capacitor. A total of two MOSFETs with low VA rating are added to provide ZVZCS for the main switches in a wide load range. The switching loss of the main switches can be optimized because the soft-switching conditions of the turn-ON and turn-OFF instants are well decoupled. The primary components can achieve reduced current stress and even current distribution because the primary current is zero during the free-wheeling stages. As the current of the auxiliary MOSFETs is zero during most operation stages, the added conduction loss can be neglected. Furthermore, the added switching loss can also be neglected because these MOSFETs can achieve zero-voltage turn-OFF and zero-current turn-ON. The circuit, operation principles, and some technical analyses are discussed in this letter, and experimental results are also provided to evaluate the proposed converter.**

***Index Terms*—Three-level dc–dc converter (TLDC), wide operation range, zero-voltage and zero-current switching (ZVZCS).**

I. Introduction

HIGH performance and high input dc–dc converters have become hot issues in power electronics due to a large amount of existing and potential market demand [1], [2]. Three-level (TL) dc–dc converter (TLDC) is an attractive solution to high input dc–dc industrial applications because the primary switches sustain only one-half input voltage. Several new topologies of the TLDC and corresponding controlling strategies have been reported [3]–[6]. Some important concepts and trends of the TLDCs were well discussed in [3]. In [4], a TLDC with four switches was proposed, which features reduced volume of a passive filter and wide ZVS load range. A TLDC with less primary circulating current was proposed in [5], and the ZVS load range of a TL dual active bridge dc–dc converter was analyzed in [6]. Among all the TLDCs, the converter in Fig. 1(a) shows some obvious advantages [7]. As shown in Fig. 1(a), two half-bridge (HB) cells are series connected, and the voltage stress of the primary switches is $V_{in}/2$. The primary structure of the converter in Fig. 1(a) is very similar to that of the circuits with power devices directly series connected. Besides, the static and dynamic voltage balance problems have been well solved. Consequently, this converter has the simplest structure among all TLDCs. To minimize the voltage spike on the main switches,

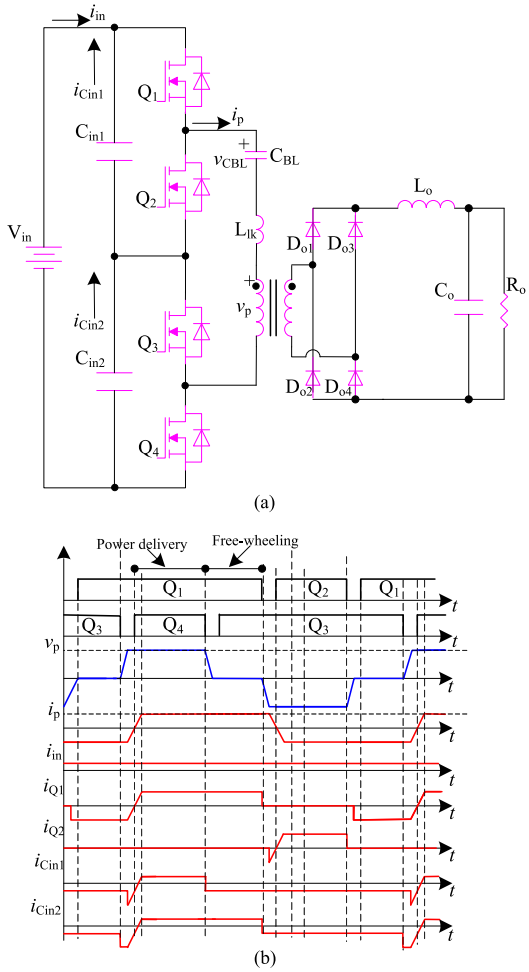

Fig. 1. TLDC in [7]. (a) Configuration. (b) Key waveforms.

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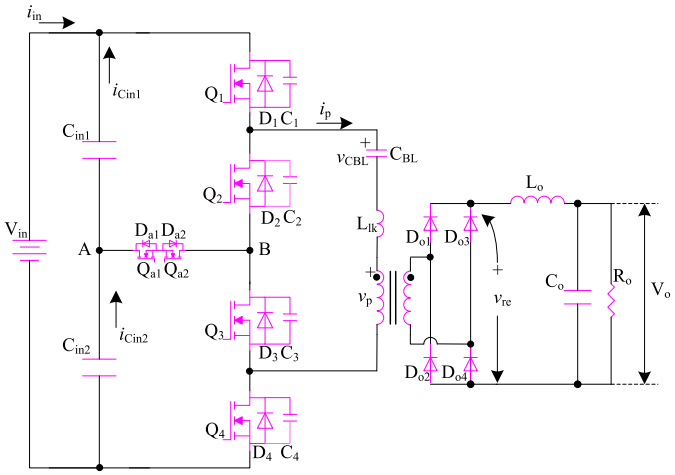

Fig. 2. Proposed ZVZCS TLDC.

the parasitic inductances among the input capacitors and power devices should be as small as possible. As depicted in Fig. 1(a), the area of the circuit loop of $C_{\rm in1}$, $C_{\rm in2}$, and Q_1 to Q_4 could be very small, which reduces the possible voltage spike on the primary switches. As proved in [7], the OFF-state voltages on the main switches are clamped by the input capacitors, and unlike other clamping devices, the bulky input capacitors can absorb more resonant energy stored in the parasitic inductances without a reverse recovery problem, which means the main switches can be kept in the safe operation area even under fast dynamic transition instant. Furthermore, as conventional two-level HB power modules can be adopted, the VA rating, performance, and cost of these modules are superior to that of TL power modules.

However, the converter in [7] also has some shortcomings. As shown in Fig. 2(b), the gate signals of the main switches are in an asymmetrical pulsewidth modulation (APWM) mode. With the decrease in the duty ratio, the currents of Q_1 to Q_4 would be imbalanced, which would cause designing problems of the power devices and heat sink. As proved in Fig. 1(b), the current distribution of $C_{\rm in1}$ and $C_{\rm in2}$ is also imbalanced, and this imbalance problem would be worsened with the increase in the output power and input voltage [8]. In addition, the current stress of the power devices and input capacitors during the free-wheeling stages is inversely proportional to the duty ratio, which would result in high conduction loss. Finally, some switches cannot achieve soft switching in a wide load range due to less resonant energy stored in the leakage inductance of the transformer. To solve these problems, several good research papers have been published in [8]–[10]. However, a new TLDC with a simple and compact primary structure, even and reduced current stress of the primary components, reduced primary circulating current, and wide load range soft-switching performance is still a valuable task.

A new zero-voltage and zero-current switching (ZVZCS) TLDC is proposed in this letter, which overcomes most drawbacks of the converter in Fig. 1(a). The main switches in the proposed converter are switched in new soft-switching type, and the switching loss can be optimized because the soft-switching conditions of the turn-ON and turn-OFF instants are well decoupled.

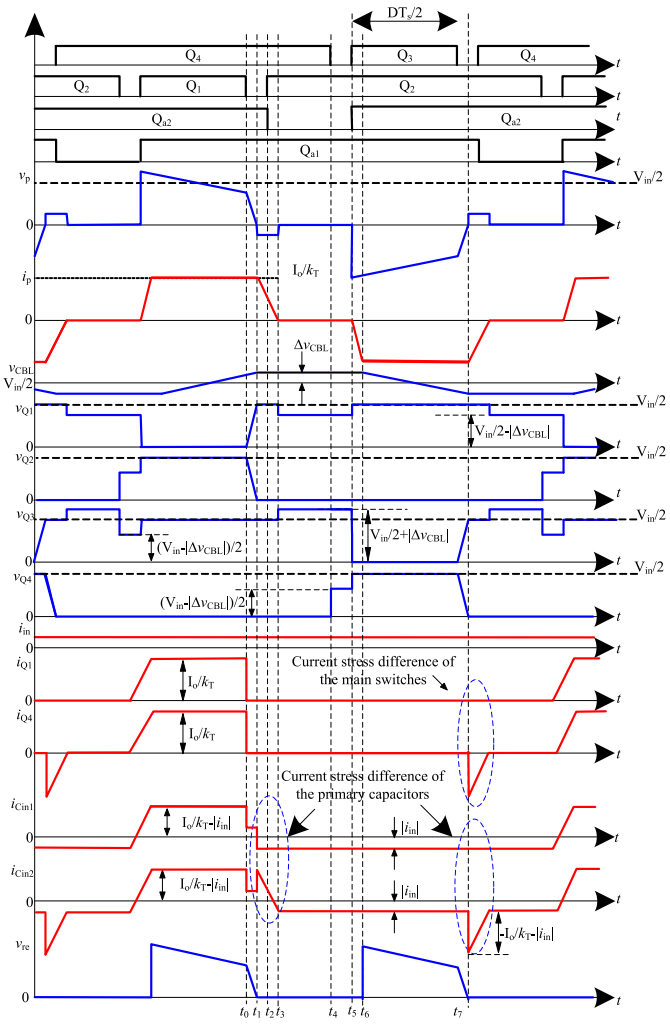

Fig. 3. Key waveforms of the proposed ZVZCS TLDC.

The primary current is kept zero during the free-wheeling stages by a new circuit configuration, and the auxiliary conduction and switching loss caused by this configuration can be neglected. In addition, all above-mentioned features are obtained without complex control strategies.

II. Circuit and Principle of Operation

Fig. 2 shows the configuration of the proposed converter. In the primary side, Q_1 to Q_4 are series connected. Q_{a1} and Q_{a2} are added between points A and B, which are used to block the reverse primary current during the free-wheeling stages. $C_{\rm in1}$ and $C_{\rm in2}$ are the input capacitors, and each input capacitor sustains one-half input voltage. $C_{\rm BL}$ is the blocking capacitor, which powers the secondary side over the one-half switching period as well as provides ZVZCS for the main switches. L_{lk} is the leakage inductance of the transformer. In the secondary side, D_{o1} to D_{o4} are the rectifier diodes, and L_o and C_o are the components of the output filter. R_o is the load resistor.

Fig. 3 shows the key waveforms of the proposed converter, and the first six stages in one switching cycle are illustrated in Fig. 4. Before the discussion, some assumptions are listed as follows:

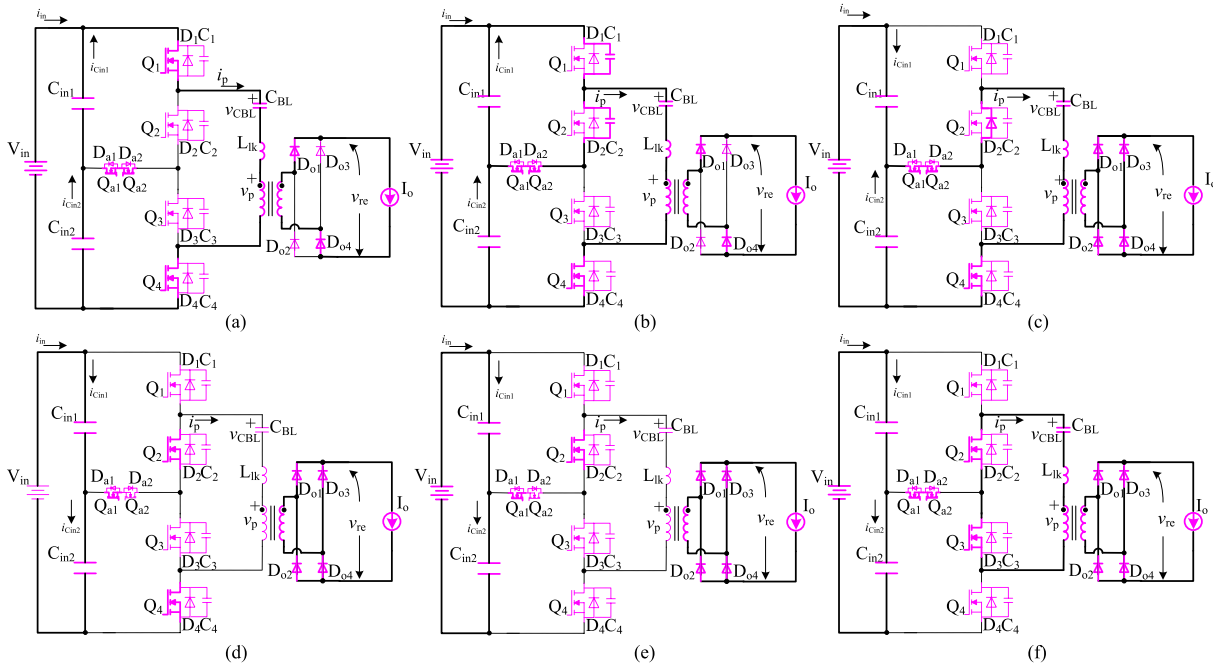

Fig. 4. First six stages over one switching cycle. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

all power devices are ideal components, and ON-state voltage drop and OFF-state leakage current of the primary switches are neglected; $C_{\rm in1}$ and $C_{\rm in2}$ are large enough, and the voltage ripple on them can be neglected; $C_{\rm BL}$ is designed with a specific value, which generates reset voltage of the primary current and provides partial energy to the load; $\Delta v_{C\rm BL} = v_{C\rm BL} - V_{\rm in}/2$; the current ripple of L_o is neglected, and represented by I_o in this letter.

Mode 1 [Fig. 4(a), before t_0]: Q_1 and Q_4 are ON; primary powers the load; Q_{a1} and Q_{a2} are ON, and D_{o1} and D_{o4} are conducted. $v_{C\rm BL}$ increases with the rate given as follows:

$$\frac{dv_{C\rm BL}}{dt} = \frac{I_o}{k_T C_{\rm BL}}. \tag{1}$$

During this period, $v_p = V_{\rm in}/2 - \Delta v_{C\rm BL}$; $v_{re} = (V_{\rm in} - 2\Delta v_{C\rm BL})/2k_T$; $i_p = I_o/k_T$. $i_{C\rm in1} = i_{C\rm in2} = I_o/k_T - |i_{\rm in}|$. The OFF voltages on Q_2 and Q_3 are clamped to $V_{\rm in}/2$ by $C_{\rm in1}$ and $C_{\rm in2}$. Although Q_{a1} and Q_{a2} are ON, there is no current flowing through these switches.

Mode 2 [Fig. 4(b), t_0–t_1]: At t_0, Q_1 is OFF, and v_{Q1} increases slowly due to C_1; $v_{C\rm BL}$ increases and reaches its final value at the end of this interval; $i_p = I_o/k_T$; i_p charges C_1 and discharges C_2. This interval lasts until $v_{C1} = V_{\rm in}/2$ and $v_{C2} = 0$. $i_{C\rm in1} = i_{C\rm in2} = I_o/2k_T - |i_{\rm in}|$. v_{Q3} is $V_{\rm in}/2$, and v_{Q1} and v_{Q2} are smaller than $V_{\rm in}/2$.

Mode 3 [Fig. 4(c), t_1–t_3]: At t_1, D_2 conducts naturally, and all secondary rectifier diodes are conducted to free-wheel I_o. During this interval, Q_2 should be switched ON to achieve ZVS, and according to Fig. 2, Q_2 is turned ON at t_2, and Q_{a2} is turned OFF at the same time. $v_{C\rm BL}$ is $V_{C\rm BLMAX}$, and $V_{C\rm BLMAX} - V_{\rm in}/2$ is fully applied to L_{lk} to reset i_p, and i_p is given as follows:

$$i_p(t) = \frac{I_o}{k_T} - \frac{V_{C\rm BLMAX} - V_{\rm in}/2}{L_{lk}}(t - t_1). \tag{2}$$

At the end of this interval, i_p is zero, and the interval is given as follows:

$$T_{31} = \frac{I_o L_{lk}}{k_T (V_{C\rm BLMAX} - V_{\rm in}/2)}. \tag{3}$$

During this interval, $i_{C\rm in1}$ is $-|i_{\rm in}|$ and $i_{C\rm in2}$ is $I_o/k_T - |i_{\rm in}|$. v_{Q1} and v_{Q3} are clamped to $V_{\rm in}/2$ by $C_{\rm in1}$ and $C_{\rm in2}$.

Mode 4 [Fig. 4(d), t_3–t_4]: At t_3, i_p is zero, and i_p cannot change to the negative value because of D_{a2}. After t_3, Q_4 can achieve zero-current switching (ZCS). During this period, $v_{C\rm BL} = V_{C\rm BLMAX}$ and $i_{C\rm in1} = i_{C\rm in2} = -|i_{\rm in}|$. The voltage on D_{a2} is $V_{C\rm BLMAX} - V_{\rm in}/2$, and the voltage rating of Q_{a1} and Q_{a2} is determined by $V_{C\rm BLMAX} - V_{\rm in}/2$. v_{Q3} is clamped by $C_{\rm BL}$ with the value of $V_{\rm in}/2 + \Delta v_{C\rm BL}$ and v_{Q1} is $V_{\rm in}/2 - \Delta v_{C\rm BL}$.

Mode 5 [Fig. 4(e), t_4–t_5]: At t_4, Q_4 is turned OFF with ZCS. $i_{C\rm in1} = i_{C\rm in2} = -|i_{\rm in}|$. v_{Q3} is $V_{\rm in}/2 + |\Delta v_{C\rm BL}|$, while v_{Q1} and v_{Q3} are $(V_{\rm in} - \Delta v_{C\rm BL})/2$.

Mode 6 [Fig. 4(f), t_5–t_6]: At t_5, Q_3 and Q_{a2} are gated ON, and Q_3 can achieve ZCS because the change rate of i_p is limited by L_{lk}; Q_2 has been turned ON at t_2; i_p is given as follows:

$$i_p(t) = -\frac{V_{C\rm BLMAX}}{L_{lk}}(t - t_5). \tag{4}$$

When i_p is $-I_o/k_T$, this mode is finished, and the interval is given as follows:

$$T_{56} = \frac{L_{lk} I_o}{k_T V_{C\rm BLMAX}}. \tag{5}$$

At t_6, i_p is $-I_o/k_T$. The circuit goes into the second-half switching cycle, and the energy stored in $C_{\rm BL}$ powers the load. $v_p = -V_{\rm in}/2 + \Delta v_{C\rm BL}$; $v_{re} = -(V_{\rm in} - 2\Delta v_{C\rm BL})/2k_T$; $i_p = -I_o/k_T$; $i_{C\rm in1} = i_{C\rm in2} = -|i_{\rm in}|$. Although Q_{a1} and Q_{a2} are ON, the current of Q_{a1} and Q_{a2} is zero.

III. Brief Discussion

A. Soft Switching of Q_2 and Q_4

Turn-ON instants: Q_2 and Q_4 can achieve zero-voltage turn-ON. As the energy reserved in the output inductance is large enough to discharge the corresponding capacitors, Q_2 and Q_4 can obtain zero-voltage turn-ON in a wide load range.

Turn-OFF instants: Q_2 and Q_4 are turned OFF after i_p is reset to zero. Thus, with proper designing, Q_2 and Q_4 can obtain zero-current turn-OFF in a wide load range.

B. Soft Switching of Q_1 and Q_3

Turn-ON instants: When Q_1 and Q_3 are ON, i_p increases slowly from zero because L_{lk} limits the change rate of i_p. Consequently, Q_1 and Q_3 can obtain zero-current turn-ON. To reduce the turn-ON switching loss further, low driving resistors of Q_1 and Q_3 are preferred.

Turn-OFF instants: When Q_1 and Q_3 are OFF, v_{Q1} and v_{Q3} vary with flat slope from zero because of C_1 and C_3. Thus, Q_1 and Q_3 can obtain zero-voltage turn-OFF. To reduce the turn-OFF switching loss further, additional capacitors could be parallel connected with Q_1 and Q_3. In addition, as the turn-ON instants of Q_1 and Q_3 are zero-current type, thus, a larger value of C_1 and C_3 could not affect the soft-switching condition of the turn-ON instants.

C. Soft Switching of Q_{a1} and Q_{a2}

Q_{a2} is selected as an example. As shown in Figs. 3 and 4(c), Q_{a2} is switched OFF at t_2, and D_{a2} conducts naturally to free-wheel i_p; thus, Q_{a2} can achieve zero-voltage turn-OFF. As shown in Figs. 3 and 4(f), Q_{a2} is switched ON at t_5, and Q_{a2} can achieve zero-current turn-ON because no current flows through Q_{a2} at this instant.

D. Voltage Balance Principle of the Input Capacitors

The initial voltages on $C_{\rm in1}$ and $C_{\rm in2}$ are $V_{\rm in}/2$ due to the configuration of the circuit, and the voltages on the input capacitors can be balanced if charge balance of these capacitors can be kept over one switching cycle. As depicted in Figs. 3 and 4, only the ac content of the positive pulse of i_p flows through $C_{\rm in1}$ and $C_{\rm in2}$, and dc current of the positive pulse of i_p can be provided by $V_{\rm in}$. Thus, $C_{\rm in1}$ and $C_{\rm in2}$ can achieve stable voltage over one switching cycle. Detailed information can be found in [7]–[10].

E. Comparison

1) Comparison With the Converter in Fig. 1(a): Tables I and II illustrate the comparisons between the proposed converter and the converter in Fig. 1(a).

Main switches: As illustrated in Fig. 3, in one-half switching cycle, the current difference between Q_1 and Q_4 is the negative current pulse flowing through Q_4, but the time of this pulse is very short, which is usually smaller than 1 μs. Hence, the added rms value is usually smaller than 0.01 per-unit, and the current distribution among the main switches is almost even. As the primary circulating current is reset to zero, the current stress on the main switches is smaller than that of the converter in Fig. 1(a). As given in Table I, the voltage stress on Q_3 is $V_{\rm in}/2 + \Delta v_{C\rm BL}$, which is slightly higher than that of the converter in Fig. 1(a). However, as $\Delta v_{C\rm BL}$ is usually small, which may be small than 30 V, thus, the increase in the voltage stress on Q_3 can be accepted.

Primary capacitors: As shown in Figs. 3 and 1(b), the current distribution between the input capacitors is more even than that of the converter in Fig. 1(a). During the primary current reset intervals, $i_{C\rm in2}$ is not identical to $i_{C\rm in1}$. As the time of this interval is very short and does not vary with the duty ratio, the current imbalance among the input capacitors can also be neglected. Furthermore, the current stress of the input capacitors can also be reduced because the primary current is reset to zero during the free-wheeling stages. As given in Table II, the current stress of $C_{\rm BL}$ is smaller than that of the converter in Fig. 1(a). In addition, the required capacitance of $C_{\rm BL}$ in the proposed converter is also smaller than that of the converter in Fig. 1(a).

Soft-switching load range: As proved in [7] and Table I, two main switches cannot achieve ZVS in a wide load range because only the energy reserved in the leakage inductance can be utilized to charge the corresponding output capacitors of the main switches, which results in low efficiency performance with light load current. In addition, the turn-OFF switching loss of the main switches cannot be optimized because large output capacitance would greatly narrow the ZVS load range of the turn-ON instants. However, the soft-switching conditions in the proposed converter are much better than those of the converter in Fig. 1(a). As proved in the previous section, Q_2 and Q_4 are switched with zero-voltage turn-ON and zero-current turn-OFF in a wide load range, while Q_1 and Q_3 are turned ON with zero-current and OFF with zero-voltage. In addition, the turn-OFF switching loss of Q_1 and Q_3 can be further optimized without much influence on the turn-ON instants.

2) Brief Comparison With a Conventional Primary Reset ZVZCS TLDC: Compared with a conventional primary reset ZVZCS TLDC [11], the proposed converter has the following good features. The current of the cutting-off components is greatly reduced, which is only about 0.05 times than that of the converter in [11]. The primary structure of the proposed converter is more concise because no power devices are directly inserted into the main path of power transfer. As Q_{a1} and Q_{a2} can transfer and block bidirectional current, the proposed ZVZCS solution can support more soft-switching schemes, e.g., phase shift PWM or APWM. With the APWM switching scheme, the switching loss of the main switches in the proposed converter can be further reduced because the soft-switching conditions of the turn-ON and turn-OFF instants are well decoupled.

IV. Experimental Results

The performance of the proposed converter is verified by a 1.1 kW prototype, and the main parameters are listed as follows: $V_{\rm in}$ is varied from 400 to 600 V, the output voltage is 220 V, the maximum output current is 5 A, switching frequency is 100 kHz,

TABLE I
COMPARISON OF THE MAIN SWITCHES

Item	Q_1		Q_2		Q_3		Q_4	
	Proposed	Fig.1 (a)	Proposed	Fig.1 (a)	Proposed	Fig.1 (a)	Proposed	Fig.1 (a)
Voltage stress	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2+\Delta v_{CBL}$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$
Current stress	normal	normal	normal	large	normal	normal	normal	large
Turn-on soft switching	ZCS, easy	ZVS, easy	ZVS, easy	ZVS, hard	ZCS, easy	ZVS, easy	ZVS, easy	ZVS, hard
Turn-off soft switching	ZVS, easy	ZVS, normal	ZCS, easy	ZVS, normal	ZVS, easy	ZVS, normal	ZCS, easy	ZVS, normal

TABLE II
COMPARISON OF THE PRIMARY CAPACITORS

Item	C_{in1}		C_{in2}		C_{BL}	
	Proposed	Fig.1 (a)	Proposed	Fig.1 (a)	Proposed	Fig.1 (a)
Voltage stress	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2+\Delta v_{CBL}$	$V_{in}/2$
Current stress	Normal	Large	Normal	Large	Small	Large
Capacitance	Normal	Large	Normal	Large	Small	Large

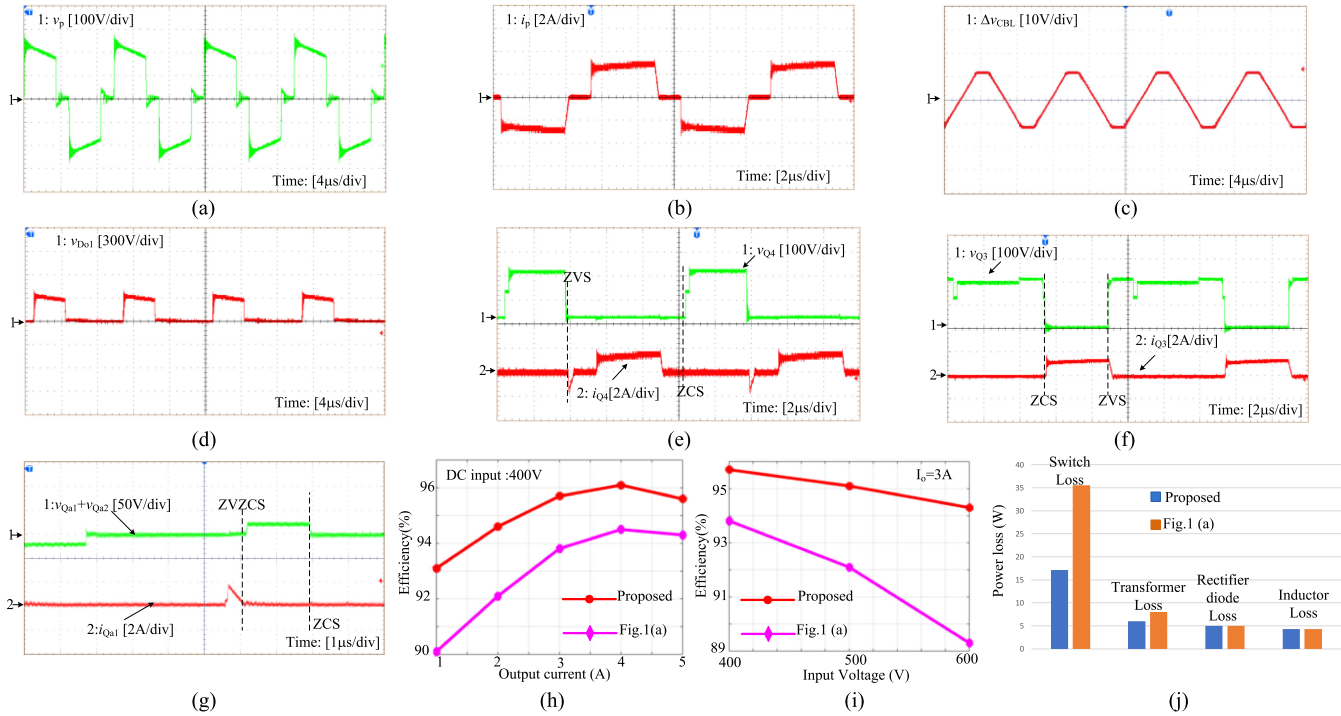

Fig. 5. Experimental results and power loss analysis. (a) v_p. (b) i_p. (c) Δv_{CBL}. (d) v_{Do1}. (e) v_{Q4} and i_{Q4}. (f) v_{Q3} and i_{Q3}. (g) $v_{Qa1}+v_{Qa2}$ and i_{Qa1}. (h) Efficiency with 400 V input voltage. (i) Efficiency with 3 A output current. (j) Power loss analysis, when $V_{\mathrm{in}}=500$ V, $I_o=3$ A.

$C_{\mathrm{in1}}=C_{\mathrm{in2}}=40\ \mu$F, $C_{\mathrm{BL}}=3\ \mu$F, IPB60R160P6 is used as the main switches, and IPB049N08N5 is adopted as Q_{a1} and Q_{a2}. During the efficiency comparison, the converters in Fig. 1(a) are also tested. The experimental results and power loss analysis are presented in Fig. 5.

v_p is illustrated in Fig. 5(a), and the high level of v_p is not a constant value because $v_{C\mathrm{BL}}$ is varied during power transferring stages. As shown in Fig. 5(b), i_p is reset to zero during the free-wheeling stages and keeps zero because of D_{a1} and D_{a2}. As presented in Fig. 5(c), C_{BL} is charged or discharged by i_p with a constant value during the power transfer stages; thus, the voltage of C_{BL} will increase or decrease linearly with time. During the free-wheeling stages, $v_{C\mathrm{BL}}$ keeps constant because i_p is zero. v_{Do1} is shown in Fig. 5(d), and the voltage stress on the rectifier diode is slightly increased.

As depicted in Fig. 5(e), Q_4 is operated in zero-voltage turn-ON and zero-current turn-OFF mode. During the turn-ON instant, i_{Q4} is negative because D_4 conducts naturally; consequently, this switch can obtain zero-voltage turn-ON. At the turn-OFF instant, i_{Q4} is zero; thus, the turn-OFF switching loss can be removed. As shown in Fig. 5(f), Q_3 is operated in zero-voltage turn-OFF and zero-current turn-ON mode. During the turn-ON instant, i_{Q3} keeps zero due to L_{lk}; thus, this switch can obtain zero-current turn-ON. At the turn-OFF instant, v_{Q3} increases

slowly due to the large value of C_3; thus, the turn-OFF switching loss can also be minimized. As presented in Fig. 5(e) and (f), the OFF voltages on the primary switches are clamped around $V_{\rm in}/2$. As shown in Fig. 5(g), Q_{a1} and Q_{a2} are switched in the soft-switching mode, and the rms value of i_{Qa1} is very small.

The efficiency curves in Fig. 5(h) and (i) are tested from the dc-link side to the output. As presented in Fig. 5(h), the efficiency of the proposed converter with light load current is clearly higher than that of the converter in Fig. 1(a) due to a wide soft-switching load range. As presented in Fig. 5(h), the proposed converter has better efficiency performance with high load current because both the turn-ON and turn-OFF switching loss can be optimized. In Fig. 5(i), both efficiency curves drop with the increase in the input voltage, but the decreasing rate of the proposed converter is much lower than that of the converter in Fig. 1(a) because the proposed converter can achieve reduced switching loss at both turn-ON and turn-OFF instants. Fig. 5(j) shows the power loss distribution analysis at 3 A load current when $V_{\rm in} = 500$ V. Because both turn-ON and turn-OFF switching loss can be optimized, the total switching loss of the main switches in the proposed converter is lower than that of the converter in Fig. 1(a). In addition, the main switches of the proposed converter produce smaller conduction loss owing to reduced circulating current.

V. Conclusion

A new ZVZCS TLDC is proposed and analyzed in this letter. The proposed converter has some good features, such as even and reduced current stress of the primary components, wide load range soft-switching characteristics, and simple switching scheme. In addition, the ZVZCS solution proposed in this letter can also be applied to other TLDCs. The only shortcoming of the proposed converter is the voltage stress on Q_3 is slightly higher than $V_{\rm in}/2$. The proposed converter can be used in many high input dc–dc industrial applications, e.g., down-stage dc–dc converter after 3ϕ power factor correction and dc interfaces for microgrids.

References

[1] J. R. Pinheiro and I. Barbi, "The three-level ZVS PWM converter—A new concept in high-voltage dc-to-dc conversion," in *Proc. 1992 Int. Conf. Ind. Electron., Control, Instrum., Automat.*, 1992, pp. 173–178.

[2] P. M. Barbosa and F. C. Lee, "Design aspects of parallel three-phase DCM boost rectifiers," in *Proc. 30th Annu. IEEE Power Electron. Spec. Conf. Rec.*, 1999, pp. 331–336.

[3] X. Ruan, B. Li, Q. Chen, S. Tan, and C. K. Tse, "Fundamental considerations of three-level dc–dc converters: Topologies, analyses, and control," *IEEE Trans. Circuits Syst. I, Regul. Papers*, vol. 55, no. 11, pp. 3733–3743, Dec. 2008.

[4] Y. Shi and X. Yang, "Wide load range ZVS three-level dc–dc converter: Four primary switches, capacitor clamped, two secondary switches, and smaller output filter volume," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3431–3443, May 2016.

[5] Z. Guo, K. Sun, and D. Sha, "Improved ZVS three-level dc–dc converter with reduced circulating loss," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6394–6404, Sep. 2016.

[6] L. Jin, B. Liu, and S. Duan, "ZVS soft switching operation range analysis of three-level dual active bridge dc-dc converter under phase shift control strategy," *IEEE Trans. Ind. Appl.*, to be published.

[7] R. G. Barbi, R. Redl, and N. O. Sokal, "DC/DC converter: Four switches $V_{\rm pk} = V_{\rm in}/2$, Capacitive turn-off snubbing, ZV turn-on," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 918–927, Jul. 2004.

[8] D. Liu, F. Deng, Q. Zhang, and Z. Chen, "Zero-voltage switching PWM strategy based capacitor current-balancing control for half-bridge three-level dc/dc converter," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 357–369, Jan. 2018.

[9] D. Liu, F. Deng, Z. Gong, and Z. Chen, "Input-parallel output-parallel three-level dc/dc converters with interleaving control strategy for minimizing and balancing capacitor ripple currents," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 5, no. 3, pp. 1122–1132, Mar. 2017.

[10] W. Liu, H. Jin, W. Yao, and Z. Lu, "An interleaved PWM method with better voltage-balancing ability for half-bridge three-level dc/dc converter," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4594–4598, Jun. 2018.

[11] X. Ruan, L. Zhou, and Y. Yan, "Soft-switching PWM three-level converters," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 612–622, Sep. 2001.