Switched Tank Converters

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***Abstract*—This paper presents a new class of switched tank converters (abbreviated as STCs) for high-efficiency high-density nonisolated dc–dc applications where large voltage step down (up) ratios are required. Distinguished from switched capacitor converters, the STCs uniquely employ *LC* resonant tanks to partially replace the flying capacitors for energy transfer. Full soft charging, soft switching, and minimal device voltage stresses are achieved under all operating conditions. The STCs feature very high efficiency, power density, and robustness against component nonidealities over a wide range of operating conditions. Furthermore, thanks to the full resonant operation, multiple STCs can operate in parallel with inherent droop current sharing, offering the best scalability and control simplicity. These attributes make STC a disruptive and robust technology viable for industry's high volume adoption. A novel equivalent DCX building block principle is introduced to simplify the analysis of STC. A 98.9% efficiency STC product evaluation board (4-to-1, 650 W) has been developed and demonstrated for the next-generation of 48-V bus conversion for data center servers.**

***Index Terms*—DCX, switched tank converters (STCs), switched capacitor converters (SCCs), soft charging, soft switching.**

I. Introduction

RECENT advancement of semiconductor power devices including both wide-band-gap devices (GaN and SiC) and silicon devices (Trench MOS, LDMOS, etc.) has been pushing power conversion to higher efficiency and density, due to the continuous improvement of the device figure of merits (FOM). In the meantime, however, passive components including capacitors and magnetics do not obey Moores law. Particularly in many modern power electronics applications, magnetic components are becoming bottlenecks in terms of further efficiency and density improvement. For instance, in telecom and data center motherboards where high ratio dc–dc bus conversion is often required, transformer-based topologies such as active-clamp forward, full bridge, and *LLC* resonant converters are prevailing regardless of galvanic isolation requirement. Transformer design and integration for these topologies have become the greatest challenge for system optimization as it heavily dictates the overall system efficiency and density. On the other

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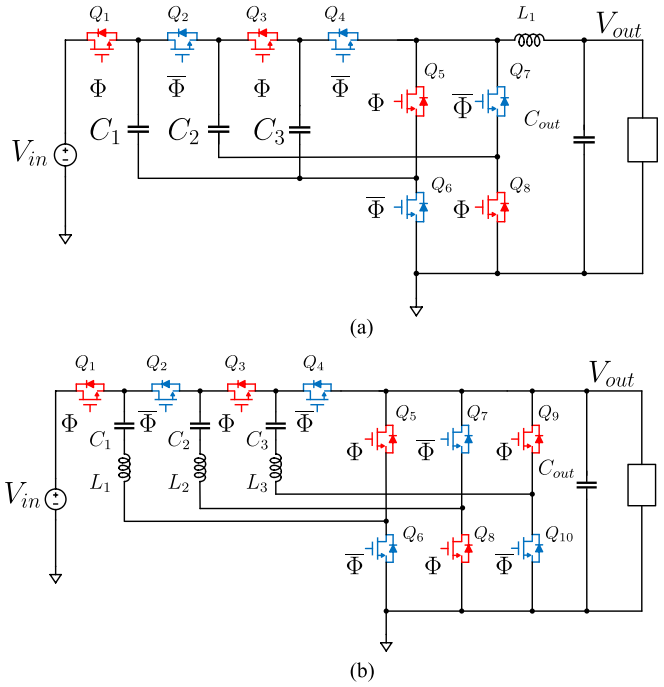

Fig. 1. Examples of prior SCC derivative topologies with inductors. (a) 4-to-1 Dickson SCC with one aggregated inductor. (b) 4-to-1 multilevel modular SCC with distributed inductors.

be either a pure ac or a dc plus some ac ripples, depending upon the specific inductor locations in the circuit. One example of SCC using an aggregated inductor is given in Fig. 1(a). Second, inductors can be distributed in an SCC topology as well [21], [29], [30]. The inductor count increases along with switch and capacitor count. In certain circumstances, stray inductors can be used. One example of SCC with distributed inductors is shown in Fig. 1(b). Regardless of using aggregated inductors or distributed inductors in SCCs, multiple ways of PWM control are available to achieve not only soft charging but also resonant soft switching (ZVS [31]–[34] or ZCS [21], [24]–[27], [29], [30], [35]–[37]) and regulation [38], [39].

From the abovementioned, it seems plenty of SCC derivative solutions are available and ready for the industry to adopt for wide and high volume use. However, in order to make any of these SCC-based solutions viable for mass production design, a lot more hidden challenges behind the scene are something that the industry cannot get around and must be addressed. In this paper will be discussed a new class of switched capacitor-based converters defined as switched tank converters (abbreviated as STCs and first introduced in [1]) in order to overcome some limitation to the wide use of such kind of solutions. The paper is organized as follows. In Section II will be described the main problems related to the usage of SCC converter as component nonidealities, stress, and scalability. After considering all these practical challenges discussed above, a disruptive new class of STCs are proposed in Section III. The key attributes of STCs will be elaborated. An equivalent DCX building block modeling approach is then introduced in Section IV for STC circuit analysis. By using this model, the analysis of mismatch effects are analyzed in Section V. One STC topology has been selected for the 48-V data center bus converter application described in Section VI. A fully functional 650-W 4-to-1 STC product evaluation board has been developed. Experimental performance data will be demonstrated in Section VII and the conclusion will be drawn in Section VIII.

II. SCC Application Challenges

In this section, the main obstacles to the uses of SCC solution in widespread applications considering high volume robustness, reliability, and the device technology opportunity in the market will be discussed. The immunity to component variations and parasitics, voltage stress of MOSFETs, and issue related to the scalability of these solutions will be covered.

A. Immunity to Component Nonidealities

Most of the abovementioned topologies are using Class II ceramic capacitors (X7R, X7S, X5R, etc.), which inherently have a very wide tolerance band over temperature (e.g., up to $\pm 22\%$ for X7S), dc bias (e.g., a 100-V Class II MLCC can derate by 70% with 50 V bias) and part-to-part variation (higher than $\pm 10\%$). However, these topologies often rely on precisely determined flying capacitors to either satisfy full soft charging requirement [22] or match the switching frequency to *LC* resonance for soft switching. In addition, the parasitic loop inductances cannot be ignored in high current applications. Therefore, the electrical characteristics consistency among different products can hardly be guaranteed once the volume goes high. Undesirable corner cases tend to show up from Monte Carlo or worst case analysis. In some other cases, topologies with distributed inductors, for instance, the one shown in Fig. 1(b), create a lot of challenges for designing all possible inductor current commutation paths during dead time considering *LC* tolerances and control timing mismatches. A converter topology whose electrical characteristics vary heavily with component mismatches, large tolerances, or loop parasitics is not viable for industry production.

B. Capacitor Material Consideration

In most SCC topologies, the electrical characteristics (operation modes, current waveforms, output impedance, losses, etc.) are often associated with flying capacitor values. While Class II ceramic capacitors with large variations are mostly seen in existing literatures, Class I ceramic capacitors are rarely evaluated and used in SCC topologies. Class I ceramic capacitors (C0G, U2J, etc.) use very low dielectric constant and low loss factor dielectric material to offer very stable capacitance, low tolerance (less than $\pm 5\%$), and low ESRs across all operating conditions. They are ideal capacitor candidates for SCCs that require tight capacitor matching, resonant operation, and high current. However, due to the very low dielectric constant and small capacitance, Class I ceramic capacitors usually carry much higher ac voltage ripples than Class II ceramic capacitors in power conversion. It becomes undesirable if switching MOSFETs can see these ripples across drain to source. Therefore, how to appropriately apply Class I ceramic capacitors to SCC-based topologies

and fully leverage their superior electrical performance remains a challenge.

C. Worst Case Voltage Stress of MOSFETs

One of the key enablers for high efficiency high density of SCC-based topologies is the opportunity to use low-voltage rating MOSFETs with better FOMs. For example, in a step-down Dickson and its derivative SCC topologies, all switching devices have either V_{out} or $2V_{\text{out}}$ as maximum drain source voltage during normal operation regardless of the high side V_{in}. However, in order to reliably use low-voltage devices, the voltage stress of these devices should never exceed their absolute max rating under all worst case circumstances. The simplest question to ask is whether the drain-to-source voltage of each device can always be clamped to a minimal dc-like voltage by a capacitor or capacitor network in the OFF state even considering loop parasitic inductances, transient events, and worst-case component variations. Apparently, the FETs (Q1–Q4) in Fig. 1(b) are not desirably clamped and, thus, can go over stress easily during switching transitions.

D. Scalability

In high current applications, there are two main aspects that must be considered for scalability: the scalability of the topology itself to different conversion ratios and power ratings and the scalability of the control/driver circuitry. For the first part, it is needed to examine how the circuit electrical characteristics change according to different conversion ratios, how easy to accommodate those changes, whether multiple converters can be connected in parallel with good current sharing, and so on. For the second part, it is desirable to have a simple uniform central controller and a scalable driver circuit that supports all topology configurations. In some cases, additional voltage sensing across floating flying capacitors are required to achieve 100% soft charging [28]. This type of complication also affects the scalability of control.

E. Minimum RMS Current

In applications where conduction losses are often dominant at heavy load, minimizing RMS current of each component becomes critical. In order to achieve this goal, it is ideal to control an SCC-based topology with or close to two symmetric switching states at near 50% duty cycle. In each switching state, current waveform should be definitive with least influence from parasitic ringings due to component nonidealities. Hence, current can be evenly delivered with minimum RMS. In some resonant SCC topologies using aggregated inductors, the same inductor may resonate with different capacitor banks in different switching states such that asymmetric duty cycle must be used to accommodate multiple resonant frequencies. In these cases, RMS current is not minimized.

F. Thermal Performance

It is always desirable to have even temperature distribution within the converter without having hot spots. This allows the converter to be capable of delivering maximum power under a given thermal environment. In other words, a good SCC topology needs to have the power stresses distributed among the devices as evenly as possible. By carefully considering all these practical challenges discussed above, a disruptive new class of STCs are proposed in Section III.

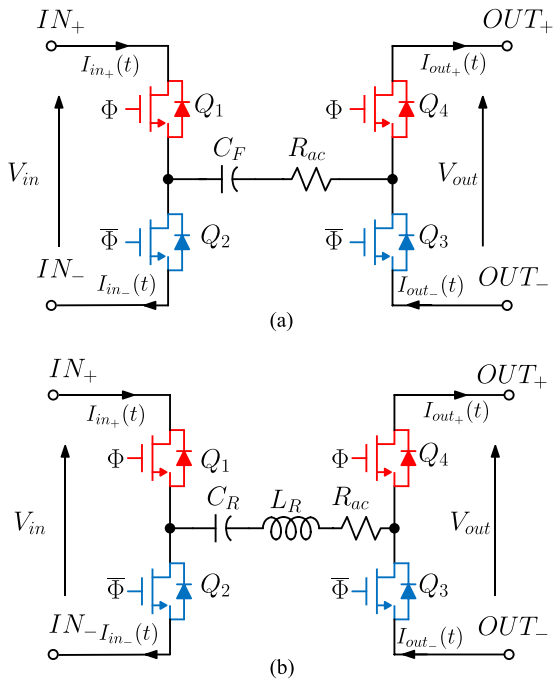

Fig. 2. Two fundamental building blocks of an STC topology. (a) Structure with a clamping capacitor. (b) Structure with a resonant tank.

III. STC Topologies

In this section, the key attributes of STC topologies will be defined. Similar to the examples reported previously in Fig. 1, STCs adopt magnetic components to perform ZCS and soft switching operation but overcoming the limitations treated in the previous section. This class of topologies can be derived from SCC structures with two topological states. The transformation of an SCC to an STC topology or the creation of a new architecture is based on composition of elementary cells. Each cell can be defined as a building block that can have two different basic structures reported in Fig. 2(a) and (b). Obviously, neither of these two building blocks can work alone. They both need an additional common mode current path between input and output in order to function correctly. For example, IN$_-$ can be tied to a dc source while OUT$_-$ is tied to reference ground. In Fig. 2 is reported a voltage generator V_{cm} with a given impedance Z_{cm} that represents the different voltage level between input and output terminals. In this condition, two STC building blocks operate on the dc values as 1:1 ideal dc transformer (DCX). The dc filtering capacitor C_F and the resonant capacitor C_R can both block the common-mode voltage difference between input and output. A detailed model on the average values of the input current and input voltage will be addressed in Section IV. The STC architecture is obtained by connecting the input and/or the output port

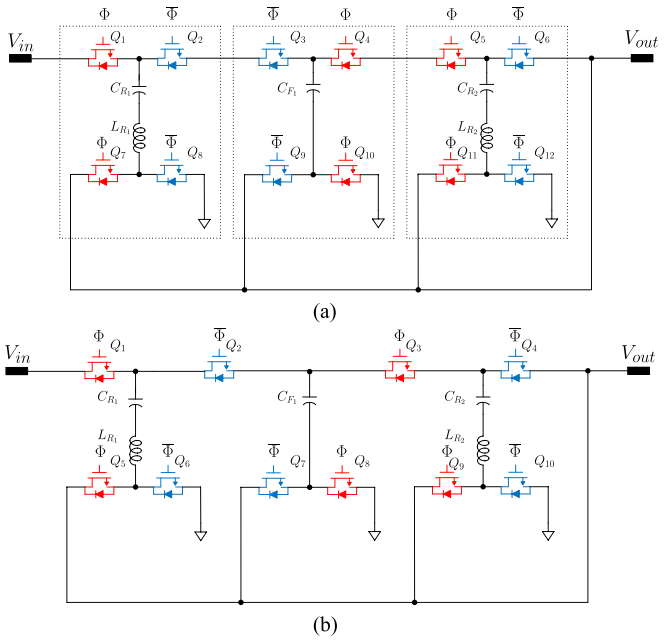

Fig. 3. 4-to-1 STC derivation. (a) Structure with building blocks. (b) Derived 4-to-1 STC topology.

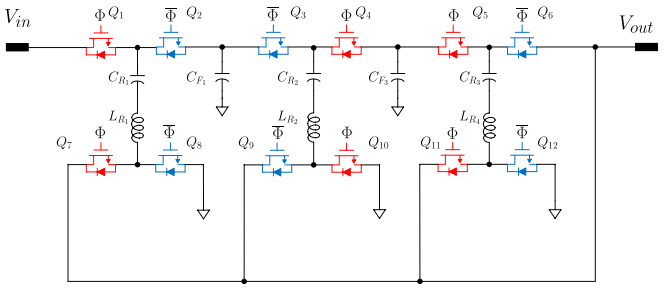

Fig. 4. 4-to-1 STC (1-phase, all switches clamped by V_{out}).

of the buildings blocks in serial or/and in parallel. The resonant block of Fig. 2(a) pairs with the block of Fig. 2(b) to essentially form a resonant operation in which the resonant building block generates a resonant current by switching approximately at the resonant frequency. The nonresonant building block stabilizes the voltage of the input and output terminals by connecting C_F (with $C_F \gg C_R$) to ground or to another stable voltage. *Substantially each combination of building blocks in which the devices during the* ON *time conduct one half period of resonant current and during the* OFF *time have a voltage drop defined by a mesh of dc filtering capacitors as C_F and/or capacitors connected to ground can be defined as an STC.* The simplest STC structure realizable is a 2-to-1 resonant SCC that requires only the building block of Fig. 2(b) with the input port (IN_+, IN_-) and the output port (OUT_+, OUT_-) connected in series. The input voltage V_{in} is across the series and the output voltage V_{out} is connected on the output port of the building block. Some examples of STC topology construction developed from an SCC are reported in Figs. 3 and 4. The two topologies are derived from a Dickson SCC converter and can be considered an extension of the 2-to-1 structure. In fact, by using the building block approach, the topology can be easily considered a serial connection of the input ports of the building blocks from V_{in} to V_{out} and a parallel connection of the output ports from ground to V_{out}, as shown in Fig. 3(a). The choice of composing two resonant blocks and one with the clamping capacitor is to maintain a resonant current in all the branches and to clamp the device OFF voltage. Later, it is possible to simplify the redundant switches and obtain the structure of Fig. 3(b). Note that the key features of this architecture is based on the alternation of the two different cells that ensures the ZCS in all the switches and a stable OFF voltage over the presence of parasitic components. In fact, the structure reported in Fig. 1(b) can be described by the connection only of resonant building blocks and cannot be defined as an STC converter. The building block of Fig. 2(a) have the main scope of maintaining the stable OFF voltages of the devices over the oscillation due to the loop inductors present on the layout. Another solution based only on the resonant building block is reported in Fig. 4. In this case, the voltage of the input terminals is clamped by capacitors connected to ground. These clamping capacitors here can be very small as their current ripples are mostly cancelled out. Even if each switch has the OFF voltage equal to V_{out}, this solution requires more switches because merging redundant switches cannot take place. In this way, the issues regarding the voltage stress of devices reported in the previous section are not present.

In terms of the current flow direction in the switches, all the switches can be divided into two categories: main switches and synchronous-rectifier (SR) switches. Taking N-Channel MOSFET as an example, a main switch has its current flow from drain to source in normal operations, vice versa, an SR switch normally has its current flow from source to drain. In certain applications, SR switches can be replaced by Schottky diodes. In a step-down STC, all the switches are normally blocked either V_{out} or $2V_{\text{out}}$ in their OFF state. Therefore, low-voltage devices with superior FOMs can be used to switch faster and achieve smaller conduction loss, which is the key enabler for both high efficiency and high density. It is often a good practice to design the topology with evenly shared current stresses so that temperature becomes equally distributed, and circuit layout becomes more convenient. The flying capacitors in STCs are characterized by two categories: resonant capacitors C_R and dc filtering capacitors C_F. Each resonant capacitor is in series connection with a resonant inductor to essentially form an *LC* resonant tank. Multiple *LC* tanks that share the same resonant frequency are incorporated in an STC to partially replace the original dc flying capacitors in SCCs. Therefore, instead of switching and transferring energy between flying capacitors like traditional SCCs, in an STC, the energy is always being transferred between one *LC* tank and another *LC* tank or a dc filtering capacitor during switching. This characteristic explains the topology name STCs. Different types of technologies are adopted for the two categories of capacitors in order to overcome the limitation reported in the previous section. High performance Class-I (e.g., C0G, U2J) MLCC capacitors can be used as resonant capacitors

TABLE I
COMPARISON BETWEEN SCC AND STC TOPOLOGIES

	SCCs	SCCs with aggregated inductors [24]-[28]	SCCs with distributed inductors [21], [29] and [30]	STCs
Soft charging	No	Partial	Full	Full
Soft switching capability	No	Yes	Yes	Yes
Immunity to component non-idealities	Poor	Medium	Very poor	Very good
Device voltage clamp	Clamped, low stress	Case by case	No clamp, very high stress	Clamped, low stress
Scalability	Poor	Medium	Very good	Very good

in an STC. Their tight tolerance ($\pm 5\%$) and low ESR (dissipation factor 0.1%) over a wide voltage and temperature range are perfectly suitable for resonant operation. Class-II (e.g., X7R, X6S, etc.) MLCC capacitors that offer much higher capacitance than Class-I capacitors are used as dc filtering capacitors, which serve for the dc filtering and clamping functions. Because a dc filtering capacitor works almost like a dc voltage source with very minimal ac ripples, it has negligible impact on the resonant operation of STC. This makes the STC operation very insensitive to the large tolerances of the Class-II MLCC capacitors. Benefiting from the resonant operation of the *LC* tanks, all the switches in an STC can be controlled to turn ON and OFF upon current reaching zero. This zero current switching (ZCS) feature allows an STC to be almost free of switching losses, particularly in low-voltage applications where MOSFET $C_{\rm oss}$ charge losses are much less significant. Hence, an STC can inherently achieve very high efficiency. As the resonant capacitors are Class-I ceramics with $\pm 5\%$ tolerance, using matched resonant inductors to get a uniform resonant frequency across all the *LC* tanks becomes viable. As will be detailed in Section V, in order to tolerate more tank-to-tank variations, simple zero current detection techniques can be applied as well to adaptively control the ON time for each resonant tank such that each *LC* resonant frequency is always on track. One of the most critical features of an STC is that every individual current conduction subcircuit loop observes at least one *LC* resonant tank with inductive impedance at high frequency. Therefore, every flying capacitor is always being softly charged and discharged during operation. This key characteristic fundamentally eliminates the previously mentioned inrush current or charge redistribution losses associated with traditional SCCs. Compared to the previously mentioned topologies that incorporate aggregated inductors for soft charging, the soft charging of STC is 100% guaranteed regardless of flying capacitor matchings and tolerances.

In order to reliably leverage the superior FOMs of low-voltage rating MOSFETs, all switch drain-to-source voltages must be always clamped to desired dc levels by dc capacitors or capacitor networks. The dc filtering flying capacitors in STC naturally serve for this purpose. Even though multiple inductors are employed in an STC, none of the switches will see them in series at the OFF state. Instead, at any switching state, all the OFF switches are always clamped at either $V_{\rm out}$ or 2 $V_{\rm out}$ by the dc flying capacitors and input/output capacitors. This ensures the reliable use of low-voltage rating devices with minimal voltage stresses.

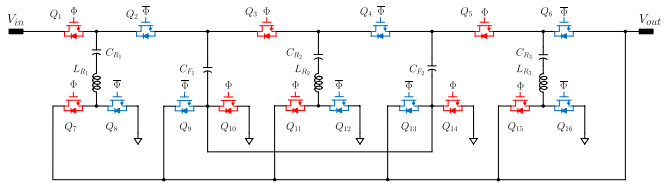

Fig. 5. 6-to-1 STC (1-phase, all switches clamped by $V_{\rm out}$ and 2 $V_{\rm out}$).

Enabled by the definitive output impedance, same STCs can be connected in parallel to operate in multiphase or multicell manners. The PWM clocks among paralleled phases or cells can be synchronized with or without phase interleaving, or even nonsynchronization. Inherent droop current balancing among phases or cells is achieved by using the same MOSFETs and *LC* tanks. This feature provides a great scalability of STCs to higher current and higher power. From the previous discussion, Table I here summarizes the comparisons of the most critical attributes of STCs and existing SCC topologies.

Fig. 4 shows a 1-phase 4-to-1 STC with all switches clamped by $V_{\rm out}$. $Q_1 - Q_6$ are the main switches and $Q_7 - Q_{12}$ are the SR switches. There are three *LC* resonant tanks (branch with L_R and C_R) and two dc filtering capacitors C_F with much lower voltage ripples (cancelled out) than the resonant capacitors C_R. In this topology, the C_F capacitors are biased by different dc voltages ($2V_{\rm out}$ and $3V_{\rm out}$) during normal operation. A 1-phase 4-to-1 STC with all switches clamped by $V_{\rm out}$ and $2V_{\rm out}$ is shown Fig. 3(b). In this topology, $Q_2 - Q_3$ and $Q_4 - Q_5$ are merged to a single switch with double voltage rating, respectively. DC filtering capacitors and resonant tanks are rearranged. Fig. 5 shows a 1-phase 6-to-1 STC which is scaled up from Fig. 3(b). C_{F_1} and C_{F_2} are connected together at one side here to provide a shorter clamping loop for Q_3 and Q_4. In Figs. 3(b) and 5, Class II ceramic capacitors are selected for C_F. This allows the resonant frequency to be determined pretty much only by L_R and C_R with very tight tolerance. Because the topology of Figs. 3(b) and 5 uses less switches and passive components, this topology becomes very compelling particularly in low-voltage (e.g., 48 V) high-current applications. The conversion ratio of this topology can be conveniently scaled up and down to even integers. As discussed earlier, STCs can support parallel operation for higher power by using multiphase or multicell configurations. Fig. 6 shows the 2-phase 4-to-1 STC topology derived from Fig. 3. Phase interleaving of 180°

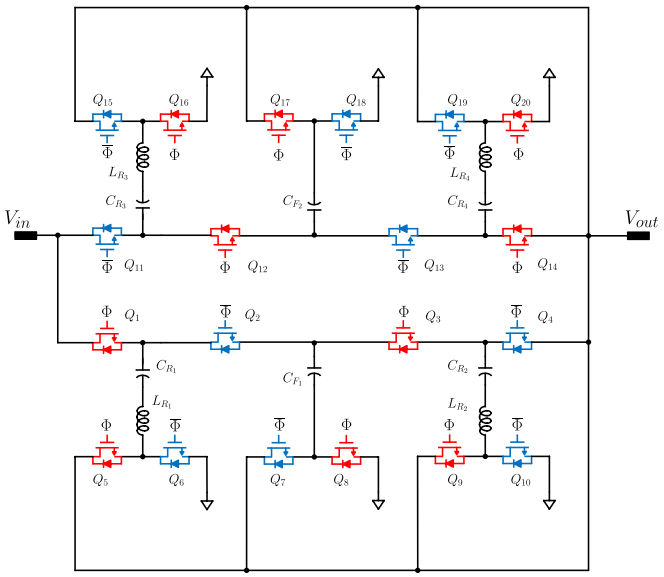

Fig. 6. 4-to-1 STC (2-phase, all switches clamped by $V_{\rm out}$ and 2 $V_{\rm out}$).

allows us to minimize input current ripple and decoupling capacitors.

IV. Analysis of the STC Topologies

A. STC Modeling

In this section, the state space average (SSA) circuit of a building block is introduced to make the circuit analysis of STC very simple and intuitive based on the approach described in [17], and in [41]–[43]. Each building block of Fig. 2(a) and (b) is driven by two gate signals, reported in Fig. 8(a), G_ϕ and $G_{\overline{\phi}}$ that are active during ϕ and $\overline{\phi}$ phase, respectively, with a dead time T_d. Each building block can be substituted by the block of Fig. 7 composed by a dc transformer and an equivalent impedance expressed as $Z_{\rm eq}$. The impedances $Z_{\rm io}$ carry the current induced by the common-mode voltage difference between the input and output port terminals. It can be easily concluded that this impedance can be approximated to

$$Z_{\rm io} \approx \frac{2}{sC_{\rm eq}} \tag{1}$$

where $C_{\rm eq}$ is C_F and C_R, respectively, for the building block of Fig. 2(a) and (b). The inductance L_R does not play a role because the resonant frequency is equal to the switching frequency and the SSA model is applicable for lower frequency. Based on the equivalent model in Fig. 7, it can be simply proved that as long as the dc blocking voltage of the transformer remains constant with dynamic load, the common mode impedance $Z_{\rm io}$ can be neglected. In an STC topology, the dc bias voltage of each flying capacitor represents the dc blocking voltage of the equivalent transformer in Fig. 7, and it will remain approximately constant under dynamic load assuming that the resonant tank building blocks are approximately matched. Apparently, any input line voltage dynamics will generate common mode current through $Z_{\rm io}$ impedances. However, the line voltage dynamics are often much slower than load dynamics in many applications, such that

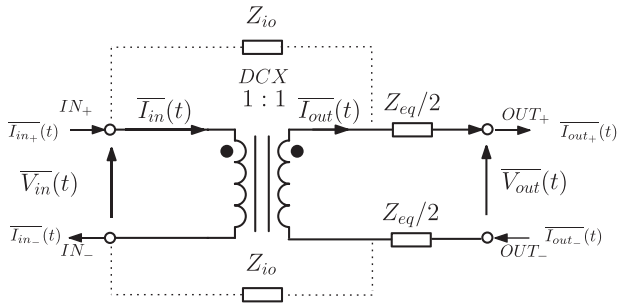

Fig. 7. Equivalent SSA model for a building block.

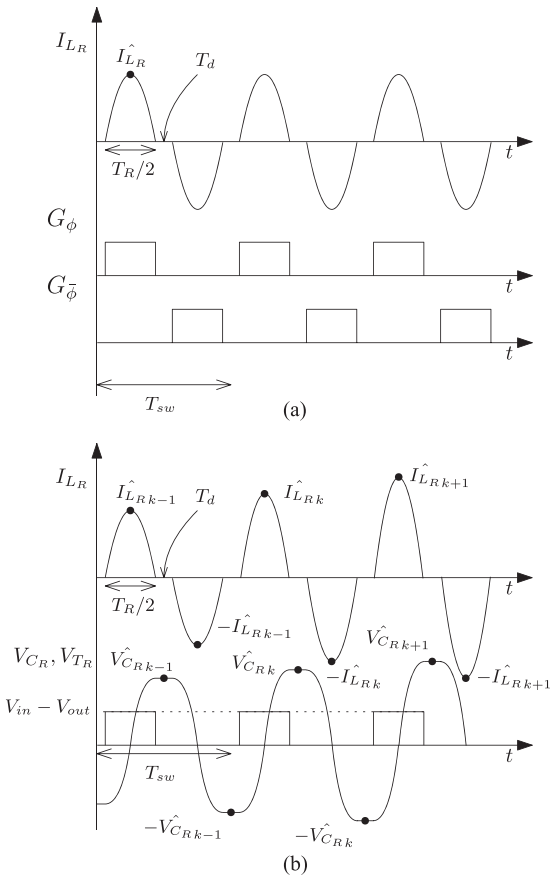

Fig. 8. (a) Driving signals and (b) waveforms of the building block of Fig. 2(b).

the contribution of $Z_{\rm io}$ impedances can be neglected as well. For the sake of simplicity, the calculation of the $Z_{\rm eq}$ is applied first on an ideal (high Q, $R_{\rm ac} \approx 0$) resonant building block. In order to calculate this contribution, the circuit of Fig. 2(b) will be analyzed with a fixed input voltage $V_{\rm in}$ and output voltage $V_{\rm out}$. This resonant switching circuit with a negligible $R_{\rm ac}$ is excited by $V_{\rm in}$ higher than $V_{\rm out}$ and the terminals IN$_-$ and OUT$_-$ are connected to ground. It exhibits the behavior reported in Fig. 8(a) in which the voltage across the resonant tank V_{T_R}, the voltage across the capacitor V_{C_R}, and the current I_{L_R} are reported. Each switch is turned ON for a period equal to $T_R/2$ and a dead time T_d is present before the turn ON of the complementary one. In this electrical condition, $I_{L_R}(t)$ exhibits a sinusoidal

transient behavior positive or negative with an amplitude $\hat{I_{L_R k}}$ that satisfies the relation (2) based on the conservation of the energy

$$\frac{\hat{I_{L_R k}}^2 L_R}{2} - \frac{\hat{V_{C_R k-1}}^2 C_R}{2} = (V_{\text{in}} - V_{\text{out}}) \frac{\hat{I_{L_R k}} T_R}{2\pi}. \quad (2)$$

Considering a period T_{sw}, the conservation of the energy can be expressed in relation of the voltage $\hat{V_{C_R k}}$

$$\frac{\hat{V_{C_R k}}^2 C_R}{2} - \frac{\hat{V_{C_R k-1}}^2 C_R}{2} = (V_{\text{in}} - V_{\text{out}}) \frac{\hat{I_{L_R k}} T_R}{\pi}. \quad (3)$$

Subtracting each element of (2) expressed for the $k+1$ period from the same equation expressed for the k period and substituting the energy of the capacitor expressed in (3), we can obtain

$$\frac{\hat{I_{L_R k+1}}^2 L_R}{2} - \frac{\hat{I_{L_R k}}^2 L_R}{2} = (V_{\text{in}} - V_{\text{out}}) \frac{\hat{I_{L_R k+1}} + \hat{I_{L_R k}}}{2\pi} T_R. \quad (4)$$

Note that the same relation can be calculated considering the conservation of the energy in a period between two peaks of the inductor currents. By simplifying (4), it is possible to obtain

$$V_{\text{in}} - V_{\text{out}} = L_R \frac{\pi}{T_R} \left(\hat{I_{L_R k+1}} - \hat{I_{L_R k}} \right). \quad (5)$$

The variation of $\overline{I_{\text{out}}(t)}$ over a period of T_{sw} can be derived as

$$V_{\text{in}} - V_{\text{out}} = \frac{\pi^2 {T_{\text{sw}}}^2}{{T_R}^2} L_R \frac{\overline{I_{\text{out}}}(t + T_{\text{sw}}) - \overline{I_{\text{out}}}(t)}{T_{\text{sw}}}. \quad (6)$$

From (6), an equivalent inductor that represents Z_{eq} impedance of Fig. 7 can be derived

$$L_{\text{eq}} = \frac{\pi^2 {T_{\text{sw}}}^2}{{T_R}^2} L_R. \quad (7)$$

Considering the presence of the lumped resistance R_{ac} that contains R_{dsON} contribution of the switches and all the losses of the resonant tank components, the equivalent resistance can be calculated by equaling the power dissipated by the tank during the operating phases and the power dissipated by the equivalent circuit with the average current $\overline{I_{\text{out}}(t)}$. The same approach was followed [17] obtaining a general expression for the SCC impedance for soft and hard charging conditions. The equivalent resistance of the building block R_{eq} can be derived considering the case of unity gain switched capacitor cell that operates in soft charging with a high Q resonance

$$R_{\text{eq}} = \frac{\pi^2 T_{\text{sw}}}{2T_R} R_{\text{ac}}. \quad (8)$$

Obviously, the equivalent impedance Z_{eq} of the building block of Fig. 2(a) with the clamping capacitor $C_F \gg C_R$ contains only the contribution of R_{eq}.

Taking the STC topology in Fig. 3(b) as an example, Q_2 and Q_3 can be split into two switches as was done for the synthesis in the previous section, reported in Fig. 3(a). The SSA equivalent circuit of the entire converter can be easily obtained by replacing each building block in the dashed box with the corresponding DCX model depicted in Fig. 7. Therefore, the 4-to-1 STC topology SSA model is composed of a matrix configuration of three DCX building blocks with their impedances as shown in Fig. 9.

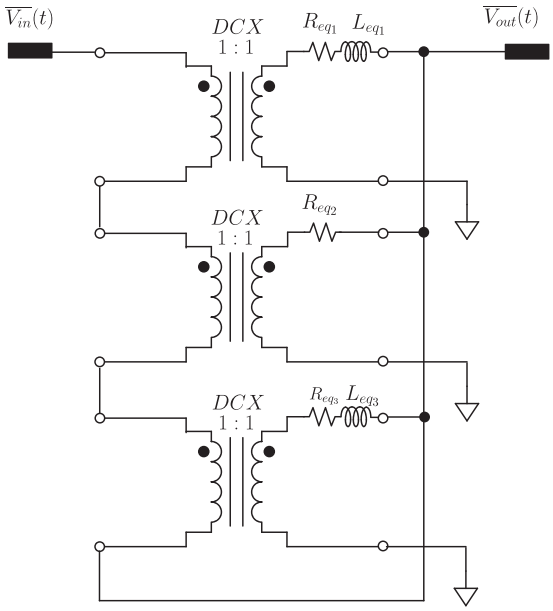

Fig. 9. Equivalent SSA model of the converter reported in Fig. 3(b).

During load transient, or equivalently for the computation of the output impedance, there is negligible variation of the common mode voltage difference between the input terminals and output terminals. Hence, in this case Z_{io} can be neglected. While in the line voltage dynamic event, or in the input impedance calculation, common-mode current that charges all the flying capacitors and the Z_{io} impedance should be taken into account. In Fig. 9, the DCX input terminals are connected in series and the outputs are connected in parallel. Each DCX block processes one-fourth of the total power. The IN$_-$ terminal of the third DCX block is connected to V_{out} such that the last one-fourth power is simply bypassed to the output. Likewise, the other STC topologies can be modeled by the matrix DCX equivalent circuit in the same manner. By simplifying the circuit, the total output impedance is

$$R_{\text{eq}_{\text{out}}} = \sum_{i=1}^{N-1} \frac{R_{\text{eq}_i}}{N^2} \quad (9)$$

and

$$L_{\text{eq}_{\text{out}}} = \sum_{i=1}^{N-1} \frac{L_{\text{eq}_i}}{N^2} \quad (10)$$

where N is equal to 4 and $L_{\text{eq}_2} = 0$.

By extending the matrix DCX model in Fig. 9 to *N*-to-1 conversion, the STC output impedance can be again described by (7)–(10). Assuming T_{sw} is sufficiently close to T_R, $R_{\text{eq}_{\text{out}}}$ is then only determined by R_{ac} of each STC building block. Equation (9) indicates that multiple STCs can operate in parallel with inherent droop current balancing. The R_{ac} mismatch between STCs is reasonably small such that good current balancing accuracy can be achieved (e.g., 10%).

In Fig. 10 are reported the comparison of transient waveforms from 10 to 40 A with an input voltage of 54 V applied to the circuit of Fig. 3(b) and its equivalent SSA model of Fig. 9.

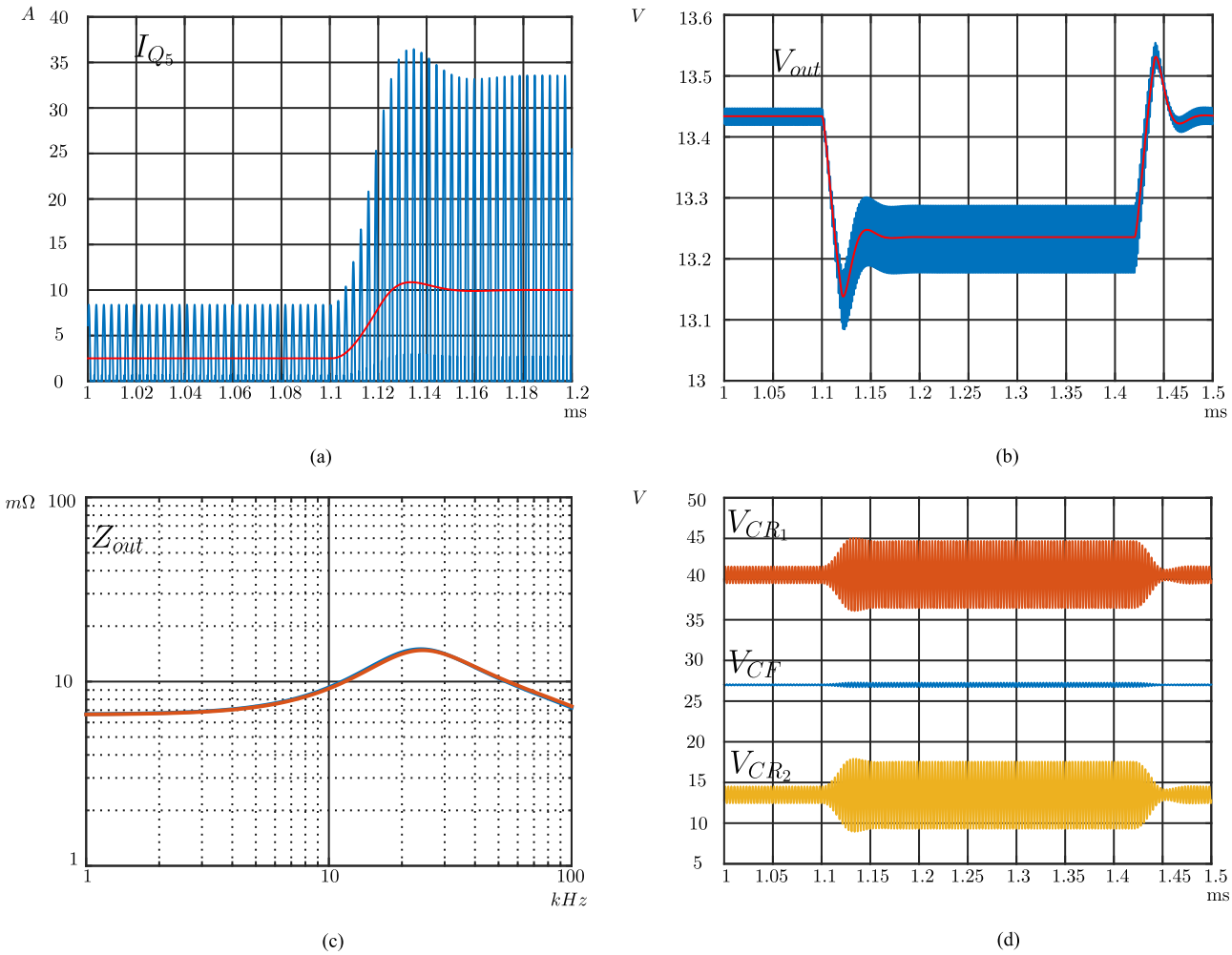

Fig. 10. Transient waveform comparisons of the converter of Fig. 3(b) and its SSA model of Fig. 9 during a load transient from 10 to 40 A. (a) I_{Q_5} outgoing current taken as positive of Fig. 3(b) (blue line) and I_{Leq_1} of Fig. 9 (red line). (b) Output voltage $V_{\rm out}$ of Fig. 3(b) (blue line) and of the SSA model (red line). (c) Simulation of the output impedance of the converter (blue line) and of the model (red line). (d) Voltage ripple of V_{CR_1}, V_{CR_2}, and V_{CF} during the load transient.

The main system parameters are: $C_R = 3.8\,\mu$F, $C_F = 60\,\mu$F, $L_R = 58$ nH. The lumped ac resistance is $R_{\rm ac} = 7\,$mΩ for the resonant tank building block and $R_{\rm ac} = 5\,$mΩ for the clamping capacitor building block, respectively. Finally, the output capacitor is composed of one 470-μF electrolytic capacitor with ESR $= 10\,$mΩ and 20 X6S MLCC capacitors of 22 μF (7 μF by considering the derating factor due to the dc bias) with ESR $= 3\,$mΩ each. As can be seen there is a good match of the converter dynamics shown in Fig. 10(a) and (b). Fig. 10(c) shows the comparison of ac simulations of the output impedance using SIMPLIS. The red line is the result obtained on the actual STC circuit and the blue line represents the associated SSA model. Finally, in Fig. 10(d) are reported the voltages V_{CR_1}, V_{CR_2}, and V_{CF} of the flying capacitors during the load transient. It shows that the bias voltage across V_{CF}, V_{CR_1}, and V_{CR_2} can be considered constant, making the contribution of $Z_{\rm io}$ in the SSA model negligible. Applying the same principle based on the matrix DCX circuit model, many other interesting circuits can be derived potentially. For example, by reconnecting the IN$_-$ terminal of the third DCX block in Fig. 9 to a 4-switch buck–boost regulator's input and connecting this buck–boost output in parallel with the STC output, a high-efficiency partial power STC-buck–boost topology with voltage regulation capability can be obtained. The DCX building block principle can be used as a simple and effective analytical tool as well to model many other SCC-based topologies.

B. Design Guidelines

Finally, the building block model introduced above is a good design tool to define the components starting from the converter specifications. As described before, the STC converter is constructed by a matrix connection of multiple fundamental building blocks that in general process part of the total output power. Each building block can be described by its SSA model characterized by the maximum output mean current, differential voltage across the primary/secondary side, and common-mode voltage from primary terminals to secondary terminals (defined as $V_{\rm cm}$ in Fig. 2). All these electrical quantities can be useful to define the maximum voltage and current of the components. The maximum bias voltage of each flying capacitor (including both the resonant capacitor C_R and the dc blocking capacitor

TABLE II
SWITCHES USED IN THE TOPOLOGY REPORTED IN FIG. 3(b)

Reference	Part Number	Q_g ($V_d = 6V$)	R_{dsON}	C_{oss}
Q_1-Q_4	BSZ025N04LS	23 nC	2.5 $m\Omega$	750 pF
Q_5-Q_{10}	BSZ013NE2LS5I	25 nC	1.3 $m\Omega$	1200 pF

C_F) is equal to the common-mode dc blocking voltage from the primary terminals to the secondary terminals of each building block. Considering the maximum output current for a given building block as $\overline{I_{\text{out}_m}}$, the maximum peak current $\hat{I_{C\,m}}$ and the rms current $I_{C_{\text{RMSm}}}$ for each capacitor can be calculated as follows:

$$\hat{I_{C\,m}} = \overline{I_{\text{out}_m}}\,\pi\frac{T_{\text{sw}}}{T_R} \tag{11}$$

$$I_{C_{\text{RMSm}}} = \frac{\hat{I_{C\,m}}}{\sqrt{2}}\sqrt{\frac{T_R}{T_{\text{sw}}}}. \tag{12}$$

As previously mentioned in Section III, high-performance Class-I (e.g., C0G, U2J) MLCC capacitors should be used as resonant capacitors C_R, meanwhile Class-II (e.g., X7R, X6S, etc.) MLCC capacitors that offer much higher capacitance are used as dc filtering/clamping capacitors C_F. In both cases, the minimum amount of capacitors is determined by their capability of supporting the max RMS current expressed in (12). Obviously, better efficiency performance can be reached by increasing the capacitor values in order to reduce the total ESR. After defining the value of C_R, the value of L_R is determined by the operating frequency F_{sw}. The inductance is dimensioned considering the maximum peak current and the rms current reported, respectively, in (11) and (12). The voltage stress of the switches has been already discussed in the previous session. The maximum current is expressed by (11) and the RMS current is $1/\sqrt{2}$ of the value calculated by (12). Finally, each loss contribution can be calculated. The losses of the passive components in each building block can be calculated by $I_{C_{\text{RMSm}}}$ and the ac resistance. The loss related to each MOSFET has three main contributions: the conduction loss, the C_{oss} loss due to the ZCS working condition, and the gate driver loss. Considering each MOSFET conducts $I_{C_{\text{RMSm}}}$ for one half of the period T_{sw} and the drain–source voltage during the dead time T_d before the next turn ON approximatively equals to one-half of V_{dsOFF}, each MOSFET loss can be expressed as follows:

$$\begin{aligned} P_{\text{MOS}} &= P_{\text{MOScond}} + P_{\text{MOSsw}} + P_{dr} \\ &= R_{\text{dsON}}\frac{{I_{C_{\text{RMSm}}}}^2}{2} + \left(\frac{V_{\text{dsOFF}}}{2}\right)^2 C_{\text{oss}} f_{\text{sw}} + V_{dr} Q_g f_{\text{sw}} \end{aligned} \tag{13}$$

Even if P_{MOSsw} and P_{dr} create a frequency limitation, these two contributions are not dominant for the STC architecture reported in Figs. 3–6, in which V_{dsOFF} is V_{out} or $2V_{\text{out}}$. In fact considering the 4-to-1 STC topology reported in Fig. 3(b) with an input voltage $V_{\text{IN}} = 54$ V, a maximum output current of $I_{\text{out}} = 50$ A and the switches listed in Table II, the total MOSFET losses (reported in Table III for different switching frequencies) are modest compared with the output power ($P_{\text{out}} \cong 650$ W at maximum load).

TABLE III
TOTAL MOSFET LOSS COMPARISON AT DIFFERENT SWITCHING FREQUENCIES WITH $V_{\text{IN}} = 54$ V, $I_{\text{out}} = 50$ A

f_{sw}	P_{dr}	P_{MOSsw}	$P_{MOScond}$ at $I_{OUT} = 25\,A$	$P_{MOScond}$ at $I_{OUT} = 50\,A$
200 kHz	290 mW	175 mW	1.78 W	7.15 W
400 kHz	580 mW	350 mW	1.78 W	7.15 W
800 kHz	1.16 W	700 mW	1.78 W	7.15 W

V. IMMUNITY TO COMPONENT MISMATCHES

Most of STCs topologies contain more than one resonant tank with mutual mismatches. Considering 4-to-1 topology reported in Fig. 3(b) with a small dead time T_d, the effect of the mismatch on the resonant tanks (worst case with L_R $\pm 10\%$ and C_R $\pm 5\%$) is reported in Fig. 11(a). The resonant tank with shortest T_R exhibits a bigger RMS current and the ZCS conditions are lost for both turn ON and turn OFF of the switches. A higher dead time T_d reduces difference in the RMS current as can be seen in Fig. 11(b), but the switch turn-OFF conditions are not optimal and body-diode conduction losses are present. The best solution is based on managing the ON time of each individual switch in order to achieve the ZCS during the switching transition. This operation can be obtained by using some zero-crossing detection techniques in the controller or drivers to trigger the turn OFF of the devices. Obviously, the dead time T_d reported in Fig. 8 must be sufficiently large to compensate the maximum mismatch between different resonant periods T_{Ri}. In other words in a topology with N_R resonant building blocks, T_{sw} is larger than the maximum T_{Ri} as reported in following equation:

$$T_{\text{sw}} > \max_{1\le i\le N_R} T_{Ri}. \tag{14}$$

The impact of the mismatches on the current sharing can be easily predicted by the SSA model reported in the previous section. Each resonant building block impedance Z_{eqi} can be calculated by using a different resonant period T_{Ri} in (7) and (8). The nonresonant building blocks are conducting resonant current with two different T_{Ri} in the two switching states. The equivalent resistance can be calculated by using (8) and considering the mean value of the two T_{Ri}. STC topologies such as Figs. 3–5 have a balanced current among the building blocks even if their impedances are mismatched. This consideration can be easily verified by the series connection of the equivalent DCX blocks reported in Fig. 9. For STC parallel operations, the current sharing accuracy within the two phases shown in Fig. 6 depends on the worst case mismatch of the two equivalent output resistances $R_{\text{eq}_{\text{out}}}$ of each phase calculated by (9). The variation of the phase output current I_{out} is simply derived and reported in the following equation

$$\left|\frac{\Delta I_{\text{out}}}{I_{\text{out}}}\right| = \left|\frac{\Delta R_{eq_{\text{out}}}}{R_{eq_{\text{out}}}}\right|. \tag{15}$$

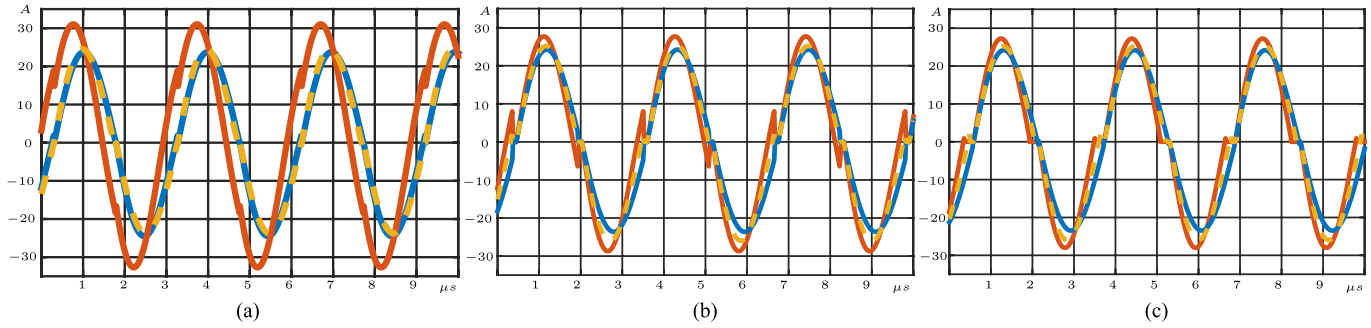

Fig. 11. Effect of the resonant tank mismatches (worst case with L_R $\pm 10\%$ and C_R $\pm 5\%$) on the two inductor currents I_{L_R} (red and blue lines) of the converter reported in Fig. 3(b) at 30 A compared with nominal condition (dashed yellow line). (a) Solution with T_d of 10 ns. (b) Solution with T_d of 100 ns. (c) Using adaptive ON time control.

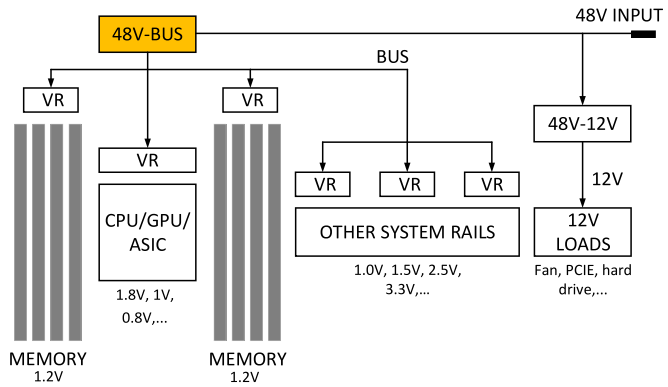

Fig. 12. Proposed power system architecture for 48-V data center server board.

VI. STC Application in Data Center

Benefiting from all the unique electrical characteristics discussed above, the proposed STC topologies can extraordinarily address the SCC technical challenges described in Section II. This makes the adoption of STCs for industry's mass production design much easier. The proposed STCs are widely applicable to high-ratio dc–dc bus conversions where galvanic isolation is not a requirement. A power system of 48-V data center is one of the emerging applications that can very well leverage the advantages of STC. Fig. 12 shows the proposed power system architecture for a typical 48-V server board in data center. A two-stage conversion approach is adopted here for the microprocessor (CPU, GPU, ASIC, etc.) core rails, memory rails, and other system house-keeping rails. The first stage bus converter uses an STC to step down the input 48 V bus to an intermediate voltage bus. Single-phase or multiphase buck regulators are used for the second-stage point-of-load power conversions. The voltage of the intermediate bus can be optimally selected to achieve the best overall performance in terms of efficiency, density, and cost.

Fig. 13 shows a 4-to-1 STC bus converter architecture implemented with the control and driving system. As reported in the schematic, the controller generates two pairs of complementary gate driver signals $G_1\phi$, $G_1\overline{\phi}$ and $G_2\phi$, $G_2\overline{\phi}$ with different dead time T_d. The correct dead time T_d in order to achieve the ZCS operation for each resonant tank is obtained by monitoring the switching node V_{1s} for the first tank and V_{2s} for the second tank. Zero current detection for each tank can be obtained by checking the body diode conduction state of Q_5, Q_6, Q_9, and Q_{10} during T_d or by measuring the ON-state voltage drop of each FET. A simple and scalable charge pump circuit is designed to generate bias power for each gate driver. A front-end buck converter is incorporated for STC start up and protections. Upon start up, the STC controller generates PWM signals first to the STC power train and then enables the buck converter to ramp up. At a steady state, the buck converter operates with 100% duty cycle to offer a 99.9% efficiency. Meanwhile, the buck inductor serves as the input filter for STC. When the STC controller detects a fault event, it immediately shuts down the buck converter such that every voltage in the downstream of the buck can be safely discharged. Detailed circuit design and operations are not in the scope of this paper.

VII. Experimental Results

A 650-W 4-to-1 STC product evaluation board shown in Fig. 14 has been designed for the data center 48-V bus conversion. The key parameters and components are listed in Table IV. To avoid confusion, the 48-V bus specifications here are based on Google data center power rack. As seen in Fig. 14, even though components are loosely populated to meet Google's data center DFM requirements, a very high power density of 500 W/in^2 is achieved with the STC power train. The driver and control circuitries can be potentially integrated by semiconductor manufacturers to offer an overall compact solution. As can be seen in Table IV, L_R is a high-current shielded inductor with low emission [40] and low tolerance, C_R is composed by Class I (U2J) capacitors, and $T_{\rm sw}$ corresponds to the relation (14).

Fig. 15(a) shows the steady-state waveforms of the drain-to-source voltages across Q_1, Q_2, and Q_8. In this 4-to-1 STC, the maximum voltage stress for Q_1–Q_4 is $2V_{\rm out}$. However, for Q_1 and Q_4, the nominal blocking voltage is $V_{\rm out}$; during the dead time (100 ns in this design), the voltage stress may increase up to $2V_{\rm out}$ due to switching timing mismatches. All the output SR FETs (Q_5–Q_{10}) have the maximum voltage stress of $V_{\rm out}$. Benefiting from zero current switching, switching spikes can barely be seen with each FET. In Fig. 15(b), the sine-wave

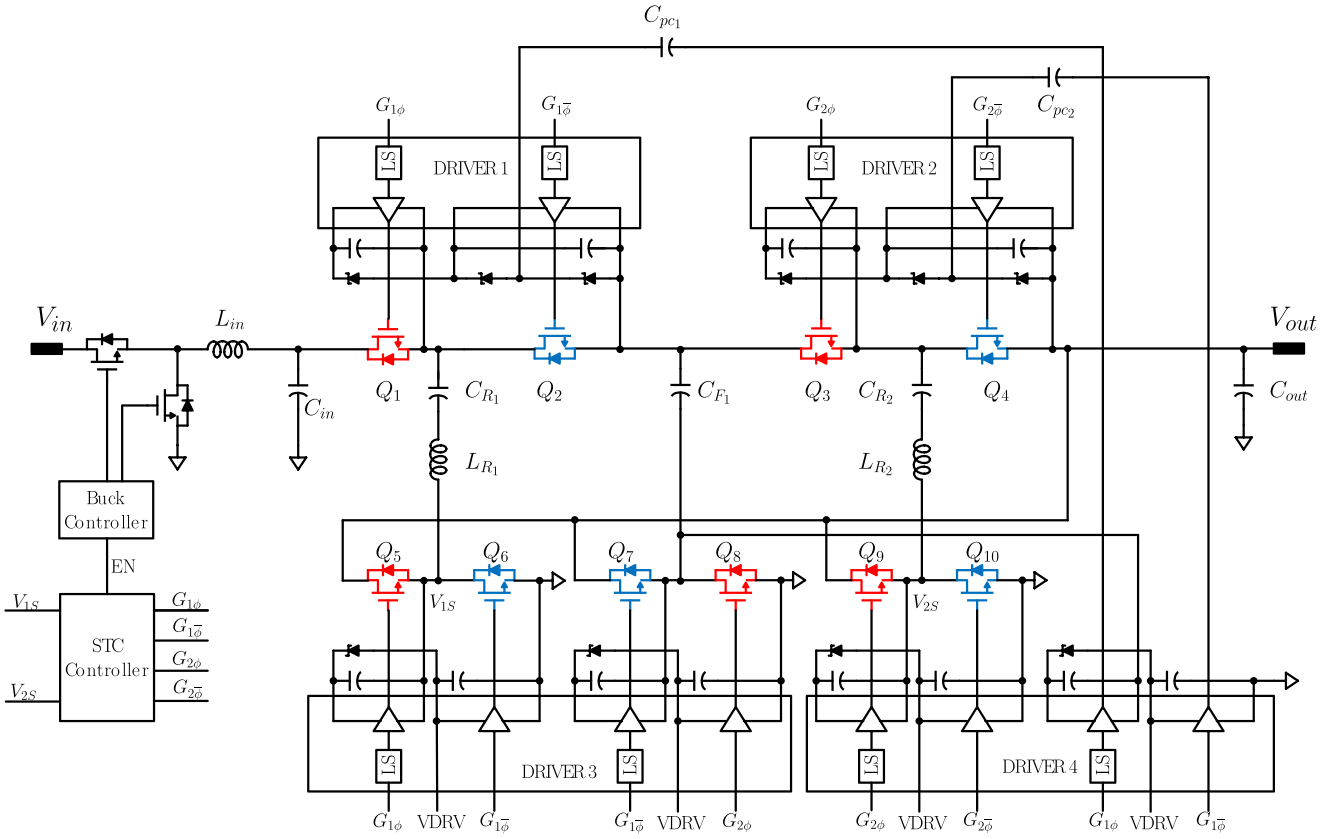

Fig. 13. STC architecture with the control and driving system.

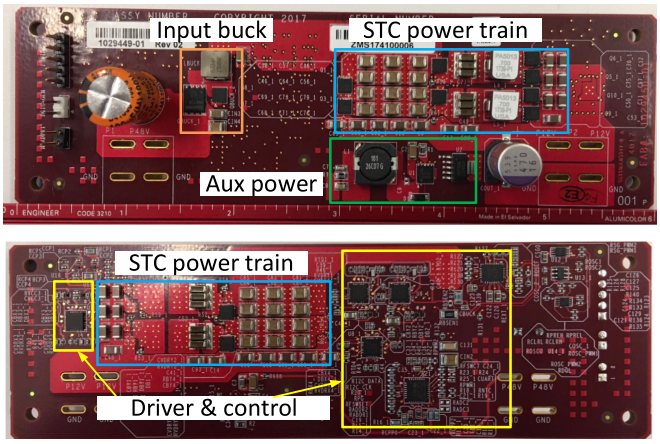

Fig. 14. Product evaluation board of 650-W 4-to-1 STC.

TABLE IV
KEY PARAMETERS AND COMPONENTS OF THE 4-TO-1 STC IN FIG. 13

Input voltage V_{in}	40 V-60 V, 54 V nominal
Output voltage V_{out}	9.5 V-15 V, 13.5 V nominal
Output current I_{out}	50 A
C_R	3.8 uF (0.47 uF, 50 V, U2 J, +/-5%, 8 pcs, Kemet)
L_R	58 nH (PA5013, +/-4 nH, Pulse)
C_F	60 uF (10 uF, 50 V, X7R, 12 pcs, Murata)
C_{IN}	35 uF (10 uF, 100 V, X7S, 12 pcs, Murata)
C_{OUT}	470 uF polymer + 140 uF MLCCs
Q_1 - Q_4	BSZ025N04LS (40 V, 2.5 mOhm)
Q_5 - Q_{10}	BSZ013NE2LS5I (25 V, 1.3 mOhm)
F_{sw}	320 kHz
STC controller	STNRG328 A (STMicro)
Gate driver	STRG04 (STMicro)
Buck controller	LTC7801 (Linear Tech)

voltage ripples across capacitor C_{R1} and C_{R2} are shown. The peak and valley are both aligned with the switching edges to achieve ZCS. Due to the charge balance principle, the currents in both resonant tanks are automatically balanced. As shown in Fig. 16 are the waveforms during the load step transients. The STC demonstrates an intrinsically fast response as there are very little energy storage components in the topology. Fig. 17 shows the start up and shut down waveforms of STC. Upon start up, the bias power becomes available first when V_{in} reaches around 15 V. At the same time, the STC controller generates switching signals to the STC power train. After a short delay (3 ms), the STC controller issues an enable signal to the input buck for ramp up. The buck converter eventually enters bypass mode (100% duty cycle) once its output voltage reaches the input.

The STC output voltage droop characteristics has been measured and shown in Fig. 18. It verifies the STC output resistance model predicted by (9). This droop characteristic allows multiple STCs for parallel operation when their internal ac resistances are well matched. Fig. 19(a) demonstrates the superior

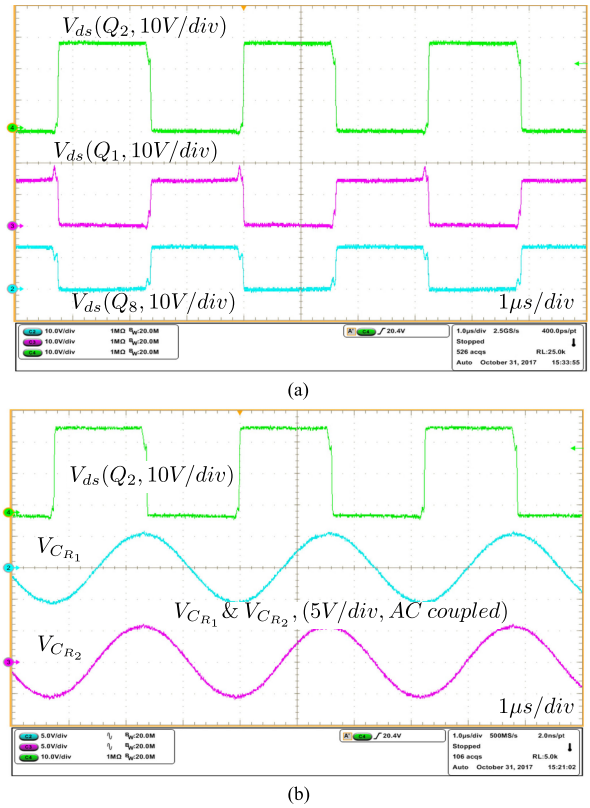

Fig. 15. STC steady-state waveforms ($V_{\text{in}} = 54$ V, $I_{\text{out}} = 50$ A). (a) V_{ds} voltages of Q_1, Q_2, and Q_8. (b) Voltage across the capacitors $C_{R_{1,2}}$.

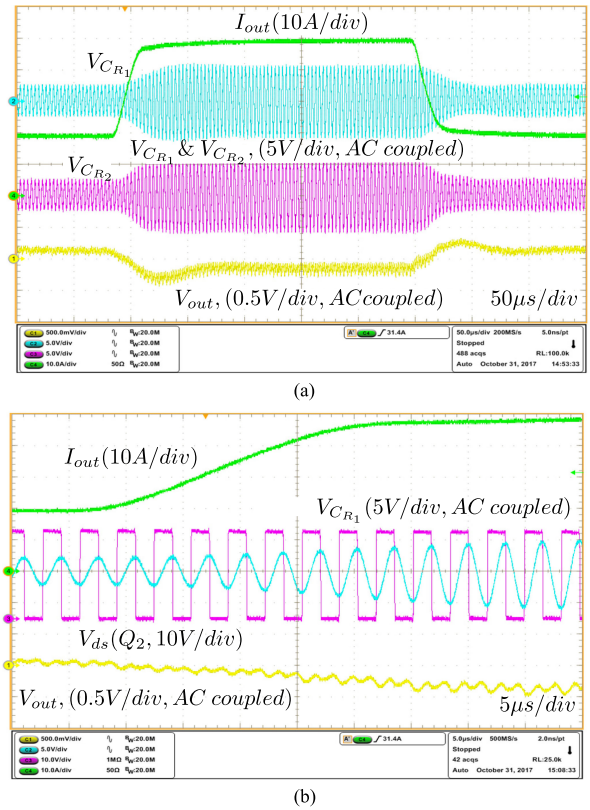

Fig. 16. STC load transient waveforms ($V_{\text{in}} = 54$ V, $I_{\text{out}} = 20$–50 A). (a) V_{out}, $V_{C_{R_{1,2}}}$, and I_{out}. (b) Detail of load step up transient with V_{ds} voltages of Q_2.

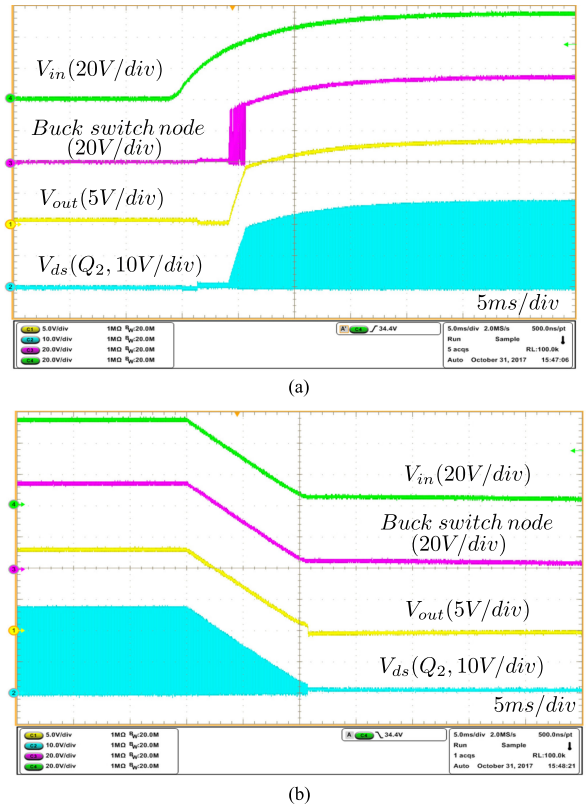

Fig. 17. STC (a) startup and (b) shut down transient main waveforms: V_{in}, buck switch node, V_{out} and V_{ds} voltages of Q_2.

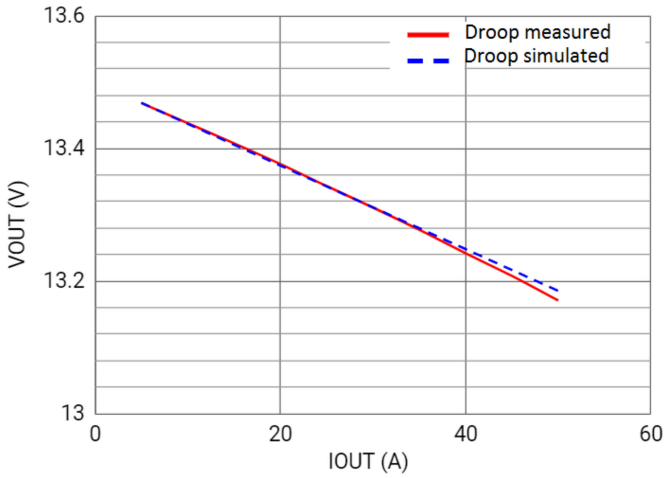

Fig. 18. STC output voltage versus output current ($V_{\text{in}} = 54$ V) (red line) and the simulated value by using the model (dashed blue line).

efficiency performance of the STC topology. The 4-to-1 STC evaluation board achieves a very high peak efficiency of 98.92% excluding bias power and 98.61% with bias power. At full load, 97.51% without bias and 97.41% with bias are still maintained. In Fig. 19(b), the loss breakdown at full load is reported. It is shown that the total loss is dominated by the conduction loss in the switches and the passive components. Optimizing the core-winding structure and taking better care of winding, ACRs

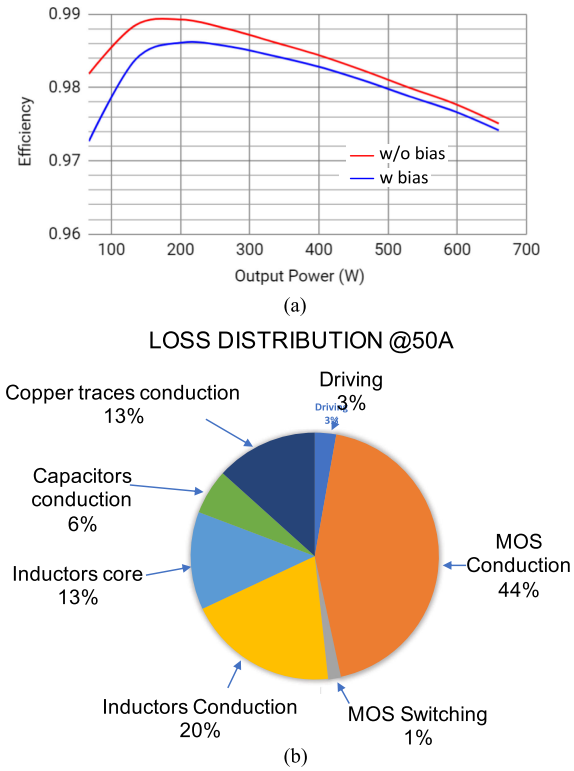

Fig. 19. (a) STC efficiency with and without bias power ($V_{\text{in}} = 54$ V). (b) Loss breakdown at full load.

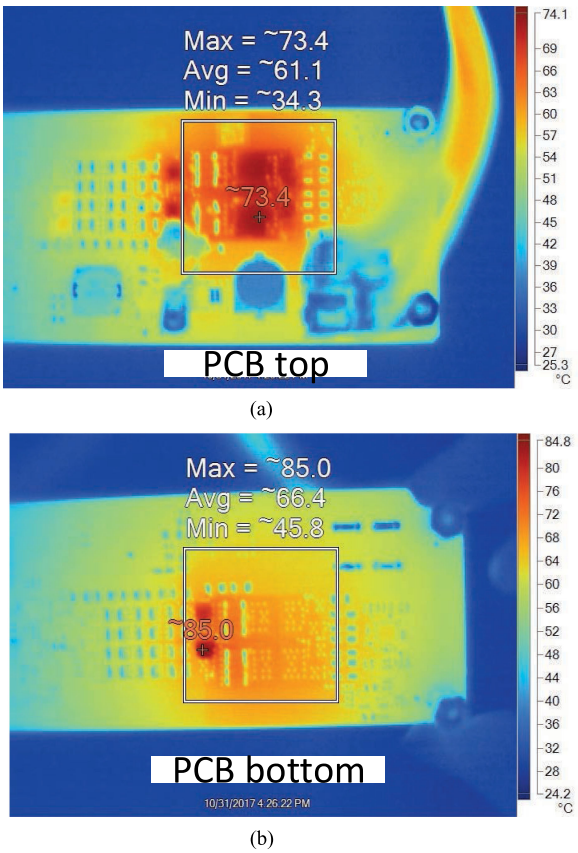

Fig. 20. STC thermal performance with fan cooling only ($V_{\text{in}} = 54$ V, $I_{\text{out}} = 50$ A, $T_a = 25$ °C).

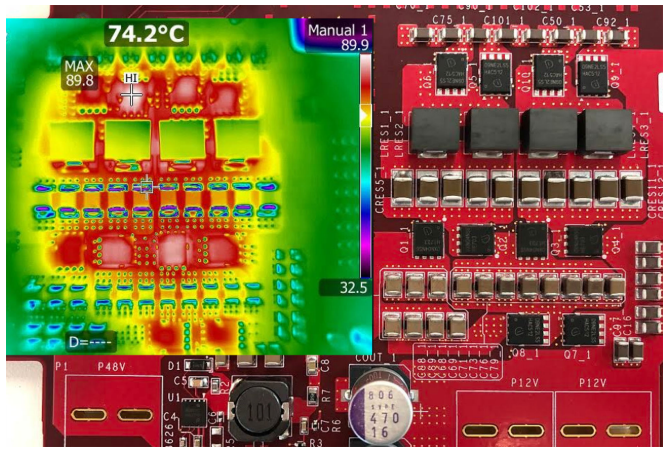

Fig. 21. STC 1.2-KW design, thermal performance with fan cooling ($V_{\text{in}} = 54$ V, $I_{\text{out}} = 92$ A, $T_a = 25$ °C).

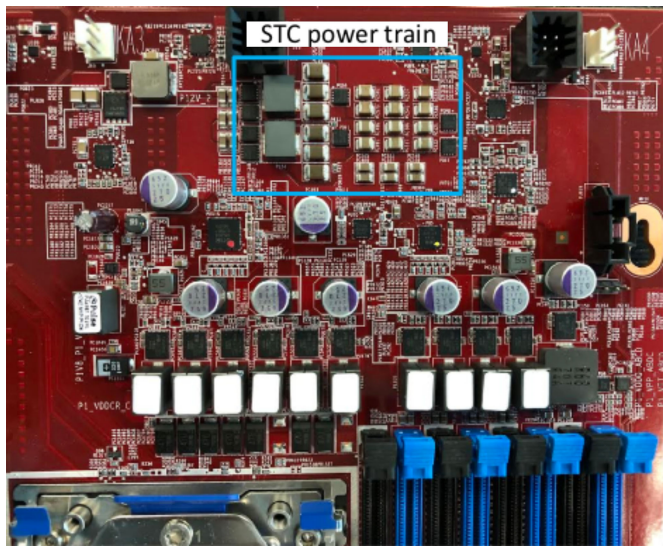

Fig. 22. Mass-production 48-V server that incorporates STC for first-stage bus conversion.

may further improve the full load efficiency. Fig. 20 shows the thermal image of the STC board with fan cooling only at full load and room temperature. It shows an extraordinary thermal performance without any heat sink, which significantly simplifies the thermal management in data center server board designs. This STC design can be easily scaled for higher power specifications by using off-the-shelf standardized components only. In Fig. 21 is reported a 1.2-kW STC design with the thermal performance under fan cooling at full load. Finally, in Fig. 22 is reported a mass-production 48-V server system design that employs a 4-to-1 STC as the first bus voltage conversion stage.

VIII. Conclusion

This paper has presented a new class of STCs for very high efficiency high density dc–dc power conversion where high conversion ratio is required. The STCs uniquely employ *LC* reso-

nant tanks to partially replace the dc flying capacitors in traditional SCCs; thus, providing complete soft charging, soft switching, and minimal device voltage stresses under all operating conditions. The proposed STC topologies overcome the fundamental technical barriers of existing SCC derivative topologies by offering strong robustness against component nonidealities, control simplicity, and extraordinary scalability. Therefore, all these features of STCs have expedited the technology maturity for industry's high volume adoption. In addition to the proposal of the STC topology, an equivalent DCX building block principle has been introduced as a simple and effective analytical tool to better understand the STCs. The same principle can also be applied to analyze other SCC-based topologies or derive new topologies. This paper focuses on one of the emerging applications, 48-V data center server board power delivery. A 650-W 4-to-1 STC evaluation board was designed for the 48-V bus converter. Experimental results have been presented to demonstrate the STC operation principles, electrical characteristics, and superior performance (efficiency, density, thermal, etc.). It should be noted that STCs can be applied to a very broad range of power conversion. Due to the scope limit, many implementation details such as gate driver design, fault protections, input buck design, component integrations, layout considerations, adaptive PWM control schemes and so on are not discussed in this paper.

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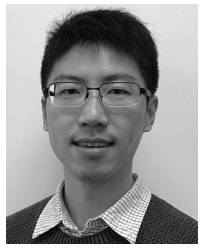

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