Source-Side Series-Virtual-Impedance Control to Improve the Cascaded System Stability and the Dynamic Performance of Its Source Converter

Xin Zhang, *Member, IEEE*, Qing-Chang Zhong, *Fellow, IEEE*, Visakan Kadirkamanathan, Jinsong He, *Student Member, IEEE*, and Jingjing Huang, *Member, IEEE*

***Abstract*—Instability problem is an important issue for dc/dc conversion cascaded systems (Cascaded system in short). Though most of the existing stabilization methods can stabilize the whole system very well, they may ignore their impacts on the dynamic performance of the original cascaded system. Unfortunately, these impacts are negative to some extent. Recently, an adaptive-series-virtual-impedance (ASVI) control strategy has been reported to address the above problem. It not only can stabilize the cascaded system via shaping the load input impedance, but also can reduce its impact on the original load converter. However, though the ASVI control strategy has already greatly reduced its impact on the load converter, its remaining impact is negative. To solve this problem, this paper moves the ASVI from the load side to the source side via a proposed *source-side series-virtual-impedance* (SSVI) control strategy for the source converter. This SSVI control strategy not only has the same stabilization function and adaptive characteristics as the ASVI control strategy, but also improves the performance of the source converter. In addition, since the SSVI control strategy is realized by changing the control block of the source converter, the performance of the load converter is not affected. Therefore, the SSVI control strategy can be treated as a supplement and expansion of the ASVI control strategy. Moreover, depending on the method of realization, the SSVI control strategy can be divided into the source stabilization methods of the cascaded system. Finally, a 100 W 48 V–32 V–24 V cascaded system has been fabricated to validate the proposed control strategy.**

***Index Terms*—Cascaded system, dynamic performance, impedance control, source-side series-virtual-impedance (SSVI), stability.**

Manuscript received January 18, 2018; revised May 1, 2018 and July 30, 2018; accepted August 6, 2018. Date of publication August 26, 2018; date of current version April 20, 2019. This work was supported by NTU-SUG grant: 'Stability, Reliability and Advanced Control of Power Electronic Systems (SCOPES)'. Recommended for publication by Associate Editor M. Molinas. *(Corresponding author: Xin Zhang.)*

X. Zhang, J. He, and J. Huang are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore (e-mail:

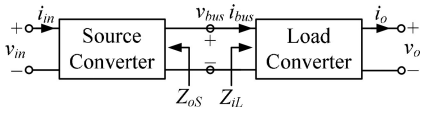


Fig. 1. Typical cascaded system.

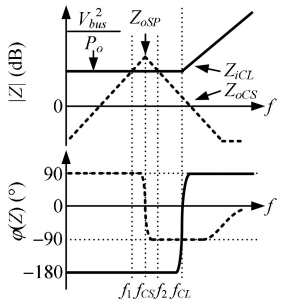


Fig. 2. Impedance Bode plots of the unstable cascaded system.

on the dynamic performance of the original cascaded system. Unfortunately, these impacts are negative to some extent. For instance, the negative resistor characteristics of the load input impedance is a potential factors that cause the system unstable; thus, most existing stabilization methods are aimed at totally remove the negative resistor characteristics from the load input impedance. However, this negative resistor characteristics is also an important guarantee of the fast dynamic performance of the load converter. To solve this kind of contradiction, a family of load stabilization methods have been proposed. In [21], both parallel-virtual-impedance (PVI) and series-virtual-impedance (SVI) control strategies have been proposed to stabilize the cascaded system via shaping the load input impedance only in a specific frequency range. As a result, both the PVI and SVI control strategies keep most dynamic performance of the original load converter. In [22] and [23], [24], the adaptive characteristic has been introduced to the PVI and SVI control strategies, respectively. With the adaptive-PVI (APVI) or adaptive-SVI (ASVI) control strategy, the load converter can be stably connected to different source converters without changing its internal structure. Besides, compared to the APVI control strategy, the ASVI control strategy can make the cascaded system more stable.

In this paper, a further investigation on the ASVI control strategy is carried out. It is found that, though the ASVI control strategy has already greatly reduced its impact on the load converter, its remaining impact is negative. In order to fix this problem, the ASVI has been moved from the load side to the source side via the proposed *source-side series-virtual-impedance* (SSVI) control strategy for the source converter. Since the ASVI has not been changed, the SSVI control strategy has the same stabilization function and adaptive characteristics with the ASVI control strategy. In addition, since the SSVI control strategy is realized by changing the control block of the source converter, the performance of the load converter is not affected. Furthermore, the proposed SSVI control strategy also improve the performance of the source converter. Therefore, the SSVI control strategy not only can be treated as a supplement/expansion of the ASVI control strategy, but also can be treated as an effective source stabilization methods of the cascaded system.

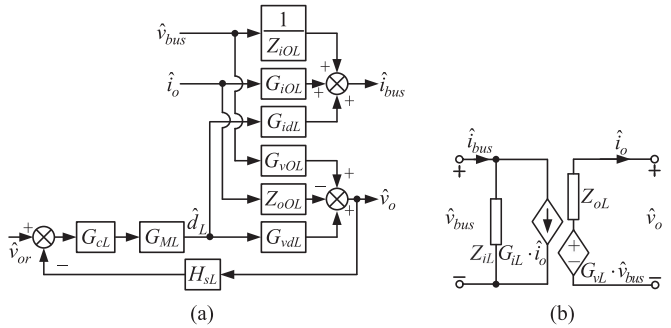


Fig. 3. Two-port network model of the original load converter. (a) Block diagram. (b) Two-port network model.

The rest parts of this paper are organized as follows: the impacts and limitations of the ASVI control strategy on the load converter is analyzed and concluded in Section II. Then, the SSVI control strategy and its impacts on the source converter have been proposed and discussed in Section III, where the SSVI control strategy is also compared with the ASVI control strategy. After that, a 100 W 48 V–32 V–24 V cascaded system is experimentally employed to verify the effectiveness of the SSVI control strategy in Section IV. Finally, Section V concludes this paper.

II. Impact of the ASVI Control Strategy on the Load Converter via Two-Port Network Analysis

In this section, the generic two-port network models of the load converter with/without the ASVI control strategy are first derived. Then, the impacts of the ASVI control strategy on the load converter is analyzed by a specific cascaded system.

A. Two-Port Network Model of the Original Load Converter

The small signal block diagram of the original load converter has been presented at Fig. 3(a), where $v_{\rm bus}$ and $i_{\rm bus}$ are the input voltage and current of the load converter, respectively; v_o and i_o are the output voltage and current of the load converter, respectively; d_L is the duty cycle of the load converter; $Z_{iOL}(s)$ is the open-loop input impedance of the load converter; $G_{iOL}(s)$ is the open loop i_o to $i_{\rm bus}$ transfer function; $G_{idL}(s)$ is the d_L to $i_{\rm bus}$ transfer function; $G_{vOL}(s)$ is the open loop $v_{\rm bus}$ to v_o transfer function; $Z_{oOL}(s)$ is the open-loop output impedance of the load converter; $G_{vdL}(s)$ is the d_L to v_o transfer function. In addition, as shown in Fig. 3(a), a voltage closed-loop has been utilized for the load converter, where $H_{sL}(s)$ and $G_{cL}(s)$ are the sampling coefficient and voltage regulator transfer function of the output voltage, respectively; $G_{ML}(s)$ is the transfer function of the modulator.

According to Fig. 3(a), the generic two-port small signal model of the original load converter is derived and presented in Fig. 3(b) [25], where $Z_{iL}(s)$ is the closed-loop input impedance of the load converter; $G_{iL}(s)$ is the closed-loop load to input current transfer function of the load converter; $G_{vL}(s)$ is the closed-loop input to output voltage transfer function of the load

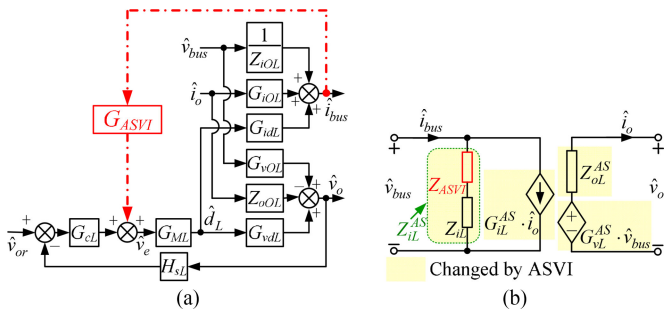


Fig. 4. Two port network model of the load converter with the ASVI control strategy. (a) Block diagram. (b) Two-port network model.

converter; $Z_{oL}(s)$ is the closed-loop output impedance of the load converter. It is known that, the performance of the original load converter can be fully described by $Z_{iL}(s) \sim Z_{oL}(s)$ [25], whose expressions can be derived as follows:

$$Z_{iL}(s) = \left.\frac{\hat{v}_{\rm bus}(s)}{\hat{i}_{\rm bus}(s)}\right|_{\hat{i}_o(s)=0} = \frac{[1+T_{vL}(s)]Z_{iOL}(s)G_{vdL}(s)}{G_{vdL}(s)-T_{vL}(s)[G_{vdL}(s)-Z_{iOL}(s)G_{idL}(s)G_{vOL}(s)]} \tag{1}$$

$$G_{iL}(s) = \left.\frac{\hat{i}_{\rm bus}(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{\rm bus}(s)=0} = G_{iOL}(s) - \frac{Z_{oOL}(s)G_{idL}(s)}{G_{vdL}(s)}\frac{T_{vL}(s)}{1+T_{vL}(s)} \tag{2}$$

$$G_{vL}(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_{\rm bus}(s)}\right|_{\hat{i}_o(s)=0} = \frac{G_{vOL}(s)}{1+T_{vL}(s)} \tag{3}$$

$$Z_{oL}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{\rm bus}(s)=0} = \frac{Z_{oOL}(s)}{1+T_{vL}(s)} \tag{4}$$

where $T_{vL}(s) = H_{sL}(s)G_{cL}(s)G_{ML}(s)G_{vdL}(s)$ is the loop gain of the voltage closed-loop of the original load converter.

B. Two-Port Network Model of the Load Converter With the ASVI Control Strategy

It is known that, in order to stabilize the cascaded system, the ASVI control strategy has been proposed in [23], which adding an adaptive virtual impedance $Z_{\rm ASVI}(s)$ in series with $Z_{iL}(s)$ to increase $|Z_{iL}(s)|$ and to avoid the intersection between $|Z_{oS}(s)|$ and the shaped $|Z_{iL}(s)|$. By Fig. 4(a), this $Z_{\rm ASVI}(s)$ can be realized by an impedance regulator $G_{\rm ASVI}(s)$

$$G_{\rm ASVI}(s) = Z_{\rm ASVI}(s)\cdot\frac{[1+T_{vL}(s)]\,P_o}{G_{idL}(s)G_{ML}(s)V_{\rm bus}^2} \tag{5}$$

$$Z_{\rm ASVI}(s) = \begin{cases} Z_{iL}^{AS}(s) - Z_{iL}(s) & f\in[f_1,\,f_2] \\ 0 & f\notin[f_1,\,f_2] \end{cases} \approx \frac{-2K_r\,(2\pi f_{RC})\,s}{s^2+2\,(2\pi f_{RC})\,s+(2\pi f_{CS})^2} \tag{6}$$

here, $Z_{iL}^{AS}(s)$ is the modified $Z_{iL}(s)$ by the ASVI control strategy, where $\left|Z_{iL}^{AS}(s)\right| > Z_{\rm oSP}$ during $(f_1,\,f_2)$ and $Z_{iL}^{AS}(s) = Z_{iL}(s)$ outside $(f_1,\,f_2)$. $f_{RC} = \text{Max}\left[(f_{CS}-f_1),(f_2-f_{CS})\right]$ is the bandwidth at -3 dB cutoff frequency of the $Z_{\rm ASVI}(s)$. During $(f_{CS}-f_{RC},\,f_{CS}+f_{RC})$, $|Z_{\rm ASVI}(s)|$ is equal to $\frac{K_r}{\sqrt{2}}$ and also equal to $\left|Z_{iL}^{AS}(j2\pi f_{CS}) - Z_{iL}(j2\pi f_{CS})\right|$ [23].

According to Fig. 4(a), the generic two-port small signal model of the load converter with the ASVI control strategy is presented in Fig. 4(b), where $Z_{iL}^{AS}(s)$, $G_{iL}^{AS}(s)$, $G_{vL}^{AS}(s)$, and $Z_{oL}^{AS}(s)$ are the improved $Z_{iL}(s)$, $G_{iL}(s)$, $G_{vL}(s)$, and $Z_{oL}(s)$ by the ASVI control strategy, respectively. Their expressions can be derived as follows:

$$Z_{iL}^{AS}(s) = \left.\frac{\hat{v}_{\rm bus}(s)}{\hat{i}_{\rm bus}(s)}\right|_{\hat{i}_o(s)=0} = Z_{iL}(s) + Z_{\rm ASVI}(s) \tag{7}$$

$$G_{iL}^{AS}(s) = \left.\frac{\hat{i}_{\rm bus}(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{\rm bus}(s)=0} = G_{iL}(s)\left(1-\frac{T_{iL}(s)}{1+T_{vL}(s)}\right)^{-1} \tag{8}$$

$$G_{vL}^{AS}(s) = \left.\frac{\hat{v}_o(s)}{\hat{v}_{\rm bus}(s)}\right|_{\hat{i}_o(s)=0} = \left(G_{\rm vOL}(s) + \frac{G_{\rm vdL}(s)}{Z_{iOL}(s)G_{idL}(s)}\frac{T_{iL}(s)}{1-T_{iL}(s)}\right)\cdot\left(1+\frac{T_{vL}(s)}{1-T_{iL}(s)}\right)^{-1} \tag{9}$$

$$Z_{oL}^{AS}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{\rm bus}(s)=0} = \left(Z_{oOL}(s) + \frac{G_{\rm vdL}(s)G_{iOL}(s)}{G_{idL}(s)}\frac{T_{iL}(s)}{1-T_{iL}(s)}\right)\cdot\left(1+\frac{T_{vL}(s)}{1-T_{iL}(s)}\right)^{-1} \tag{10}$$

where $T_{iL}(s) = G_{\rm ASVI}(s)G_{idL}(s)G_{ML}(s)$.

According to (7), the ASVI control strategy indeed adds $Z_{\rm ASVI}(s)$ in series with $Z_{iL}(s)$ to form the expected input impedance of the load converter $Z_{iL}^{AS}(s)$. According to (6), $\left|Z_{iL}^{AS}(s)\right|$ is larger than $|Z_{oS}(s)|$, thus, the ASVI control strategy can ensure the system stability.

However, according to (8)–(10), though the ASVI control strategy has shaped $Z_{iL}(s)$ to $Z_{iL}^{AS}(s)$ to achieve the purpose of stability, all the transfer functions of the load converter are actually changed. As shown in Fig. 4(b), all the changed transfer functions are marked by shadow areas.

C. Impact of the ASVI Control Strategy on the Load Converter

According to Sections II-A and II-B, though the ASVI control strategy can stabilize the cascaded system by shaping $Z_{iL}(s)$, it in fact changes all the transfer functions of the original load converter. In order to evaluate the impacts of ASVI control strategy on the load converter clearly, a detailed cascaded system is taken as an example to aid the analysis in this section. The main circuit and control block of this example system are depicted in

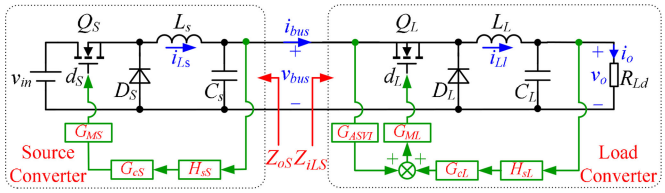


Fig. 5. Example system with the ASVI control strategy.

TABLE I
PARAMETERS OF THE EXAMPLE SYSTEM WITH THE ASVI CONTROL STRATEGY

v_{in}	48V	v_o	24V	f_{sS}	20kHz	L_S	1mH	L_L	450μH	H_{sS},H_{sL}	0.1
v_{bus}	32V	P_o	100W	f_{sL}	100kHz	C_S	150μF	C_L	220μF	G_{MS},G_{ML}	1/2.34
$G_{vS}=5+\frac{100}{s}$						$G_{vL}=3.723e^9\cdot\left(\frac{s+6.356e^3}{s+6.283e^5}\right)^2$					

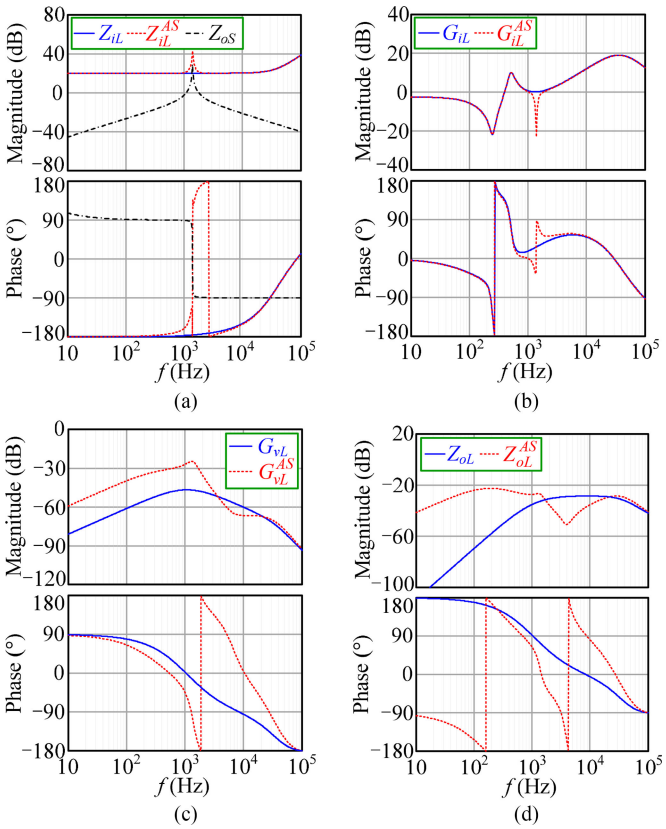


Fig. 6. Bode plots of the load converter without or with ASVI control strategy. (a) $Z_{iL}(s)$ and $Z_{iL}^{AS}(s)$. (b) $G_{iL}(s)$ and $G_{iL}^{AS}(s)$. (c) $G_{vL}(s)$ and $G_{vL}^{AS}(s)$. (d) $Z_{oL}(s)$ and $Z_{oL}^{AS}(s)$.

Fig. 5. The parameters of the example system are presented in Table I as well.

According to (1) and (7), Bode plots of $Z_{iL}(s)$ and $Z_{iL}^{AS}(s)$ of the example system are both depicted in Fig. 6(a). It is shown that, the ASVI control strategy can increase $|Z_{iL}(s)|$ during $(f_1,\ f_2)$ to ensure a total separation between $|Z_{iL}^{AS}(s)|$ and $|Z_{oS}(s)|$. Therefore, the stability of the cascaded system is guaranteed. However, it is worthy pointing out that, since the negative resistor characteristic of $Z_{iL}(s)$ is also removed by the ASVI control strategy during $(f_1,\ f_2)$ [see Fig. 6(a)], the ASVI control strategy actually has negative impact on $Z_{iL}(s)$ from the dynamic performance point of view. It is because that though the negative resistor characteristic of $Z_{iL}(s)$ is a bad news to the cascaded system stability, it is a natural guarantee of the constant power load characteristic for the load converter, which also can ensure the fast dynamic performance of the load converter. The more detailed explanations can be found in the Appendix-A.

According to (2) and (8), Bode plots of $G_{iL}(s)$ and $G_{iL}^{AS}(s)$ of the example system are both depicted in Fig. 6(b). As seen, $G_{iL}^{AS}(s)$ changes the original characteristic of the $G_{iL}(s)$ during $(f_1,\ f_2)$, but the effect is very small and can be ignored.

According to (3) and (9), Bode plots of $G_{vL}(s)$ and $G_{vL}^{AS}(s)$ of the example system are both depicted in Fig. 6(c). As seen, $|G_{vL}^{AS}(s)|$ is larger than $|G_{vL}(s)|$ at lower frequency. The expression of $G_{vL}(s)$ is as follows:

$$G_{vL}(s)\triangleq\left.\frac{\hat{v}_o(s)}{\hat{v}_{\rm bus}(s)}\right|_{\hat{i}_o(s)=0} \tag{11}$$

where $\hat{v}_o(s)$, $\hat{v}_{\rm bus}(s)$, and $\hat{i_o}(s)$ refer to the disturbance of $v_o(s)$, $v_{\rm bus}(s)$, and $i_o(s)$, respectively.

According to (11), the straightforward definition of $G_{vL}(s)$ is the ratio of $\hat{v}_o(s)$ to $\hat{v}_{\rm bus}(s)$ when $\hat{i_o}(s)=0$. According to (11), if a disturbance happened on the $v_{\rm bus}(s)$, this disturbance will transfer from $v_{\rm bus}(s)$ to $v_o(s)$ via $G_{vL}(s)$. Therefore, a larger $|G_{vL}(s)|$ means the $v_o(s)$ is sensitive and easily be affected by the $v_{\rm bus}(s)$. In other words, $|G_{vL}(s)|$ is inversely proportional to the suppression ability of v_o to the disturbance of $v_{\rm bus}$, and the larger $|G_{vL}(s)|$ the worse suppression ability of v_o to the disturbance of $v_{\rm bus}$. According to Fig. 6(c), since the ASVI control strategy increases $|G_{vL}(s)|$ at lower frequency, the ASVI control strategy has negative impacts on $G_{vL}(s)$.

According to (4) and (10), Bode plots of $Z_{oL}(s)$ and $Z_{oL}^{AS}(s)$ of the example system are both depicted in Fig. 6(d). Similar with $|G_{vL}^{AS}(s)|$, $|Z_{oL}^{AS}(s)|$ is larger than $|Z_{oL}(s)|$ at lower frequency. Since a higher $|Z_{oL}(s)|$ also means a worse dynamic response from v_o to i_o, the ASVI control strategy has negative impacts on $Z_{oL}(s)$. More discussions about the negative impact of the ASVI control on the $Z_{oL}(s)$ can be found in In Appendix-B.

It is worthy mentioning that, both $|G_{vL}^{AS}(s)|$ and $|Z_{oL}^{AS}(s)|$ should be only larger than $|G_{vL}(s)|$ and $|Z_{oL}(s)|$ during $(f_1,\ f_2)$ according to the theory of the ASVI control strategy [23]. However, in practice, $|G_{vL}^{AS}(s)|$ and $|Z_{oL}^{AS}(s)|$ may larger than $|G_{vL}(s)|$ and $|Z_{oL}(s)|$ outside of $(f_1,\ f_2)$ as well. It can be explained as follow: though the input impedance regulator of the ASVI control strategy $G_{\rm ASVI}(s)$ is suggested to be zero outside of $(f_1,\ f_2)$, it is actually realized by a nonidea resonant controller whose magnitude is very close but not equal to zero outside of $(f_1,\ f_2)$. Therefore, $G_{\rm ASVI}(s)$ cannot totally remove its impact on the load converter outside of $(f_1,\ f_2)$. As a result, if the magnitude of the original $G_{vL}(s)$ and $Z_{oL}(s)$ is already very small outside of $(f_1,\ f_2)$, their magnitude may be increased outside of $(f_1,\ f_2)$ by the ASVI control strategy.

In summary, though the ASVI control strategy can stabilize the cascaded system by shaping $Z_{iL}(s)$, it affects all the

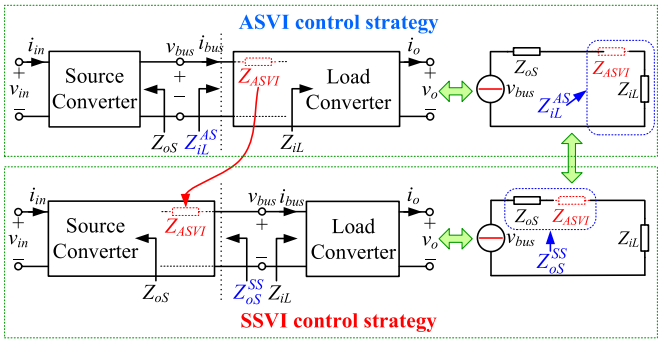


Fig. 7. Concept of the SSVI control strategy.

transfer functions and may deteriorate the characteristics of $Z_{iL}(s)$, $G_{vL}(s)$, and $Z_{oL}(s)$. This is the limitation of the ASVI control strategy.

III. Proposed SSVI Control Strategy

A. Concept of the SSVI Control Strategy

As shown in Fig. 7, the ASVI control strategy adds $Z_{\rm ASVI}(s)$ in series with $Z_{iL}(s)$ to form the final load input impedance $Z_{iL}^{AS}(s)$ and ensures $\left|Z_{iL}^{AS}(s)\right|$ always larger than $|Z_{oS}(s)|$ to stabilize the cascaded system. However, as discussed above, the ASVI control strategy deteriorates the performance of the load converter. In order to solve this problem, the $Z_{\rm ASVI}(s)$ is moved from the load side to the source side by changing the control block of the source converter instead of the load converter. To distinguish it from the ASVI control strategy, this proposed solution is called as SSVI control strategy.

As depicted in Fig. 7, since $Z_{\rm ASVI}(s)$ is in a series with $Z_{iL}(s)$ and $Z_{oS}(s)$ simultaneously, the SSVI control strategy has the same stabilization function and adaptive characteristics as the ASVI control strategy. The only difference between the SSVI and ASVI control strategies is in their physical concepts: the ASVI control strategy keeps a total separation between $|Z_{oS}(s)|$ and $|Z_{iL}(s)|$ by increasing $|Z_{iL}(s)|$, but the SSVI control strategy realizes this separation by decreasing $|Z_{oS}(s)|$. However, in later sections, it will be shown that, just this small difference helps the SSVI control strategy to overcome the drawback of the ASVI control strategy, i.e., not deteriorating but in fact improving the performance of the source converter without bringing any impact to the load converter when stabilizing the cascaded system.

The small signal control block of the original source converter has been presented in Fig. 8(a). $v_{\rm in}$ and $i_{\rm in}$ are the input voltage and current of the source converter, respectively. d_S is the duty cycle of the source converter. $Z_{iOS}(s) \sim G_{MS}(s)$ have the same definitions with $Z_{iOL}(s) \sim G_{ML}(s)$ in Fig. 3(a), where the only difference is the subscript S represents the source converter, but the subscript L represents the load converter. As with the dotted line in Fig. 8(a), the intuitive way to add $Z_{\rm ASVI}(s)$ in series with $Z_{oS}(s)$ is introducing $Z_{\rm ASVI}(s)$ between $\hat{i}_{\rm bus}$ and $-\hat{v}_{\rm bus}$ directly. However, this method cannot be achieved by control directly. In order to address this issue, the output of $Z_{\rm ASVI}(s)$ is moved to the output of $G_{cS}(s)$ and equivalent

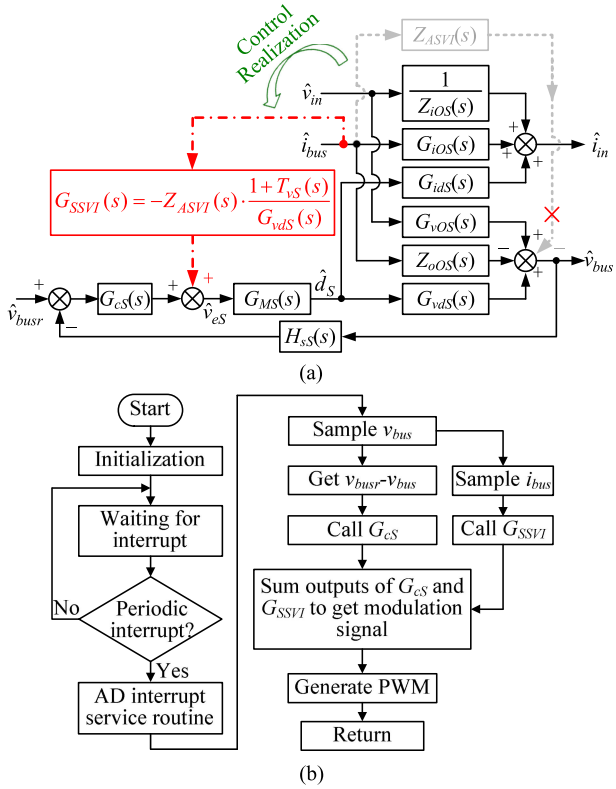


Fig. 8. Proposed SSVI control strategy and its algorithm. (a) Control block. (b) Algorithm.

adjusts the transfer function to $G_{\rm SSVI}(s)$, as shown with the dot-dashed lines.

According to Fig. 8(a), if $G_{\rm SSVI}(s)$ is required to realize $Z_{\rm ASVI}(s)$, the following relationship is in force:

$$-\hat{i}_{\rm bus}Z_{\rm ASVI}(s) = \hat{i}_{\rm bus}G_{\rm SSVI}(s)G_{MS}(s)G_{vdS}(s)\frac{1}{1+T_{vS}(s)} \tag{12}$$

where $T_{vS}(s) = H_{sS}(s)G_{cS}(s)G_{MS}(s)G_{vdS}(s)$ is the loop gain of the voltage closed-loop of the original source converter.

According to (12), the expression of $G_{\rm SSVI}(s)$ can be derived as follows:

$$G_{\rm SSVI}(s) = -Z_{\rm ASVI}(s)\cdot\frac{1+T_{vS}(s)}{G_{vdS}(s)G_{MS}(s)}. \tag{13}$$

Up to this point, Fig. 8(a) presents the fully controlled block of the proposed SSVI control strategy.

The proposed SSVI control strategy can be implemented by the digital signal processor (DSP) TMS320F28335. The mechanism for this is presented in Fig. 8(b), with both $v_{\rm bus}$ and $i_{\rm bus}$ sampled to provide the necessary information for the SSVI control strategy and the output voltage regulation. The algorithm obtains the modulation signal by adding the output of $G_{\rm SSVI}(s)$ to the output of $G_{cS}(s)$, and then generates d_S by pulsewidth modulation module.

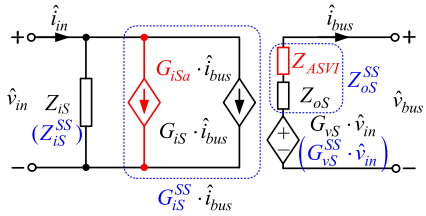


Fig. 9. Two-port network model of the source converter with the SSVI control strategy.

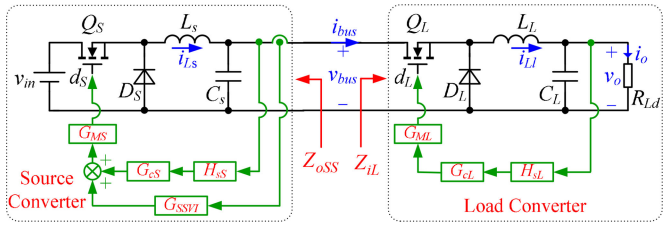


Fig. 10. Example system with SSVI control strategy.

B. Impact of the SSVI Control Strategy on the Source Converter via Two-Port Network Analysis

According to Fig. 8(a), the generic two-port small signal model of the source converter with the SSVI control strategy has been presented in Fig. 9. $Z_{iS}(s)$ is the closed-loop input impedance of the source converter; $G_{iS}(s)$ is the closed loop load to input current transfer function of the source converter; $G_{vS}(s)$ is the closed loop input to output voltage transfer function of the source converter; $Z_{oS}(s)$ is the closed-loop output impedance of the source converter. $Z_{iS}^{SS}(s)$, $G_{iS}^{SS}(s)$, $G_{vS}^{SS}(s)$, and $Z_{oS}^{SS}(s)$ are the improved $Z_{iS}(s)$, $G_{iS}(s)$, $G_{vS}(s)$, and $Z_{oS}(s)$ by the SSVI control strategy, respectively. Their expressions can be derived as follows:

$$Z_{iS}^{SS}(s)=\left.\frac{\hat{v}_{\rm in}(s)}{\hat{i}_{\rm in}(s)}\right|_{\hat{i}_{\rm bus}(s)=0}=Z_{iS}(s)$$
$$=\frac{[1+T_{vS}(s)]Z_{iOS}(s)G_{vdS}(s)}{G_{vdS}(s)-T_{vS}(s)[G_{vdS}(s)-Z_{iOS}(s)G_{idS}(s)G_{vOS}(s)]} \quad (14)$$

$$G_{iS}^{SS}(s)=\left.\frac{\hat{i}_{\rm in}(s)}{\hat{i}_{\rm bus}(s)}\right|_{\hat{v}_{\rm in}(s)=0}=G_{iS}(s)+G_{iSa}(s)$$
$$=\left[G_{iOS}(s)-\frac{Z_{oOS}(s)G_{idS}(s)}{G_{vdS}(s)}\frac{T_{vS}(s)}{1+T_{vS}(s)}\right]+\frac{T_{iS}(s)}{1+T_{vS}(s)} \quad (15)$$

$$G_{vS}^{SS}(s)=\left.\frac{\hat{v}_{\rm bus}(s)}{\hat{v}_{\rm in}(s)}\right|_{\hat{i}_{\rm bus}(s)=0}=G_{vS}(s)=\frac{G_{vOS}(s)}{1+T_{vS}(s)} \quad (16)$$

$$Z_{oS}^{SS}(s)=-\left.\frac{\hat{v}_{\rm bus}(s)}{\hat{i}_{\rm bus}(s)}\right|_{\hat{v}_{\rm in}(s)=0}=Z_{oS}(s)+Z_{\rm ASVI}(s)$$
$$=\left[\frac{Z_{oOS}(s)}{1+T_{vS}(s)}\right]+Z_{\rm ASVI}(s) \quad (17)$$

where $T_{iS}(s)=G_{\rm SSVI}(s)G_{idS}(s)G_{MS}(s)$.

According to (17), the SSVI control strategy adds $Z_{\rm ASVI}(s)$ in series with $Z_{oS}(s)$ to form the final output impedance of the source converter $Z_{oS}^{SS}(s)$. According to Fig. 7, the SSVI control strategy realizes the same stabilization function with the ASVI control strategy, thus, the SSVI control strategy can guarantee the stability of the cascaded system. According to (14) and (16), the SSVI control strategy keeps the original characteristic of $Z_{iS}(s)$ and $G_{vS}(s)$. According to (15), the SSVI control strategy changes the original characteristic of $G_{iS}(s)$. In Fig. 9, the changed transfer functions are also marked by dash borders.

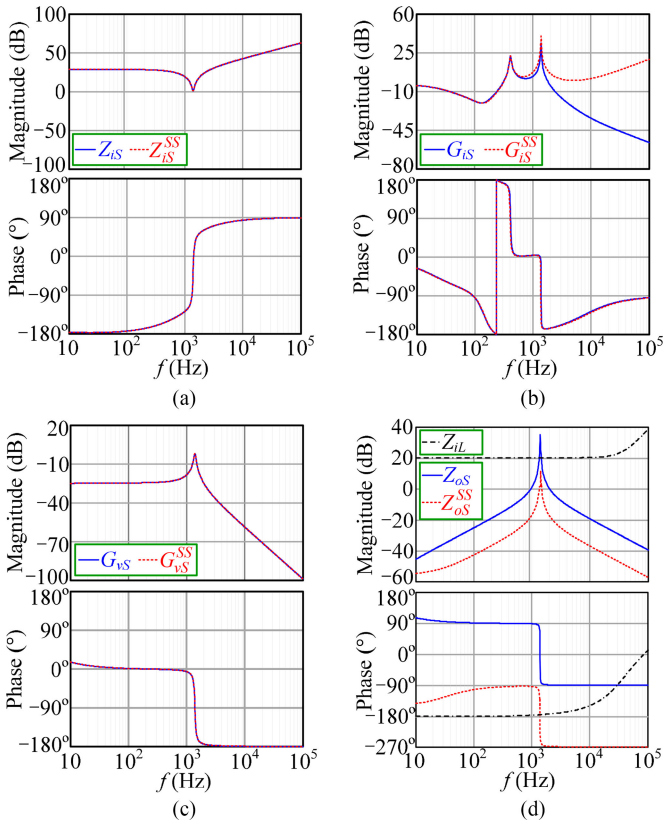


Fig. 11. Bode plots of the source converter without or with SSVI control strategy. (a) $Z_{iS}(s)$ and $Z_{iS}^{SS}(s)$. (b) $G_{iS}(s)$ and $G_{iS}^{SS}(s)$. (c) $G_{vS}(s)$ and $G_{vS}^{SS}(s)$. (d) $Z_{oS}(s)$ and $Z_{oS}^{SS}(s)$.

As with the ASVI control strategy, in order to evaluate the impact of the SSVI control strategy on the source converter clearly, the same detailed cascaded system is utilized to aid the analysis in this section. The only difference is that this example system utilizes the SSVI control strategy instead of the ASVI control strategy. The main circuit and control block of the example system with the SSVI control strategy are depicted in Fig. 10. The parameters of this example system can be found in Table I.

According to (14) and (16), Bode plots of $Z_{iS}(s)$ and $Z_{iS}^{SS}(s)$ and $G_{vS}(s)$ and $G_{vS}^{SS}(s)$ of the example system are depicted in Fig. 11(a) and (c), respectively. It can be observed that the

SSVI control strategy does not make any changes to $Z_{iS}(s)$ and $G_{vS}(s)$.

According to (15), Bode plots of $G_{iS}(s)$ and $G_{iS}^{SS}(s)$ of the example system can be plotted and presented in Fig. 11(b). The SSVI control strategy increases the amplitude of $G_{iS}(s)$ at a higher frequency. The expression of $G_{iS}(s)$ is as follows:

$$G_{iS}(s) \triangleq \left.\frac{\hat{i}_{\rm in}(s)}{\hat{i}_{\rm bus}(s)}\right|_{\hat{v}_{\rm in}(s)=0} \tag{18}$$

where $\hat{i}_{\rm in}(s)$, $\hat{i}_{\rm bus}(s)$, and $\hat{v}_{\rm in}(s)$ refer to the disturbance of $i_{\rm in}(s)$, $i_{\rm bus}(s)$, and $v_{\rm in}(s)$, respectively.

According to (18), the straightforward definition of $G_{iS}(s)$ is the ratio of $\hat{i}_{\rm in}(s)$ to $\hat{i}_{\rm bus}(s)$ when $\hat{v_{\rm in}}(s) = 0$. According to (18), if a disturbance happened on the $i_{\rm bus}(s)$, this disturbance will transfer from $i_{\rm bus}(s)$ to $i_{\rm in}(s)$ via $G_{iS}(s)$. Therefore, a larger $|G_{iS}(s)|$ means the $i_{\rm in}(s)$ is sensitive and easily be affected by the $i_{\rm bus}(s)$. In other words, $|G_{iS}(s)|$ is inversely proportional to the suppression ability of $i_{\rm in}$ to the disturbance of $i_{\rm bus}$, and the larger $|G_{iS}(s)|$ the worse suppression ability of $i_{\rm in}$ to the disturbance of $i_{\rm bus}$. Therefore, according to Fig. 11(b), the SSVI control strategy has a negative impact on $G_{iS}(s)$. However, it is worth mentioning that, since the SSVI control strategy only increases $|G_{iS}(s)|$ on the high frequency range, this impact is very small in practice.

According to (17), Bode plots of $Z_{oS}(s)$ and $Z_{oS}^{SS}(s)$ of the example system are depicted in Fig. 11(d). The SSVI control strategy decreases $|Z_{oS}(s)|$ in the whole frequency range to avoid the intersection with $|Z_{iL}(s)|$. Therefore, the stability of the cascaded system is guaranteed. In addition, since $Z_{oS}(s)$ is the closed-loop output impedance of the source converter, the smaller $|Z_{oS}(s)|$ the better source dynamic performance. Hence, the SSVI control strategy also has positive impact on $Z_{oS}(s)$ from the source performance point of view.

In summary, the SSVI control strategy can stabilize the cascaded system by reducing $|Z_{oS}(s)|$. It has no impact on $Z_{iS}(s)$ and $G_{vS}(s)$, a negligible negative impact on $G_{iS}(s)$ and a positive impact on $Z_{oS}(s)$.

C. Inherent Adaptive Characteristics of the SSVI Control Strategy

It is known that, adaptive characteristics is also one of the attractive advantages of the ASVI control strategy. As shown in Fig. 12(a), this characteristics can help the load converter find f_{CS} automatically according to different source converters, where f_{CS} is the frequency of the peak output impedance of the source converter, which is an unknown information to the load converter [23]. However, though f_{CS} is unknown to the load converter, it is a known information to the source converter. Therefore, as shown in Fig. 12(b), for the SSVI control strategy, it does not need any additional control strategy to find f_{CS} adaptively, but also can use the known f_{CS} to shape the source output impedance directly. In other words, the adaptive characteristics is also an inherent characteristics of the SSVI control strategy.

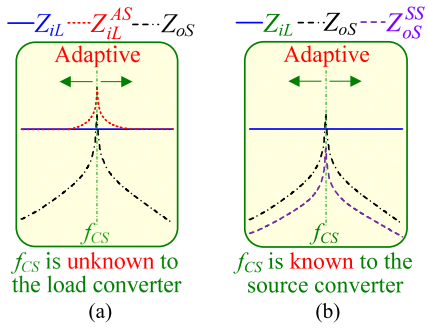


Fig. 12. Adaptive characteristics of the ASVI and SSVI control strategies. (a) ASVI control strategy. (b) SSVI control strategy.

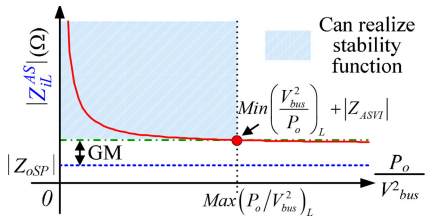


Fig. 13. Stability region of both SSVI and ASVI control strategies.

It is also worthy pointing out that, the SSVI control strategy does not need to care about the variety of the load input impedance with the changing of the load converter. It is because that, no matter how the load converter changes, its input impedance has the same negative resistor within the control bandwidth: $-\frac{v_{\rm bus}^2}{P_o}$ (As shown in Fig. 2).

D. Stability Region of the SSVI Control Strategy

According to Fig. 7, both the SSVI control and ASVI control actually adds the same additional impedance $Z_{\rm ASVI}(s)$ to the same position to stabilize the system. Therefore, both the SSVI control strategy and ASVI control strategy have the same stabilization function. Then, refer to the analysis in [23], the stability region of both SSVI and ASVI can be depicted in Fig. 13.

In Fig. 13, Z_{oSP} is the peak value of Z_{oS}; GM is the required system stability gain margin whose unit is dB; P_o is the system output power; $v_{\rm bus}$ is the system bus voltage. Max $\left(P_o/V_{\rm bus}^2\right)_L$ is equal to P_{oM}/V_{bM}^2, where P_{oM} and V_{bM} are the maximum power and the minimum input voltage of the load converter, respectively. Min $\left(V_{\rm bus}^2/P_o\right)_L = V_{bM}^2/P_{oM}$. According to Fig. 13, the stability requirement of selecting $Z_{\rm ASVI}(s)$ can be summarized as follows:

$$|Z_{\rm SVI}(j2\pi f)| > |Z_{oSP}|\,10^{\frac{GM}{20}} - \left(\frac{V_{bM}^2}{P_{oM}}\right)\ f \in [f_1,\, f_2] \tag{19}$$

where f_1 and f_2 are the intersection frequencies of the amplitude of the original source output impedance and the original load input impedance [23], respectively. Obviously, for cascaded system, during $[f_1, f_2]$, a higher $|Z_{\rm ASVI}|$ can always be found to meet the requirement of (19). In other words, no matter the SSVI control or ASVI control, they always can find suitable $Z_{\rm ASVI}(s)$ to stabilize the cascaded system.

TABLE II
COMPARISON FOR ASVI AND SSVI CONTROL STRATEGIES

	Affected converter	$Z_{i(L/S)}(s)$	$G_{i(L/S)}(s)$	$G_{v(L/S)}(s)$	$Z_{o(L/S)}(s)$
ASVI	Load converter	Negative	Little change	Negative	Negative
SSVI	Source converter	No change	Little change	No change	Postitive
	Cascaded system	Adaptive or not?	Evaluation		
ASVI	Stable	Adaptive	SSVI is better than ASVI		
SSVI	Stable	Adaptive			

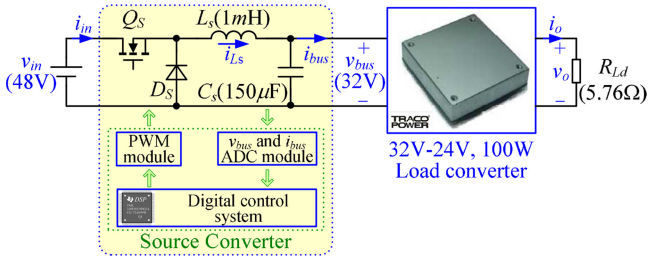


Fig. 14. Experimental system.

E. Comparison Between the ASVI and SSVI Control Strategies

By Figs. 6, 11, and 12, both the impact of the ASVI control strategy on the load converter and the impact of the SSVI control strategy on the source converter are concluded and compared in Table II. It is shown that, the SSVI control strategy not only has the same stabilization function and adaptive characteristics as the ASVI control strategy, but also has a more positive impact on the original cascaded system than the ASVI control strategy. From this point of view, the SSVI control strategy is superior to the ASVI control strategy.

However, the proposed SSVI control strategy is not perfect, it also suffers some limitations. First, it needs an additional current sensor to sensor the load current, which may increase the cost. Then, if the source converter is an input filter instead of a real power converter, the SSVI control method cannot be employed due to no duty cycle to be regulated. Therefore, the proposed SSVI is more suitable for the application whose source stage is source converter instead of input filter. It is worthy to explain that since the SSVI control method is a "control" method, it cannot do any action on the passive input filer. It is the common limitation for all the control-oriented stabilization methods. So, if we met a unstable cascaded system whose source stage is a passive input filter, we recommend the engineer to use passive damping method to shape the output impedance of the input filter [15] or use our previous proposed ASVI control method [23] to sharp the input impedance of the load converter.

IV. EXPERIMENTAL RESULTS

A. Experimental Verification of the Proposed SSVI Control Strategy

In this section, the example cascaded system presented in Fig. 14 is fabricated to validate the SSVI control strategy. Its circuit, control block, parameters, and Bode plots can be found in Section III-B, and will not be repeated here. It is worthy mentioning that, as shown in Fig. 14, to make the verification more available, the source converter is controlled by DSP

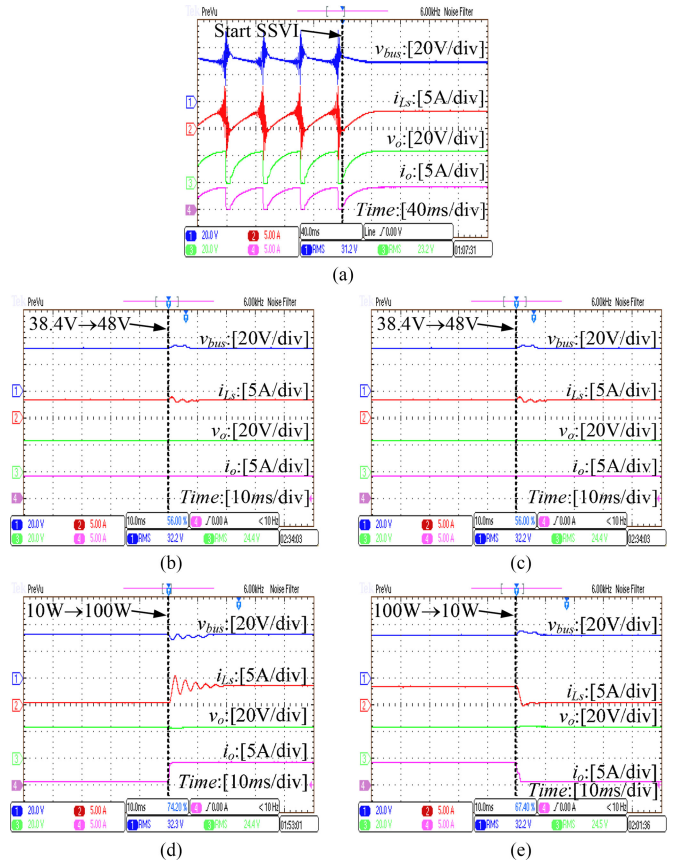


Fig. 15. Experimental waveforms of the cascaded system with the SSVI control strategy. (a) Steady-state waveforms when $V_{\rm in}$ = 48 V, P_o = 100 W. (b) Dynamic waveforms when $V_{\rm in}$: 38.4 V→ 48 V. (c) Dynamic waveforms when $V_{\rm in}$: 48 V→ 38.4 V. (e) Dynamic waveforms when P_o: 10 W→ 100 W. (f) Dynamic waveforms when P_o: 100 W→ 10 W.

TMS320F28335 to realize the SSVI control strategy, but the load converter is a special custom power module from TRACO POWER company whose control circuit is already internally integrated and can not be changed.

The experimental results of the cascaded system with the SSVI control strategy are given in Fig. 15. As shown in Fig. 15(a), this cascaded system is unstable without the SSVI control strategy. After enabling the SSVI control strategy, the cascaded system becomes stable. This phenomenon is also consistent with Bode plots in Fig. 11(d). The input voltage dynamic waveforms of the cascaded system with the SSVI control strategy at full load are presented in Fig. 15(b) and (c). In Fig. 15(b), the input voltage of the cascaded system changes from 80% rated voltage (38.4 V) to 100% rated voltage (48 V). In Fig. 15(c), the input voltage of the cascaded system changes from 48 to 38.4 V. It indicates that the SSVI control strategy can work well during any input voltage changes. The load dynamic waveforms of the cascaded system with the SSVI control strategy at rated input voltage are presented in Fig. 15(d) and (e). In Fig. 15(d), the load of the cascaded system changes from 10% full load (10 W) to 100% full load (100 W). In Fig. 15(e), the load of the cascaded system is changing from 100 to 10 W. It also indicates that the SSVI control strategy can work well during any load changes.

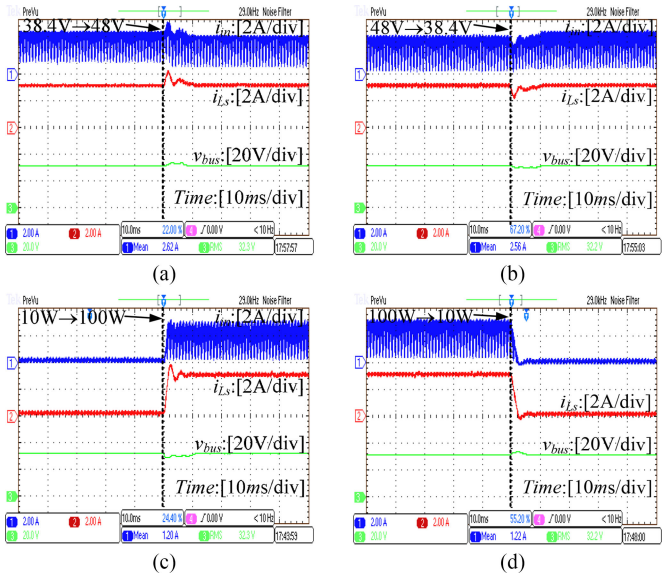


Fig. 16. Dynamic waveforms of the original source converter without the SSVI control strategy. (a) $V_{\rm in}$: 38.4–48 V. (b) $V_{\rm in}$: 48–38.4 V. (c) P_o: 10–100 W. (d) P_o: 100–10 W.

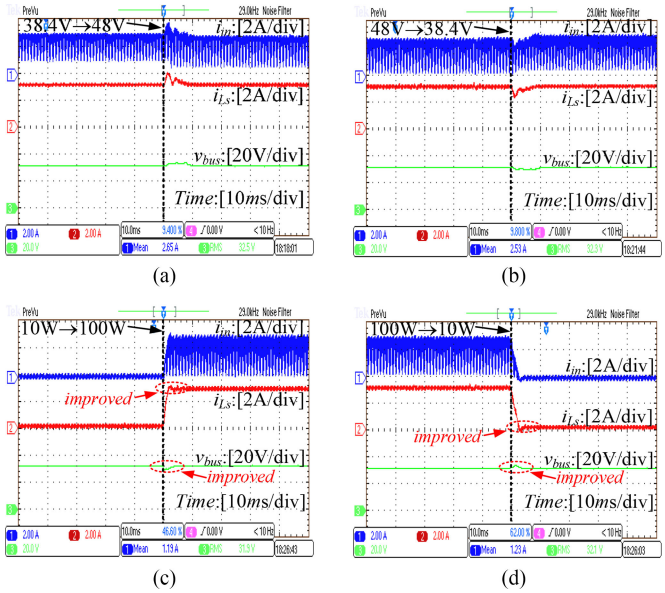


Fig. 17. Dynamic waveforms of the source converter with the SSVI control strategy. (a) $V_{\rm in}$: 38.4–48 V. (b) $V_{\rm in}$: 48–38.4 V. (c) P_o: 10–100 W. (d) P_o: 100–10 W.

The dynamic experimental waveforms of the source converter with/without the SSVI control strategy are shown and compared in Figs. 16 and 17, respectively. As seen, with the SSVI control strategy, the input voltage dynamic performance of the source converter is the same as its original performance, which verifies that the SSVI control strategy does not have any impact on $Z_{iS}(s)$ and $G_{vS}(s)$. Besides, according to Figs. 16 and 17, with the SSVI control strategy, the load dynamic performance of the source converter is better than its original performance, which verifies that the SSVI control strategy has a positive impact on $|Z_{oS}(s)|$ and a negligible impact on $G_{iS}(s)$. Therefore, the dynamic performance of the source converter becomes better with the SSVI control strategy.

It is worth to mention that since the topology, circuit parameters and control circuit of the the experimental system of this paper are different with the studied system in [21], the dynamic performance results in this paper is hence different with the results in [21] as well.

According to Fig. 15–17, the SSVI control strategy not only stabilizes the cascaded system, but also improves the performance of the source converter, as well as does not bring any impact to the load converter.

TABLE III
MAIN CIRCUIT PARAMETERS OF THE HIL SYSTEM

V_{in}	V_{bus}	V_o	P_o	f_{sS}
$48V$	$32V$	$24V$	$100W$	$20kHz$
f_{sL}	L_{fS}	C_{fS}	L_{fL}	C_{fL}
$20kHz$	$5mH$	$2200\mu F$	$2mH$	$470\mu F$

B. Experimental Comparison of the Proposed SSVI Control Strategy and the ASVI Control Strategy

In the above part, the load converter bought a real power module from the TRACO POWER company to test the actual effectiveness of the proposed SSVI control strategy. However, since its internal control structure cannot be changed due to the module package, the SSVI control method can not be compared with the ASVI control method on the same system. Therefore, in this part, another hardware-in-the-loop (HIL) experimental system has been built and both the ASVI and SSVI control methods have been compared. The parameters of the experimental system are given at Table III. Figs. 19–22 show the experimental results.

The picture of the HIL system is shown in Fig. 18(a). The schematic diagram of the HIL system is also presented in Fig. 18(b). As seen, the HIL system can be divided into two parts: main circuit part and control part. The main circuit part is realized by the real-time simulator OP5600 whose time step is 20 μs. The control part is realized by the hardware controller dSPACE 1202 (Microlab Box), whose sampling rate is 20 kHz. The main circuit part sends the information of $i_{\rm bus}$, $v_{\rm bus}$, and v_o to the control part. The control part sends the duty cycle information d_S and d_L to the main circuit part. Finally, the OP5600 sends the test waveforms to the oscilloscope. It is worthy to mention that, compared to the regular time-domain simulation, the HIL system contains the following different things, first, the control parts are realize by real hardware controller–dSPACE 1202 (Microlab Box) and, second, the main circuit part is realized by real-time simulator OP5600, which can closely mimic the actions of the real power plant part.

Fig. 19 shows the dynamic waveforms of the SSVI-control-based system when the load is changing between 10 and 100 W. Fig. 20 shows the dynamic waveforms of the ASVI-

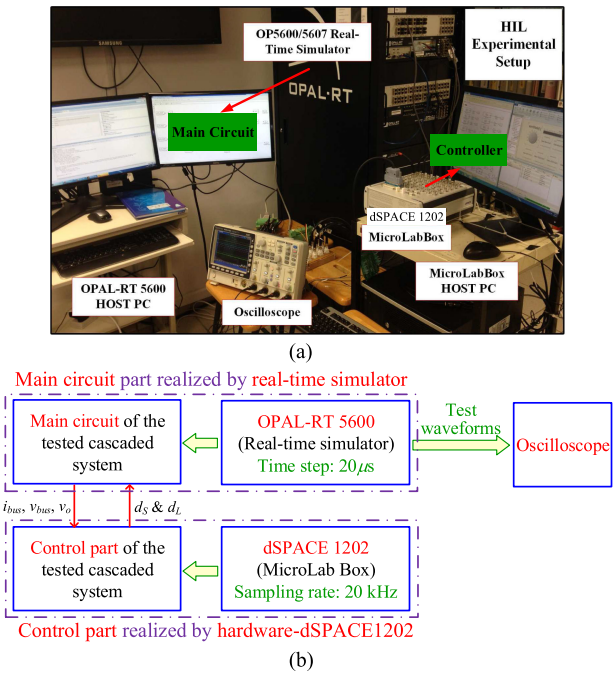


Fig. 18. Hardware-in-the loop system. (a) Picture of the HIL system. (b) Schematic diagram of the HIL system.

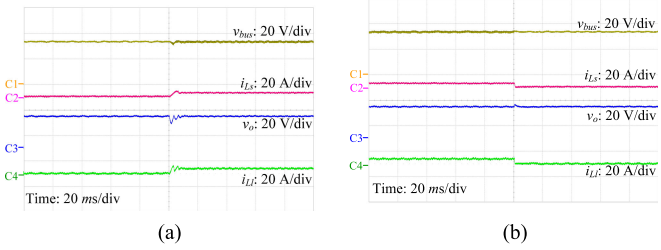


Fig. 19. Dynamic waveforms of the SSVI-control-based system when the load is changing between 10 and 100 W. (a) From 10 to 100 W. (b) From 100 to 10 W.

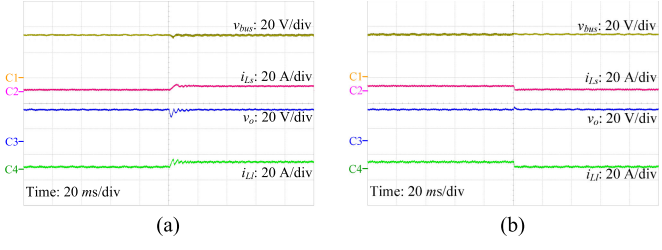


Fig. 20. Dynamic waveforms of the ASVI-control-based system when the load is changing between 10 and 100 W. (a) From 10 to 100 W. (b) From 100 to 10 W.

control-based system when the load is changing between 10 and 100 W. Fig. 21 shows the dynamic waveforms of the SSVI-control-based system when the input voltage is changing between 38.4 and 48 V. Fig. 22 shows the dynamic waveforms of the ASVI-control-based system when the input voltage is changing between 38.4 and 48 V. It can be seen that, the SSVI-control-based system indeed has better dynamic performance than the ASVI-control-based system.

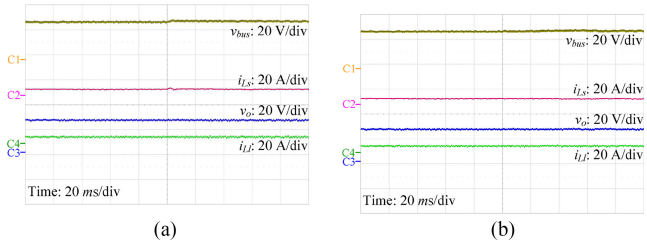


Fig. 21. Dynamic waveforms of the SSVI-control-based system when the input voltage is changing between 38.4 and 48 V. (a) From 38.4 to 48 V. (b) From 48 to 38.4 V.

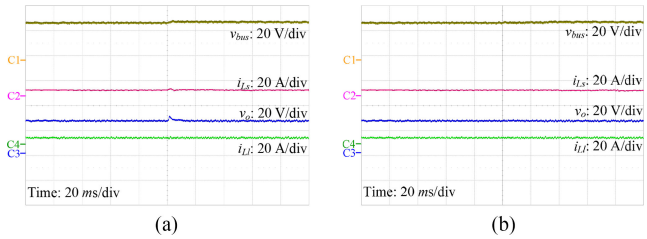


Fig. 22. Dynamic waveforms of the ASVI-control-based system when the input voltage is changing between 38.4 and 48 V. (a) From 38.4 to 48 V. (b) From 48 to 38.4 V.

V. Conclusion

The ASVI control strategy is further investigated in this paper. It is understood that though the ASVI control strategy can stabilize the cascaded system and limit its impact on the load converter in a specific frequency range, it brings negative impacts to the load converter. In order to solve this problem, the SSVI control strategy is proposed. The SSVI control strategy moves the ASVI from the load side to the source side by changing the control block of the source converter instead of the load converter. As a result, the SSVI control strategy not only has the same stabilization function and adaptive characterises as the ASVI control strategy, but also improves the performance of the source converter. In addition, since the SSVI control strategy is realized by changing the control block of the source converter, the performance of the load converter is not affected. Therefore, the SSVI control strategy is an improvement on the ASVI control strategy. Moreover, the SSVI control strategy also can be treated as a source stabilization methods of the cascaded system. Finally, the proposed SSVI strategy has been experimentally verified on a 100 W, 48 V–32 V–24 V cascaded system.

For the future work, how to apply the proposed SSVI control strategy from the typical cascaded system application to the dc-bus-based multiple converters system application will be studied. In this case, the big challenge is that any centralized or distributed converter configuration for supplying this dc bus cannot include any virtual series impedance adapted for one specific load since this could interfere with the operation of other loads or sources connected to the same bus. Our future aim is to solve the above-mentioned challenge.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for their insightful and interesting comments, which have helped the authors significantly improve the quality of this paper.

APPENDIX A
NEGATIVE IMPACT OF THE ASVI CONTROL ON THE INPUT IMPEDANCE OF THE LOAD CONVERTER

First of all, the negative resistor characteristics of the load input impedance $Z_{iL}(s)$ is explained as follows.

If a dc/dc converter controls its output voltage (V_o) and designs its closed loop very well, its output voltage will be always equal to its reference voltage. In other words, if the load resistor (R_{load}) of this dc/dc converter is constant, then its output power (P_o) is constant ($P_o = V_o^2/R_{\text{Load}}$). This is why closed-loop controlled dc/dc converter also be called as constant power load. In addition, when we design the dc/dc converter, usually assume or try to make its output power is equal to its input power to achieve high efficiency, i.e.,

$$P_o = P_{\text{in}} = V_{\text{in}} I_{\text{in}} \tag{20}$$

where V_{in} and I_{in} are the input voltage and current of the dc/dc converter.

If the disturbances are added on the (20), it can be derived that

$$P_o + \hat{p_o} = (V_{\text{in}} + \hat{v_{\text{in}}}) \left(I_{\text{in}} + \hat{i_{\text{in}}} \right). \tag{21}$$

Since the dc/dc converter is a constant power load, then it can be obtained

$$\hat{p_o} = 0. \tag{22}$$

Substituting (22) to (21) and ignore the second-order disturbance, it can be obtained that

$$P_o = V_{\text{in}} I_{\text{in}} + V_{\text{in}} \hat{i_{\text{in}}} + \hat{v_{\text{in}}} I_{\text{in}}. \tag{23}$$

Substituting (20) to (23), it can be obtained that

$$Z_{iL} \triangleq \frac{\hat{v_{\text{in}}}}{\hat{i_{\text{in}}}} = -\frac{V_{\text{in}}^2}{P_o}. \tag{24}$$

According to (20)–(24), it can be seen that if a dc/dc converter has a good output voltage closed loop, its input impedance is a negative resistor whose value is equal to the value in (24). Therefore, the negative resistor is a natural guarantee of the constant power load characteristics of the load converter, which also means fast dynamic performance. In other words, thought the negative resistor characteristics is not a good new for the cascaded system stability, it is beneficial to the dynamic performance of the load converter.

Hence, since ASVI control makes the input impedance of the converter become positive resistor during f_1 and f_2, it actually brings negative impact on the output voltage closed loop. In order to show this negative impact in a straightforward way, Figs. 23 and 24 show the time domain simulation results of the load converter without/with the ASVI control method in Table I when its input voltage is changing between 25.6 V (32 V × 0.8) to 38.4 V (32 V × 1.2). It can be seen that, the ASVI

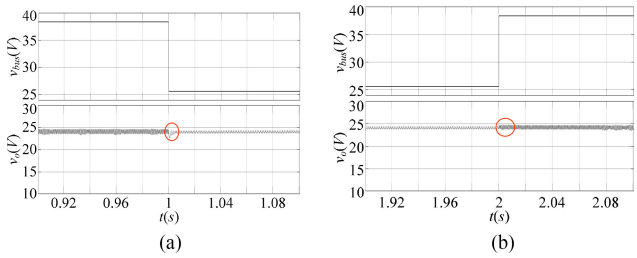


Fig. 23. Dynamic time domain simulation waveforms of the load converter without ASVI control when its input voltage is changing between 25.6 and 38.4 V. (a) From 38.4 to 25.6 V. (b) From 25.6 to 38.4 V.

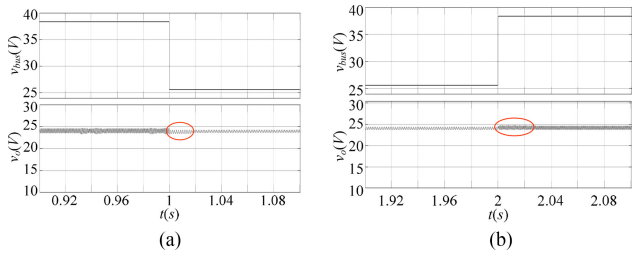


Fig. 24. Dynamic time domain simulation waveforms of the load converter with ASVI control when its input voltage is changing between 25.6 and 38.4 V. (a) From 38.4 to 25.6 V. (b) From 25.6 to 38.4 V.

control strategy brings longer setting-time to the load converter and reduces its dynamic response speed when the input voltage is changing. In addition, it also can be seen that, the ASVI control strategy reduces the overshoot of the load converter when the input voltage is changing. The above phenomenon can be explained in conjunction with the input impedance Bode plot of the load converter as shown in Fig. 6(a). According to Fig. 6(a), the ASVI control brings two impacts to the input impedance of the load converter, first, reduce the bandwidth and, second, make the input impedance characteristics change from negative resistor to positive resistor within a certain frequency range. So, reduce bandwidth means slower dynamic response speed and positive resistor means increased system damping and smaller overshoot.

APPENDIX B
NEGATIVE IMPACT OF THE ASVI CONTROL ON THE OUTPUT IMPEDANCE OF THE LOAD CONVERTER

According to the definition of output impedance, the expression of $Z_{oL}(s)$ can be expressed as

$$Z_{oL} \triangleq \hat{v_o}/\hat{i_o}. \tag{25}$$

By (25), it can be obtained that

$$\hat{v_o} = Z_{oL} \cdot \hat{i_o}. \tag{26}$$

According to (26), it can be seen that, if a disturbance happened on the load, the corresponding disturbance will occur on the output voltage through the output impedance. In other words, if the amplitude of the output impedance is larger, the disturbance transfer from the load to the output voltage will be bigger, otherwise, the disturbance will be smaller. Therefore,

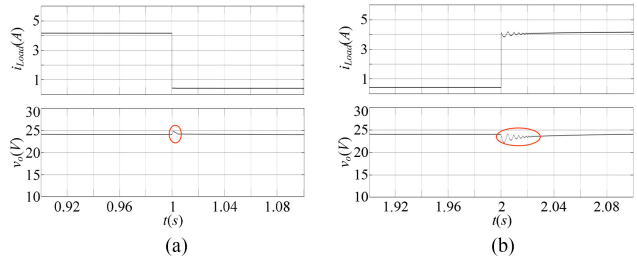


Fig. 25. Dynamic time domain simulation waveforms of the load converter without ASVI control when its load is changing between 10 and 100 W. (a) From 100 to 10 W. (b) From 10 to 100 W.

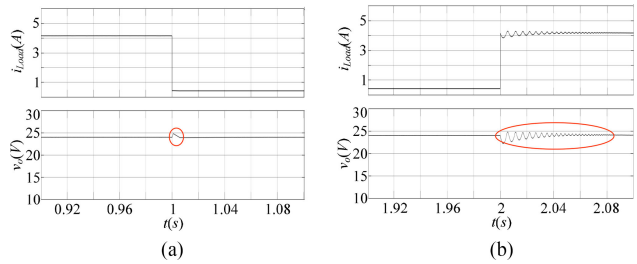


Fig. 26. Dynamic time domain simulation waveforms of the load converter with ASVI control when its load is changing between 10 and 100 W. (a) From 100 to 10 W. (b) From 10 to 100 W.

the following conclusion can be obtained: "higher $|Z_{oL}(s)|$ also means a worse dynamic response from v_o to i_o."

Since the ASVI control method increases the amplitude of the output impedance of the load converter, it actually makes the output voltage of the load converter is more sensitive to the load changing, which is a negative impact according to the above analysis. In order to show this negative impact in a straightforward way, Figs. 25 and 26 show the time domain simulation results of the load converter without/with the ASVI control method in Table I when its load is changing between 10 to 100 W. It can be seen that, the ASVI control worse the dynamic performance of the load converter when its load is changing. The above phenomenon can be explained in conjunction with the input impedance Bode plot of the load converter as shown in Fig. 6(d). According to Fig. 6(d), the ASVI control strategy totally increased the amplitude of the output impedance of the load converter at the low frequency range. Since the load converter is a dc/dc converter whose output voltage is a dc value (0 Hz), the low frequency characteristic of the load output impedance actually determines the main performance. Thus, as shown in Figs. 25 and 26, the ASVI give a poorer dynamic response on both setting time and overshoot when the system is exposed to a load step.

REFERENCES

[1] R. Turner, S. Walton, and R. Duke, "Stability and bandwidth implications of digitally controlled grid-connected parallel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3685–3694, Nov. 2010.

[2] R. Haroun, A. Cid-Pastor, A. El Aroudi, and L. Martinez-Salamero, "Synthesis of canonical elements for power processing in dc distribution systems using cascaded converters and sliding-mode control," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1366–1381, Mar. 2014.

[3] S. y. Lu, L. Wang, T. M. Lo, and A. V. Prokhorov, "Integration of wind power and wave power generation systems using a dc microgrid," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 2753–2761, Jul. 2015.

[4] C. H. Rivetta, A. Emadi, G. A. Williamson, R. Jayabalan, and B. Fahimi, "Analysis and control of a buck dc–dc converter operating with constant power load in sea and undersea vehicles," *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 559–572, Mar. 2006.

[5] W. Du, J. Zhang, Y. Zhang, and Z. Qian, "Stability criterion for cascaded system with constant power load," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1843–1851, Apr. 2013.

[6] N. Mukherjee and D. Strickland, "Control of cascaded dc–dc converter-based hybrid battery energy storage systems—Part I: Stability issue," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2340–2349, Apr. 2016.

[7] Y. Zhao, W. Qiao, and D. Ha, "A sliding-mode duty-ratio controller for dc/dc buck converters with constant power loads," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1448–1458, Mar. 2014.

[8] M. Amin and M. Molinas, "Small signal stability assessment of power electronics based power systems: A discussion of impedance and eigenvalue based methods," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 5014–5030, Sep. 2017.

[9] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," in *Proc. IEEE Conf. Rec. Annu. Meet. Ind. Appl. Soc.*, May 1979, pp. 366–382.

[10] X. Wang, R. Yao, and F. Rao, "Subsystem-interaction restraint in the two-stage dc distributed power systems with decoupling-controlled-integration structure," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1555–1563, Dec. 2005.

[11] L. Wang, Q. S. Vo, and A. V. Prokhorov, "Stability improvement of a multimachine power system connected with a large-scale hybrid wind-photovoltaic farm using a supercapacitor," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 50–60, Sep. 2017.

[12] L. Herrera, E. Inoa, F. Guo, J. Wang, and H. Tang, "Small-signal modeling and networked control of a PHEV charging facility," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1121–1130, Mar. 2014.

[13] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for dc power distribution systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3525–3535, Sep. 2014.

[14] A. Aldhaheri and A. H. Etemadi, "Stabilization and performance preservation of dc–dc cascaded systems by diminishing output impedance magnitude," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1481–1489, Oct. 2017.

[15] M. Cespedes, L. Xing, and J. Sun, "Constant-power load system stabilization by passive damping," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1832–1836, Jul. 2011.

[16] X. Zhang, X. Ruan, H. Kim, and C. K. Tse, "Adaptive active capacitor converter for improving stability of cascaded dc power supply system," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1807–1816, Apr. 2013.

[17] A. Khaligh, A. Rahimi, and A. Emadi, "Modified pulse-adjustment technique to control dc/dc converters driving variable constant-power loads," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1133–1146, Mar. 2008.

[18] X. Liu, A. Forsyth, and A. Cross, "Negative input-resistance compensator for a constant power load," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3188–3196, Dec. 2007.

[19] X. Zhang, D. Vilathgamuwa, K.-J. Tseng, B. Bhangu, and C. Gajanayake, "Power buffer with model predictive control for stability of vehicular power systems with constant power loads," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5804–5812, Dec. 2013.

[20] A. Rahimi and A. Emadi, "Active damping in dc/dc power electronic converters: A novel method to overcome the problems of constant power loads," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1428–1439, May 2009.

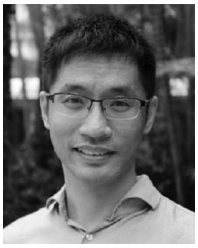
[21] X. Zhang, X. Ruan, and Q.-C. Zhong, "Improving the stability of cascaded systems via shaping the input impedance of the load converter with a parallel or series virtual impedance," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7499–7512, Dec. 2015.

[22] X. Zhang, Q.-C. Zhong, and W. Ming, "Stabilization of a cascaded dc converter system via adding a virtual adaptive parallel impedance to the input of the load converter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1826–1832, Mar. 2016.

[23] X. Zhang and Q.-C.Zhong, and W. Ming, "Stabilization of cascaded dc/dc converters via adaptive series-virtual-impedance control of the load converter," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6057–6063, Sep. 2016.

[24] X. Zhang and Q. C. Zhong, "Improved adaptive-series-virtual-impedance control incorporating minimum ripple point tracking for load converters in dc systems," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8088–8095, Dec. 2016.

[25] L. Arnedo, "System level black-box models for dc–dc converters," Ph.D. dissertation, Virginia Polytech. Inst. State Univ., Blacksburg, VA, Sep. 2008.



Xin Zhang (M'15) received the Ph.D. degree in automatic control and systems engineering from the University of Sheffield, Sheffield, U.K., in 2016 and the second Ph.D. degree in electronic and electrical engineering from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2014.

He is currently an Assistant Professor of power engineering at the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. He was the Postdoctoral Research Fellow (January 2017–September 2017) with the City University of Hong Kong and the Research Associate (February 2014–December 2016) with the University of Sheffield. His research interests include power electronics, power system, and advanced control theory, together with their applications in various sectors.

Dr. Zhang was the recipient of the highly-prestigious Chinese National Award for Outstanding Students Abroad in 2016.

Qing-Chang Zhong (M'04–SM'04–F'17) received the Ph.D. degree in control and power engineering from the Imperial College London, London, U.K., in 2004, and the second Ph.D. degree in control theory and engineering from Shanghai Jiao Tong University, Shanghai, China, in 2000.

He is the Max McGraw Endowed Chair Professor in energy and power engineering with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL, USA, and the Founding Director of Syndem LLC, Chicago, IL, USA.

Dr. Zhong is a Distinguished Lecturer of IEEE Power Electronics, Control Systems, and Power and Energy Societies, and the Vice-Chair of IFAC TC Power and Energy Systems. He was a Senior Research Fellow of Royal Academy of Engineering, U.K., and the U.K. Representative to European Control Association. He serves/d as an Associate Editor for IEEE TRANSACTIONS ON AUTOMATIC CONTROL/IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS/IEEE TRANSACTIONS ON POWER ELECTRONICS/IEEE TRANSACTIONS ON CONTROL SYSTEMS AND TECHNOLOGY/IEEE ACCESS/IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He proposed to continue adopting the synchronization mechanism of synchronous machines to unify the integration of non-synchronous distributed generators and flexible loads to achieve autonomous operation of power systems. He is a Fellow of IET.

Visakan Kadirkamanathan received the B.A. and Ph.D. degrees in electrical and information sciences from Cambridge University Engineering Department, Cambridge, U.K.

Following brief Postdoctoral Research positions with the Universities of Surrey and Cambridge, he was appointed as a Lecturer with the Department of Automatic Control and Systems Engineering, University of Sheffield. He is currently a Professor in signal and information processing and is also the Director of the Rolls-Royce University Technology Centre for Control and Monitoring Systems Engineering, Sheffield, U.K. He has authored or co-authored more than 180 papers in peer-reviewed journals and conferences. His research interests include areas of modelling, signal processing and control with applications in aerospace, biomedical and other dynamic systems.

Dr. Kadirkamanathan was the Editor-in-Chief of the *International Journal of Systems Science* among other conference and journal activities.

Jinsong He (S'18) received the B.Sc. degree from the School of Eelectrical Engineering, Wuhan University, Wuhan, China, in 2018. He is working toward the Ph.D. degree with the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore.

From January 2018 to June 2018, he finished his final year project in Clean Energy Research, NTU, Singapore. His research interests include power electronics stability and control.

Jingjing Huang (S'11–M'18) received the B.S. degree from the Henan University of Science and Technology, Luoyang, China, in July 2008, and the Ph.D. degree from Xi'an Jiaotong University, Xi'an, China, in March 2014, both in electrical engineering.

She has been working with Xi'an University of Technology as a Lecturer since April 2014. She is currently a Postdoctoral Research Fellow with Nanyang Technological University, Singapore since December 2016. Her research interests include renewable energy system, high-frequency transformer, hybrid ac/dc microgrid, and high-power converters.