Output-Series Connected Dual Active Bridge Converters for Zero-Voltage Switching Throughout Full Load Range by Employing Auxiliary *LC* Networks

Zhiqiang Guo, *Member, IEEE*, Deshang Sha, *Senior Member, IEEE*, and Keling Song

***Abstract*—This paper presents an output-series connected dual active bridge (DAB) converter for efficient zero-voltage switching (ZVS) by employing dual auxiliary *LC* networks in high-output voltage applications. The dual auxiliary *LC* networks are integrated into the converter for ZVS throughout full load range. The gate signals of the output side switches can control the current in the *LC* networks. By analyzing the working modes of the converter, the modulation trajectory is designed in terms of the boundaries of the ZVS range. The conduction loss caused by the auxiliary *LC* networks is adjusted according to the voltage and load power. The modulation scheme can achieve seamless transition between the adjacent working modes. The conduction loss of the proposed converter is compared with the conventional output-series DAB converter. Although the conduction loss is increased under light loads, all the switches can achieve ZVS. The reduced switching loss can improve the overall efficiency. Finally, a 1.3 kW experimental prototype was built to verify the effectiveness of the proposed converter and the modulation scheme, which demonstrates the ZVS performance and efficiency improvement.**

***Index Terms*—Auxiliary *LC* networks, dual active bridge (DAB), output-series, zero-voltage switching (ZVS).**

I. Introduction

THE dual active bridge (DAB) converter was proposed in energy storage system for high efficiency and high power density applications [1]. By using the single phase shift (SPS) between two full bridges, the bidirectional power can be achieved. Because of the galvanic isolation and high voltage gain adjusted by turns ratio of the transformer, DAB converter has become a popular solution to energy storage system [2], [3]. However, only using single phase shifted control cannot achieve high efficiency over wide battery voltage range. When

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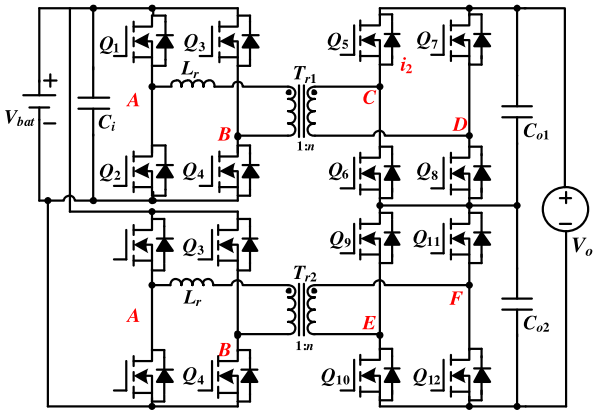

Fig. 1. Input-parallel output-series dual active bridge converter.

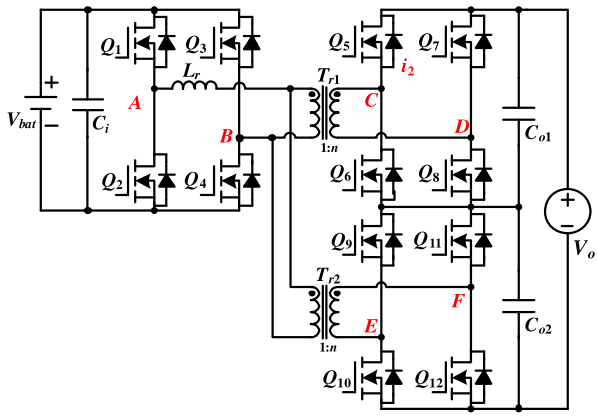

Fig. 2. Output-series dual active bridge converter.

working modes on ZVS and RMS current optimization can be used for high efficiency [16]. However, the converter still cannot achieve ZVS under some circumstances. The TZM modulation with an inductor in parallel with the transformer can keep all the switches working in ZVS [17]. In ETH, DAB converters with full-load-range ZVS can be achieved by using commutation inductors in parallel with the active full bridges [18]. By using auxiliary commutation inductors with variable frequency and variable phase shift, DAB converter is extended to bidirectional ac–dc converters for full-operation-range ZVS [19], [20]. However, the commutation inductors have circulating current in all operation modes. Accordingly, the conduction loss is increased in all the operation modes. The T-type bridge leg used in DAB converter can achieve low RMS current [21], [22]. However, ZVS achievement for all switches becomes complex since there are more switches. In [23], a two-working-mode modulation scheme for the DAB converter with a dc blocking capacitor is proposed for wide voltage conversion range. However, there must be a gradual transition between the two working modes, which may affect the dynamic performance.

In order to meet high dc-link voltage requirement, the three-level or series-connected topologies permit low voltage rating switches to be used in this situation. A three-level DAB converter in different working modes is used in 1 kV dc bus voltage [24]. However, the converter still works in two-level modulation. Clamping diodes and flying capacitors have to be used to decouple the voltage stress of the outer and inner switches. Although the conduction loss is optimized in different operation modes, the switches still work in hard switching. A neutral-point clamped DAB converter is developed to improve the efficiency and balance the capacitor voltages [25]. However, the complicated modulation still cannot guarantee wide ZVS. In [26], a high-voltage DAB converter with series-connected half bridges is used in the high-voltage side. Likewise, Fig. 1 shows the input-parallel output-series DAB converter suitable for high output dc-link voltage [27]. By sharing the switches in battery side, the output-series dual active bridge (OSDAB) converter can be derived in Fig. 2. Compared with the three-level DAB converter, output-series DAB converter is more flexible in high-voltage applications. However, the converter still cannot achieve ZVS over wide battery voltage range and full load range.

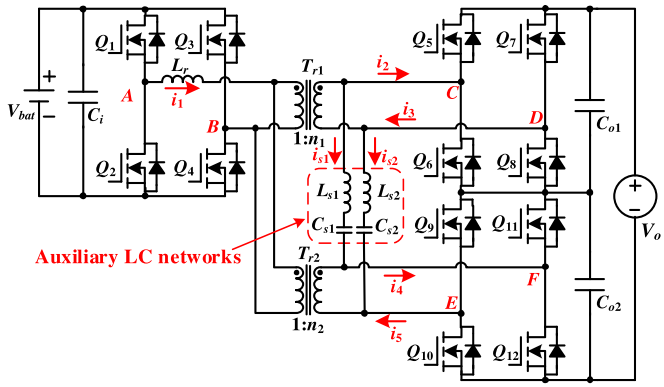

Fig. 3. Output-series dual active bridge converter with dual auxiliary *LC* network.

In this paper, an output-series DAB converter with dual auxiliary *LC* networks (OSDAB plus dual *LC*) is proposed in order to achieve ZVS throughout full load range. The dual *LC* networks are connected across the midpoints of the output full bridges. The phase shift of the output full bridge can control the current in the auxiliary *LC* networks. The current in the auxiliary *LC* networks can guarantee all the switches work in ZVS. In order to reduce the conduction loss caused by the *LC* networks, the modulation trajectory is designed according to the boundaries of the ZVS range. The currents in auxiliary *LC* networks can guarantee that all the switches work in the soft switching. When the converter can achieve ZVS without *LC* networks, the currents in the auxiliary *LC* networks are regulated to zero. The conduction loss cause by the auxiliary *LC* networks for different battery voltages and load power can be optimized.

This paper is organized as follows. An output-series DAB converter with dual auxiliary *LC* networks and its operation modes are described in Section II. The key feature and ZVS operating range of the proposed converter are analyzed in Section III. In terms of the ZVS boundaries, the modulation trajectory is investigated and the converter can achieve seamless transition between adjacent working modes. The experimental prototype is built to verify the performance of the proposed converter in Section IV. Finally, Section V provides the conclusion.

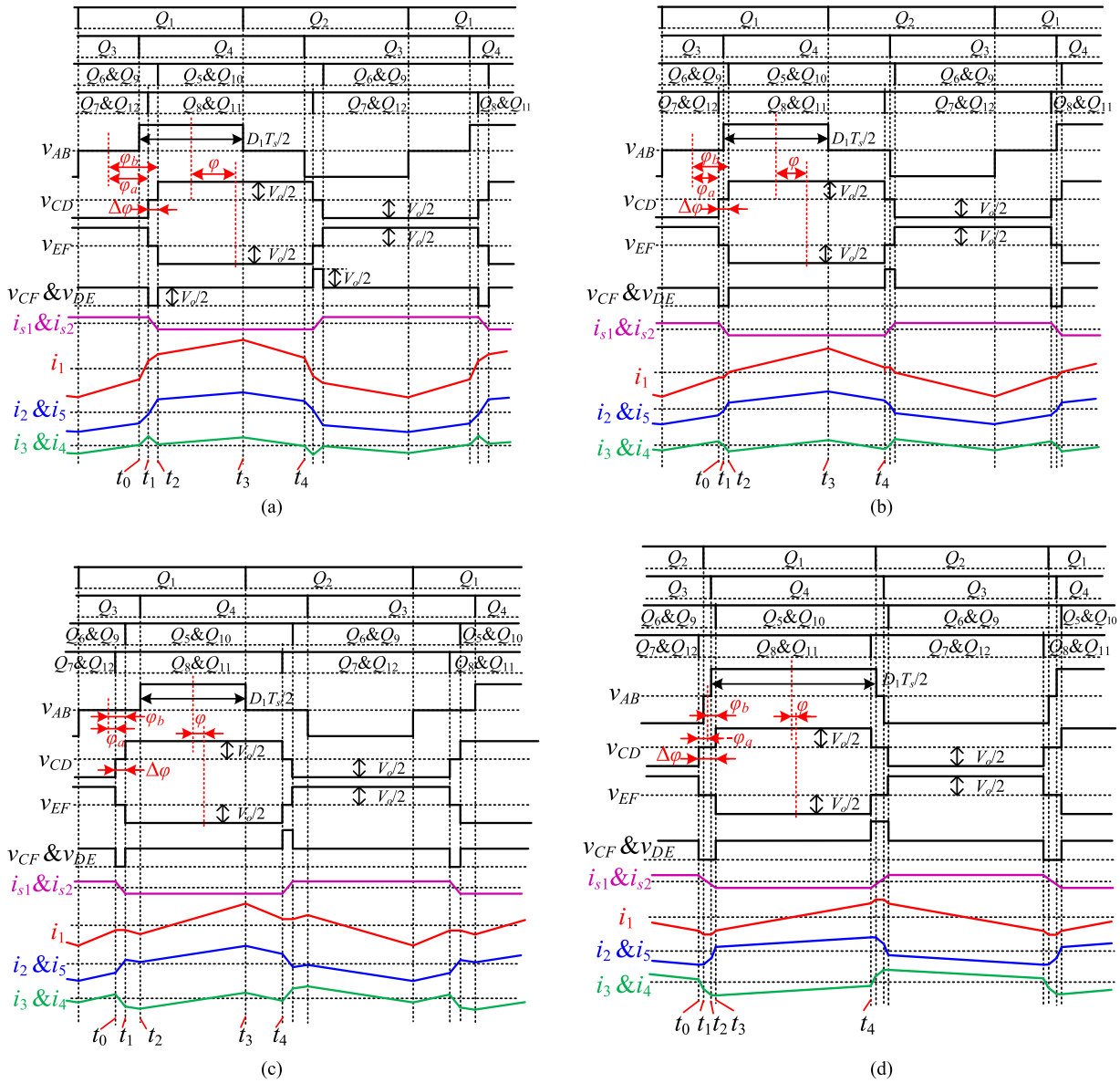

Fig. 4. Working modes in forward power flow. (a) Mode 1*a*. (b) Mode 2*a*. (c) Mode 3. (d) Mode 4.

II. Working Modes of the Proposed Converter

Fig. 3 shows the topology of the output-series DAB converter with dual auxiliary *LC* networks. V_{bat} is the battery voltage. On the battery side, the power stage is a full bridge. On the output side, the power stage is composed of two full bridges, whose output voltage is connected in series to form the output voltage. C_{o1} and C_{o2} are the output capacitors. The output voltage is V_o. There are two transformers. Their turns ratio are $1{:}n_1$ and $1{:}n_2$, respectively, where n_1 and n_2 are equal to n. L_r is the series inductance. The three full bridges are linked with series inductor and two transformers. In the two transformers, the two windings in the battery side are parallel. The power transmitted from the battery to the output is defined as the forward power flow, conversely, is defined as the reverse power flow. L_{s1}, L_{s2}, C_{s1}, and C_{s2} constitute two auxiliary *LC* networks used to achieve wide ZVS. Taking the forward power flow into consideration, the converter can work in four modes, which are shown in Fig. 4. The gate signals for $Q_1 - Q_{12}$ are 50% duty cycle. As seen in Fig. 4, some switches are driven by the same gate signals. v_{AB} is the output voltage of the battery side full bridge. D_1 is its effective duty cycle. T_s is the switching period. v_{CD} and v_{EF} are controlled by the phase shift of the two output-side full bridges, and their waveforms are symmetric in the horizontal coordinates. φ is the phase shift between v_{AB} and v_{CD}. $\Delta\varphi$ is the phase shift between Q_8 and Q_5. φ_a is equal to $\varphi - \frac{\Delta\varphi}{2}$, and φ_b is equal to $\varphi + \frac{\Delta\varphi}{2}$. φ_a and φ_b are illustrated in Fig. 4. Due to the symmetry of the forward and reverse power flow, there are also four working modes in reverse power flow. In terms of the range of φ_a and φ_b, the boundary conditions of the working modes are shown in Table I. Mode 1*a* and Mode 1*b* are the symmetrical working modes, and Mode 2*a* and Mode 2*b* are the symmetrical working modes. Mode 3 and Mode 4

TABLE I
BOUNDARY CONDITION FOR EACH MODE

Forward Power Flow		Reverse Power Flow	
Working Mode	Boundary condition	Working Mode	Boundary condition
Mode 1*a*	$\frac{1}{2}-\frac{D_1}{2}\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le\frac{1}{2}$	**Mode 1*b***	$-\frac{1}{2}\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le-\left(\frac{1}{2}-\frac{D_1}{2}\right)$
Mode 2*a*	$-\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_a}{\pi}\le\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_b}{\pi}\le\frac{1}{2}$	**Mode 2*b***	$-\frac{1}{2}\le\frac{\varphi_a}{\pi}\le-\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_b}{\pi}\le\left(\frac{1}{2}-\frac{D_1}{2}\right)$
Mode 3	$-\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_a}{\pi}\le\frac{\varphi_b}{\pi}\le\left(\frac{1}{2}-\frac{D_1}{2}\right)$		
Mode 4	$\frac{\varphi_a}{\pi}\le-\left(\frac{1}{2}-\frac{D_1}{2}\right)\le0\le\left(\frac{1}{2}-\frac{D_1}{2}\right)\le\frac{\varphi_b}{\pi}$		

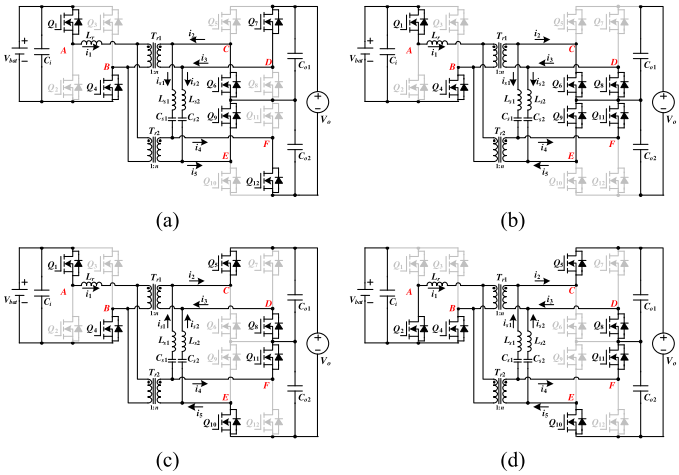

Fig. 5. Topological stages with half switching period in Mode 1*a*. (a) $[t_0, t_1]$. (b) $[t_1, t_2]$. (c) $[t_2, t_3]$. (d) $[t_3, t_4]$.

are the common working modes in both forward and reverse power flow. Only forward power flow will be analyzed in this paper. The same conclusion can be drawn for the reverse power flow by using the same method. As seen, $v_{\rm CF}$ and $v_{\rm DE}$ are voltages across the two *LC* networks, which are larger than zero. The capacitances of C_{s1} and C_{s2} are large enough to filter out the dc voltage offset, which guarantees that the average currents in L_{s1} and L_{s2} are equal to zero. The voltages across C_{s1} and C_{s2} are $V_o/2$. The phase shift angle $\Delta\varphi$ can control the current in the auxiliary *LC* networks. $\Delta\varphi$ is the small value. Otherwise, there is large current in the *LC* networks, which degrades the efficiency. Therefore, D_1 can only be regulated in a wide range to meet the voltage-second balance across the both side of the transformers. In this case, the converter can be modulated by EPS. In order to meet voltage-second balance across the both side of the transformer, the converter should meet $nV_{\rm bat}D_1=\frac{V_o}{2}(1-\frac{\Delta\varphi}{\pi})\approx\frac{V_o}{2}$. Therefore, the effective voltage gain meets the condition: $M=V_o/nV_{\rm bat}=2D_1\le2$. The turns ratio of the transformer should be designed in consideration with the minimum battery voltage. The turns ratio of the transformer can be designed as $n=V_o/2V_{\rm bat\_min}$, where $V_{\rm bat\_min}$ is the minimum battery voltage. Assuming $L_{s1}=L_{s2}=L_s$, $C_{s1}=C_{s2}=C_s$, and $i_{s1}=i_{s2}=i_s$, and defining $X_r=2\pi L_r/T_s$ and $X_s=2\pi L_s/T_s$, the currents in converter meet the following conditions:

$$\begin{cases} i_2=i_5=\frac{i_1}{2n}-i_s \\ i_3=i_4=\frac{i_1}{2n}+i_s. \end{cases} \tag{1}$$

Ignoring the dead time of the gate signals, there are four working stages for each working mode in half of the switching period. To explain, the working stages in Mode 1*a* are shown in Fig. 5.

Stage 1 ($[t_0, t_1]$) [see Fig. 5(a)]: Prior to t_0, Q_1, Q_3, Q_6, Q_7, Q_9, and Q_{12} are ON, and Q_2, Q_4, Q_5, Q_8, Q_{10}, and Q_{11} are OFF. At t_0, Q_3 is switched OFF and i_1 is negative. The junction capacitor of Q_4 is discharged, and Q_4 is turned ON with ZVS. i_1 is increased, and i_{s1} and i_{s2} are positive. The currents in this stage are expressed as follows:

$$\begin{cases} i_1(t)=i_1(t_0)+\frac{V_{\rm bat}+V_o/(2n)}{L_r}(t-t_0) \\ i_s(t)=i_s(t_0). \end{cases} \tag{2}$$

Stage 2($[t_1, t_2]$) [see Fig. 5(b)]: At t_1, Q_7 and Q_{12} are turned OFF. Because i_3 and i_4 are positive at this time, the junction capacitors of Q_8 and Q_{11} start to be discharged. Until the voltage across Q_8 and Q_{11} reaches zero, Q_8 and Q_{11} are turned ON with ZVS. i_1 is still increased, while i_{s1} and i_{s2} start to decrease. The currents in this stage are expressed as follows:

$$\begin{cases} i_1(t)=i_1(t_1)+\frac{V_{\rm bat}}{L_r}(t-t_1) \\ i_s(t)=i_s(t_1)-\frac{V_o}{2L_s}(t-t_1). \end{cases} \tag{3}$$

Stage 3($[t_2, t_3]$) [see Fig. 5(c)]: At t_2, Q_6 and Q_9 are turned OFF. i_2 and i_5 are positive and large enough, so the junction capacitors of Q_5 and Q_{10} are discharged. Until the voltage across Q_5 and Q_{10} reaches zero, Q_5 and Q_{10} are turned ON with ZVS. In this stage, the energy starts to transmit from the battery side to the output side. The currents in this stage are expressed as follows:

$$\begin{cases} i_1(t)=i_1(t_1)+\frac{V_{\rm bat}-V_o/(2n)}{L_r}(t-t_2) \\ i_s(t)=i_s(t_2). \end{cases} \tag{4}$$

Stage 4($[t_3, t_4]$) [see Fig. 5(d)]: At t_4, Q_1 is turned OFF. The current in the primary side of the transformer will charge and discharge the junction capacitors of Q_1 and Q_2. When the voltage across Q_1 reaches zero and the voltage across Q_2 reaches $V_{\rm bat}$, Q_2 is turned ON with ZVS. The currents in this stage are expressed as follows:

$$\begin{cases} i_1(t)=i_1(t_1)-\frac{V_o/(2n)}{L_r}(t-t_3) \\ i_s(t)=i_s(t_3). \end{cases} \tag{5}$$

According to (1)–(5), currents i_1, i_2, i_3, i_4, i_5 at the time of t_0, t_1, t_2, and t_3 can be derived. The working stages in Mode 2*a*, Mode 3, and Mode 4 can be analyzed in the same method. The key feature of the working modes will be analyzed in accordance with these currents.

TABLE II
ZVS CONDITIONS FOR Q_1 AND Q_4

	Mode 1*a*	**Mode 2*a***
ZVS for Q_1	$-i_1(t_3)=-I_{base}\left[\frac{1}{8}\left(\frac{\varphi_a}{\pi}+\frac{\varphi_b}{\pi}-D_1\right)+\frac{D_1}{4M}\right]\le -I_{ZVS1}$	$-i_1(t_3)=-I_{base}\left[\frac{D_1}{4M}+\frac{1}{8}\left(D_1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\right]\le -I_{ZVS1}$
ZVS for Q_4	$i_1(t_0)=I_{base}\left[\frac{1}{8}\left(2-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}-D_1\right)-\frac{D_1}{4M}\right]\le -I_{ZVS1}$	$i_1(t_1)=I_{base}\left[\frac{1}{8}\left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)-\frac{D_1}{4M}\right]\le -I_{ZVS1}$
	Mode 3	**Mode 4**
ZVS for Q_1	$-i_1(t_3)=-I_{base}\left[\frac{D_1}{4M}-\frac{1}{8}\left(D_1-\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)\right]\le -I_{ZVS1}$	$i_1(t_1)=I_{base}\left[\frac{1}{8}\left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)-\frac{D_1}{4M}\right]\le -I_{ZVS1}$
ZVS for Q_4	$i_1(t_2)=I_{base}\left[\frac{1}{8}\left(D_1+\frac{\varphi_b}{\pi}+\frac{\varphi_a}{\pi}\right)-\frac{D_1}{4M}\right]\le -I_{ZVS1}$	$i_1(t_2)=I_{base}\left[\frac{1}{8}\left(1+\frac{\varphi_a}{\pi}-\frac{\varphi_b}{\pi}\right)-\frac{D_1}{4M}\right]\le -I_{ZVS1}$

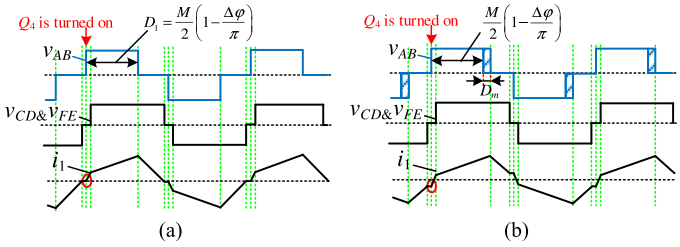

Fig. 6. Key waveforms of Mode 2*a* with specific duty cycle. (a) $D_1=\frac{M}{2}(1-\frac{\Delta\varphi}{\pi})$. (b) $D_1=\frac{M}{2}(1-\frac{\Delta\varphi}{\pi})+D_m$.

III. KEY FEATURE AND MODULATION SCHEME OF THE CONVERTER

A. ZVS Analyses for Q_1-Q_4

Because of the symmetry in two halves of the switching period, the ZVS conditions for Q_1 and Q_2 are the same, and the ZVS conditions for Q_3 and Q_4 are the same. Therefore, ZVS performance of Q_1 and Q_4 will be analyzed, and Q_3 and Q_2 work in the same condition. In order to achieve ZVS for Q_1 and Q_4, i_1 should be negative and large enough, i.e., $i_1\le -I_{ZVS1}$, where I_{ZVS1} is the minimum current to charge or discharge the junction capacitors during the dead time for ZVS of Q_1-Q_4. I_{ZVS1} is associated with $C_{\rm oss}$ (output capacitance) of the switches. The proximate evaluation of I_{ZVS1} can be expressed as $V_{\rm bat}C_{{\rm oss}(Q1-Q4)}/t_{\rm dead}$, where $t_{\rm dead}$ is the dead time of the switches.

According to i_1 at the commutation time, the ZVS boundaries of Q_1 and Q_4 in different working modes are shown in Table II. $I_{\rm base}$ is defined as the normalized current, where $I_{\rm base}=\frac{V_oT_s}{nL_r}$. Taking Mode 2*a* for example, if D_1 is equal to $\frac{V_o}{2nV_{\rm bat}}(1-\frac{\Delta\varphi}{\pi})=\frac{M}{2}(1-\frac{\Delta\varphi}{\pi})$, the key waveform of i_1 is shown in Fig. 6(a). When Q_4 is turned ON, i_1 is equal to zero. Therefore, Q_4 works in hard switching. If D_1 is set to be larger than $\frac{M}{2}(1-\frac{\Delta\varphi}{\pi})$, i.e., $D_1=\frac{M}{2}(1-\frac{\Delta\varphi}{\pi})+D_m$, the key waveform of i_1 is shown in Fig. 6(b). When Q_4 is turned ON, i_1 is less than zero. Therefore, Q_4 has the potential to achieve ZVS. Substituting $D_1=\frac{M}{2}(1-\frac{\Delta\varphi}{\pi})+D_m$ into Table II, the ZVS conditions for Q_1 and Q_4 are shown in Table III. The ZVS conditions for Q_1 and Q_4 in different modes can be synthesized to the same. As long as $\frac{I_{\rm base}D_m}{4M}\ge I_{\rm ZVS1}$, i.e., $D_m\ge\frac{4L_rI_{\rm ZVS1}}{V_{\rm bat}T_s}$, Q_1 and Q_4 can guarantee ZVS in all the working modes. D_m is designed as $\frac{4L_rI_{\rm ZVS1}}{V_{\rm bat}T_s}$ in the following analyses and converter design.

B. ZVS Analyses for Q_5-Q_{12}

Because of the symmetry in two halves of the switching period, the ZVS conditions for Q_5, Q_6, Q_9, and Q_{10} are the same, and the ZVS conditions for Q_7, Q_8, Q_{11}, and Q_{12} are the same. Therefore, the ZVS conditions for Q_5 & Q_{10} and Q_8 & Q_{11} will be analyzed in half of the switching period. The commutations during the dead time for Q_5 & Q_{10} and Q_8 & Q_{11} are shown in Fig. 7. To achieve ZVS of Q_5 & Q_{10} and Q_8 & Q_{11}, i_2, i_5, i_3, and i_4 should be positive and large enough, i.e., $i_2=i_5\ge I_{ZVS2}$ and $i_3=i_4\ge I_{ZVS2}$, where I_{ZVS2} is the minimum current to charge and discharge the junction capacitor for ZVS of Q_5-Q_{12} during the dead time. The proximate evaluation of I_{ZVS2} can be expressed as $V_oC_{{\rm oss}(Q5-Q12)}/2t_{\rm dead}$. The ZVS constraints on Q_5 & Q_{10} and Q_8 & Q_{11} are shown in Table IV.

To achieve ZVS of Q_5 & Q_{10} and Q_8 & Q_{11} in all the working modes, the following conditions should be satisfied.

1) As seen in Table IV of Mode 1*a*, the ZVS boundary of Q_5 & Q_{10} is rewritten as follows:

$$\Delta\varphi\ge\frac{1}{\frac{M}{4X_s}-\frac{M-2}{8n^2X_r}}\left[\frac{I_{\rm ZVS2}}{nV_{\rm bat}}-\frac{(M-2)\pi}{8n^2X_r}-\frac{\varphi}{2n^2X_r}\right]=\Delta\varphi_d. \tag{6}$$

2) In Mode 1*a*, the ZVS boundary of $Q8$ & $Q11$ is rearranged as follows:

$$\Delta\varphi\ge\frac{1}{\frac{M}{4X_s}-\frac{M+2}{8n^2X_r}}\left[\frac{I_{\rm ZVS2}}{nV_{\rm bat}}-\frac{(M-2)\pi}{8n^2X_r}-\frac{\varphi}{2n^2X_r}\right]=\Delta\varphi_e. \tag{7}$$

TABLE III
DERIVED ZVS CONDITIONS FOR Q_1 AND Q_4

	Mode 1*a*	**Mode 2*a***
ZVS for Q_1	$-i_1(t_3)=-I_{base}\left[\frac{1}{8}\left(\frac{2\varphi_a}{\pi}+1-D_1\right)+\frac{D_m}{4M}\right]\le-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$	$-i_1(t_3)=-I_{base}\left[\frac{1}{8}\left(\frac{2\varphi_a}{\pi}+1-D_1\right)+\frac{D_m}{4M}\right]\le-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$
ZVS for Q_4	$i_1(t_0)=I_{base}\left[\frac{1}{8}\left(1-D_1-\frac{2\varphi_a}{\pi}\right)-\frac{D_m}{4M}\right]\le-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$	$i_1(t_1)=-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$
	Mode 3	**Mode 4**
ZVS for Q_1	$-i_1(t_3)=-I_{base}\left[\frac{1}{8}\left(\frac{2\varphi_a}{\pi}+1-D_1\right)-\frac{D_m}{4M}\right]\le-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$	$i_1(t_1)=-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$
ZVS for Q_4	$i_1(t_2)=-I_{base}\left[\frac{1}{8}\left(1-D_1-\frac{2\varphi_b}{\pi}\right)+\frac{D_m}{4M}\right]\le-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$	$i_1(t_1)=-\frac{I_{base}D_m}{4M}\le-I_{ZVS1}$

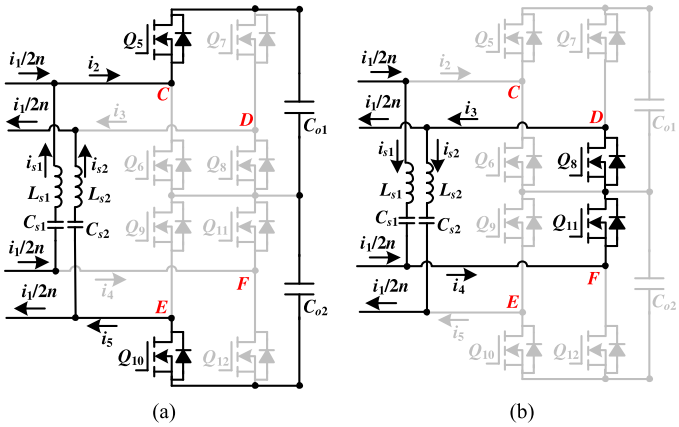

Fig. 7. Commutations during the dead time for Q_5 & Q_{10} and Q_8 & Q_{11}. (a) Q_5 & Q_{10}. (b) Q_8 & Q_{11}.

Comparing (6) with (7), $\Delta\varphi_e$ is greater than $\Delta\varphi_d$. Therefore, as long as (7) is satisfied, (6) must be satisfied.

3) As seen in Table IV, the ZVS boundary of $Q5$ & $Q10$ in Mode 2*a* is the same as that in Mode 1*a*, which is expressed as (6).
4) The ZVS boundary of $Q8$ & $Q11$ in Mode 2*a* is rewritten as follows:

$$\Delta\varphi \ge \frac{4X_s}{V_o}\left(I_{\mathrm{ZVS2}}+\frac{D_m\pi}{8n^2X_r}\right). \tag{8}$$

It is independent of φ.

5) The ZVS constraints on Q_5-Q_{12} in Mode 3 are the same as Q_8 & Q_{11} in Mode 2*a*, which is expressed as (8).
6) The ZVS boundary of Q_5 & Q_{10} in Mode 4 is the same as that in Mode 1*a*.
7) The ZVS boundary of Q_8 & Q_{11} in Mode 4 is rearranged as follows:

$$\Delta\varphi \ge \frac{1}{\frac{MT_s}{4X_s}-\frac{M-2}{8n^2X_r}}\left[\frac{I_{\mathrm{ZVS2}}}{nV_{\mathrm{bat}}}-\frac{(M-2)\pi}{8n^2X_r}+\frac{\varphi}{2n^2X_r}\right]. \tag{9}$$

As long as (9) is true, (6) must be satisfied.

Above all, the ZVS boundary of Q_5-Q_{12} can be synthesized to (7) in Mode 1*a*, (6) and (8) in Mode 2*a*, (8) in Mode 3, and (9) in Mode 4.

C. Modulation Trajectory

In terms of the analyses of the ZVS boundaries of Q_5-Q_{12}, the ZVS range can be calculated with specific parameters. Fig. 8 shows the three-dimensional surface of the ZVS boundary versus V_{bat} and φ, where $L_r=24\,\mu$H, $T_s=12.5\,\mu$s, $L_s=22\ \mu$H, $n=1.5$, $I_{zvs1}=2$ A, $I_{zvs2}=2$ A, and $V_o=600$ V. The vertical axis is $\Delta\varphi$. The space above the surface is the ZVS area, and the space below the surface is hard switching area. Fig. 9 shows the ZVS range of Q_5-Q_{12} with different battery voltages. Fig. 9 is the vertical section of Fig. 8. The shadowed area in Fig. 9 is the ZVS range for Q_5-Q_{12}. As seen, with the increase of the battery voltage, the converter becomes more difficult to achieve ZVS. By using the currents in the auxiliary *LC* networks, i.e., $\Delta\varphi$ is large enough, the converter can guarantee ZVS of Q_5-Q_{12}. However, it will cause more conduction loss with large $\Delta\varphi$. In order to achieve ZVS with low conduction loss, the modulation trajectory should be designed according to the boundary conditions analyzed in Section III-C. The designed modulation trajectory is the red solid line shown in Fig. 9.

In (7), setting $\Delta\varphi_e=0$, φ is calculated as follows:

$$\varphi=\frac{2nI_{\mathrm{ZVS}}X_r}{V_{\mathrm{bat}}}-\frac{\pi}{4}(M-2)=\varphi_n. \tag{10}$$

The coordinate of the point *N* in Fig. 9 is expressed as $(\varphi_n,\,0)$, which varies with the battery and output voltages. The point *M* is on the boundary condition between Mode 1*a* and Mode 2*a*, which is expressed as follows:

$$\Delta\varphi=\frac{1}{1+M/2}\left[2\varphi+\left(\frac{M}{2}+D_m-1\right)\pi\right]. \tag{11}$$

Then, in terms of (7) and (11), the coordinate of the point *M* in Fig. 9 is expressed as $(\varphi_m,\,\Delta\varphi_m)$, where eq.(12) shown at the bottom of the next page.

TABLE IV
ZVS CONDITIONS FOR Q_5 & Q_{10} AND Q_8 & Q_{11}

	Mode 1*a*	**Mode 2*a***
ZVS for Q_5&Q_{10}	$i_2(t_2)=i_5(t_2)$ $=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}+\left(\frac{2\varphi}{\pi}+\frac{\Delta\varphi}{\pi}-1\right)\frac{1}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left[\frac{1}{16n}\left(1-\frac{2}{M}\right)+\frac{1}{4nM}\frac{\varphi}{\pi}+\left(\frac{nL_r}{8L_s}-\frac{1}{16n}+\frac{1}{8nM}\right)\frac{\Delta\varphi}{\pi}\right]\geq I_{ZVS2}$	$i_2(t_2)=i_5(t_2)$ $=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}-\left(1-\frac{2\varphi}{\pi}-\frac{\Delta\varphi}{\pi}\right)\frac{1}{8nM}+\frac{nLr}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left[\frac{1}{16n}\left(1-\frac{2}{M}\right)+\frac{1}{4nM}\frac{\varphi}{\pi}+\left(\frac{nL_r}{8L_s}-\frac{1}{16n}+\frac{1}{8nM}\right)\frac{\Delta\varphi}{\pi}\right]\geq I_{ZVS2}$
ZVS for Q_8&Q_{11}	$i_3(t_1)=i_4(t_1)$ $=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}+\left(\frac{2\varphi}{\pi}-\frac{\Delta\varphi}{\pi}-1\right)\frac{1}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left[\frac{1}{16n}\left(1-\frac{2}{M}\right)+\frac{1}{4nM}\frac{\varphi}{\pi}+\left(\frac{nL_r}{8L_s}-\frac{1}{16n}-\frac{1}{8nM}\right)\frac{\Delta\varphi}{\pi}\right]\geq I_{ZVS2}$	$i_3(t_0)=i_4(t_0)=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}-\frac{D_1}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left(-\frac{D_m}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right)\geq I_{ZVS2}$
	Mode 3	**Mode 4**
ZVS for Q_5&Q_{10}	$i_2(t_1)=i_5(t_1)=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}-\frac{D_1}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left(-\frac{D_m}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right)\geq I_{ZVS2}$	$i_2(t_3)=i_5(t_3)$ $=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}+\left(\frac{2\varphi}{\pi}+\frac{\Delta\varphi}{\pi}-1\right)\frac{1}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left[\frac{1}{16n}\left(1-\frac{2}{M}\right)+\frac{1}{4nM}\frac{\varphi}{\pi}+\left(\frac{nL_r}{8L_s}-\frac{1}{16n}+\frac{1}{8nM}\right)\frac{\Delta\varphi}{\pi}\right]\geq I_{ZVS2}$
ZVS for Q_8&Q_{11}	$i_3(t_0)=i_4(t_0)=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}-\frac{D_1}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left(-\frac{D_m}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right)\geq I_{ZVS2}$	$i_3(t_0)=i_4(t_0)$ $=I_{base}\left[\left(1-\frac{\Delta\varphi}{\pi}\right)\frac{1}{16n}-\left(1+\frac{2\varphi}{\pi}-\frac{\Delta\varphi}{\pi}\right)\frac{1}{8nM}+\frac{nL_r}{8L_s}\frac{\Delta\varphi}{\pi}\right]$ $=I_{base}\left[\left(1-\frac{2}{M}\right)\frac{1}{16n}-\frac{1}{4nM}\frac{\varphi}{\pi}+\left(\frac{nL_r}{8L_s}-\frac{1}{16n}+\frac{1}{8nM}\right)\frac{\Delta\varphi}{\pi}\right]\geq I_{ZVS2}$

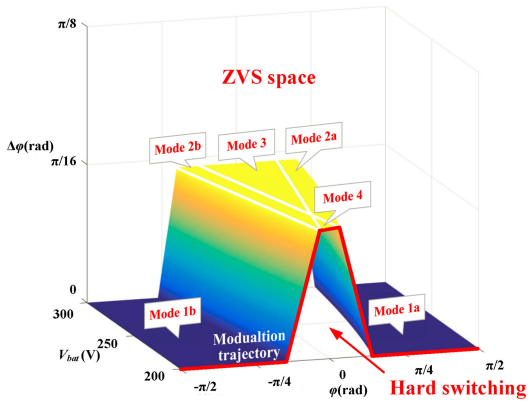

Fig. 8. Three-dimensional (3-D) surface of the ZVS boundary versus V_{bat} and φ.

Point M also varies with the battery and output voltages. Therefore, the line MN in Fig. 9 is expressed as follows:

$$\Delta\varphi=\frac{\Delta\varphi_m}{\varphi_m-\varphi_n}(\varphi-\varphi_n). \tag{13}$$

The modulation trajectory can be illustrated as a flowchart shown in Fig. 10. The control diagram is shown in Fig. 11. As seen in Fig. 11, the output voltage is controlled by a proportional-integral (PI) controller. The output of the PI controller is the phase shift angle φ. As seen in the flowchart as shown in Fig. 10, $\Delta\varphi$ is calculated in accordance with φ. Then, the gate signals of Q_1-Q_{12} are generated in terms of D_1, φ, $\Delta\varphi$. As seen in (10) and (12) shown at the bottom of this page, the turning points of the modulation trajectory are associated with L_r and L_s. Due to the manufacture and nonlinearity of the inductor, L_r and L_s may not be equal to their nominal values, which may make the points M and N deviate away from their set points. However, point M is still located on the boundary condition between Mode 1*a* and Mode 2*a*, and point N is still located on the horizontal axis. As long as points M and N are located in the shadowed area of Fig. 9, the modulation scheme for ZVS is still effective and not very sensitive to the parameter of L_r and L_s.

According to the modulation trajectory and closed-loop control diagram, D_1 versus phase shift angle and battery voltage

$$\begin{cases}\varphi_m=X_s\left(\frac{M+2}{M}\right)\left[\frac{I_{ZVS}}{nV_{bat}}-\frac{M-2}{8n^2X_r}-\left(\frac{0.5\pi M}{X_s(M+2)}-\frac{0.25\pi}{n^2X_r}\right)(M+D_m-1)\right]\\ \Delta\varphi_m=4X_s\left[\frac{I_{ZVS}}{V_o}-\frac{(1-2/M)\pi}{8n^2X_r}+\frac{\pi}{4n^2X_rM}(M+D_m-1)\right]\end{cases} \tag{12}$$

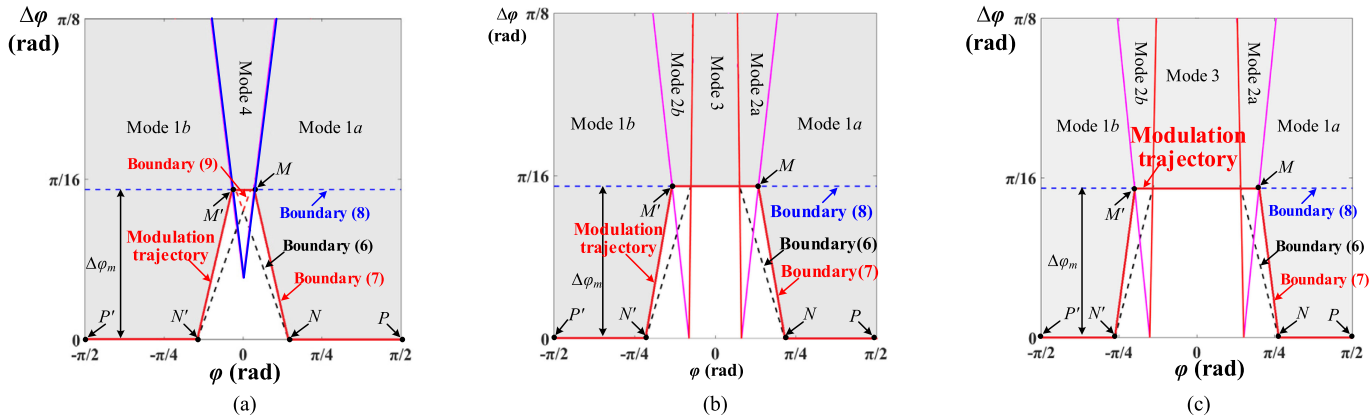

Fig. 9. ZVS range and modulation trajectory for different battery voltages. (a) $V_{\text{bat}} = 200$ V. (b) $V_{\text{bat}} = 250$ V. (c) $V_{\text{bat}} = 300$ V.

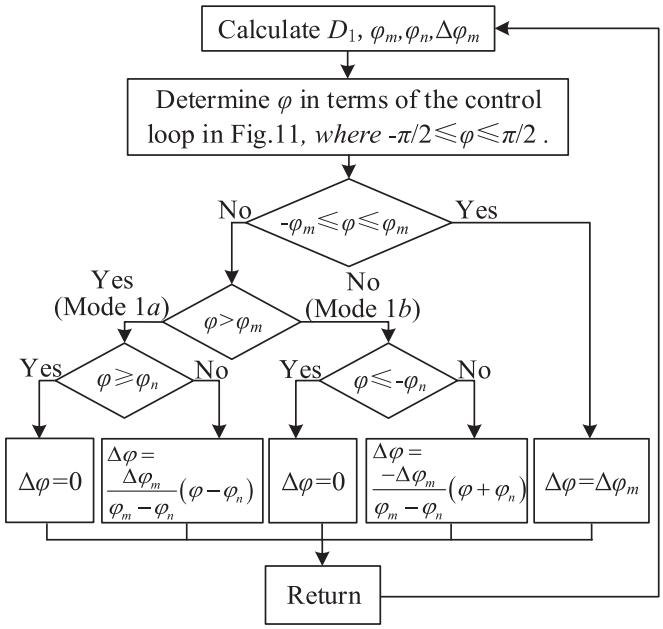

Fig. 10. Flowchart of the modulation trajectory.

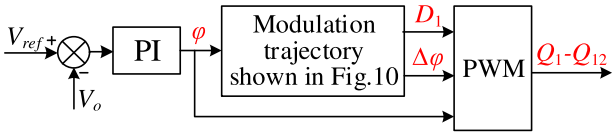

Fig. 11. Closed-loop control diagram.

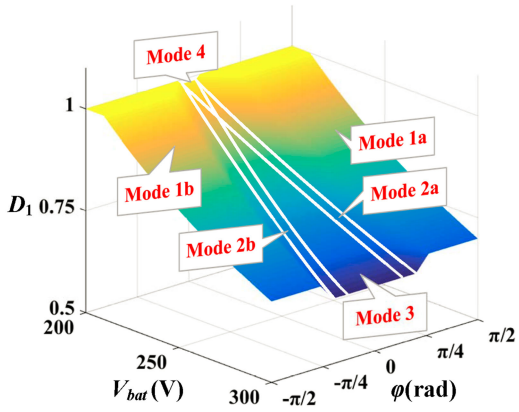

Fig. 12. D_1 versus phase shift angle φ and battery voltage V_{bat}.

TABLE V
OUTPUT POWER EXPRESSIONS IN DIFFERENT WORKING MODES

Working mode	Output power
Mode 1*a*	$P_o = \frac{MV_{bat}^2}{8X_r}\left(2\varphi_a + 2\varphi_b + 2D_1\pi - D_1^2\pi - \frac{2\varphi_a^2}{\pi} - \frac{2\varphi_b^2}{\pi} - \pi\right)$
Mode 2*a*	$P_o = \frac{MV_{bat}^2}{8X_r}\left(4\varphi_a D_1 + 4\varphi_b + 2D_1\pi - D_1^2\pi - \frac{4\varphi_b^2}{\pi} - \pi\right)$
Mode 3	$P_o = \frac{MV_{bat}^2}{4X_r}(\varphi_a + \varphi_b)D_1$
Mode 4	$P_o = \frac{MV_{bat}^2}{4X_r}\left(\varphi_a + \varphi_b + \frac{\varphi_a^2}{\pi} - \frac{\varphi_b^2}{\pi}\right)$

is shown in Fig. 12. As depicted in Fig. 12, D_1 can seamlessly transit between the adjacent working modes.

The output power expressions in different working modes are shown in Table V. The output power in different working modes is not associated with the parameters of the *LC* networks, which demonstrates that the *LC* networks have no impact on the output performance.

The output power versus the phase shift angle and battery voltage in per unit (p.u.) is shown in Fig. 13, where $L_r = 24\,\mu$H, $T_s = 12.5\,\mu$s, $L_s = 22\,\mu$H, $n = 1.5$, $I_{zvs1} = 2$ A, $I_{zvs2} = 2$ A, and $V_o = 600$ V. Fig. 13(a) shows the relationship among output power, battery voltage, and phase shift in three dimensions. Fig. 13(b) is the right lateral view of Fig. 13(a). In the range of φ from $-\pi/2$ to $\pi/2$, the output power is monotonically increasing. Fig. 13(c) shows the curves of the output power versus the phase shift angle. It illustrates that the converter can achieve seamless transition between the adjacent working modes, which demonstrates that the

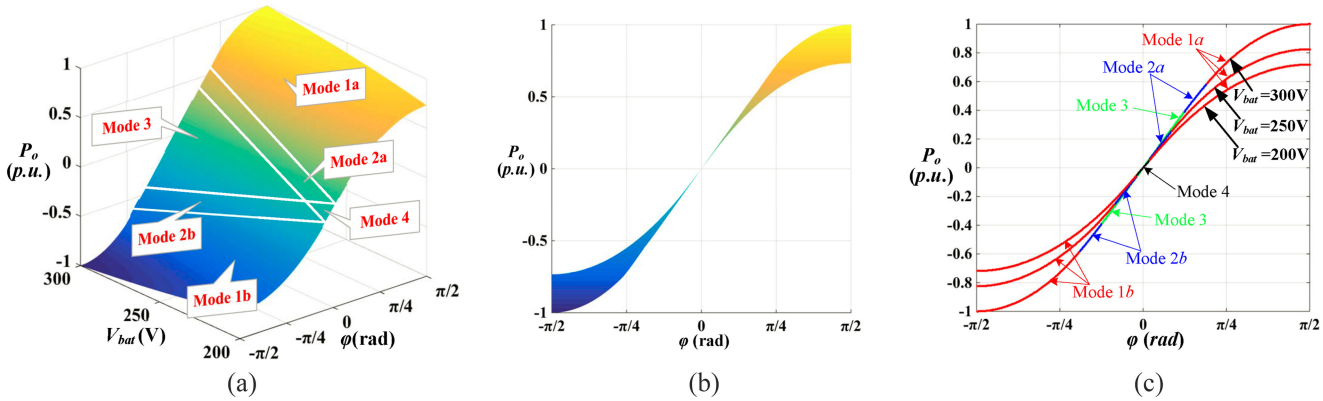

Fig. 13. Output power versus phase shift angle φ and battery voltage V_{bat}. (a) Three-dimensional surface. (b) Right lateral view of Fig. 13(a). (c) Two-dimensional curves of the output power versus φ.

bidirectional power flow can be controlled by the phase shift angle.

D. Design of the Auxiliary Inductor L_s

As seen in Fig. 9, the slope of the *MN* should be lower than zero. Otherwise, the modulation trajectory cannot be implemented in seamless transition. Therefore, according to (7), the following condition should be satisfied:

$$L_s < \frac{L_r}{\frac{1}{2n^2} + \frac{1}{n^2 M}}. \tag{14}$$

In terms of Fig. 13, L_r should be first selected to meet the load requirement in different voltages. Then, L_s can be designed in terms of (14). L_{s1} and L_{s2} may not be equal to the set values in the circuit, which may cause the difference of currents in L_{s1} and L_{s2}. If the current in the auxiliary is large enough, the modulation scheme is still effective for wide ZVS.

E. Switch Conduction Loss Comparison

The RMS of i_1, i_2, i_3, i_4, and i_5 can be evaluated to investigate the conduction loss. The RMS of i_1 reflect the conduction loss of $Q_1 - Q_4$; the RMS of i_2 and i_5 reflect the conduction loss of Q_5, Q_6, Q_9, and Q_{10}; the RMS of i_3 and i_4 reflect the conduction loss of Q_7, Q_8, Q_{11}, and Q_{12}. The RMS current in the converter can be defined as follows: eq.(15) shown at the bottom of thi page.

The RMS currents versus the output power with different voltage gain are illustrated in Fig. 14. The solid lines are the RMS currents of the proposed converter, and the dashed lines are the RMS currents of the conventional OSDAB converter (shown in Fig. 2). The series inductance and turns ratio of the transformers in both converters are the same. The OSDAB is also operated in duty ratio control on the battery side. As seen in Fig. 14, the RMS current in the conventional OSDAB converter

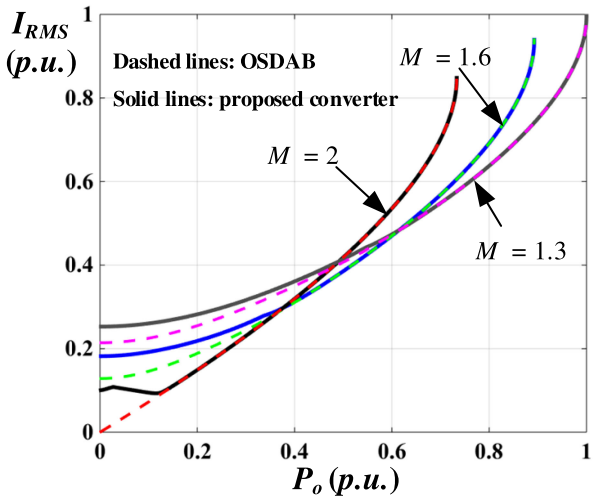

Fig. 14. RMS currents in p.u. in the converter versus the output power (dashed lines: conventional OSDAB converter without *LC* networks; solid lines: proposed converter).

is lower than that in the proposed converter under light loads, but ZVS in the proposed converter can be achieved. Furthermore, the RMS current in the converter is very low under light loads, so the conduction loss does not affect the total loss too much. With the increase of the battery voltage, the conventional OSDAB converter will work in hard switching in wide load range, which lowers the efficiency. All the switches in the proposed converter can achieve ZVS even in no load case. The switching loss can be dramatically reduced, and the efficiency can be improved. In heavy loads, the current in the transformer can maintain all the switches in ZVS, so the RMS current curves of the two converters coincide in heavy loads. In this case, the proposed converter actually works in the same mode as the conventional OSDAB converter. Therefore, the currents in dual *LC*

$$I_{\text{RMS}} = \frac{2}{n}\sqrt{\frac{1}{T_s}\int_0^{Ts} {i_1}^2(t)dt} + \sqrt{\frac{1}{T_s}\int_0^{Ts} {i_2}^2(t)dt} + \sqrt{\frac{1}{T_s}\int_0^{Ts} {i_3}^2(t)dt} + \sqrt{\frac{1}{T_s}\int_0^{Ts} {i_4}^2(t)dt} + \sqrt{\frac{1}{T_s}\int_0^{Ts} {i_5}^2(t)dt} \tag{15}$$

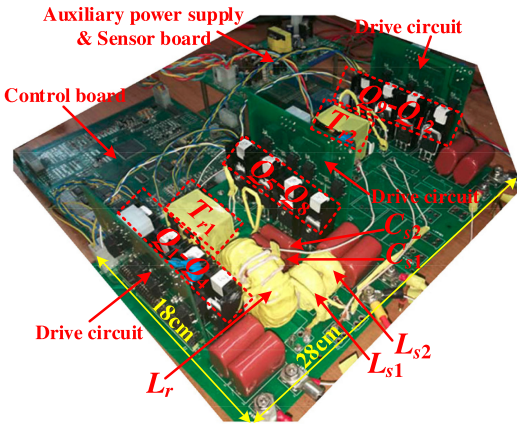

Fig. 15. 1.3 kW experimental prototype for test.

TABLE VI
DETAILED SPECIFICATIONS

Items	Symbol	Parameter
Battery voltage	V_{bat}	200 V~300 V
Output voltage	V_o	600 V
Turns ratio of the transformers	n	1.5
Switching frequency (period)	$f_s\,(T_s)$	80 *k*Hz (12.5 μs)
Switches	$Q_{1\text{-}12}$	FQA28N50
Series inductor	L_r	24 μH
Auxiliary inductor L_{s1}	L_{s1}	22 μH
Auxiliary inductor L_{s2}	L_{s2}	22 μH
Auxiliary capacitor C_{s1}	C_{s1}	4.7 μF
Auxiliary capacitor C_{s1}	C_{s2}	4.7 μF
Output filter capacitance	C_{o1}, C_{o2}	20 μF
Dead time	t_{dead}	400*ns*

networks are equal to zero, and the loss caused by *LC* networks is reduced to zero.

IV. Experimental Verifications

To verify the proposed output-series DAB converter with dual auxiliary *LC* networks, a 1.3 kW experimental prototype is built. In energy storage system, the output can be linked to a dc bus to compensate the mismatch of the power supply and load demands. Therefore, the output voltage is set as a constant value of 600 V, and the battery voltage is 200–300 V. Fig. 15 shows the prototype of the test. The series inductor is selected as 25 μH to meet the load requirement. According to (14), L_s should be less than 54 μH. In the experimental prototype L_s is selected as 22 μH. The detailed specifications are shown in Table VI. As seen, the volume of L_{s1}, L_{s2}, C_{s1}, and C_{s2} is very small, so they do not affect the power density and do not cost too much. I_{ZVS1} and I_{ZVS2} are evaluated as 2 A.

Fig. 16 shows the key waveforms of $v_{\rm AB}$, $v_{\rm CD}$, and $v_{\rm EF}$, when $V_{\rm bat} = 250$ V and $P_o = 650$ W. $v_{\rm CD}$ and $v_{\rm EF}$ are symmetrical with the horizontal axis, the currents in the dual auxiliary *LC* networks are determined by $v_{\rm CF}$ and $v_{\rm DE}$. As seen in the figure,

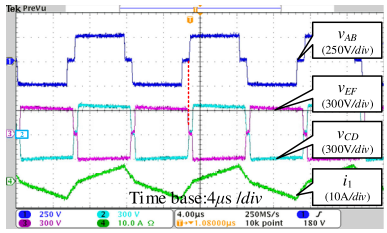

Fig. 16. Measured key waveforms of $v_{\rm AB}$, $v_{\rm CD}$, and $v_{\rm EF}$ when $V_{\rm bat} = 250$ V, $P_o = 650$ W.

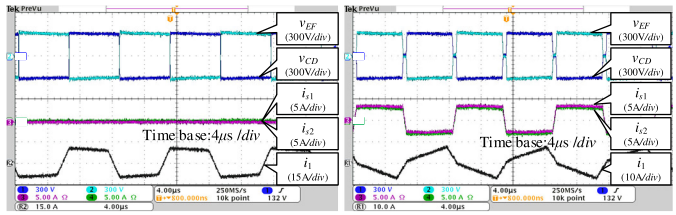

Fig. 17. Currents in the auxiliary *LC* networks. (a) $V_{\rm bat} = 200$ V and $P_o = 650$ W. (b) $V_{\rm bat} = 250$ V and $P_o = 650$ W.

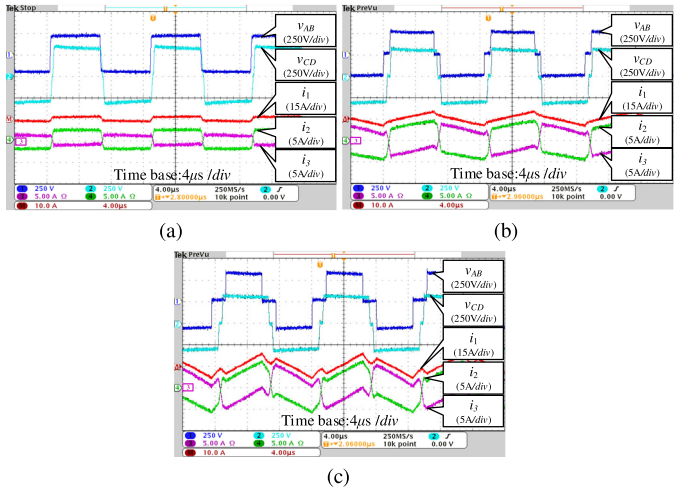

Fig. 18. Measured key waveforms for the forward power flow in light loads. (a) $V_{\rm bat} = 200$ V, $P_o = 300$ W. (b) $V_{\rm bat} = 250$ V, $P_o = 300$ W. (c) $V_{\rm bat} = 300$ V, $P_o = 300$ W.

the converter works in Mode 2*a*. The voltage amplitudes of $v_{\rm CD}$ and $v_{\rm EF}$ are almost same, which reflects the voltage balance of the output capacitors.

Fig. 17 shows the waveforms of $v_{\rm CD}$, $v_{\rm EF}$, and currents in the auxiliary *LC* networks. As seen in Fig. 17(a), when $V_{\rm bat} = 200$ V and $P_o = 650$ W, the converter can achieve ZVS even without the *LC* networks. Therefore, i_{s1} and i_{s2} are controlled to zero. As seen in Fig. 17(b), when $V_{\rm bat} = 250$ V and $P_o = 650$ W, i_{s1} and i_{s2} are adjusted to be large enough for ZVS. In all these cases, i_{s1} and i_{s2} are the same.

Fig. 18 shows the forward power flow when the converter works in light loads. Fig. 18(a) shows experimental results when the battery voltage is 200 V. In this case, the converter works in Mode 4. The phase shift angle $\Delta\varphi$ causes current difference

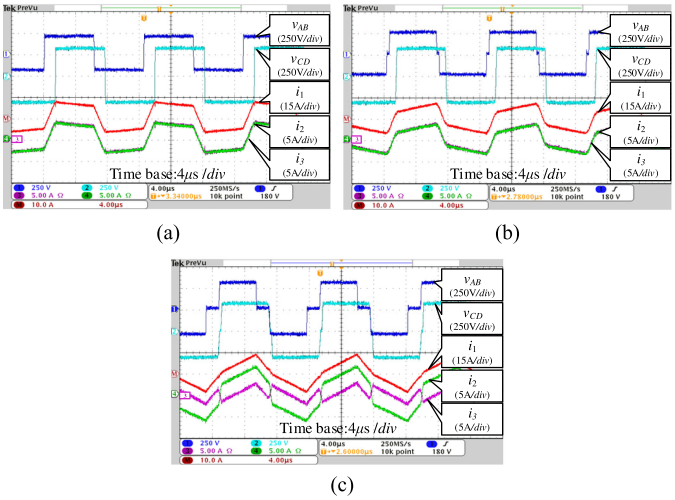

Fig. 19. Measured key waveforms for the forward power flow in heavy loads. (a) $V_{\text{bat}} = 200$ V, $P_o = 1300$ W. (b) $V_{\text{bat}} = 250$ V, $P_o = 1300$ W. (c) $V_{\text{bat}} = 300$ V, $P_o = 1300$ W.

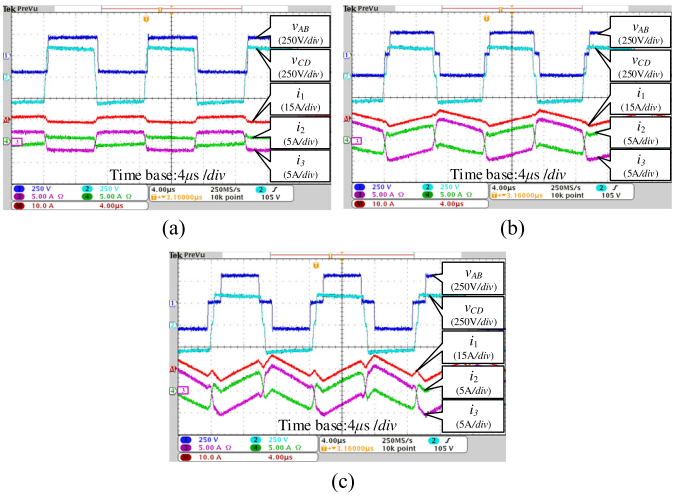

Fig. 20. Measured key waveforms for the reverse power flow in light loads. (a) $V_{\text{bat}} = 200$ V, $P_o = -328$ W. (b) $V_{\text{bat}} = 240$ V, $P_o = -313$ W. (c) $V_{\text{bat}} = 280$ V, $P_o = -300$ W.

between i_2 and i_3, so the converter can achieve ZVS of all the switches in this case. Fig. 18(b) and (c) show the forward experimental results in light loads when the battery voltages are 250 and 300 V, respectively. With the increase of the battery voltage, $\Delta\varphi$ is adaptively regulated to keep the converter work in ZVS over the wide battery voltage.

Fig. 19 shows the key waveforms for the forward power flow in heavy loads. Fig. 19(a) and (b) show the experimental results when the battery voltages are 200 and 250 V, respectively. In these two cases, the converter works in Mode 1*a*. The converter can achieve ZVS of all the switches even if $\Delta\varphi$ is equal to zero. In Fig. 19(c), when the battery voltage is 300 V, $\Delta\varphi$ is regulated to be greater than zero for ZVS. The conventional OSDAB converter will lose ZVS.

Fig. 20 shows the key waveforms for the reverse power flow with light loads. In Fig. 20(a), the converter works in Mode 4.

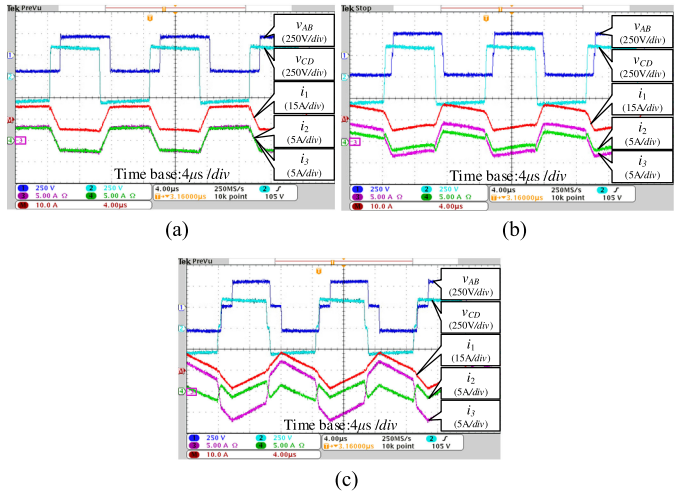

Fig. 21. Measured key waveforms for the reverse power flow in heavy loads. (a) $V_{\text{bat}} = 200$ V, $P_o = -1200$ W. (b) $V_{\text{bat}} = 240$ V, $P_o = -1250$ W. (c) $V_{\text{bat}} = 280$ V, $P_o = -1268$ W.

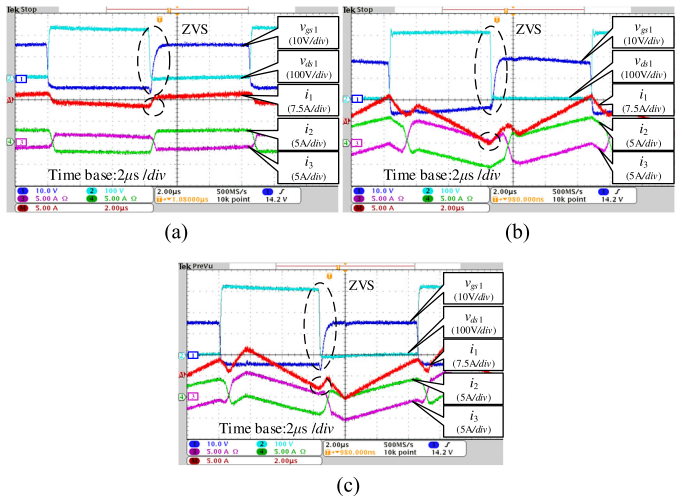

Fig. 22. Gate signal and drain–source voltage of switch Q_1. (a) $V_{\text{bat}} = 200$ V, $P_o = 300$ W. (b) $V_{\text{bat}} = 300$ V, $P_o = 300$ W. (c) $V_{\text{bat}} = 300$ V, $P_o = -300$ W.

In Fig. 20(b), the converter works in Mode 2*b*. In Fig. 20(c), the converter works in Mode 3. In these cases, $\Delta\varphi$ is greater than zero for the ZVS of $Q_5 - Q_8$. The working modes in Fig. 20 are nearly symmetrical with those in Fig. 18.

Fig. 21 shows the key waveforms for the reverse power flow with heavy loads. As shown in Fig. 21(a) and (b), when the battery voltages are 200 and 240 V and the load power is -1200 W, the converter works in Mode 1*b*. In Fig. 21(b), the converter works in Mode 1*b*, and $\Delta\varphi$ is a little greater than zero. As illustrated in Fig. 21(c), with the increase of the battery voltage, the phase shift angle is decreased and the converter switches to Mode 2*b*.

Fig. 22 shows the gate signal and drain–source voltage of switch Q_1. In all different working modes, i_1 is less than zero during the commutation interval. The energy storage in the junction capacitor is discharged by i_1, illustrating that Q_1 works in

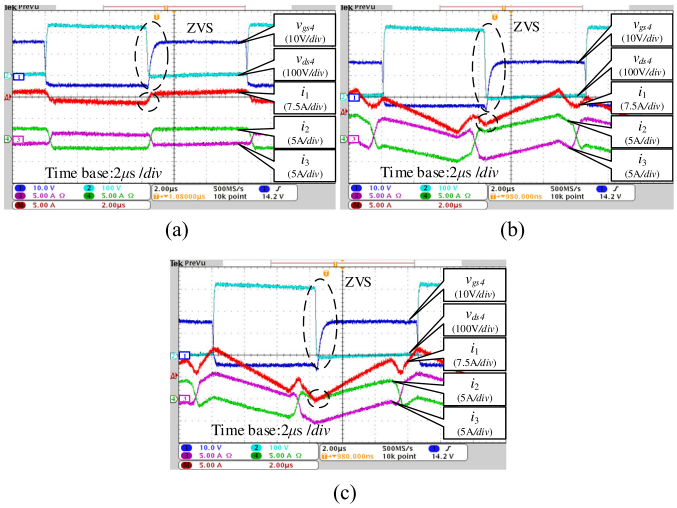

Fig. 23. Gate signal and drain–source voltage of switch Q_4. (a) $V_{\text{bat}} = 200$ V, $P_o = 300$ W. (b) $V_{\text{bat}} = 300$ V, $P_o = 300$ W. (c) $V_{\text{bat}} = 300$ V, $P_o = -300$ W.

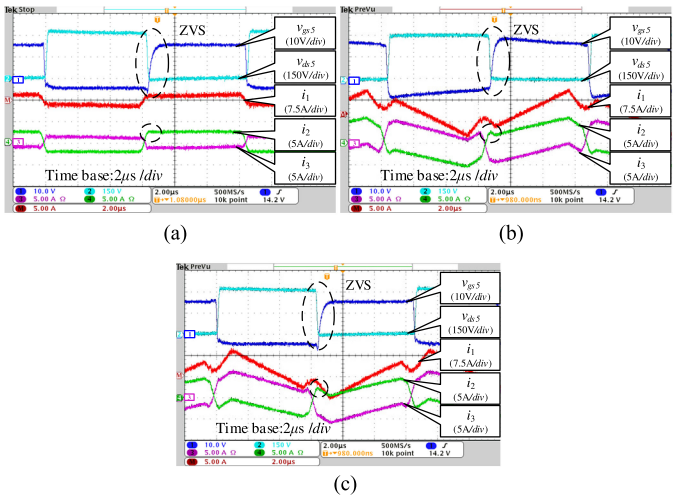

Fig. 24. Gate signal and drain–source voltage of switch Q_5. (a) $V_{\text{bat}} = 200$ V, $P_o = 300$ W. (b) $V_{\text{bat}} = 300$ V, $P_o = 300$ W. (c) $V_{\text{bat}} = 300$ V, $P_o = -300$ W.

ZVS for both forward and reversed power flow. Q_2 works in the same mode with Q_1, so it can also achieve ZVS.

Fig. 23 shows the gate signal and drain–source voltage of switch Q_4. i_1 is still less than zero during the commutation interval of Q_4. It also illustrates that Q_4 can achieve ZVS. Q_3 works in the same modes with Q_4, which demonstrates that Q_3 can also achieve ZVS.

Fig. 24 shows the gate signal and drain–source voltage of switch Q_5. As seen in different working modes, before Q_5 is turned ON, i_2 is large enough to charge and discharge the junction capacitors of Q_6 and Q_5. Q_5 can work in ZVS in both forward and reverse power flow. Q_6, Q_9, and Q_{10} operate in the same ZVS constraint as Q_5, so they are also easy to achieve ZVS.

Fig. 25 shows the gate signal and drain–source voltage of switch Q_8. As seen during the dead time interval of Q_8, i_3 is large enough to charge and discharge the junction capacitors of Q_7 and Q_8. It validates the ZVS performance for Q_8 in both

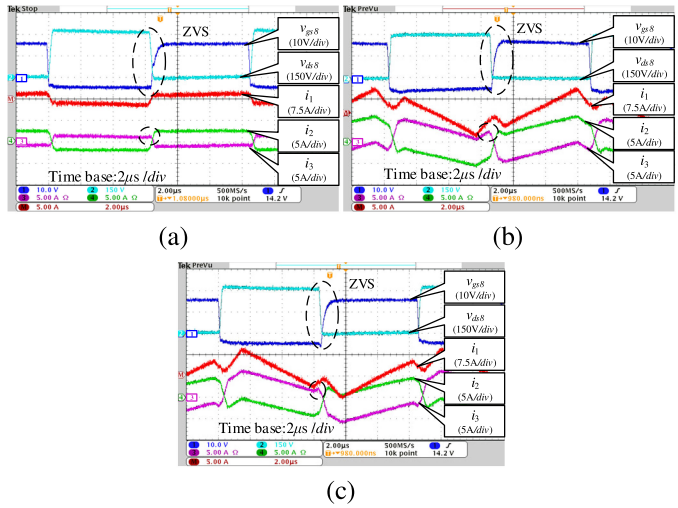

Fig. 25. Gate signal and drain–source voltage of switch Q_8. (a) $V_{\text{bat}} = 200$ V, $P_o = 300$ W. (b) $V_{\text{bat}} = 300$ V, $P_o = 300$ W. (c) $V_{\text{bat}} = 300$ V, $P_o = -300$ W.

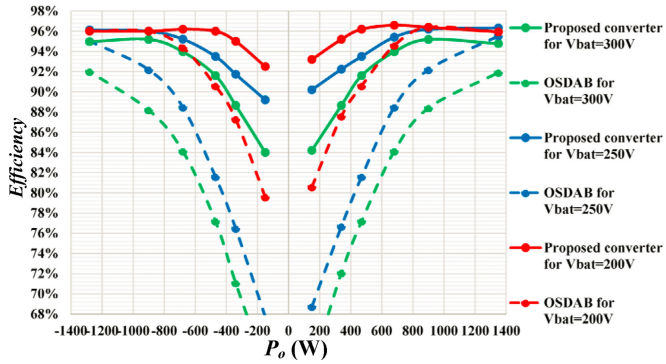

Fig. 26. Efficiency curves for the proposed converter and OSDAB.

forward and reverse power flow. Q_7, Q_{11}, and Q_{12} operate in the same working mode as Q_8, so they can also achieve ZVS.

The measured efficiency curves for the proposed converter and OSDAB converter (shown in Fig. 2) are shown in Fig. 26. When the battery voltage is 200 V, the OSDAB can achieve ZVS in heavy load even without auxiliary *LC* networks. Therefore, at 200 V battery voltage, the efficiency curves of the proposed converter and OSDAB converter coincide in heavy load. In all the working modes, the proposed converter can achieve ZVS, so the efficiency of the proposed converter is greatly improved compared with the OSDAB converter. Especially at the 300 V battery voltage and a 1350 W load, an efficiency improvement of more than 2% is achieved.

The calculated loss distribution in 1.3 kW output power is shown in Fig. 27. In 200 V battery voltage, the current amplitude is lower than 250 and 300 V battery voltage, so series inductor core loss is lower than that in 250 and 300 V battery voltage. The calculated RMS in the series inductor versus the battery voltage in the rated load is shown in Fig. 28. The RMS current in 250 V battery voltage is lower than that in 200 and 300 V battery voltages, so the copper loss in the series inductor and transformer is lower than that in 200 and 300 V battery voltage.

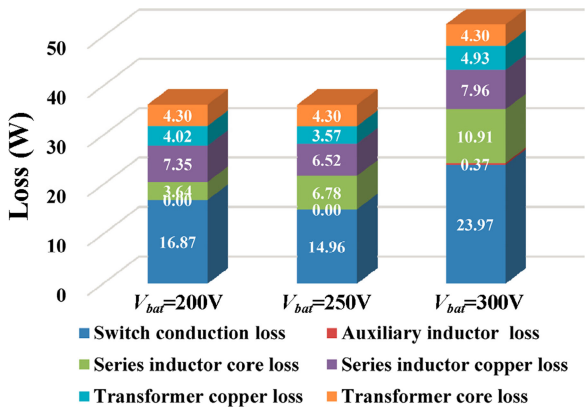

Fig. 27. Loss breakdown in 1.3 kW output power.

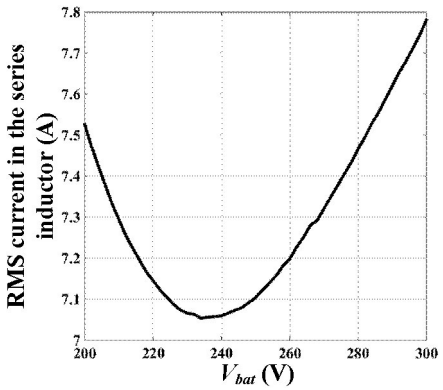

Fig. 28. RMS current in the series inductor versus the battery voltage in 1.3 kW.

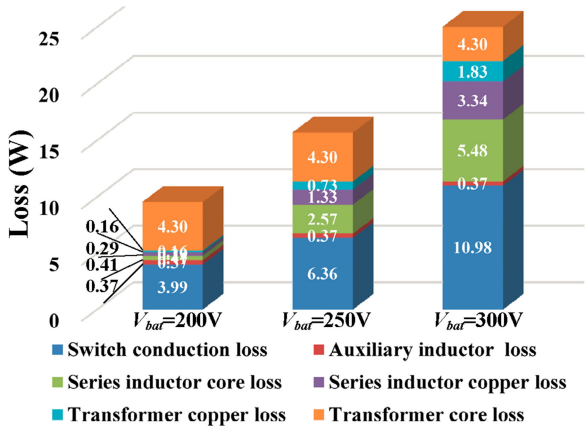

Fig. 29. Loss breakdown in 200 W output power.

In 200 and 250 V, the converter can achieve ZVS for all the switches even without *LC* networks. Therefore, the loss caused by *LC* networks is almost zero. In 300 V battery voltage, all the switches can achieve ZVS with *LC* networks. The loss caused by *LC* networks is very low. Because of the ZVS of all the switching, the switching loss can be ignored, and the efficiency is dramatically improved.

Fig. 29 shows the calculated loss distribution in 300 W output power. When the battery voltage is 200 V, the peak current and RMS current in the transformers are very low. Therefore, the conduction loss and core loss are very low. With the increase of the battery voltage, the peak current and RMS current in the transformers are increased. The conduction loss and core loss are increased simultaneously.

V. Conclusion

This paper presents an output-series dual active bridge converter with dual auxiliary *LC* networks. This converter can meet the high output dc-link voltage requirement. The two auxiliary *LC* networks are connected with the bridge legs of the two output full bridges. With the aid of the dual auxiliary *LC* networks, the converter can achieve ZVS performance of the output full bridges over full load range and wide battery voltage range. The ZVS boundaries of all the switches have been analyzed, and the modulation trajectory is designed according to the ZVS boundaries. The flowchart of the modulation trajectory can guarantee seamless transition between the adjacent working modes. Therefore, the converter can achieve ZVS with low conduction loss. Although the conduction loss in the proposed converter is a little bit greater than the conventional OSDAB converter, the proposed converter has a good tradeoff between the ZVS performance and the conduction loss in auxiliary circuit. Finally, the experimental results validate the ZVS performance in the proposed converter. The efficiency curves demonstrate the efficiency improvement in the OSDAB with dual *LC* networks.

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