Investigation of a Non-isolated Reduced Redundant Power Processing DC/DC Converter for High-Power High Step-Up Applications

Charoula G. Zogogianni, Emmanuel C. Tatakis, and Vlado Porobic

***Abstract*—In this paper, a nonisolated high step-up dc/dc converter, belonging to the family of reduced redundant power processing converters (R2P2), is investigated for high-power applications. The selection of this topology as the most suitable for such applications among those belonging to the R2P2 family is justified. Emphasis is given on the theoretical analysis of the real step-up voltage ratio of the converter, and voltage and current stresses under continuous and discontinuous conduction modes of operation, taking into account the nonideality of the topology components, namely the parasitic resistances of semiconductor devices and inductors and the voltage drop of diodes. The theoretical analysis and the behavior of the selected converter are experimentally validated through a 2 kW prototype. Moreover, the overall efficiency of the chosen converter is experimentally investigated for various step-up voltage ratios and for a high-power range, considering a waste heat recovery system for a maritime application.**

***Index Terms*—DC–dc power conversion, high power applications, high step-up voltage ratio, reduced redundant power processing converters, switched mode power supplies.**

I. Introduction

IN RECENT years, dc/dc converters have gained increased popularity, since they are employed in various applications, such as industrial applications, automotive industry, electric vehicles, renewable energy systems, etc., [1]–[4]. Particularly, systems that include renewable sources (photovoltaics, wind turbines, etc.), as well as fuel cells and thermoelectric generators (TEGs), require converters with wide voltage conversion ratios, high power density and improved efficiency. To satisfy these requirements, several voltage step-up dc/dc converters have been proposed in literature [5]–[12].

Manuscript received April 11, 2018; revised July 1, 2018; accepted August 9, 2018. Date of publication August 30, 2018; date of current version April 20, 2019. This work was supported by the State Scholarships Foundation (IKY) funded by the Action "Scholarship Program for postgraduate studies of second cycle" within the OP "Human Resources Development, Education and Lifelong Learning", 2014-2020, co-funded by the European Social Fund (ESF) and Greek State. Recommended for publication by Associate Editor C. K. Tse. *(Corresponding author: Charoula Georgios Zogogianni.)*

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Taking all the aforementioned facts into account, our study is focused on the nonisolated reduced redundant power processing (R2P2) topologies that offer simpler design and so higher reliability. The basic idea of this family of converters is to produce noncascaded configurations, employing a three-port network (input port, output port, and energy storage element) and elementary converters (e.g., Bk, Bt, BB, Flyback, etc.), that can lead to high step-up voltage ratios avoiding the double power processing. Hence, all R2P2 configurations have better efficiency than the cascaded one (referred as Configuration I-I in literature) and this is proven both theoretically and experimentally in [27], [28]. Thus, this family seems promising for high-power and high voltage gain applications, and it is chosen here for further investigation.

Initially, R2P2 converters were presented and reported for power factor correction (PFC) applications [27]–[32]. In ac/dc applications, the energy storage element is required for power balancing due to the difference between the instantaneous ac input power and dc output power. In [27]–[29] the general concept of R2P2 is analyzed, while in [30]–[34] specific applications of R2P2 PFC are presented, employing different combinations of elementary converters. For example, the R2P2 I-IIIB configuration is employed both in [33], including a single-ended primary-inductor converter (SEPIC) and a BB converter for LED applications, as well as in [34], consisting of a three-phase rectifier and a BB converter. Most of the papers related to this subject, present isolated topologies based on the R2P2 principle. However, the experimental results are of some hundreds of watts or, in some cases, up to 1 kW [31], [32], with efficiencies of up to 90%, emphasizing mostly the functionality of the converter and the total harmonic distortion of the input current.

Nevertheless, this family of converters can be also employed towards the development of new topologies of dc/dc converters for high step-up applications [35]–[37]. In dc/dc applications, the energy storage element, e.g., capacitor in R2P2 concept, does not serve for power balancing between the input and output of the converter, but it is acting as a buffer for the instantaneous power balancing between the two internal elementary converters A and B. Therefore, the R2P2 concept can be applied in dc/dc applications in order to avoid redundant power processing and so increase the overall efficiency.

Palomo and Morales were the first to employ the R2P2 principle to produce single-input single-output (SISO) dc/dc converters [35], focusing on topologies that can be transformed in single-switch equivalent topologies. Nevertheless, the experiments were up to 100 W and the step-up voltage ratio up to 7. In addition to this, in [38] it is proven that single-switch R2P2 topologies are not necessarily more efficient, since the conduction losses in the switch are increased dramatically, leading to efficiency degradation. In [36], the R2P2 principle and the appropriate power flow graphs are employed to synthesize double-input single-output converters, so the three-port network consists of two input sources and load instead of input port, energy storage element and output port that is employed for SISO converters. This modified network produces different possible configurations compared to SISO ones, dedicated for applications with two different types of renewable energy sources. Their systematic study is out of the scope of the work presented in this paper.

In this paper, a nonisolated SISO R2P2 topology, namely I-IIB BB/Bt, is selected as the most suitable among the R2P2 converters, comparing their voltage gain and efficiencies, to be employed as a highly efficient high step-up dc/dc converter for high-power applications (up to 2 kW). Since the chosen converter is desired to operate at high power, emphasis is given in the analysis of converter, taking into account the nonidealities of the topology components in all operational modes, namely continuous and discontinuous conduction mode (CCM and DCM, respectively) in order to estimate their effect on the real step-up voltage ratio and the stresses in semiconductor devices. Experiments are conducted employing a prototype designed to handle a power up to 2 kW to prove the high efficiency of the converter, operating at high power and with high step-up voltage ratio, as well as to validate the theoretical analysis. To increase further the efficiency of the proposed converter, silicon carbide (SiC) semiconductor devices are employed.

This paper is organized as follows. In Section II, an analysis of the R2P2 family for nonisolated SISO configurations is presented and the choice of the converter under investigation is justified. In Section III, the operation, as well as the analysis of voltage gain and voltage and current stresses of the proposed step-up converter, is presented, considering ideal elements. Analysis of the voltage gain and stresses of the converter, considering nonideal components, is presented in Section IV, for both operational modes, namely CCM and DCM. Experimental results are shown and compared with theoretical ones in Section V to prove the validity of the analysis and to show the high efficiency of the converter. Finally, conclusions are discussed in Section VI.

II. Selection of a Non-isolated R2P2 Converter

Each SISO R2P2 configuration consists of a three-port network, namely input port, output port, and energy storage element, e.g., capacitor, and two basic converters A and B, placed in different power flow paths, as shown in [27], [39]. For a complete overview and easy comparison, the voltage gain *M* and the efficiency η were calculated and tabulated in Table I, for each of the 16 nonisolated R2P2 configurations, as a function of the voltage ratios and efficiencies of the individual basic converters ($M_A, M_B, \eta_A,$ and η_B, respectively). Due to cumbersome calculations, we don't include further details on these calculations, as this is not the scope of this paper.

First, the configurations IIA-IIIA, IIB-IIIB, IIC-IIIC cannot be implemented in reality for nonisolated topologies because short circuits (SC) are created, specifically,

1) IIA-IIIA: SC of input voltage or capacitor;
2) IIB-IIIB: SC of output voltage or capacitor;
3) IIC-IIIC: SC of Converter B input or Converter A output.

Therefore, despite the fact that 16 possible R2P2 configurations are reported in literature, in the case of nonisolated SISO topologies, 13 can be implemented in reality and so, the efficiency and the voltage gain for the rest three configurations are not shown in Table I.

TABLE I
VOLTAGE GAIN AND EFFICIENCY FOR THE 16 NON-ISOLATED R2P2 CONFIGURATIONS

Configuration	Voltage ratio M	Efficiency η	Configuration	Voltage ratio M	Efficiency η
I-I	$M_A M_B$	$\eta_A \eta_B$	IIA-IIIB	$\frac{M_A(1+M_B)}{M_A+1}$	$\eta_B \frac{(M_A+\eta_A)(M_B+1)}{(M_A+1)(M_B+\eta_B)}$
I-IIA	$M_B(1+M_A)$	$\eta_A \eta_B \frac{M_A+1}{M_A+\eta_A}$	IIA-IIIC	$\frac{M_A(1+M_B)}{M_A M_B+1}$	$\frac{(M_A M_B+\eta_A \eta_B)(M_B+1)}{(M_A M_B+1)(M_B+\eta_B)}$
I-IIB	M_A+M_B	$\eta_A \eta_B \frac{M_A+M_B}{M_A \eta_B+M_B \eta_A}$	IIB-IIIA	$\frac{M_B(1+M_A)}{M_B+1}$	$\frac{\eta_A(M_A+1)(M_B+\eta_B)}{(M_A+\eta_A)(M_B+1)}$
I-IIC	$M_A M_B+1$	$\eta_A \eta_B \frac{M_A M_B+1}{M_A M_B+\eta_A \eta_B}$	IIB-IIIB	-	-
I-IIIA	$\frac{M_A M_B}{M_A+M_B}$	$\frac{M_A \eta_B+M_B \eta_A}{M_A+M_B}$	IIB-IIIC	$\frac{M_A+M_B}{M_B+1}$	$\frac{\eta_A(M_A+M_B)(M_B+\eta_B)}{(M_B+1)(M_A \eta_B+M_B \eta_A)}$
I-IIIB	$\frac{M_A M_B}{M_A+1}$	$\eta_B \frac{M_A+\eta_A}{M_A+1}$	IIC-IIIA	$\frac{M_B(1+M_A)}{M_A+M_B}$	$\frac{(M_A+1)(M_A \eta_B+M_B \eta_A)}{(M_A+\eta_A)(M_A+M_B)}$
I-IIIC	$\frac{M_A M_B}{M_A M_B+1}$	$\frac{M_A M_B+\eta_A \eta_B}{M_A M_B+1}$	IIC-IIIB	$\frac{M_A M_B+1}{M_A+1}$	$\frac{\eta_B(M_A+\eta_A)(M_A M_B+1)}{(M_A+1)(M_A M_B+\eta_A \eta_B)}$
IIA-IIIA	-	-	IIC-IIIC	-	-

Observing carefully Table I, it is concluded that configurations I-IIIC, IIA-IIIC, and IIB-IIIC result always in voltage step-down topologies, considering Bk, Bt or BB as possible topologies for individual converters A and B. Moreover, the configurations I-IIIA, I-IIIB, and IIC-IIIB result in voltage gain M lower than M_A or M_B and the configurations IIA-IIIB, IIB-IIIA, and IIC-IIIA result generally in low M. Therefore, these six configurations are not suitable for high step-up applications. Hence, we conclude that I-IIA, I-IIB, and I-IIC have the highest voltage gain among all. From these three configurations though, I-IIB has the highest efficiency (see Appendix), so this is chosen in the present paper for further investigation.

Considering the basic nonisolated dc/dc converters Bk, Bt, and BB as potential candidates for A and/or B and employing them for the I-IIB configuration, we conclude that there are only four possible nonisolated topologies, namely (a) Bk/BB, (b) Bt/BB, (c) BB/Bk, and (d) BB/Bt, as shown in Fig. 1.

The topologies (a), (c) and (b), (d), respectively, are equivalent as far as the functionality is concerned. However, the topologies (a), (c) result in lower M compared to (b), (d), since a Bk converter is included, and M is derived from the sum of M_A and M_B. Therefore, topologies (a) and (c) are not suitable for high step-up applications.

Despite the fact that topologies (b), (d) are equivalent, in Bt/BB case, the voltage stress of the capacitor V_C is bigger $(V_C = V_O + V_{\text{in}})$ compared to BB/Bt case $(V_C = V_O - V_{\text{in}})$, where V_{in} and V_O are the input and output voltages of the overall converter, respectively. Therefore, the topology R2P2 I-IIB BB/Bt is chosen to be further analyzed.

III. R2P2 I-IIB BB/Bt CONVERTER ANALYSIS CONSIDERING IDEAL ELEMENTS

The R2P2 I-IIB BB/Bt converter topology is redesigned in Fig. 2 for simplicity reasons. This converter seems to be somewhat similar to this presented in [40]. However, in reality, the absence of C_1 and D_2 in the proposed topology in [40] causes

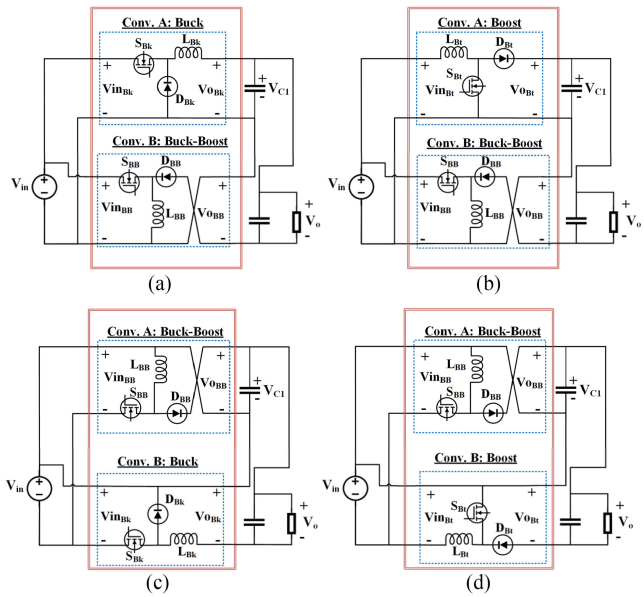


Fig. 1. Four possible non-isolated topologies for R2P2 I-IIB configuration.

oscillations and overvoltages [41], making it unsuitable for high-power applications.

For our analysis, the two inductors are of the same value for symmetrical functionality. Also, to have a simple driver circuit, we consider that the switches are turned ON simultaneously, with the same duty cycle.

When the switches S_1, S_2 are turned ON, the inductors L_1, L_2 are charged in parallel from the dc source. The energy demand from the load R_o is covered by the output capacitor C_o. When the switches are turned OFF, the two inductors are connected in series through the diodes D_1, D_2, releasing their energy to the load and the output capacitor.

Considering whether the inductors current is decreased to zero for a time interval or not, two operating modes can be defined: CCM and DCM for both inductors simultaneously, since during

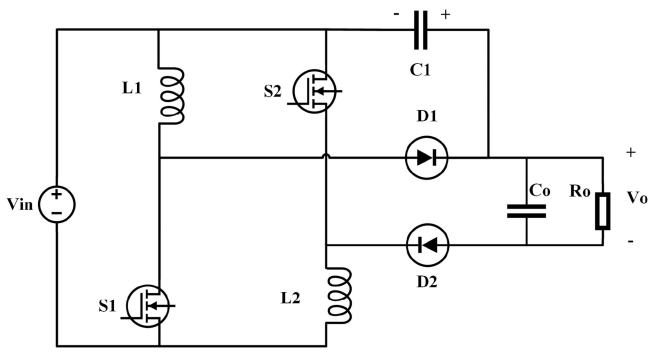


Fig. 2. R2P2 I-IIB BB/Bt converter under investigation.

TABLE II
VOLTAGE STRESSES OF R2P2 I-IIB BB/Bt CONVERTER UNDER IDEAL CONDITIONS IN CCM AND DCM

Voltage stresses	Transistors ON CCM & DCM	Transistors OFF ($I_L \neq 0$) CCM & DCM	Transistors OFF ($I_L = 0$) DCM only
V_{DS}	0	$(V_{in}+V_o)/2$	V_{in}
V_L	V_{in}	$(V_{in}-V_o)/2$	0
V_D	$-(V_{in}+V_o)/2$	0	$(V_{in}-V_o)/2$

OFF time they are connected in series through the diodes and they are forced to operate in the same mode. For the analysis that follows, it is considered that inductors are of the same value $(L_1 = L_2 = L)$ and both switches and diodes are identical to each other.

For a complete overview of the converter functionality, the voltage stresses on the transistors $V_{\mathrm{DS}_1} = V_{\mathrm{DS}_2} = V_{\mathrm{DS}}$, inductors $V_{L_1} = V_{L_2} = V_L$ and the output diodes $V_{D_1} = V_{D_2} = V_D$ are shown in Table II for CCM and DCM under ideal conditions. The output voltage V_o can be expressed as $V_{\mathrm{in}}\ V_{\mathrm{NO|CCM}}^{(\mathrm{ideal})}$ or $V_{\mathrm{in}}\ V_{\mathrm{NO|DCM}}^{(\mathrm{ideal})}$ where $V_{\mathrm{NO|CCM}}^{(\mathrm{ideal})}$ and $V_{\mathrm{NO|DCM}}^{(\mathrm{ideal})}$ is the ideal step-up voltage ratio of the converter in CCM and DCM accordingly.

Moreover, waveforms of the voltages and currents of the converter elements are depicted in Fig. 3(a) and (b) for CCM and DCM, respectively.

The analysis of the converter operation will be first performed considering ideal elements. Since voltage of capacitor C_1 is constant $(V_C = V_O - V_{\mathrm{in}})$, the capacitor does not affect the steady-state characteristics of the converter and according to authors' previous work [41], the following step-up voltage ratios V_{NO} can be achieved, depending on which mode, CCM or DCM, the converter is operating:

$$V_{\mathrm{NO|CCM}}^{(\mathrm{ideal})} = \frac{V_o}{V_{\mathrm{in}}} = M = M_A + M_B = \frac{d}{1-d} + \frac{1}{1-d}$$

$$\Rightarrow\ V_{\mathrm{NO|CCM}}^{(\mathrm{ideal})} = \frac{1+d}{1-d} \tag{1}$$

$$V_{\mathrm{NO|DCM}}^{(\mathrm{ideal})} = \frac{V_o}{V_{\mathrm{in}}} = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{(d^2 R_o)}{(L f_s)}} \tag{2}$$

where d is the duty cycle, I_o is the output current, $R_o = V_o/I_o$ is the output load, and f_s is the switching frequency.

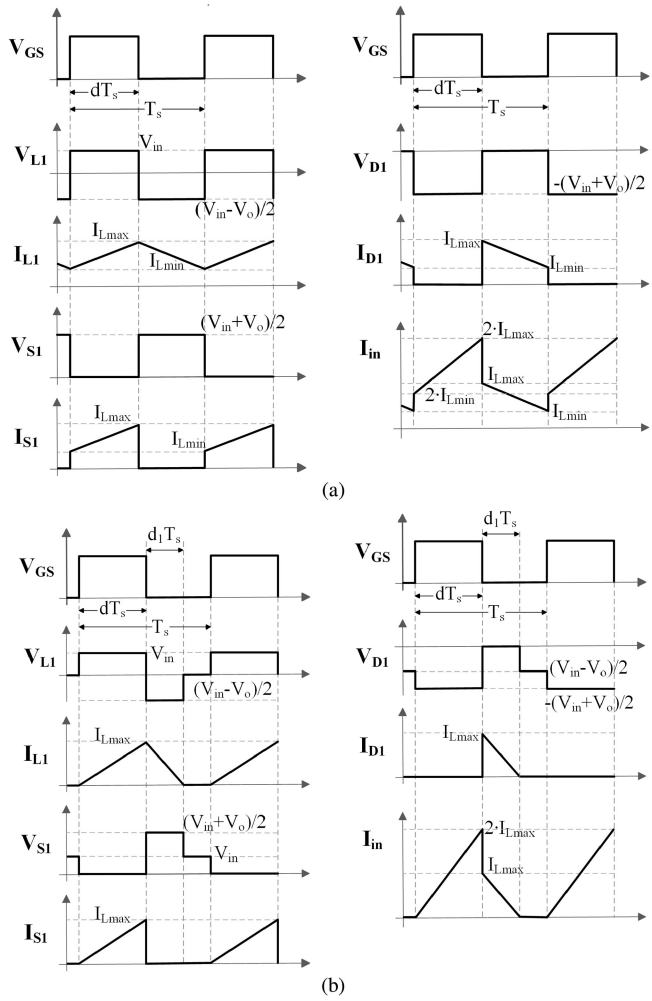


Fig. 3. Voltage and current waveforms of the converter operating in (a) CCM and (b) DCM. From top to bottom: pulses, voltage and current of L_1, voltage and current of S_1, pulses, voltage and current of D_1, input current.

Also, for DCM, the output boundary current I_{ob} is expressed as an equation of the maximum value of the inductors current $I_{L,\max}$

$$I_{ob} = \frac{I_{L,\max}}{2}(1-d) = \frac{V_{\mathrm{in}} d\,(1-d)}{2Lf_s} = \frac{V_o d(1-d)^2}{2\,(1+d)\,Lf_s}. \tag{3}$$

The normalized output current of the converter is defined as the ratio between I_o and the maximum value of the output boundary current $I_{ob|\max}$ and is denoted as $I_{\mathrm{NO},o}$ or $I_{\mathrm{NO},i}$, whether V_o or V_{in} is considered constant accordingly.

$$I_{\mathrm{NO},o} = \frac{I_o}{I_{ob|\max}} = \frac{I_o}{0.0567 \cdot V_o/(f_s \cdot L)}\ ,\ V_o = \mathrm{const.} \tag{4}$$

$$I_{\mathrm{NO},i} = \frac{I_o}{I_{ob|\max}} = \frac{I_o}{V_{\mathrm{in}}/(8 \cdot f_s \cdot L)}\ , V_{\mathrm{in}} = \mathrm{const.} \tag{5}$$

Taking (5) into account, the step-up voltage ratio for DCM, while V_{in} is constant, can be written as follows:

$$V_{\mathrm{NO|DCM}}^{(\mathrm{ideal})} = \frac{V_o}{V_{\mathrm{in}}} = \frac{d^2 + (I_{\mathrm{NO},i}/8)}{(I_{\mathrm{NO},i}/8)}. \tag{6}$$

TABLE III
CURRENT STRESSES OF R2P2 I-IIB BB/Bt CONVERTER

Current stresses	CCM	DCM
$I_{sw,rms}$	$\frac{V_{in}}{2}\sqrt{d}\cdot\sqrt{\left(\frac{I_o}{1-d}\right)^2+\frac{1}{12}\left(\frac{V_{in}d}{Lf_s}\right)^2}$	$\sqrt{\frac{d}{3}}\cdot\frac{V_{in}d}{Lf_s}$
$I_{L,avg}$	$\frac{I_o}{1-d}$	$\frac{V_{in}d}{2Lf_s}(d+d_1)$
$I_{D,avg}$	I_o	I_o

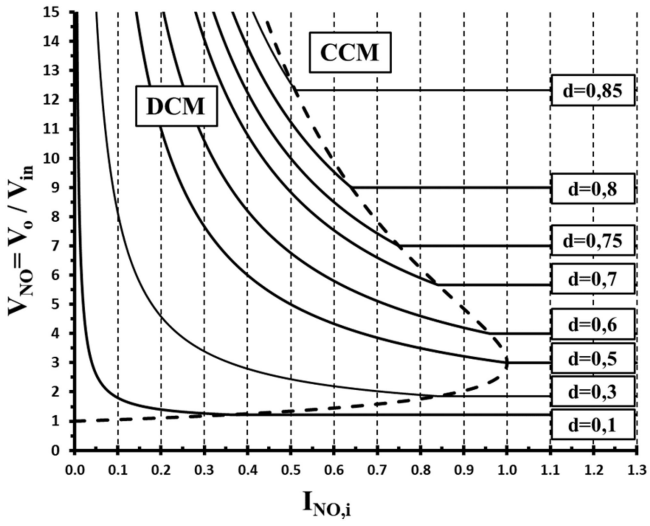


Fig. 4. Theoretical characteristic curves $V_{\rm NO} = f(I_{{\rm NO},i})$ for the converter with d as parameter, while $V_{\rm in}$ is constant.

Moreover, when the converter operates in DCM with constant V_o, duty cycle can be calculated as follows:

$$d = \frac{1}{2}\sqrt{0.0567\cdot I_{{\rm NO},o}\cdot\left[\left(\frac{2}{V_{\rm NO|DCM}^{(\rm ideal)}}-1\right)^2-1\right]}. \quad (7)$$

Moreover, the current stresses, namely the rms current in transistors $I_{sw,\rm rms}$, the average current in inductors $I_{L,\rm avg}$ and diodes $I_{D,\rm avg}$ are presented in Table III for CCM and DCM. The quantity d_1 denotes the duration that diode conducts in DCM and is equal to

$$d_1 = \frac{2V_oLf_s}{R_oV_{\rm in}d} = \frac{2V_{\rm NO|DCM}^{(\rm ideal)}\cdot Lf_s}{R_od}. \quad (8)$$

The output characteristic curves of the converter are presented in Fig. 4, based on (1), (6). It can be noticed that for a specific voltage gain, smaller duty cycle is needed for this converter, compared to the classical Bt one. In other words, with the same duty cycle for both converters, bigger voltage gain can be achieved with this converter, rather than with the traditional Bt. Moreover, the dependency of the duty cycle from $I_{{\rm NO},o}$ in both CCM and DCM for different values of $V_{\rm NO}$, is shown in Fig. 5.

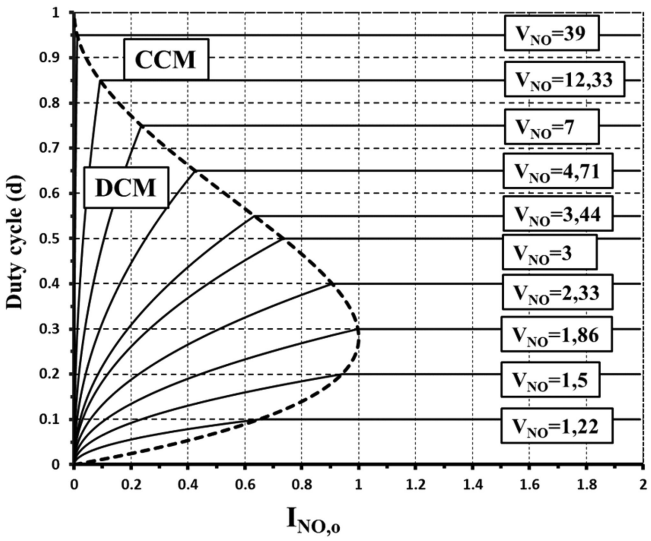


Fig. 5. Theoretical characteristic curves $d = f(I_{{\rm NO},o})$ for the converter with $V_{\rm NO}$ as parameter, while V_o is constant.

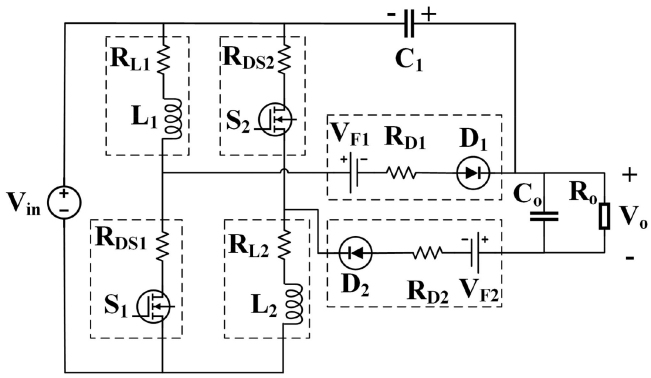


Fig. 6. Equivalent circuit of the converter for analysis with nonideal elements.

IV. R2P2 I-IIB BB/Bt CONVERTER ANALYSIS CONSIDERING NONIDEAL ELEMENTS

A. Continuous Conduction Mode

The effect of nonideal components on the step-up voltage ratio in CCM will be analyzed in this section. The equivalent circuit model of the step-up converter with parasitic elements is depicted in Fig. 6. Parasitic resistances of switches $R_{{\rm DS}_x}$ and inductors R_{L_x} are taken into account, as well as diodes forward voltages V_{F_x} and resistances R_{D_x}, with $x = 1, 2$ denoting the different elements of the converter. Due to the symmetrical nature of the circuit, it is assumed that $R_{{\rm DS}_1} = R_{{\rm DS}_2} = R_{\rm DS,on}$, $R_{L_1} = R_{L_2} = R_L$, $R_{D_1} = R_{D_2} = R_D$, and $V_{F_1} = V_{F_2} = V_F$.

The equivalent circuits when the transistors are ON and OFF are shown in Fig. 7. The capacitor C_1 does not affect the steady state characteristics of the converter, so it is omitted from this analysis.

Because of the parasitic resistances of the converter elements, the currents flowing through these elements will not have triangular shape (such as in Fig. 3), but exponential, depending on the R-L circuits shown in Fig. 6. However, since in reality

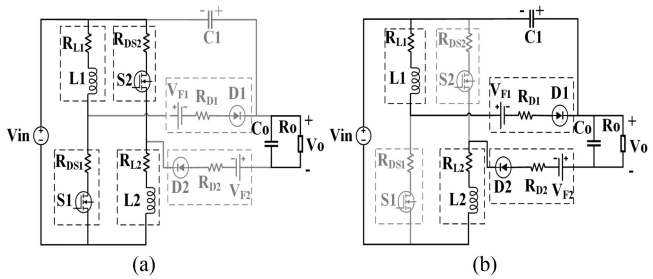


Fig. 7. Equivalent circuit of the converter when transistors are (a) ON (first state) and (b) OFF (second state).

the parasitic resistances are of small value, linear approximation has been assumed in order to calculate converter currents.

Based on the circuits presented in Fig. 7, the voltage across inductor L_1 for the first and second state ($u_{L_1}^{(0-dT_s)}$ and $u_{L_1}^{(dT_s-T_s)}$, respectively) can be written accordingly as follows:

$$u_{L_1}^{(0-dT_s)} = V_{\text{in}} - i_{sw}(t)\cdot(R_L + R_{\text{DS,on}}) \tag{9}$$

$$u_{L_1}^{(dT_s-T_s)} = \frac{V_{\text{in}} - i_D(t)\cdot(2R_D + 2R_L) - (V_o + 2V_F)}{2} \tag{10}$$

where the switch and diode currents are denoted as i_{sw} and i_D, respectively, and $T_s = 1/f_s$ is the switching period.

Since steady-state is assumed, volt-second balance for inductor L_1 can be applied as follows:

$$\frac{1}{T_s}\left[\int_0^{dT_s} u_{L_1}^{(0-dT_s)}dt + \int_{dT_s}^{T_s} u_{L_1}^{(dT_s-T_s)}dt\right] = 0. \tag{11}$$

Substituting (9) and (10) in (11), it is obtained as follows:

$$V_{\text{in}}\cdot d - (R_L + R_{\text{DS,on}})\cdot I_{sw,\text{avg}} + \frac{V_{\text{in}} - (V_o + 2V_F)}{2} \cdot (1-d) - (R_D + R_L)\cdot I_{D,\text{avg}} = 0. \tag{12}$$

In order to calculate the voltage ratio M, (12) dictates the evaluation of the average value of the switch and diode currents, $I_{sw,\text{avg}}$ and $I_{D,\text{avg}}$, respectively. Therefore, taking into account the waveforms of the currents in Fig. 3 and above-mentioned assumptions, it can be written

$$I_{sw,\text{avg}} \cong \frac{I_{L,\min}^{\text{CCM}} + I_{L,\max}^{\text{CCM}}}{2}\cdot d \tag{13}$$

$$I_{D,\text{avg}} \cong \frac{I_{L,\min}^{\text{CCM}} + I_{L,\max}^{\text{CCM}}}{2}\cdot (1-d) \tag{14}$$

where $I_{L,\min}^{\text{CCM}}$ and $I_{L,\max}^{\text{CCM}}$ are the minimum and maximum value of inductor current, respectively, in CCM. Moreover

$$I_{D,\text{avg}} = I_o = \frac{V_o}{R_o}, \tag{15}$$

since the average value of the current flowing through the output capacitor C_o is zero because of the steady-state consideration. Consequently

$$I_{L,\min}^{\text{CCM}} + I_{L,\max}^{\text{CCM}} \cong \frac{2I_o}{1-d} \Rightarrow I_{sw,\text{avg}} \cong I_o\cdot\frac{d}{1-d}. \tag{16}$$

TABLE IV
OPERATING CONDITIONS OF THE PROTOTYPE OF THE CONVERTER FOR CCM

V_{in} (V)	R_o (Ω)	L_1=L_2 (mH)	f_s (kHz)
50	150	1	50

TABLE V
PARASITIC ELEMENTS OF THE PROTOTYPE OF THE CONVERTER

$R_{DS,on}$ (Ω)	R_D (Ω)	V_F (V)	R_L (Ω)
0,16	0,3	1,5	0,25

Substituting (15), (16) in (12) and after some mathematical manipulations, (17) is extracted, where the real voltage ratio between output and input voltage of the converter operating in CCM is denoted as $V_{\text{NO|CCM}}^{(\text{real})}$

$$V_{\text{NO|CCM}}^{(\text{real})} = \frac{V_O}{V_{\text{in}}} = \frac{1+d}{1-d}\cdot\left[1 - \frac{2V_F(1-d)}{V_{\text{in}}(1+d)}\right] \cdot\left[\frac{1}{1 + \frac{2(R_D+R_L)}{R_O(1-d)} + \frac{2d(R_{\text{DS,on}}+R_L)}{R_O(1-d)^2}}\right]. \tag{17}$$

Taking into account (1), the relation (17) can be rewritten into (18), with the intention to emphasize the effect of parasitic elements on the ideal voltage ratio

$$V_{\text{NO|CCM}}^{(\text{real})} = V_{\text{NO|CCM}}^{(\text{ideal})}\cdot\left[1 - \frac{2V_F(1-d)}{V_{\text{in}}(1+d)}\right] \cdot\left[\frac{1}{1 + \frac{2R_D}{R_O(1-d)} + \frac{2dR_{\text{DS,on}}}{R_O(1-d)^2} + \frac{2R_L}{R_O(1-d)^2}}\right]. \tag{18}$$

In order to clearly show the effect of each parasitic element on the voltage gain, different graphs are presented hereafter, varying each one of the parasitic elements, while eliminating the others (zero value). All the following graphs are produced, assuming that the converter is operating under the conditions and values shown in Tables IV and V. These values are the real values of the converter prototype, which will be presented in Section V, and are used for the following graphs, in order to have a real evaluation of the converter behavior.

The effect on V_{NO} as a function of duty cycle d for different values of parameter $R_{\text{DS,on}}$ is presented in Fig. 8. It is obvious that the difference between ideal and real voltage ratio becomes significant after $d = 0,7$. This is expected, since after $d = 0.7$, the conduction time of transistors becomes high enough and therefore conduction losses play an important role. It can be noticed that the bigger the $R_{\text{DS,on}}$, the bigger the relative difference between the ideal and real step-up voltage ratio is. For example, if $R_{\text{DS,on}}$ is three times its nominal value, while $d = 0.75$, the loss in voltage gain is up to 7.1%. This must be taken into account, while designing the converter and integrate it in a system. For instance, knowing the real step-up voltage ratio of the converter, the designer is able to predict how many

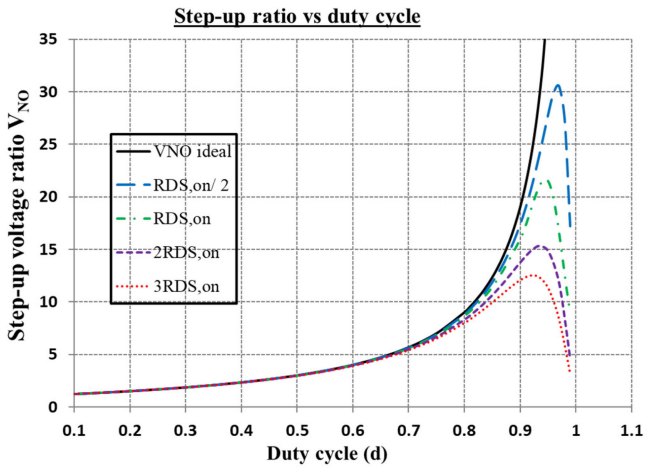


Fig. 8. Ideal and real voltage gain in CCM in absolute values, as a function of the duty cycle d, having $R_{\mathrm{DS,on}}$ as parameter.

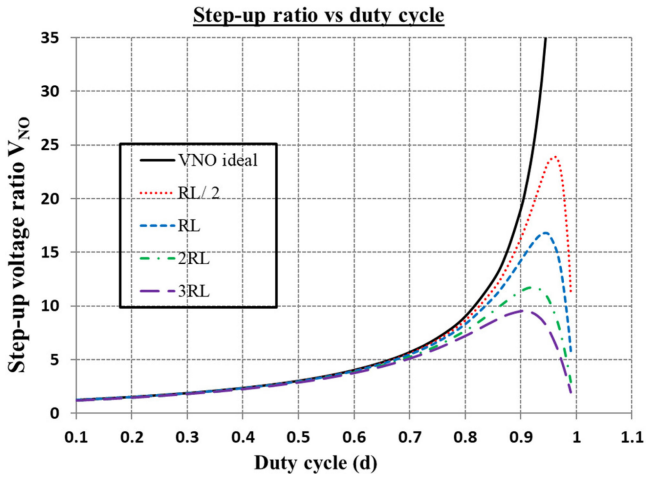


Fig. 10. Ideal and real voltage gain in absolute values as a function of duty cycle for several values of parameter R_L.

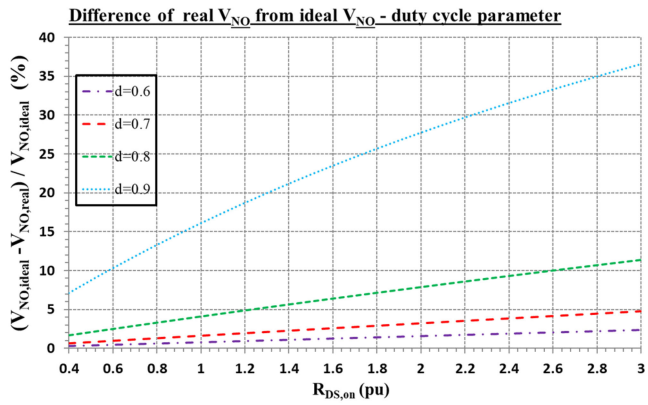


Fig. 9. Relative difference of the ideal and real voltage gain in CCM as a function of $R_{\mathrm{DS,on}}$ for different duty ratios d.

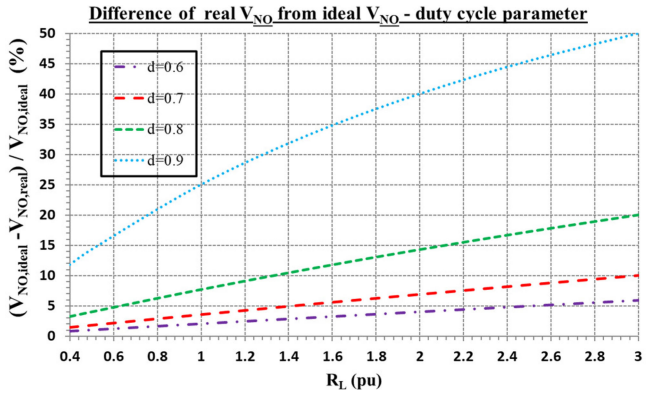


Fig. 11. Relative difference of the ideal and real voltage gain as a function of R_L for different duty cycles d.

TEGs (or other renewable sources) must be connected in series in order to achieve required values of the output voltage.

In Fig. 9, the voltage gain as a function of $R_{\mathrm{DS,on}}$ for several duty cycles is presented. It is obvious that the voltage gain is significantly affected, particularly for high duty ratios. Doubling the $R_{\mathrm{DS,on}}$ value, e.g., from 1 to 2 p.u., will almost double the percentage loss, if the converter is operating with $d = 0.8$.

In a similar way, diagrams for all other parasitic elements can be obtained. Figs. 10 and 11 show the effect of R_L variation on the voltage gain, while the effect of R_D and V_F are shown in Fig. 12(a) and (b), respectively. It is worth noticing that the diodes resistance and their voltage drop don't have significant effect in voltage gain loss, compared to the effects of $R_{\mathrm{DS,on}}$ and R_L. The voltage gain is the most sensitive to the change of R_L and then to $R_{\mathrm{DS,on}}$. This is logical, since the resistance of the inductors is present during the whole period of converter operation and also because its value is bigger than this of the transistor. Doubling the R_L value, e.g., from 1 to 2 p.u., will almost double the percentage loss, if the converter is operating with $d = 0.8$, like with the case of $R_{\mathrm{DS,on}}$, but the percentage loss is bigger in value (as shown in Fig. 11) compared with the case of $R_{\mathrm{DS,on}}$.

Comparing the previous results, one can conclude that to achieve high voltage gain, the most important is to choose inductors and transistors with as low resistance as possible, while designing the converter. For low $R_{\mathrm{DS,on}}$ and R_L, the temperature of the components must be also kept low. For the transistors, this can be achieved either with huge heatsinks or by using new semiconductor devices, like SiC, gallium nitride, etc. For this reason, in this paper, the transistors for the experimental prototype were chosen to be SiC MOSFETs.

B. Discontinuous Conduction Mode

Using the same equivalent circuits shown in Fig. 7, analysis of the voltage gain can be conducted, taking into account the nonideality of the converter elements, while operating in DCM. The difference here is that the time interval that diodes are conducting is not anymore $(1 - d)T_s$, but $d_1 T_s$. This time interval needs to be defined by the circuit equations, making the analysis more complicated and the equations more complex compared to CCM.

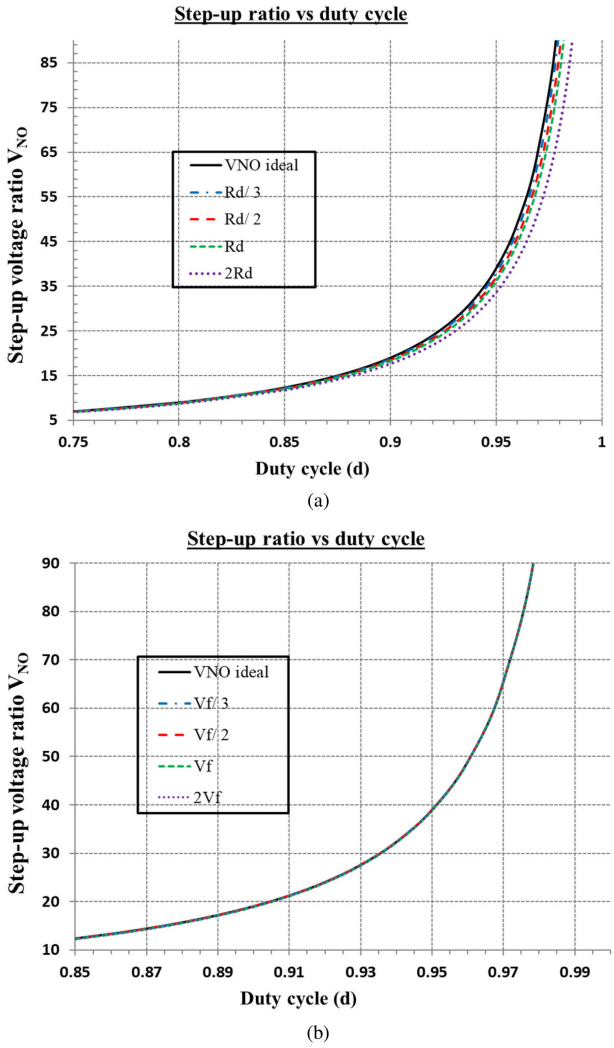


Fig. 12. Ideal and real voltage gain in absolute values as a function of duty cycle d for several values of a) R_D and b) V_F.

So, applying the volt-second balance to L_1 and using (9) and (10) for $d_1 T_s$, it can be deduced as follows:

$$V_{\text{in}} \cdot d - (R_L + R_{\text{DS,on}}) \cdot I_{sw,\text{avg}} + \frac{V_A}{2} \cdot d_1 - (R_D + R_L) \cdot I_{D,\text{avg}} = 0 \tag{19}$$

where

$$V_A = V_{\text{in}} - (V_o + 2V_F). \tag{20}$$

Again, in order to calculate the voltage gain, it is necessary to evaluate the average values of the transistor and diode currents, $I_{sw,\text{avg}}$ and $I_{D,\text{avg}}$, respectively, as well as the quantity d_1. Therefore, it can be written as follows:

$$I_{sw,\text{avg}} \cong \frac{I_{L,\max}^{\text{DCM}}}{2} \cdot d \Rightarrow I_{L,\max}^{\text{DCM}} \cong \frac{2I_{sw,\text{avg}}}{d} \tag{21}$$

$$I_{D,\text{avg}} \cong \frac{I_{L,\max}^{\text{DCM}}}{2} \cdot d_1 = I_o \Rightarrow d_1 \cong \frac{2I_o}{I_{L,\max}^{\text{DCM}}} \tag{22}$$

TABLE VI
OPERATING CONDITIONS OF THE PROTOTYPE OF THE CONVERTER FOR DCM

V_{in} (V)	R_o (Ω)	L_1=L_2 (mH)	f_s (kHz)
50	150	0,05	20

where $I_{L,\max}^{\text{DCM}}$ is the maximum value of inductor current in DCM (the minimum value $I_{L,\min}^{\text{DCM}}$ is of course zero). Furthermore, for the time interval $0 - dT_s$, using (9), it can be deduced as follows:

$$\frac{1}{T_s}\int_0^{dT_s} [V_{\text{in}} - i_{S1}(t) \cdot (R_L + R_{\text{DS,on}})]\, dt = \frac{L}{T_s}\int_0^{I_{L,\max}} di$$
$$\Rightarrow V_{\text{in}} \cdot d - (R_L + R_{\text{DS,on}}) \cdot I_{sw,\text{avg}} = L f_s \cdot I_{L,\max}^{\text{DCM}}. \tag{23}$$

Substituting (21) to (23), $I_{sw,\text{avg}}$ can be calculated as follows:

$$I_{sw,\text{avg}} = \frac{V_{\text{in}} \cdot d^2}{2Lf_s + d(R_L + R_{\text{DS,on}})}. \tag{24}$$

So, it can be concluded that

$$d_1 = \frac{V_o}{R_o \cdot V_{\text{in}} \cdot d} \cdot [2Lf_s + d(R_L + R_{\text{DS,on}})]. \tag{25}$$

Substituting (15) and (24) in (19), a 2-degree polynomial of V_{NO} is formed, where only the positive solution can be accepted, as presented the following:

$$V_{\text{NO|DCM}}^{(\text{real})} = \frac{1}{2}\left[1 + \lambda - \frac{2d(R_L + R_D)}{\rho} - \frac{2V_F}{V_{\text{in}}}\right] \tag{26}$$

where

$$\lambda = \sqrt{\frac{16Lf_s R_o d^2}{\rho^2} + \left[1 - \frac{2d(R_L + R_D)}{\rho} - \frac{2V_F}{V_{\text{in}}}\right]^2} \tag{27}$$

$$\rho = 2Lf_s + d(R_L + R_{\text{DS,on}}). \tag{28}$$

It can be easily observed that the equation of the voltage gain for DCM is more complex than this for CCM [see (18)].

In order to evaluate the effect of nonideal elements on the voltage ratio of DCM, different graphs are presented here, assuming that the converter is operating under the conditions described in Table VI. Note that now the inductor is 20 times smaller than the one used in CCM (see Table IV), so its resistance R_L is also assumed to be 20 times smaller $(R_L = 0,25/20)$. This value was on purpose selected to assure that the converter is operating in DCM under the whole range of the duty cycle. The other parasitic elements are the same with those presented in Table V.

Similar graphs like those presented in CCM, can be obtained here by varying one parameter, while eliminating the others. Figs. 13 and 14 show the effect of $R_{\text{DS,on}}$ on the voltage gain. Because R_L is very small, now the dominant role for the effect on the voltage gain plays the resistance $R_{\text{DS,on}}$. This is proven through Fig. 15, where one can notice the smaller effect of R_L on the voltage gain.

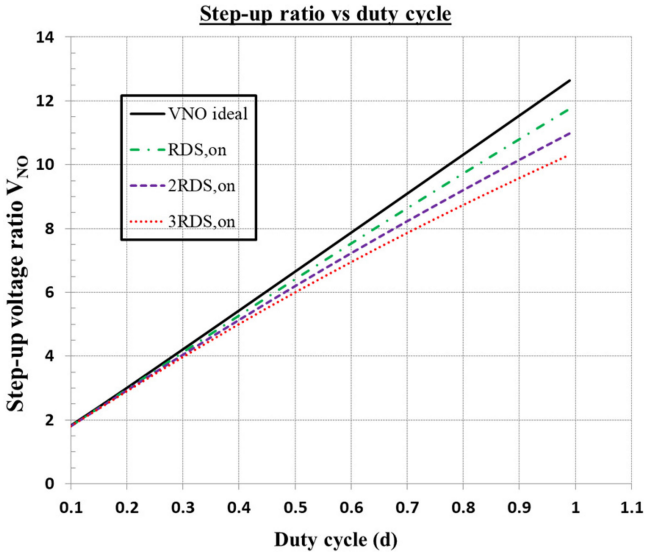


Fig. 13. Ideal and real voltage gain in absolute value as a function of the duty cycle for several values of $R_{\mathrm{DS,on}}$.

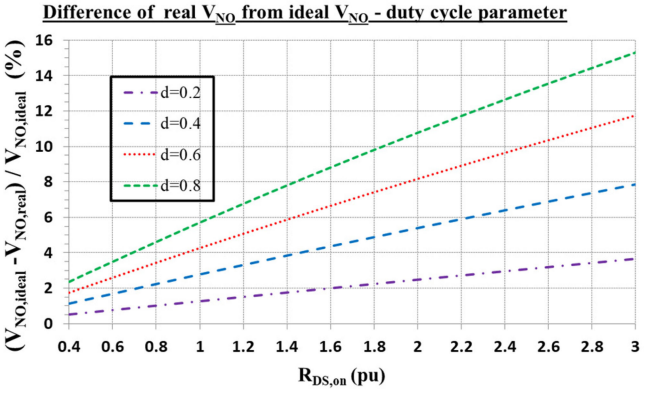


Fig. 14. Ideal and real voltage gain relative difference, as a function of $R_{\mathrm{DS,on}}$ for several values of duty cycle d.

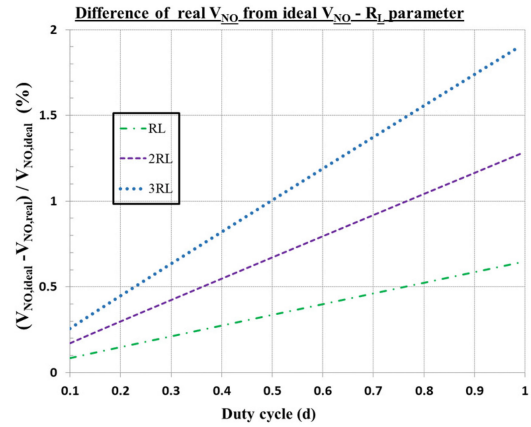
C. Voltage and Current Stresses Under Nonideal Conditions

The voltage stresses under nonideal conditions, when the converter is operating in CCM or DCM, are presented in Table VII, calculated with the use of the equivalent circuits presented in Fig. 7. As far as the current stresses is concerned, we consider these presented in Table III, since linear approximation has been adopted.

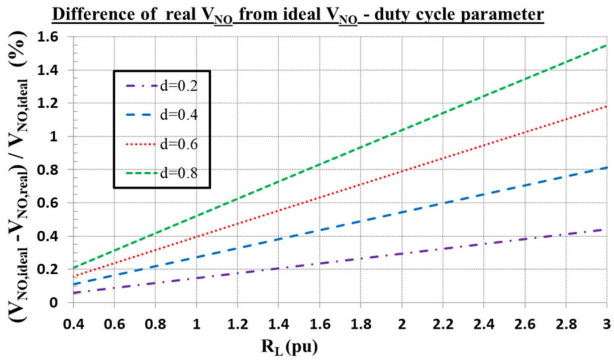
Practically, the equations describing the voltage stresses in DCM are the same with these in CCM (see Table VII), since the same equivalent circuits (see Fig. 7) are employed. However, the equations describing the voltage gain [see (18) and (26)] and extrema of inductor current [see (29)–(31)] in CCM and DCM differ, resulting in different values in voltage stresses.

The extrema of inductor current in CCM and DCM can be easily calculated as follows:

$$I_{L,\max}^{\mathrm{CCM}} = V_{\mathrm{in}} \left[\frac{V_{\mathrm{NO|CCM}}^{(\mathrm{real})}}{R_o\,(1-d)} + \frac{d}{2Lf_s} \right] \tag{29}$$



(a)



(b)

Fig. 15. Ideal and real voltage gain in their relative difference, as a function of a) duty cycle for several values of R_L and b) R_L for several values of duty cycle d.

TABLE VII
VOLTAGE STRESSES OF R2P2 I-IIB BB/Bt CONVERTER UNDER NON-IDEAL CONDITIONS IN CCM AND DCM

Voltage stress	CCM	DCM
V_{DS}	$\frac{V_{in}}{2}\left(V_{NO\|CCM}^{(real)}+1\right)$ $+R_D I_{L,max}^{CCM}+V_F$	$\frac{V_{in}}{2}\left(V_{NO\|DCM}^{(real)}+1\right)$ $+R_D I_{L,max}^{DCM}+V_F$
V_L	$-\frac{V_{in}}{2}\left(V_{NO\|CCM}^{(real)}-1\right)$ $-(R_L+R_D)I_{L,max}^{CCM}-V_F$	$-\frac{V_{in}}{2}\left(V_{NO\|DCM}^{(real)}-1\right)$ $-(R_L+R_D)I_{L,max}^{DCM}-V_F$
V_D	$-\frac{V_{in}}{2}\left(V_{NO\|CCM}^{(real)}+1\right)$ $+R_{DS,on}I_{L,min}^{CCM}$	$-\frac{V_{in}}{2}\left(V_{NO\|DCM}^{(real)}+1\right)$

$$I_{L,\min}^{\mathrm{CCM}} = V_{\mathrm{in}} \left[\frac{V_{\mathrm{NO|CCM}}^{(\mathrm{real})}}{R_o\,(1-d)} - \frac{d}{2Lf_s} \right] \tag{30}$$

$$I_{L,\max}^{\mathrm{DCM}} = \frac{V_{\mathrm{in}} d}{Lf_s} \tag{31}$$

while $I_{L,\min}^{\mathrm{DCM}}$ is equal to zero.

Observing Table VII, it is clear that the real voltage gain V_{NO} is playing the protagonist role in the effect on the voltage stresses. This means that the diagrams showing the relative

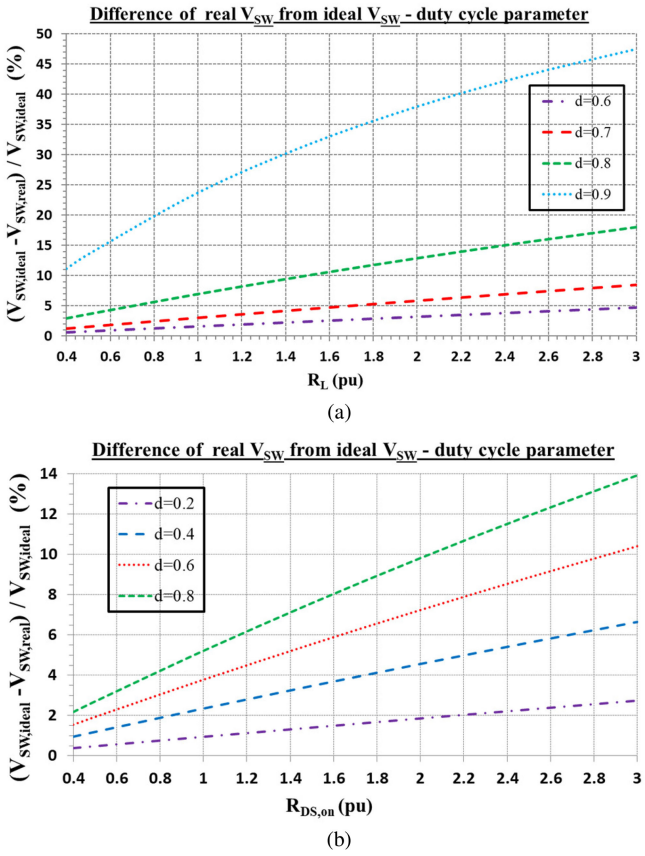


Fig. 16. Relative difference of the ideal and real voltage stress on switch for different duty cycles a) in CCM as a function of R_L and b) in DCM as a function of $R_{\mathrm{DS,on}}$.

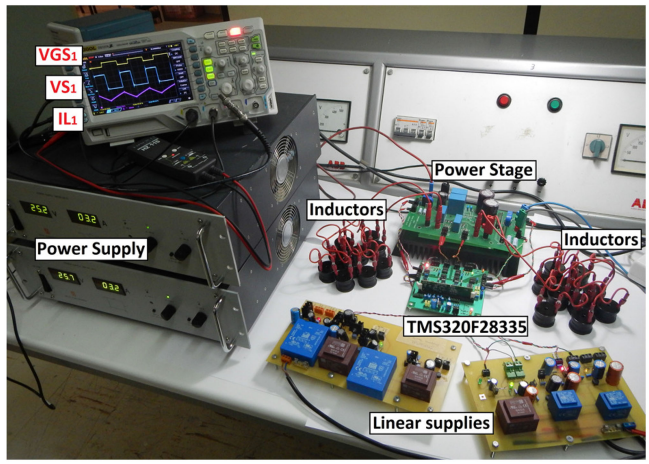


Fig. 17. 2-kW prototype of the I-IIB BB/Bt converter.

TABLE VIII
CONVERTER COMPONENTS FOR CCM OPERATION

Component	Type
S_1, S_2	C2M0160120D
D_1, D_2	IDH05G120C5
C_1	50 uF
L_1, L_2	1140-101K-RC (10 in series)

difference of the ideal and real voltage stresses, while varying each one of the parasitic elements, are very similar to those presented for the relative difference of the ideal and real voltage gain in CCM (see Figs. 9, 11, and 12) and DCM (see Figs. 14 and 15). To further illustrate this, the relative difference of the ideal and real voltage stress on the switch is depicted in Fig. 16 as an example, while the converter is operating in CCM and DCM. The parasitic elements R_L and $R_{\mathrm{DS,on}}$ are considered for this example as variables in CCM [see Fig. 16(a)] and DCM [see Fig. 16(b)], respectively, because of their dominant role in the real voltage gain, as stated and presented in Sections IV-A and IV-B accordingly.

To conclude this analysis, considering the operating conditions of the converter and all of its parasitic elements, one can predict its real voltage gain, as well as the voltage and current stresses in the semiconductor devices.

V. EXPERIMENTAL RESULTS

A 2-kW prototype of the dc/dc R2P2 I-IIB BB/Bt converter, shown in Fig. 17, was designed and built with the intention to operate in different input voltage levels.

Special attention was given to the design of printed circuit, so as to achieve low inductance layout, enabling fast switching with minimal ringing. The converter is controlled with the microcontroller TMS320F28335. The power analyzer LMG500 was employed in the setup for accurate measurements.

Three sets of experiments were conducted with this prototype to test the converter operation and verify the theoretical analysis presented in Section IV.

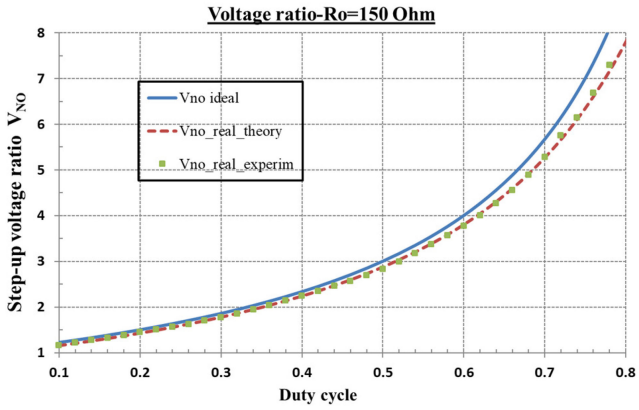
The first two sets are conducted to evaluate the theoretical analysis in case of CCM and DCM operation, accordingly. The semiconductor devices were selected to have significant parasitic values, so that the difference between the ideal and real characteristics is easily noticeable.

The third set of experiments is conducted in order to evaluate the converter efficiency, assuming a maritime application of a waste heat recovery system (WHRS) for a real ship [42]. For this experimental set, semiconductor devices with improved characteristics are selected, to achieve the highest possible efficiency.

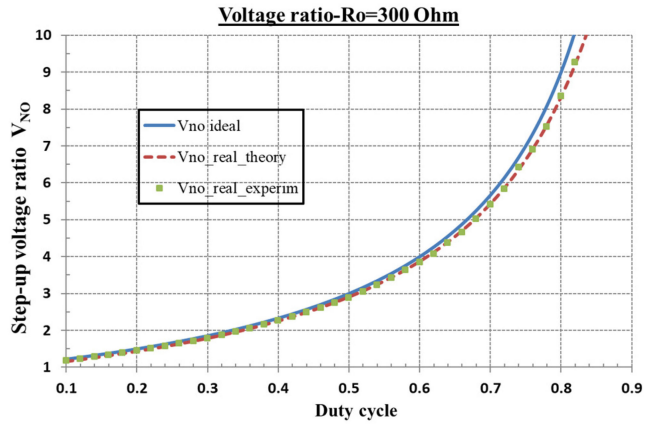
A. Validation of CCM Operation

To have a clearly noticeable difference between the ideal and real voltage gain, this set of experiments was conducted with low input voltage and high current. The selected components are presented in Table VIII, the corresponding values of the parasitic elements are shown in Table V and the operating conditions have been presented in Table IV. Therefore, keeping input voltage constant at $V_{\mathrm{in}} = 50$ V and switching frequency at $f_s = 50$ kHz, the output voltage of the converter was measured, varying duty cycle for two different loads of $R_o = 150$ Ohm and $R_o = 300$ Ohm.

The experimental results together with the theoretical ones are depicted in Fig. 18 for the whole range of duty cycle.

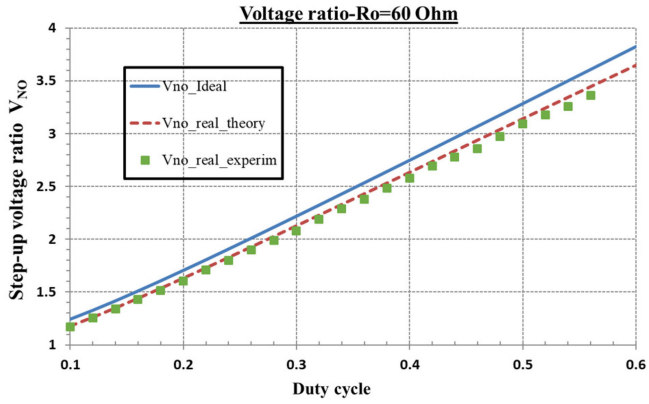


(a)

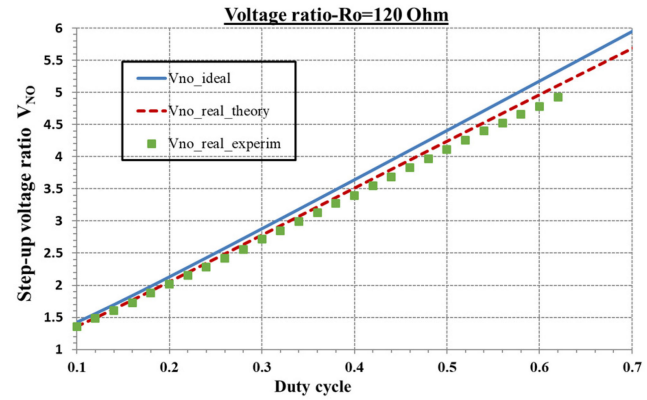


(b)

Fig. 18. Experimental and theoretical results for output voltage of the converter in CCM for a) $R_o = 150$ Ohm and b) $R_o = 300$ Ohm.



(a)



(b)

Fig. 19. Comparison of experimental and theoretical results of output voltage of the converter for DCM operating with $f_s = 20$ kHz when a) $R_o = 60$ Ohm and b) $R_o = 120$ Ohm.

The experimental results are in good accordance with the theoretical ones, which proves the correctness of the linear approximation and the validity of the theoretical analysis. Furthermore, it can be easily observed that the difference between the ideal and real step-up voltage ratio is negligible in low duty ratios and becomes more significant for duty ratios higher than 0.6. Also, the heavier the load of the converter is, the bigger the declination of the real step-up voltage ratio from the ideal one is, since the currents flown via the components of the converter are higher and produce more losses.

B. Validation of DCM Operation

Like the first set, the output voltage of the converter was measured, keeping the input voltage constant at $V_{\text{in}} = 50$ V and changing the duty cycle. The components used in this set are the same, except that the inductors value is now 100 μH (one 1140-101K-RC used for each inductor) and $R_L = 0.025\ \Omega$. This set of experiments was conducted for two loads of $R_o = 60\ \Omega$ and $R_o = 120\ \Omega$ and for a switching frequency of $f_s = 20$ kHz. The experimental results are presented in Fig. 19.

The experimental data follow the theoretical lines in a very good fashion, which confirms the validity of the theoretical analysis.

TABLE IX
CONVERTER COMPONENTS FOR EFFICIENCY EVALUATION

Component	Type
S_1, S_2	SCH2080KEC
D_1, D_2	STPSC20065D

C. Efficiency Evaluation

This set of experiments is conducted to prove that R2P2 I-IIB BB/Bt converter can operate with high efficiency for high power applications and for high step-up voltage ratios. The converter components employed for this set of experiments are shown in Table IX.

We consider a WHRS with TEGs for a ship with dc bus of 625 V [42]. The R2P2 I-IIB BB/Bt converter is employed for the interconnection of TEGs to the dc bus. Therefore, it is desired to evaluate its efficiency under various step-up voltage ratios, while keeping the output voltage constant at $V_o = 625$ V.

Taking this application into account, the converter operating conditions are presented in Table X.

To achieve different step-up voltage ratios, the input voltage of the converter is changed. For every step-up voltage ratio, the efficiency of the R2P2 I-IIB BB/Bt converter is

TABLE X
CONVERTER OPERATING CONDITIONS

Description	Value
Input voltage	48 V-125 V
Output Voltage	625 V
Output Power range	200 W-2000 W
Switching frequency	50 kHz

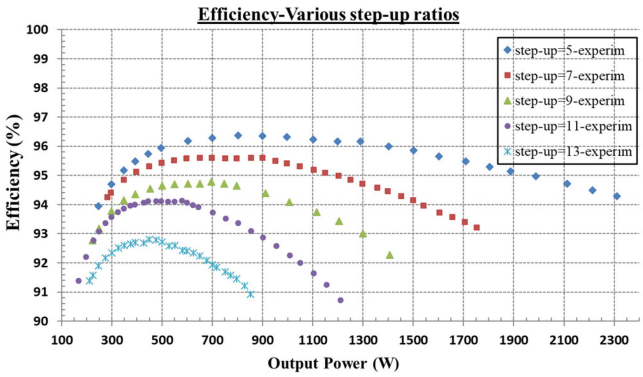


Fig. 20. Efficiency of the I-IIB BB/Bt converter under various step-up voltage ratios and a high-power range.

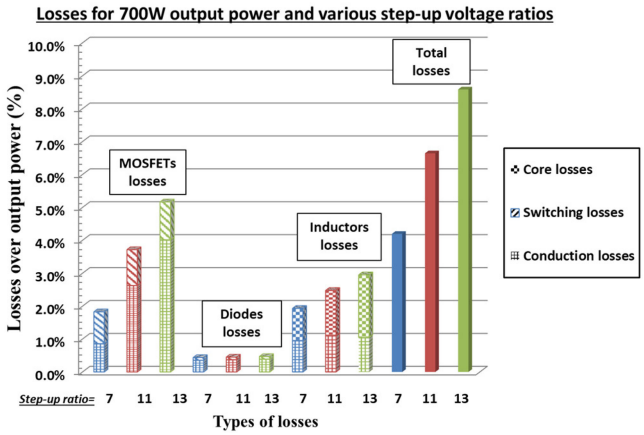


Fig. 21. Breakdown of losses of the I-IIB BB/Bt prototype, operating at 700 W output power for various step-up voltage ratios.

measured, varying the power demanded by the load and adjusting the duty cycle in order the output voltage to be kept constant.

In Fig. 20, the efficiency of the converter is depicted. It is verified that this converter can operate with high efficiency and high voltage gain, in a high-power range, making it suitable for high power high step-up applications, considering also its simple design and so its increased reliability, which is one of the most important priorities in marine applications.

For a complete overview, breakdown of power losses for the prototype at 700 W output power and three different step-up voltage ratios, namely 7, 11, and 13, can be found in Fig. 21 [43], [44].

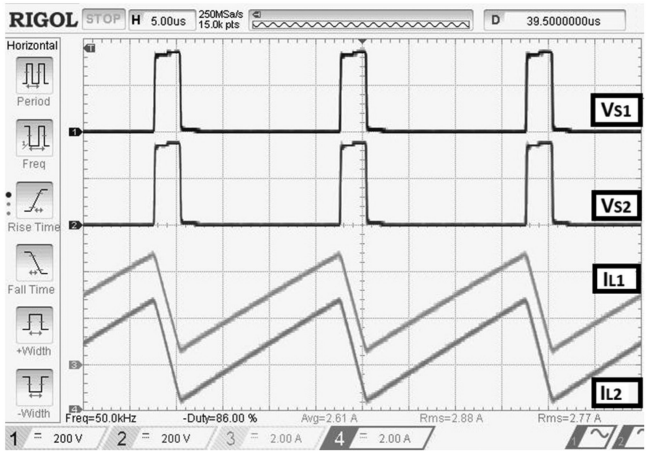


Fig. 22. Waveforms of the R2P2 I-IIB BB/Bt converter for step-up voltage ratio equal to 13.

It is worth noticing that conduction losses on switches play an important role in overall efficiency, so transistors with low $R_{\mathrm{DS,on}}$ should be selected. Also, the reverse recovery losses of diodes are negligible, since SiC Schottky diodes were employed in this prototype.

In Fig. 22, waveforms of transistors' voltages and inductors' currents are shown for step-up voltage ratio $=13$ and output power $P_o = 200$ W. It is proven that the converter operates well without any noise and spikes in the waveforms, due to the improved layout design, even in such high step-up voltage ratio and high duty cycle (d $= 0.86$). Also, it is confirmed that the converter operates in CCM region.

VI. CONCLUSION

In this paper, the nonisolated high step-up I-IIB BB/Bt converter was selected as the most suitable among the SISO R2P2 family to be used for high power applications. Particularly, emphasis was given on the prediction of the real step-up voltage ratio and semiconductor stresses, taking into consideration the effect of the nonideality of the topology elements. Theoretical analyses were presented for this converter in all operational modes, showing the declination of the real step-up voltage ratio and voltage stresses from their ideal values. It is proven that the leading role in affecting the step-up voltage ratio and so the voltage stresses, is the parasitic resistance of the transistors and inductors. Experiments conducted in a high-power range and high step-up voltage ratios validated the theoretical analysis and proved the high efficiency of the converter and so the suitability for high power applications, such as waste heat recovery systems. Moreover, experimental results verified the accuracy of the theoretical analysis considering the influence of the parasitic elements.

APPENDIX

Here, a comparison of efficiencies of R2P2 I-IIA, I-IIB, and I-IIC configurations is presented, with the intention to prove that I-IIB has the highest efficiency among them.

Let us suppose that $\eta_{I-IIB} > \eta_{I-IIC}$. According to Table I, this means that

$$\eta_A\eta_B\frac{M_A+M_B}{M_A\eta_B+M_B\eta_A} > \eta_A\eta_B\frac{M_AM_B+1}{M_AM_B+\eta_A\eta_B}$$
$$\Rightarrow (M_A+M_B)(M_AM_B+\eta_A\eta_B) > (M_AM_B+1)(M_A\eta_B+M_B\eta_A)$$
$$\Rightarrow M_A^2M_B+M_A\eta_A\eta_B+M_AM_B^2+M_B\eta_A\eta_B > M_A^2M_B\eta_B+M_AM_B^2\eta_A+M_A\eta_B+M_B\eta_A$$
$$\Rightarrow M_A^2M_B(1-\eta_B)+M_AM_B^2(1-\eta_A) > M_A\eta_B(1-\eta_A)+M_B\eta_A(1-\eta_B)$$
$$\Rightarrow M_B\left(M_A^2-\eta_A\right)(1-\eta_B)+M_A\left(M_B^2-\eta_B\right)\times(1-\eta_A) > 0.$$

Taking into account that high voltage gain and high efficiency are a prerequisite, it is considered that M_A and M_B are greater than one. Therefore, the above inequality is valid, because $M_A^2 > \eta_A$ and $M_B^2 > \eta_B$. So, the efficiency of I-IIB configuration is higher than the efficiency of I-IIC configuration.

Let us suppose that $\eta_{I-IIB} > \eta_{I-IIA}$. According to Table I, this means that

$$\eta_A\eta_B\frac{M_A+M_B}{M_A\eta_B+M_B\eta_A} > \eta_A\eta_B\frac{M_A+1}{M_A+\eta_A}$$
$$\Rightarrow (M_A+M_B)(M_A+\eta_A) > (M_A\eta_B+M_B\eta_A)(M_A+1)$$
$$\Rightarrow M_A^2+M_A\eta_A+M_AM_B+M_B\eta_A > M_A^2\eta_B+M_AM_B\eta_A+M_A\eta_B+M_B\eta_A$$
$$\Rightarrow M_A(1-\eta_B)+M_B(1-\eta_A)+\eta_A > \eta_B.$$

This inequality is valid because, generally, η_A and η_B are of similar value in reality. So, the efficiency of I-IIB configuration is higher than the efficiency of I-IIA configuration.

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