Investigation of a Four-Switch Four-Leg Inverter: Modulation, Control, and Application to an IPMSM Drive

Wei Li, Shengxiexian Xuan, Qiang Gao, and Ling Luo

***Abstract*—A permanent magnet synchronous motor (PMSM) drive based on a novel four-switch inverter is investigated in this work. No dead-time insertion/compensation is needed for the inverter because its upper and lower power devices will not shoot through. Two space vector pulsewidth modulation approaches for the four-switch inverter are developed that enable the suppression of the zero sequence voltage/current. Finally, simulation and experimental results verify that the PMSM can be effectively controlled with the novel four-switch inverter, and the system has good dynamic and static performance. The proposed approach provides a feasible alternative for low-cost motor drives.**

***Index Terms*—Four-switch inverter, permanent magnet synchronous motor (PMSM), space vector pulsewidth modulation (SVPWM).**

I. Introduction

In RECENT years, the variable frequency speed regulation system based on the standard six-switch voltage source inverter (VSI) has gained a wide range of applications. However, the relatively high cost of this topology hinders its promotion in a large number of applications where low power motor drives are used, such as treadmills, washing machines, and air conditioners. In order to reduce the cost of the inverter, tremendous efforts have been devoted to the research and development of new topologies by the academia and the industry.

In [1], a topology that connects the motor's neutral line with the ac power supply has been proposed, which uses the leakage inductance of the motor as the input line inductance. The rectifier of this topology uses two active power switches. As this topology uses the motor leakage inductance instead of the input line inductance, thereby reducing the cost, but the current flowing through the motor will increase and the maximum current requirement of the motor will be higher. Since the rectifier uses two active power switches, the dc-link voltage can be regulated, and the input power factor can be close to 1.

Manuscript received July 17, 2018; accepted August 28, 2018. Date of publication September 9, 2018; date of current version April 20, 2019. This work was funded by the LG Electronics China Research Center. Recommended for publication by Associate Editor H.-P. Nee. *(Corresponding author: Qiang Gao.)*

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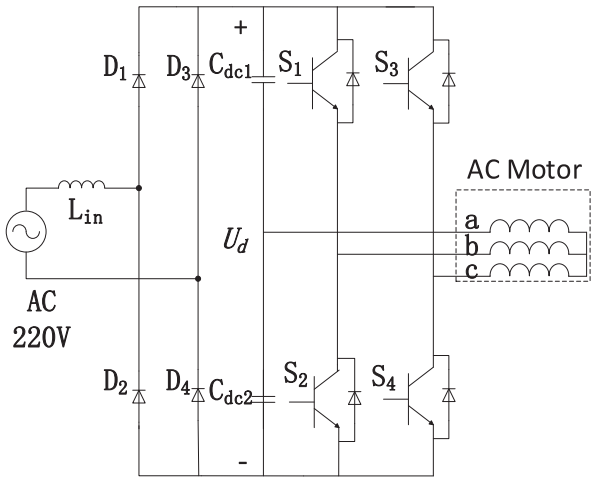

Fig. 1. Main circuit of the traditional four-switch inverter.

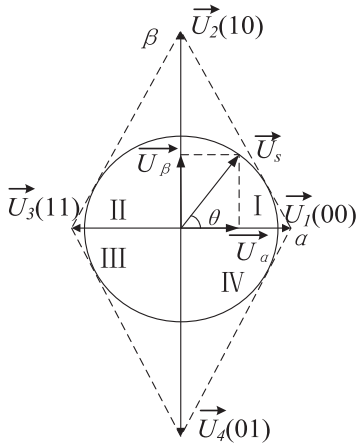

Fig. 2. Synthesized voltage vectors of the traditional four-switch inverter.

motor, which is an IPMSM in this work, will be examined. Two novel space vector pulsewidth modulation (SVPWM) schemes are developed in order to suppress the zero-sequence current that arises due to the access to the neutral point of the IPMSM. Simulations and experiments have been carried out to verify the operation principles of the IPMSM drive.

The remaining paragraphs are organized as follows. Section II briefly reviews the main circuit of the novel four-switch inverter. Section III describes the proposed SVPWM scheme devoted to suppress the zero sequence current. Sections IV and V present the simulation and experimental results, respectively, followed by the conclusion and discussion in Section VI.

II. Topology and SVPWM of the Novel Four-Switch Inverter

A. Topology

The main circuit of the traditional four-switch inverter [6]–[11] is shown in Fig. 1, where the terminal of phase *a* is connected to the midpoint of the dc-link capacitors. Its voltage space vectors are illustrated in Fig. 2, where it can be found that only four voltage vectors ($\overrightarrow{U_1} - \overrightarrow{U_4}$) are available without any

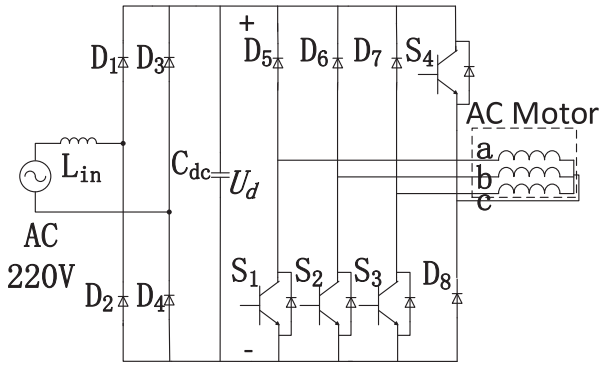

Fig. 3. Main circuit of the novel four-switch inverter.

zero voltage vectors. In Fig. 2, if the dc-link voltage is U_d, the magnitude of the voltage vector $\overrightarrow{U_1}$ equals to $\sqrt{3}/3U_d$, so the largest achievable amplitude of the output phase voltage vector $\overrightarrow{U_s}$ of the inverter(the radius of the inscribed circle of the quadrilateral formed by the four voltage vectors) is $\sqrt{3}/6U_d$. Further calculation shows that the maximum modulation index is

$$\sqrt{3}/6 * U_d * \sqrt{3}/U_d = 50\%. \tag{1}$$

Therefore, compared with the standard six-switch VSI, its loading capacity is significantly reduced. Additionally, similar to the standard six-switch VSI, normally a dead time needs to be applied to prevent the shoot-through of the legs for phases *b* and *c* [15], [16]. As well known, this dead time will cause distortion in the phase currents, especially at low speeds or light loads, which necessitates the dead-time compensation [17]–[19].

A different inverter topology that also consists of four active power switches has been proposed in [12], as shown in Fig. 3. It can be seen that the output of the inverter is made up of four legs, with each leg formed by series of a diode and a power switch. It should be noted that the diodes (D_5–D_8) and the insulated gate bipolar transistor (IGBT)s (S_1–S_4) of each leg in Fig. 3 can be swapped in principle. The fourth leg is connected to the neutral of the motor. In this paper, the feasibility of feeding an ac motor with this inverter, i.e., an interior permanent magnet synchronous motor (IPMSM) as an example in this paper, is investigated. For this purpose, the SVPWM of this inverter will be explored first.

B. SVPWM of the Novel Four-Switch Inverter

Assume that the dc-link voltage is U_d, and 1 and 0 represent turn-ON and turn-OFF of the IGBTs in each leg, respectively. Thus the four power switches, S_1–S_4 in Fig. 3 can form 16 switching states, as listed in Table I. Among the eight switching states with $S_4 = 1$, each corresponds to a complex voltage space vector. For example, the vector of the switching state 0111 is expressed as

$$\begin{aligned}\overrightarrow{U_1}(0111) &= 2/3 * \left[U_a + U_b e^{j\frac{2\pi}{3}} + U_c e^{j\frac{4\pi}{3}}\right] \\ &= 2/3 * \left[0 + (-U_d)\, e^{j\frac{2\pi}{3}} + (-U_d)\, e^{j\frac{4\pi}{3}}\right] \\ &= -2/3U_d\,. \end{aligned} \tag{2}$$

TABLE I
VOLTAGE VECTORS OF THE FOUR-SWITCH FOUR-LEG INVERTER

Voltage vectors of the four-switch inverter Symbols of voltage vectors	Switching states (S_1~S_4)	Output phase voltages			Complex form of the voltage vectors
		U_a	U_b	U_c	
$\overrightarrow{U_0}$	(0 0 0 1)	0	0	0	0
$\overrightarrow{U_1}$	(0 1 1 1)	0	-U_d	-U_d	$\frac{2}{3}U_d e^{j0}$
	(0 1 1 0)	U_d	0	0	
$\overrightarrow{U_2}$	(0 0 1 1)	0	0	-U_d	$\frac{2}{3}U_d e^{j\frac{\pi}{3}}$
	(0 0 1 0)	U_d	U_d	0	
$\overrightarrow{U_3}$	(1 0 1 1)	-U_d	0	-U_d	$\frac{2}{3}U_d e^{j\frac{2\pi}{3}}$
	(1 0 1 0)	0	U_d	0	
$\overrightarrow{U_4}$	(1 0 0 1)	-U_d	0	0	$\frac{2}{3}U_d e^{j\pi}$
	(1 0 0 0)	0	U_d	U_d	
$\overrightarrow{U_5}$	(1 1 0 1)	-U_d	-U_d	0	$\frac{2}{3}U_d e^{j\frac{4\pi}{3}}$
	(1 1 0 0)	0	0	U_d	
$\overrightarrow{U_6}$	(0 1 0 1)	0	-U_d	0	$\frac{2}{3}U_d e^{j\frac{5\pi}{3}}$
	(0 1 0 0)	U_d	0	U_d	
$\overrightarrow{U_7}$	(1 1 1 1)	-U_d	-U_d	-U_d	0
$\overrightarrow{U_8}$	(0 0 0 0)	U_d	U_d	U_d	0
$\overrightarrow{U_9}$	(1 1 1 0)	0	0	0	0

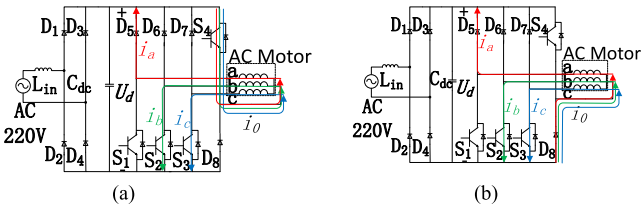

Fig. 4. Three-phase current direction of the novel four-switch inverter. (a) 0111. (b) 0110.

Fig. 4(a) shows the current direction corresponding to the switch state 0111.

Among the remaining eight switching states, the switching states, 0000 and 1110, create zero voltage vectors. The voltage space vectors created by the rest of the six switching states with $S_4 = 0$ are dependent on the current amplitudes through S_1–S_3. In other words, if the current in any of the three phases decreases to zero, the voltage space vectors corresponding to these six switching states will no longer be certain. Otherwise, these six voltage space vectors are the same as those with $S_4 = 1$. Take the switching state (0110) as an example, assuming nonzero currents on S_1–S_3, one has

$$\begin{aligned}\overrightarrow{U_1}(0110) &= 2/3 * \left[U_a + U_b e^{j\frac{2\pi}{3}} + U_c e^{j\frac{4\pi}{3}}\right] \\ &= 2/3\left[U_d + (0)\, e^{j\frac{2\pi}{3}} + (0)\, e^{j\frac{4\pi}{3}}\right] \\ &= -2/3 U_d \\ &= \overrightarrow{U_1}(0111). \end{aligned} \tag{3}$$

Fig. 4(b) shows the current direction corresponding to the switch state 0110.

Fig. 5 shows all the active voltage vectors in Table I. One can see that each vector has one redundant switching state, which

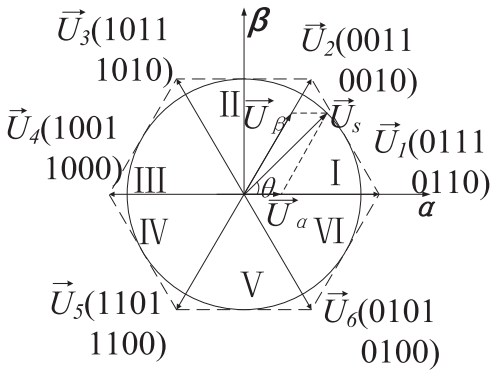

Fig. 5. Synthesized voltage vectors of the novel four-switch inverter.

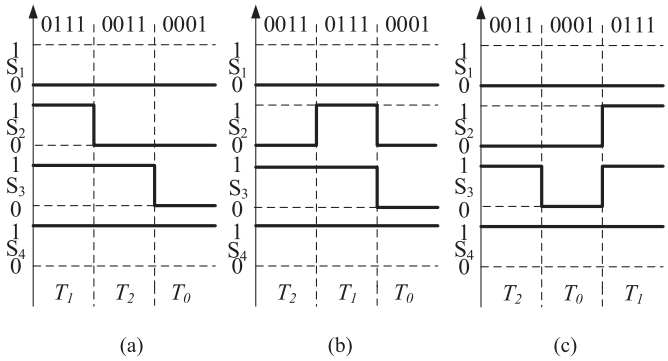

Fig. 6. Three possible PWM waveforms for a reference voltage vector in sector I for the FSV.

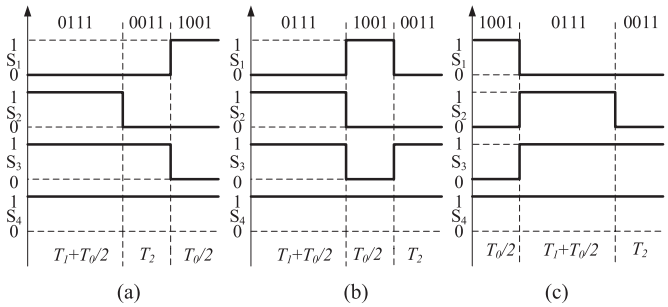

Fig. 7. Three possible PWM waveforms for a reference voltage vector in sector I for the SSV when two opposite voltage vectors are $\overrightarrow{U_1}$ and $\overrightarrow{U_4}$.

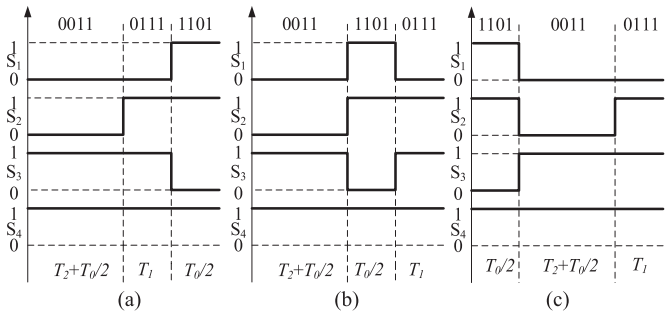

Fig. 8. Three possible PWM waveforms for a reference voltage vector in sector I for the SSV when two opposite voltage vectors are $\overrightarrow{U_2}$ and $\overrightarrow{U_5}$.

exists when all the phase currents are nonzero. This redundancy provides the flexibility for common mode current suppression, as will be explained later.

As shown in Fig. 5, a reference voltage vector can be synthesized through the application of two adjacent active and one nonactive voltage vectors. The calculation of the dwell times is very similar to a standard six-switch VSI inverter [20], and therefore will not be repeated for conciseness of the paper.

In terms of the way to generate a zero voltage vector, two SVPWM schemes for this inverter topology, named first-typed SVPWM (for short: FSV) and second-typed SVPWM (for short: SSV), are investigated. There are two nonzero voltage vectors and one standard zero voltage vector, listed in Table I, in one PWM cycle for the FSV, the same as for a six-switch VSI inverter. On the other hand, while the two active voltage vectors remain the same as for the FSV, the SSV uses two opposite voltage vectors to replace a zero voltage vector. For example, in sector I, the two active voltage vectors are 0111 (or 0110), 0011 (or 0011) and the two opposite voltage vectors are 0111 (or 0110), 1001 (or 1000). The dwell time of the two opposite voltage vectors is $T_0/2$ for both, with T_0 being the total dwell time of the zero voltage vector.

C. Sequence of the Voltage Vectors in One PWM Cycle

To reduce the switching frequency, the sequence of the voltage vectors within a PWM period needs to be arranged properly. For the convenience of the discussion, only those voltage vectors with $S_4 = 1$ will be considered.

Within a PWM cycle in the FSV, there are two active voltage vectors and one inactive voltage vector. Assuming the asymmetric PWM, Fig. 6 only shows half of all six possible PWM waveforms, and the remaining three are symmetrical to these waveforms. The sequence shown in Fig. 6(a) is preferred than the other five options in terms of minimum commutation times in each cycle, and therefore it is chosen for the following simulation and experiment.

Within a PWM cycle for the SSV, there are two active voltage vectors, as well as two opposite active voltage vectors that form an inactive vector. For this purpose, in each sector there are totally three choices of applying two opposite voltage vectors, i.e., $\overrightarrow{U_1}$ and $\overrightarrow{U_4}$, $\overrightarrow{U_2}$ and $\overrightarrow{U_5}$, or $\overrightarrow{U_3}$ and $\overrightarrow{U_6}$. For example, when the reference voltage resides in sector I, the first choice for zero voltage vector generation is to apply the voltage vector $\overrightarrow{U_1}$, and its opposite voltage vector, i.e., $\overrightarrow{U_4}$. Similarly, the second choice is to apply the voltage vector ($\overrightarrow{U_2}$) and its opposite voltage vector ($\overrightarrow{U_5}$). The third choice ($\overrightarrow{U_3}$ and $\overrightarrow{U_6}$) does not contain $\overrightarrow{U_1}$ and $\overrightarrow{U_2}$, which will lead to a higher switching frequency. Thus, only the first two choices will be discussed in the following.

Corresponding to the first choice mentioned above, Fig. 7 shows three out of six possible PWM waveforms. Meanwhile, Fig. 8 shows three out of six possible PWM waveforms corresponding to the second choice mentioned above. The remaining PWM waveforms can be obtained following the same principles and are not given for conciseness. It can be seen that the sequences shown in Figs. 7(a) and 8(a) are preferred due to

fewer commutation times in each cycle. In this work, the sequence in Fig. 7(a) is chosen for the following simulation and experiment.

It is worth noting that the symmetric PWM scheme can also be used in the FSV or SSV, and better harmonic performance can be expected at the expense of a higher switching frequency. This remains to be investigated in the future.

D. Maximum Modulation Index and Dead Time

As shown in Table I, the magnitude of the six voltage vectors is $2/3U_d$, so the peak value of the output phase voltage vector $\overrightarrow{U_s}$ of the inverter (the radius of the inscribed circle in Fig. 5) is $\sqrt{3}/3U_d$. Further calculation shows that the maximum modulation ratio is

$$\sqrt{3}/3 * U_d * \sqrt{3}/U_d = 100\%. \tag{4}$$

Therefore, in principle, this topology is capable of generating the same phase voltages as a standard six-switch VSI.

Due to the fact that each leg comprises a diode and an IGBT in series, no dead time or dead-time compensation is essentially needed. This feature eases the control of the inverter to a large extent compared with the standard six-switch VSI or the traditional four-switch inverter.

III. Zero Sequence Voltage and Its Suppression

Despite the benefits mentioned above, the access of the neutral of a load inevitably creates a path for the zero-sequence current. In the following paragraphs, two simple methods to suppress the zero-sequence voltage are presented.

A. Generation of Zero Sequence Voltage

The zero sequence voltage U_0 is defined as the average value of the three-phase output voltages, i.e.,

$$U_0 = 1/3\,(U_a + U_b + U_c)\,. \tag{5}$$

Similarly, the zero sequence current I_0 is defined as

$$I_0 = 1/3\,(I_a + I_b + I_c)\,. \tag{6}$$

While using the eight switching states when $S_4 = 1$ can form a reference voltage space vector, the analysis shows that other switching states, except the switching state 0001, will produce a negative zero sequence voltage on the motor. For example, in sector I, if the switching states 0111 and 0011 are used, the corresponding zero sequence voltage is shown in Fig. 9(b). It can be seen that a zero sequence voltage with the amplitude of $2/3U_d$ is generated. Similar zero-sequence voltages will result if one looks at other sectors. Therefore, if only the eight switching states when $S_4 = 1$ are used, a zero sequence voltage will be created, which becomes more serious when the motor operates under high loads or at high speeds, because in these cases the zero vector's dwell time is close to zero and a large zero-sequence voltage will be created, leading to an enormous zero sequence current. This will generate a large resistive loss on the stator windings, or even prohibit the normal operation of the whole drive.

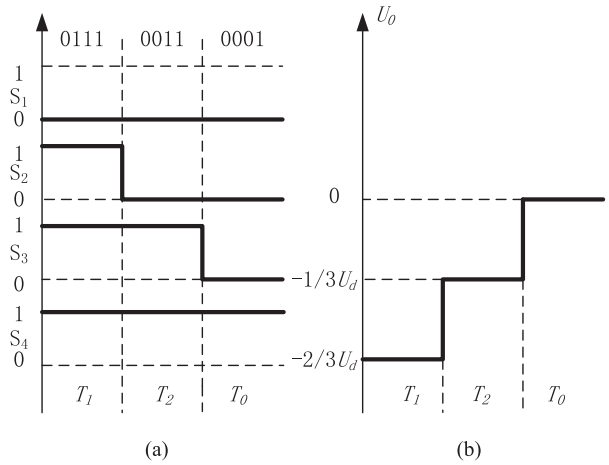

Fig. 9. PWM waveforms and zero sequence voltage waveform in sector I without voltage vector replacement for the FSV. (a) PWM waveforms. (b) Zero sequence voltage waveform.

B. Voltage Vector Replacement Method

It is worth mentioning that the main circuit of the novel four-switch inverter in Fig. 3 only allows the phase currents to flow out of the motor (i.e., negative currents). It implies that only negative zero-sequence current is present, which is induced by a negative zero-sequence voltage in the motor initially. As a result, in order to suppress the zero-sequence current, the initial voltage vectors (those voltage vectors corresponding to $S_4 = 1$) should be replaced by their respective redundant vectors (those voltage vectors corresponding to $S_4 = 0$) whenever it is possible, because these redundant vectors yield positive zero-sequence voltages. For this end, the following mechanism is proposed to enable the voltage vector replacement.

As mentioned previously, when none of the phase currents is zero, the switching states 1000, 1100, 0100, 0110, 0010, 1010 can also produce the six voltage space vectors, $\overrightarrow{U_1} - \overrightarrow{U_6}$, as shown in Table I, and more importantly will produce a positive zero sequence voltage on the load.

The practical operation when applying the above-mentioned principle of vector replacement will be discussed next.

When the output phase voltage is $-U_d$, 0, or $+U_d$, the corresponding phase current will increase, freewheel, or decrease, respectively, in opposite directions. Therefore, the phase current whose corresponding output phase voltage is $+U_d$ after the replacement needs to be checked whether it is large enough, so that it will not decrease to zero after the replacement and the currents in the rest two phases only need to be checked whether they equal zero. For example, if the voltage vector changes from 0011 to 0010, I_a and I_b need to be checked whether they are larger than the current threshold I_t, and I_c needs to be checked whether it is 0. To ensure the phase currents do not decrease to 0, I_t needs to be set large enough. However, the times of the replacement will decrease if I_t is too large.

If the FSV is chosen, the times of the replacement in each PWM cycle can be 0, 1, or 2. For example, in sector I, if one of the phase currents is zero or I_a and I_b are both less than I_t, the initial voltage vectors cannot be replaced and the variation of

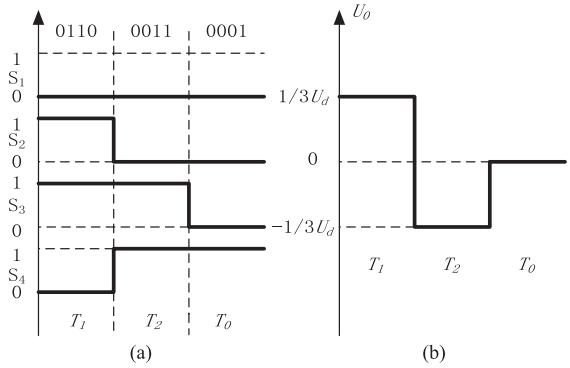

Fig. 10. PWM waveforms and zero sequence voltage waveform in sector I when one voltage vector (0111) is replaced for the FSV. (a) PWM waveforms. (b) Zero sequence voltage waveform.

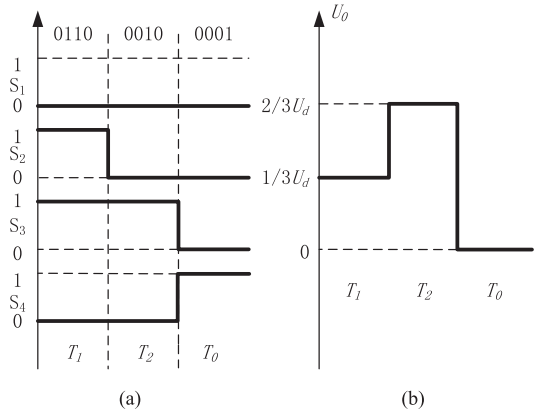

Fig. 11. PWM waveforms and zero sequence voltage waveform in sector I when two voltage vectors (0111 and 0011) are replaced for the FSV. (a) PWM waveforms. (b) Zero sequence voltage waveform.

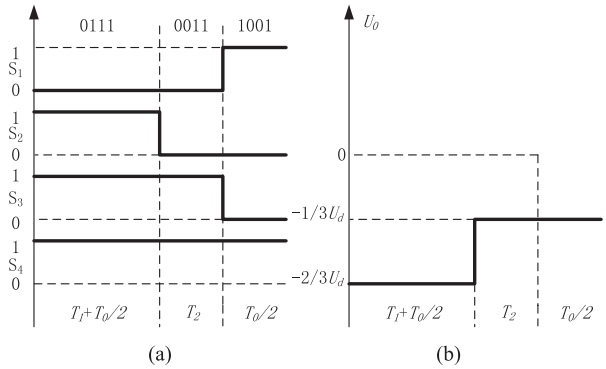

Fig. 12. PWM waveforms and zero sequence voltage waveforms in sector I without voltage vector replacement for the SSV. (a) PWM waveforms. (b) Zero sequence voltage waveforms.

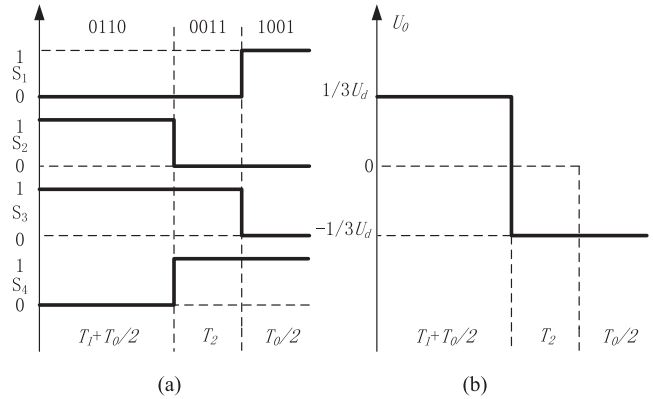

Fig. 13. PWM waveforms and zero sequence voltage waveforms in sector I when one voltage vector (0111) is replaced for the SSV. (a) PWM waveforms. (b) Zero sequence voltage waveforms.

zero sequence voltage in one PWM cycle is shown in Fig. 9(b). Besides, if none of the phase currents are zero and I_a is larger than I_t and I_b is less than I_t, the switching state 0111 is replaced with the switching state 0110 and the variation of zero sequence voltage in one PWM cycle is shown in Fig. 10(b). Finally, if none of the phase currents are zero and I_a and I_b are both larger than I_t, the switching states 0111, 0011 are replaced with the switching states 0110, 0010, respectively, and the variation of zero sequence voltage in one PWM cycle is shown in Fig. 11(b). One can find out that, compared with the zero sequence voltage shown in Fig. 9(b), the zero sequence voltage is changed from $-2/3U_d$ to $1/3U_d$ after introducing the vector (0110) and changed from $-1/3U_d$ to $2/3U_d$ after introducing the vector (0010). More importantly, the averaged zero-sequence voltage within each PWM cycle is largely reduced. In other sectors, the times of the replacement in each PWM cycle can be 0, 1, or 2, too.

Similar to the FSV, if the SSV is chosen, the times of the replacement in each PWM cycle can be 0, 1, 2, or 3. The PWM waveforms and the variation of zero sequence voltage in one PWM cycle are shown in Figs. 12–16, where the waveforms in Fig. 12 correspond to the case when none of the switching states are replaced, and the waveforms in Fig. 13 correspond to the case

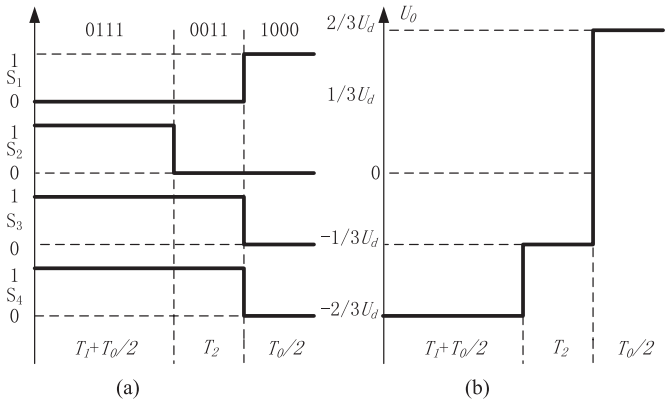

Fig. 14. PWM waveforms and zero sequence voltage waveforms in sector I when one voltage vector (1001) is replaced for the SSV. (a) PWM waveforms. (b) Zero sequence voltage waveforms.

when the switching state 0111 is replaced with the switching state 0110, and the waveforms in Fig. 14 correspond to the case when the switching state 1001 is replaced with the switching states 1000, and the waveforms in Fig. 15 correspond to the case when the switching states 0111 and 0011 are replaced with the switching states 0110 and 0010, respectively, and the waveforms

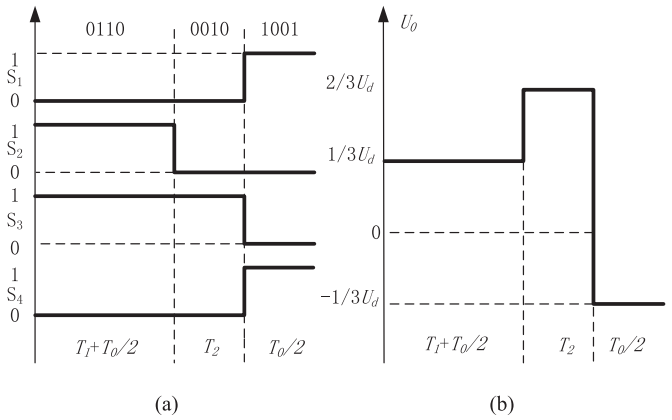

Fig. 15. PWM waveforms and zero sequence voltage waveforms in sector I when two voltage vectors (0111 and 0011) are replaced for the SSV. (a) PWM waveforms. (b) Zero sequence voltage waveforms.

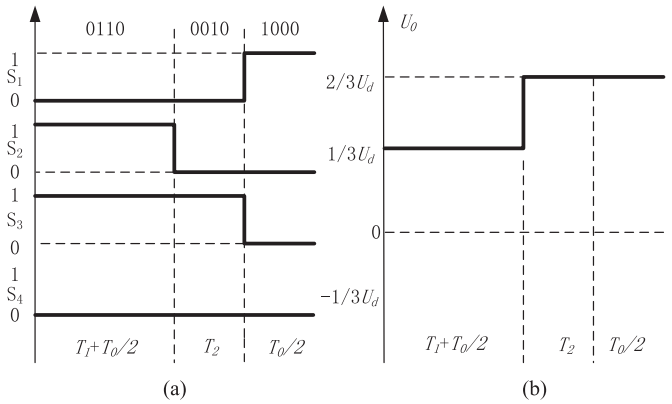

Fig. 16. PWM waveforms and zero sequence voltage waveforms in sector I when three voltage vectors (0111, 0011. and 1001) are replaced for the SSV. (a) PWM waveforms. (b) Zero sequence voltage waveforms.

TABLE II
MOTOR AND SYSTEM PARAMETER

PARAMETER	VALUE
Stator resistance R_a	2.5 Ω
d-axis inductance L_d	8.7 mH
q-axis inductance L_q	17.5 mH
Linkage flux Ψ_a	0.1 Wb
Number of pole pairs P	2
Rated torque	0.5 N.m
Input voltage	220 V_{rms}
Input frequency f_{in}	50 Hz
DC-link capacitance C_{dc}	1 mF
Sampling frequency f_s	10 kHz
moment of inertia J	0.0000833 $K_g.m^2$

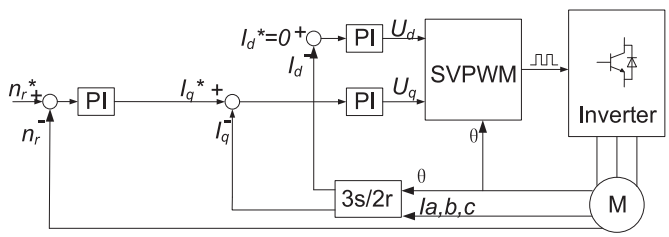

Fig. 17. Simplified control block diagram of the PMSM drive.

in Fig. 16 correspond to the case when the switching states 0111, 0011, and 1001 are replaced with the switching states 0110, 0010, and 1000, respectively. One can find out that, compared with the zero sequence voltage shown in Fig. 12(b), the zero sequence voltage is changed from $-2/3U_d$ to $1/3U_d$ after introducing the vector (0110), and from $-1/3U_d$ to $2/3U_d$ after introducing the vector (0010), and from $-1/3U_d$ to $2/3U_d$ after introducing the vector (1000).

Therefore, using the above-mentioned algorithm of voltage vector replacement, both the FSV and SSV can reduce or even reverse the polarity of zero sequence voltage, and hence reduce the zero sequence current effectively. Additionally, when using the SSV, the initial voltage vectors can be replaced more frequently than when using the FSV.

IV. SIMULATION RESULTS

Without the voltage vector replacement, the zero sequence current would be so large that it will become impractical to test the algorithm in reality, because of the current limitation of the motor and the power switches. Hence, simulation is adopted first to evaluate the control of the IPMSM with the novel inverter and the zero sequence current with and without the proposed SVPWM schemes.

The motor and the system parameters in the simulation model are listed in Table II. The simplified control block diagram is illustrated in Fig. 17 [21]. The d-axis reference current i_d* is set to 0 for simplicity and the threshold I_t is set to -0.5 A.

When the motor is run under 0.5 Nm at 2000 r/min, the waveforms of the speed, i_d, i_q, the three-phase currents, and the zero-sequence current are shown in Figs. 18–23, where the waveforms in Figs. 18 and 19 correspond to the case when the switching states are not replaced at all, and the waveforms in Figs. 20 and 21 correspond to the case of the FSV with voltage vector replacement, and the waveforms in Figs. 22 and 23 correspond to the case of the SSV with voltage vector replacement.

As shown in Figs. 18, 20, and 23, the measured speeds/currents all can track their reference values very well in these three algorithms.

However, in Fig. 19, when the switching states are not replaced, a large zero-sequence current of about 25 A flows through the motor. After using the algorithm FSV or SSV, the zero-sequence current has been reduced to about 2.5 A. In addition, the zero-sequence current when using the SSV, as in Fig. 23, is suppressed more than when using the FSV, as shown

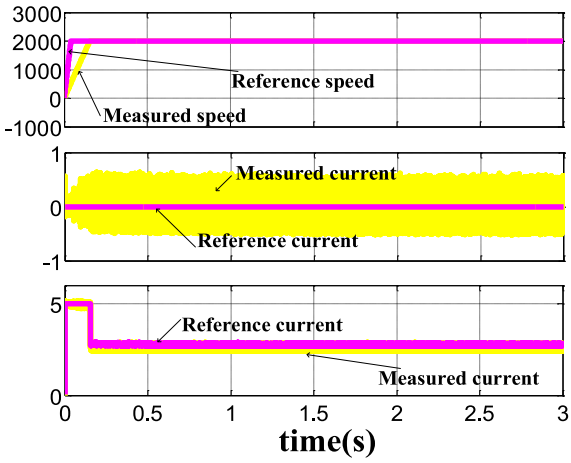

Fig. 18. Speed, i_d, i_q of the PMSM before the replacement of voltage vectors. Top: the speeds (r/min), middle: i_d (A), and bottom: i_q (A).

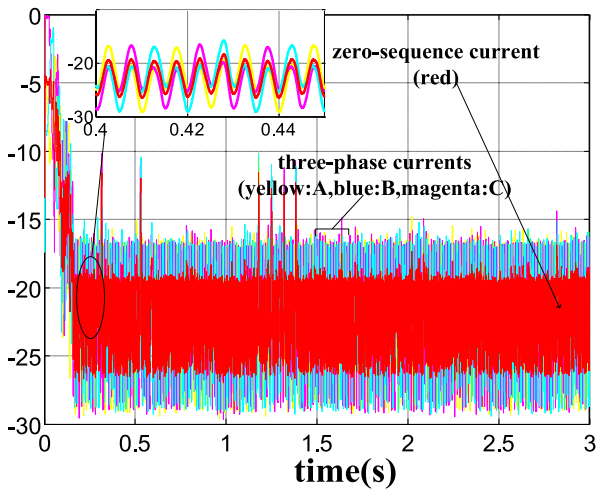

Fig. 19. Three-phase currents and the zero-sequence current before the replacement of voltage vectors.

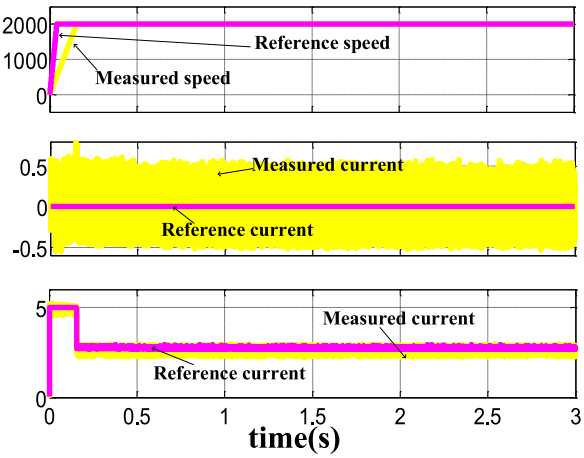

Fig. 20. Speed, i_d, i_q of the PMSM when using the FSV. Top: the speed (r/min), middle: i_d (A), and bottom: i_q (A).

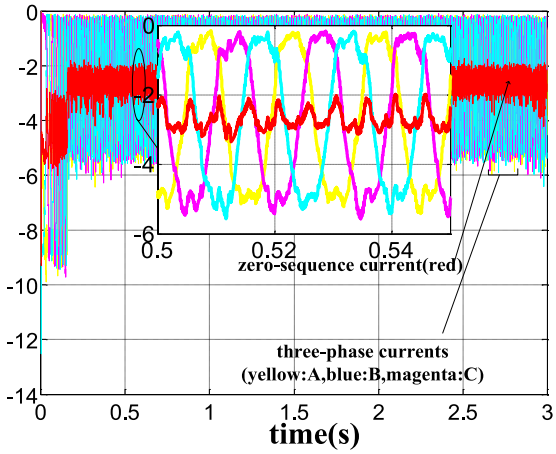

Fig. 21. Three-phase currents and the zero-sequence current of the PMSM when using the FSV.

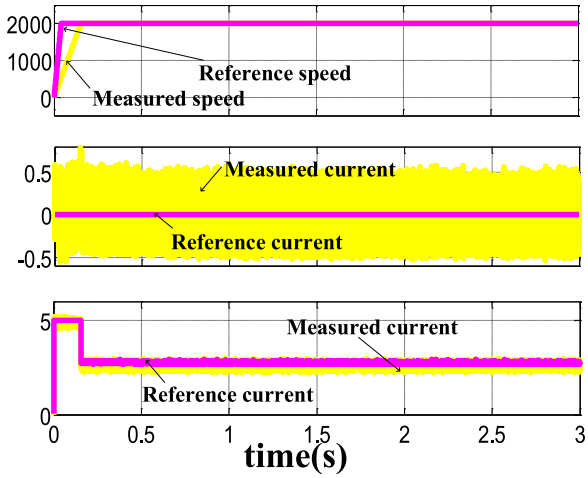

Fig. 22. Speed, i_d, i_q of the PMSM when using the SSV. Top: the speed (r/min), middle: i_d (A), and bottom: i_q (A).

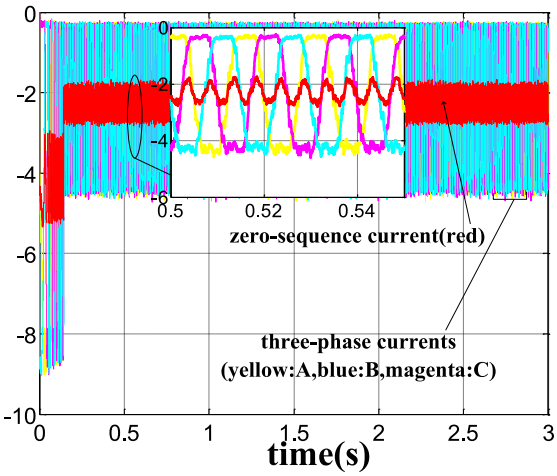

Fig. 23. Three-phase currents and the zero-sequence current of the PMSM when using the SSV.

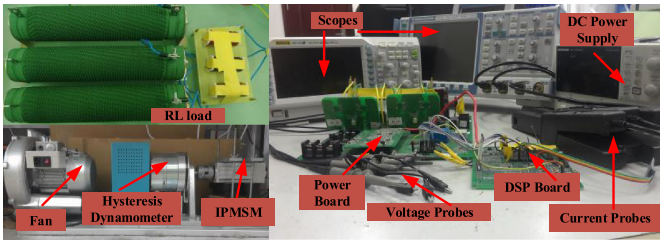

Fig. 24. Photo of the test rig.

TABLE III
LOAD AND SYSTEM PARAMETERS

PARAMETER	VALUE
R	100 Ω
inductance L	5 mH
Input voltage	177 V_{rms}
Input frequency f_{in}	50 Hz
DC-link capacitance C_{dc}	1 mF
Sampling frequency f_s	10 kHz

in Fig. 21, and the amplitude of the three-phase currents when using the SSV is also smaller.

V. EXPERIMENTAL RESULTS

For the purpose of examining the SVPWM scheme, open-loop experiments, where a three-phase *R–L* load is used, are performed first. Then the practical closed-loop operation of an IPMSM drive with the novel inverter and its SVPWM scheme is tested.

Fig. 24 shows the photo of the test-rig. A hysteresis dynamometer is used as the load of the permanent magnet synchronous motor (PMSM). A TI TMS320F28335 implements the vector control, SVPWM, and the zero sequence current suppression algorithm. The switching frequency is set to 10 kHz; and dc-link capacitance is 940 μF. In the experiment, two oscilloscopes (ROHDE&SCHWARZ RTM2034 and RIGOL DS1104) are used to record different waveforms.

A. RL Load

The load and the system parameters are listed in Table III and the threshold I_t is -0.5 A.

Figs. 25 and 26 show the waveforms of the *RL* load for the FSV. In Fig. 25, the three-phase currents and zero-sequence current and PWM are illustrated, where the zero-sequence current is about -1.5 A. Fig. 26 shows the three-phase voltages and synchronizing signal.

Similar to Figs. 25 and 26, Figs. 27 and 28 show the waveforms of the *RL* load for the SSV. It is illustrated in Fig. 27 that the zero-sequence current is about -1 A, implying better zero

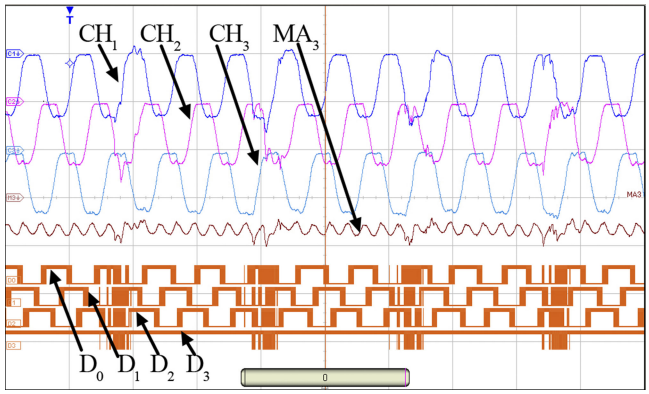

Fig. 25. Three-phase currents and the zero-sequence current and PWM waveforms of the *RL* load for the FSV. $CH_1 - CH_3$: Phases A, B, C currents (A), MA_3: Zero-sequence current (A), D_0–D_3: PWM waveforms for S_1–S_4 ($CH_1 - CH_3$, MA_3: 2 A/grid, Time: 50 ms/grid).

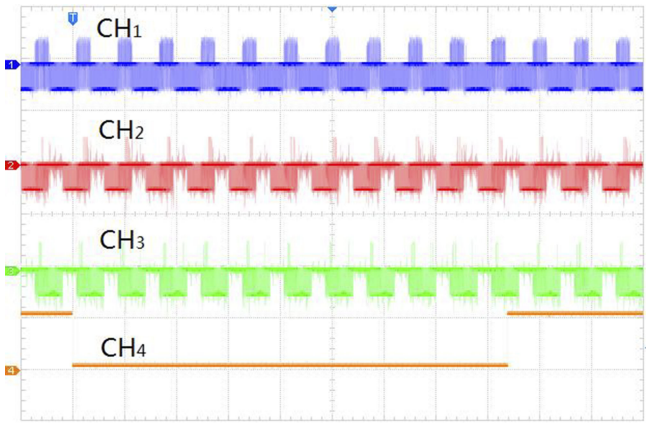

Fig. 26. Three-phase voltages and synchronizing signal of the *RL* load for the FSV. $CH_1 - CH_3$: Phases A, B, C voltages (V), CH_4: synchronizing signal ($CH_1 - CH_3$: 500 V/grid, Time: 50 ms/grid).

current suppression with the SSV. Fig. 28 shows the three-phase voltages and synchronizing signal.

Because of the low sampling rate of the oscilloscopes, the data of the waveforms are plotted into graphics in MATLAB and part of the graphics for the FSV is shown in Fig. 29, while the zoomed plot with the SSV is shown in Fig. 30. In Fig. 29, it can be seen that, for the voltage vector in sector I, I_a and I_b are both larger than I_t. Therefore, the switching states 0111 and 0011 are replaced by 0110 and 0010, respectively, and I_a and I_b both decrease. In Fig. 30, the voltage vector is in sector I, and I_a, I_b, and I_c are all larger than I_t. Therefore, the switching states 0111, 0011, and 1001 are replaced by 0110, 0010, and 1000, respectively, and I_a, I_b, and I_c all decrease.

B. PMSM Load

The PMSM's parameters are the same as those in Table II and the threshold I_t is -0.5 A. As mentioned previously, the zero-sequence current can be reduced more under the SSV, so only the algorithm SSV is used next.

Under speed transients, Fig. 31 shows three-phase currents and the zero-sequence current waveforms, while Fig. 32 shows

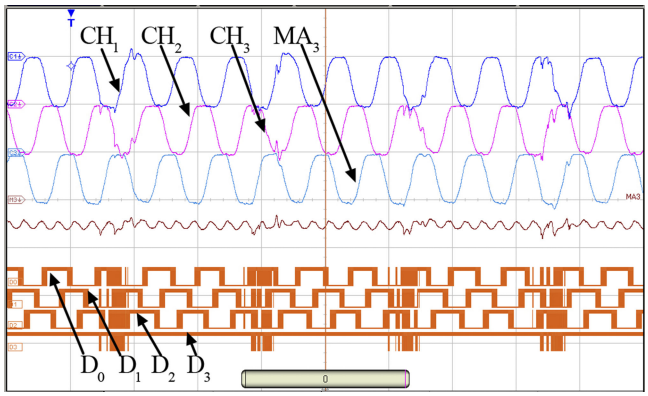

Fig. 27. Three-phase currents and the zero-sequence current and PWM of the *RL* load for the SSV. CH_1-CH_3: Phases A, B, C currents (A), MA_3: Zero-sequence current (A), D_0–D_3: PWM waveforms for S_1–S_4 (CH_1-CH_3, MA_3: 2 A/grid, Time: 50 ms/grid).

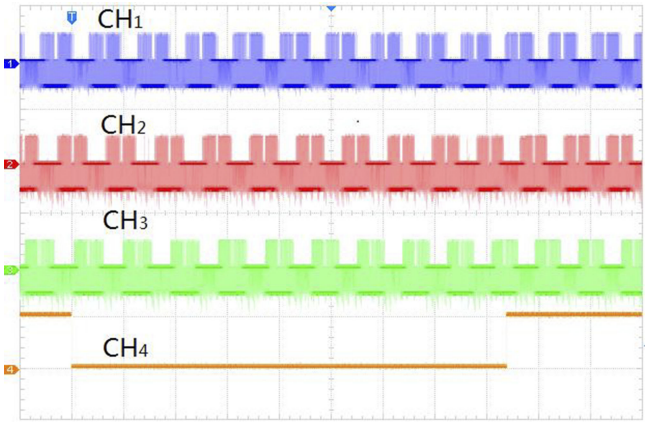

Fig. 28. Three-phase voltages and synchronizing signal of the *RL* load for the SSV. CH_1-CH_3: Phases A, B, C voltages (V), CH_4: synchronizing signal (CH_1-CH_3: 500 V/grid, Time: 50 ms/grid).

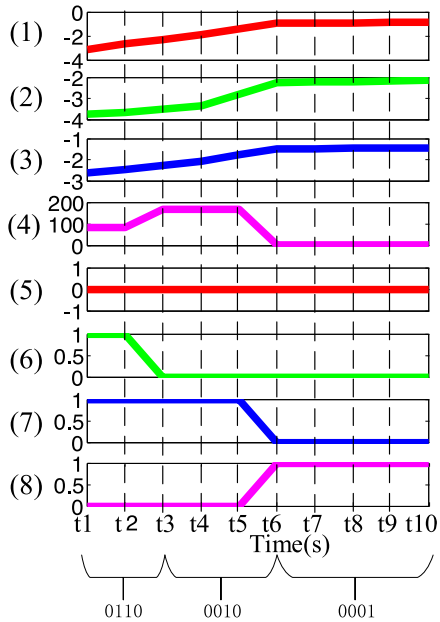

Fig. 29. Zoomed plot of the *RL* load for the FSV. Time: $t_1 = 0.18291$ s, 0.0001 s/grid. (1)–(3): Phases A, B, C currents (A). (4): Zero-sequence voltages (V). (5)–(8): PWM waveforms for S_1–S_4.

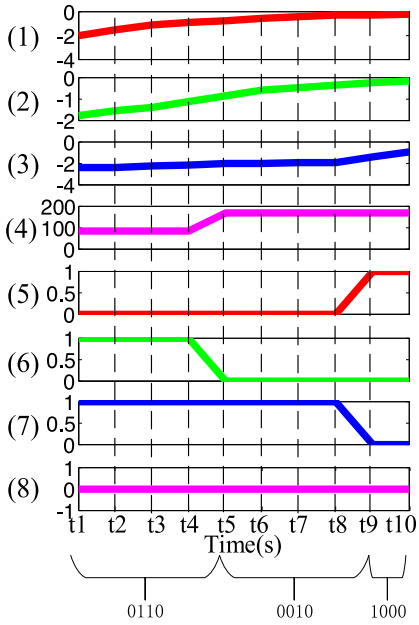

Fig. 30. Zoomed plot of the *RL* load for the SSV. Time: $t_1 = 0.20450$ s, 0.0001 s/grid. (1)–(3): Phases A, B, C currents (A). (4): Zero-sequence voltages (V). (5)–(8): PWM waveforms for S_1–S_4.

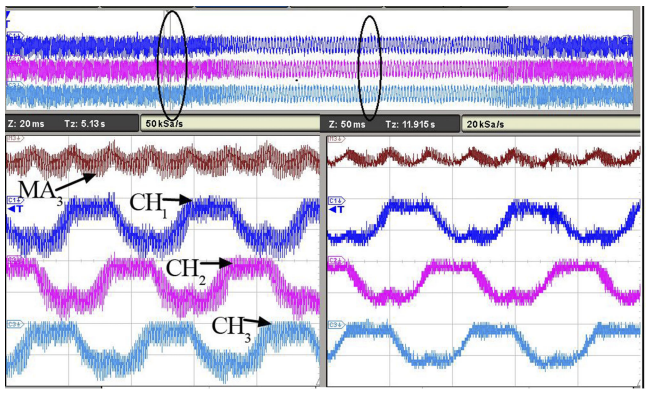

Fig. 31. Three-phase currents and the zero-sequence current of the PMSM under speed transients. CH_1–CH_3: Phases A, B, C currents (A). MA3: Zero-sequence current (A) (CH_1–CH_3, MA_3: 2 A/grid, Time: 2 s/grid, 20 ms/grid, 50 ms/grid).

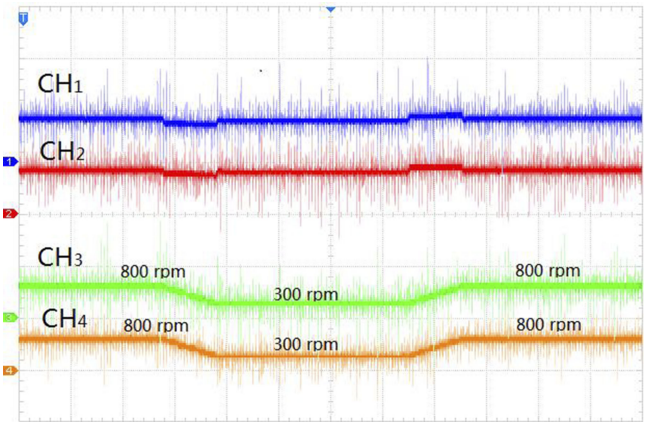

Fig. 32. Speed, i_q of the PMSM under speed transients. CH_1: Reference i_q, CH_2: Measured i_q, CH_3: Reference speed, CH_4: Measured speed (CH_1, CH_2: 2 A/grid, CH_3, CH_4: 1600 rpm/grid, Time: 2 s/grid).

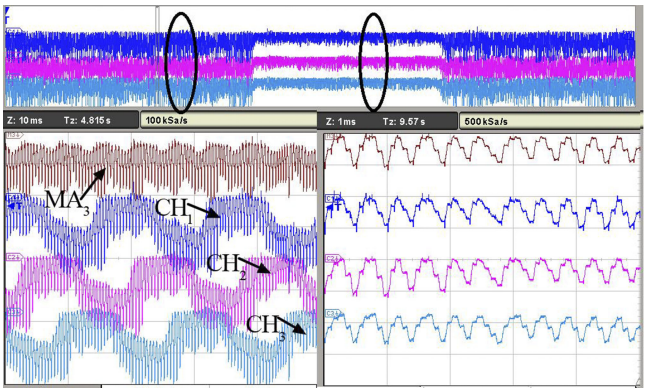

Fig. 33. Three-phase currents and the zero-sequence current of the PMSM under torque transients. CH_1–CH_3: Phases A, B, C currents (A), MA3: Zero-sequence current (A) (CH_1–CH_3, MA_3: 2 A/grid, Time: 2 s/grid, 10 ms/grid, 1 ms/grid).

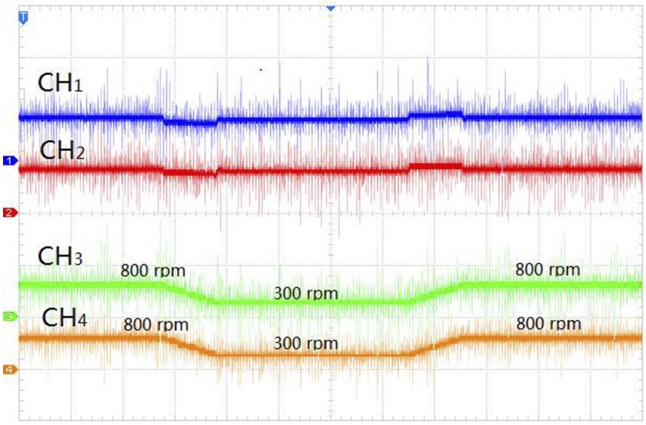

Fig. 34. Speed, i_q of the PMSM under torque transients. CH_1: Reference i_q, CH_2: Measured i_q, CH_3: Reference speed, CH_4: Measured speed (CH_1, CH_2: 2 A/grid, CH_3, CH_4: 1600 rpm/grid, Time: 2 s/grid).

the speed, i_d, i_q waveforms. The reference speed ramps between 800 and 300 r/min under 0.5 Nm are performed for 8 s, followed by a speed change to 800 r/min.

Under torque transients, Fig. 33 shows three-phase currents and the zero-sequence current waveforms, while Fig. 34 shows the speed, i_d, i_q waveforms. The drive is controlled to a reference load 0.5 Nm at 2000 r/min and then subject to a load step to no load, followed by a load step to a 0.5 Nm load.

From Figs. 31–34, it is clear that good speed and current tracking can be achieved both during speed transients and torque transients.

VI. Discussion and Conclusion

In this paper, the principle of a nonstandard four-switch inverter topology has been analyzed and a tailored SVPWM method, which involves two schemes (FSV and SSV), has been proposed. In each PWM cycle, the FSV employs two active vectors plus an inactive vector, while in the SSV, each PWM cycle consists of only active vectors. In order to address the zero sequence voltage/current issue arising from the access to the neutral of the load, the unique feature of this topology, i.e., the provision of the redundant voltage vectors, is exploited, such that the initial active vectors (corresponding to $S_4 = 1$) in each PWM cycle will be replaced by their respective redundant vectors (corresponding to $S_4 = 0$) whenever it is allowed. It needs to be noticed that the voltage vectors can be replaced more frequently in the SSV than in the FSV. Finally, simulation and experiment results prove the scheme's feasibility. Simulation and experiment results show that the SSV is a better choice to suppress the zero sequence current.

Compared with a standard four-switch inverter with a maximum modulation index of 0.5, a unit modulation index can be achieved at the price of four diodes. On the other hand, this topology replaces two active power switches and their drivers in a standard six-switch inverter with four diodes and achieves the same modulation index. No dead-time generation or dead-time compensation is needed for this four-switch four-leg inverter. In the meantime, with the use of the proposed zero sequence voltage suppression methods, the zero sequence current can be reduced to a large extent, although it cannot be completely eliminated. It should be pointed out that this zero sequence current also has a close relationship with the stator leakage inductance, which indicates that a motor with a large leakage inductance can further reduce the zero sequence current. In this sense, a PMSM with tooth-wound stator windings seems to be more preferred to be used together with the inverter in question, since it is known that this type of windings not only saves costs but also leads to a larger leakage inductance than integral-slot windings.

Therefore, from the general viewpoint, it is felt by the authors that this four-switch four-leg topology provides a feasible solution with a competitive performance/price ratio. Hence, it is expected to find its applications in low-cost or low-power ac motor drives.

References

[1] J. Itoh and K. Fujita, "Novel unity power factor circuits using zero-vector control for single-phase input systems," *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 36–43, Jan. 2000.

[2] H. S. Jung *et al.*, "Control of three-phase inverter for ac motor drive with small dc-link capacitor fed by single-phase ac source," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1074–1081, Mar./Apr. 2014.

[3] Y. Son and J. I. Ha, "Discontinuous grid current control of motor drive system with single-phase diode rectifier and small dc-link capacitor," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1324–1334, Feb. 2017.

[4] R. Maheshwari, S. Munk-Nielsen, and K. Lu, "An active damping technique for small dc-link capacitor based drive system," *IEEE Trans. Ind. Inform.*, vol. 9, no. 2, pp. 848–858, May 2013.

[5] C. B. Jacobina, N. Rocha, and E. C. D. S. Junior, "Single-phase to three-phase dc-link converters with reduced controlled switch count," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1150–1160, Mar./Apr. 2014.

[6] Z. Zeng *et al.*, "Hybrid space vector modulation strategy for torque ripple minimization in three-phase four-switch inverter-fed PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2122–2134, Mar. 2017.

[7] B. E. Badsi, B. Bouzidi, and A. Masmoudi, "DTC scheme for a four-switch inverter-fed induction motor emulating the six-switch inverter operation," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3528–3538, Jul. 2013.

[8] C. Zhu, Z. Zeng, and R. Zhao, "Comprehensive analysis and reduction of torque ripples in three-phase four-switch inverter-fed PMSM drives using space vector pulse-width modulation," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5411–5424, Jul. 2017.

[9] P. Karamanakos *et al.*, "Variable switching point predictive torque control for the four-switch three-phase inverter," in *Proc. 2013 IEEE Int. Symp. Sensorless Control Electr. Drives Predictive Control Electr. Drives Power Electron.*, 2013, pp. 1–8.

[10] R. Antal *et al.*, "Novel, four-switch, z-source three-phase inverter," in *Proc. 36th Annu. Conf. IEEE Ind. Electron. Soc.*, 2010, pp. 619–624.
[11] C. Xia *et al.*, "A current control scheme of brushless dc motors driven by four-switch three-phase inverters," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 547–558, Mar. 2017.
[12] S. Gairola, Priti, and L. N. Paliwal, "A new power converter for SRM drive," in *Proc. Int. Conf. Power, Control Embedded Syst.*, 2010, pp. 1–6.
[13] E. Sunan *et al.*, "The use of Miller converter for permanent magnet reluctance generator driven wind energy conversion system," in *Proc. Int. Conf. Electr. Mach. Syst.*, 2013, pp. 167–172.
[14] G. S. Buja, R. Menis, and M. I. Valla, "Variable structure control of an SRM drive," *IEEE Trans. Ind. Electron.*, vol. 40, no. 1, pp. 56–63, Feb. 1993.
[15] U. Abronzini *et al.*, "Steady-state dead-time compensation in VSI," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5858–5866, Sep. 2016.
[16] D. M. Park and K. H. Kim, "Parameter-independent online compensation scheme for dead time and inverter nonlinearity in IPMSM drive through waveform analysis," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 701–707, Feb. 2013.
[17] M. A. Herran *et al.*, "Adaptive dead-time compensation for grid-connected PWM inverters of single-stage PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2816–2825, Jun. 2013.
[18] J. M. Schellekens, R. A. M. Bierbooms, and J. L. Duarte, "Dead-time compensation for PWM amplifiers using simple feed-forward techniques," in *Proc. XIX Int. Conf. Electr. Mach.*, 2010, pp. 1–6.
[19] D. B. Rathnayake *et al*., "An enhanced pulse-based dead-time compensation technique for PWM-VSI drives," in *Proc. Int. Conf. Ind. Inf. Syst.*, 2015, pp. 1–5.
[20] R. W. Zhu and X. J. Wu, "Simplified SVPWM that integrates overmodulation and neutral point potential control," *J. Power Electron.*, vol. 14, no. 5, pp. 926–936, 2014.
[21] R. Bai *et al.*, "Research on double-close-loop fuzzy controlled SVPWM VSR for EV charger," in *Proc. Int. Conf. Power Electron. Syst. Appl.*, 2011, pp. 1–4.

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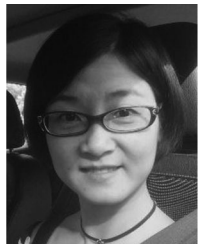

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