Flyback PFC With a Series-Pass Module in Cascode Structure for Input Current Shaping

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***Abstract*—A flyback power factor corrector (PFC) using a series-pass module (SPM) to shape its input current is presented. The input current is profiled by the SPM with its waveform controlled to be in the same wave shape and phase with the supply voltage and its magnitude controlled to regulate the output voltage. The SPM is constructed by two series-connected power semiconductor devices in a cascode structure. One of them is a high-voltage device of low ON-state resistance for sharing major voltage stress, while the other one is a low-voltage device with high-output impedance for profiling the current through the SPM. The SPM has a local control for clamping the voltage across the low-voltage device. Such arrangement allows the PFC to exhibit lower total input current harmonic distortion than that using a single high-voltage series-pass device. To minimize power loss, the operating point of the low-voltage device is regulated around the boundary between its high-gain and fully turn-ON operating region by adjusting the duty cycle of the main switch in the flyback converter. A 100-W 85–265-Vac/36-Vdc prototype has been built and evaluated. The conducted electromagnetic interference under different supply voltages will also be given.**

***Index Terms*—AC–DC power conversion, flyback converter, input filtering, power electronics, power factor corrector (PFC), power semiconductor filter, rectifiers, total harmonic distortion (THD).**

I. Introduction

FLYBACK power factor corrector (PFC) has been widely used in low-power applications. Its basic structure consists of a diode bridge for initial ac–dc rectification and a flyback dc–dc converter for shaping the waveform of the input current in phase with the supply voltage [1]. As the input current of the flyback dc–dc converter is pulsating, an input filter is required to prevent the unwanted pulsating current from getting into

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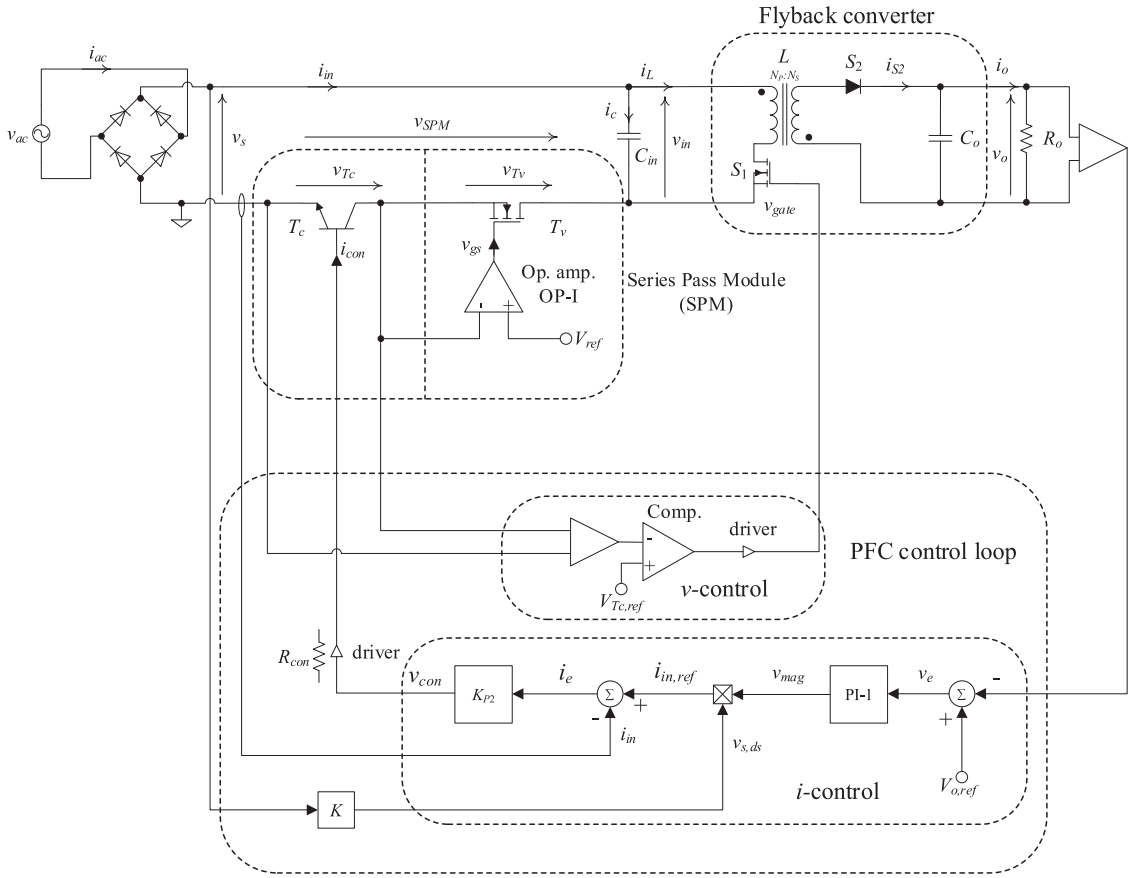


Fig. 1. Flyback PFC with a SPM.

Instead of using a single device, a cascode structure with two series-connected power devices to form a series-pass module (SPM) for profiling the input current is presented. One of them is a high-voltage device with low ON-state resistance for sharing major voltage stress, while the other one is a low-voltage device with high-output impedance for shaping the input current. The PFC can exhibit lower THD$_i$ than that with a single device for the SPD, even when the input current is small. A 100-W 85–265-Vac/36-Vdc prototype has been built and evaluated. A performance comparison with the PFC using a single high-voltage SPD will be given. The measurement results of the conducted electromagnetic interference (EMI) under different supply voltages will be presented.

II. System Architecture

Fig. 1 shows the proposed flyback PFC. The power conversion stage is similar to the standard one, except that a SPM is connected in series with the input of the flyback dc/dc converter. A capacitor $C_{\rm in}$ is connected at the input of the converter. The SPM comprises two series-connected power devices T_c and T_v which are in a cascode structure. T_c is a low-voltage bipolar junction transistor (BJT) and T_v is a high-voltage MOSFET. T_c is used to control the current through the SPM and T_v is used to regulate the voltage across T_c. An operational amplifier, OP-I, senses the voltage across T_c, v_{Tc}, compares it with a voltage reference $V_{\rm ref}$, and generates a control signal for T_v. If $v_{Tc} > V_{\rm ref}$, the gate-source voltage of T_v will be reduced. The effective output impedance of T_v will increase and the voltage across T_v will also be increased. The voltage across the SPM is mostly shared by T_v. If $v_{Tc} < V_{\rm ref}$, the gate-source voltage of T_v will increase. The effective output impedance of T_v will reduce and the voltage across T_v will reduce. Thus, the voltage across T_c is regulated at $V_{\rm ref}$ by such a feedback mechanism. The SPM is considered to be a current control device for profiling the input current of the flyback converter $i_{\rm in}$ [33], [34].

T_c is used to control the current through the SPM, as low-voltage BJTs have high Early voltage or, equivalently, high-output impedance [32] and [35]. Fig. 2 shows comparisons of the $i_c - v_{ce}$ characteristics of two BJTs. They are FZT853 and 2SC4140 with current ratings of 6 and 18 A, respectively, and voltage ratings of 100 and 400 V, respectively. The low-voltage BJT, FZT853, has high Early voltage and output impedance [32]. The collector current is relatively constant under a constant base current, irrespective to the variation of the collector–emitter voltage, resulting in small input current ripple for the flyback converter. Although operating a high-current, high-voltage BJT, 2SC4140, at low current can give a higher output impedance, for example, operating it at 2 A only, its utilization is low, and the saturation voltage is higher than FZT853 under a particular collector–emitter current. In addition, low-voltage BJTs have low saturation voltage, and, thus, have low conduction loss [32].

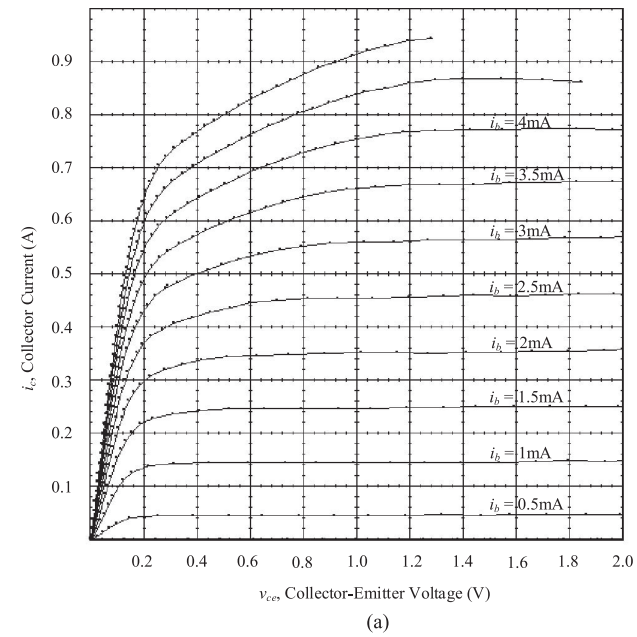


Fig. 2. $i_c - v_{ce}$ characteristics of two BJTs. (a) FZT853 (measured by Tektronix 370-A programmable curve tracer). (b) 2SC4140 (source: https://www.semicon.sanken-ele.co.jp/sk_content/2sc4140_ds_en.pdf) [38].

Hence, a low-voltage BJT is chosen for T_c to profile the input current of the flyback converter.

The current through T_c is controlled by the signal $v_{\rm con}$, generated by the controller "*i*-control." The operation is described as follows. The downscaled output voltage v_o of the PFC is sensed and compared with the output voltage reference $V_{o,\rm ref}$ to generate the error signal v_e. A proportional-plus-integral controller PI-1 is used to process v_e and generate the signal $v_{\rm mag}$ to determine the magnitude of $i_{\rm in}$. $v_{\rm mag}$ is multiplied by the downscaled rectified input voltage $v_{s,ds}$ to generate the input current reference $i_{\rm in,ref}$. The error i_e, which is the difference between $i_{\rm in}$ and $i_{\rm in,ref}$, is processed by another error amplifier K_{P2} to generate $v_{\rm con}$.

The voltage across T_c, v_{Tc}, is regulated by a peak-voltage modulator, namely "*v*-control." It is sensed and compared with a voltage reference $V_{Tc,\rm ref}$ to dictate the state of the main switch $\rm S_1$ of the flyback converter. If $v_{Tc} > V_{Tc,\rm ref}$, $\rm S_1$ will be turned OFF. $C_{\rm in}$ will undergo charging by $i_{\rm in}$ to reduce the voltage across SPM, $v_{\rm SPM}$. Conversely, if $v_{Tc} < V_{Tc,\rm ref}$, $\rm S_1$ will be turned ON. $C_{\rm in}$ will undergo discharging to the converter. If $v_{Tc} = V_{Tc,\rm ref}$, the state of $\rm S_1$ remains unchanged. To reduce the power loss of T_c, $V_{Tc,\rm ref}$ is set at a very low value, typically less than 1 V.

Fig. 3(a) shows the theoretical waveforms of the input current $i_{\rm in}$, flyback transformer current i_L, input capacitor current i_c, voltage across SPM $v_{\rm SPM}$, voltage across T_c v_{Tc}, and gate signal $v_{\rm gate}$ to $\rm S_1$. Fig. 3(b) shows the details of the waveforms in three switching cycles. Normally, $v_{Tc} < V_{\rm ref}$, T_v is fully turned ON. Thus

$$v_{\rm SPM} = v_{Tc} + i_{\rm in}\, R_{{\rm on},Tv} \tag{1}$$

where $R_{{\rm on},Tv}$ is the ON-state resistance of T_v.

The value of $i_{\rm in}$ is small near the zero crossings. $\rm S_1$ is turned OFF because $v_{\rm SPM}$ is high. $C_{\rm in}$ will undergo charging by $i_{\rm in}$ in order to reduce $v_{\rm SPM}$. However, as the value of $i_{\rm in}$ is small, the rate of rise of v_s is faster than the rate of rise of the voltage across $C_{\rm in}$, $v_{\rm in}$. v_{Tc} is regulated at $V_{\rm ref}$ by controlling the biasing condition of T_v through the OP-I. Thus

$$v_{Tv} = v_{\rm SPM} - V_{\rm ref}. \tag{2}$$

III. Principle of Operation

The principle of operation is described as follows. For simplicity, the following assumptions have been made.

1) All components are ideal.
2) v_s and $i_{\rm in}$ are constant within a switching cycle.

The flyback converter operates in CCM. Each cycle starts at $t_0 = (n-1)t_{\rm sw}$ and ends at $t_4 = n\,t_{\rm sw}$, where $t_{\rm sw}$ is the switching period. The circuit response in one period is described as follows.

1) Mode 1

As shown in Fig. 3(b), mode 1 starts at t_0 and ends at t_2

$$i_L(t) = I_L(t_0) + \frac{V_s - v_{\rm SPM}(t_0)}{L} t \tag{3}$$

$$\Delta i_L(t) = \frac{V_s - V_{\rm SPM,min}}{L}(t - t_0) \tag{4}$$

$$v_{\rm in}(t) = V_s - v_{\rm SPM}(t) \tag{5}$$

$$V_{\rm SPM,min} = v_{\rm SPM}(t_0) \;=\; V_{Tc,\rm ref} - \frac{I_{\rm in}}{C_{\rm in}} T_d \tag{6}$$

$$v_{\rm in}(t_0) = V_s - V_{\rm SPM,min} \tag{7}$$

where $t \in [t_0,\, t_2]$, $I_{\rm in}$, $I_L(t_0)$, and $\Delta i_L(t)$ are the average values of input current $i_{\rm in}$, the initial inductor current at the beginning of mode 1, and the change of inductor current in mode 1, respectively. V_s, $V_{\rm SPM,min}$, and $v_{\rm in}(t_0)$ are the average values of v_s, the minimum voltage across SPM, and the initial

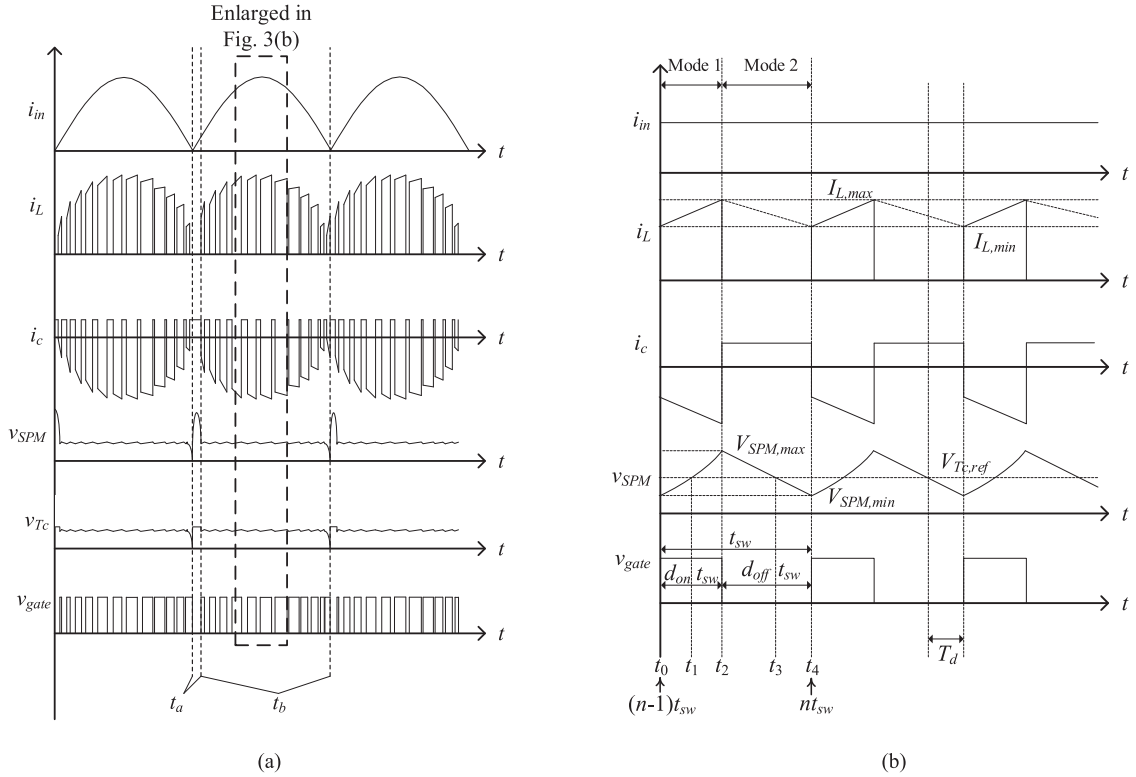


Fig. 3. Key voltage and current waveforms. (a) Theoretical waveforms. (b) Zoomed waveforms.

voltage across $C_{\rm in}$, equivalently input voltage of the flyback converter, respectively, at t_0

For $t \in [t_0,\ t_1]$

$$i_c(t) = I_{\rm in} - i_L(t) \tag{8}$$

$$v_{\rm in}(t) = \frac{1}{C_{\rm in}} \int_{t_0}^{t} i_c(\tau)\, d\tau + v_{\rm in}(t_0). \tag{9}$$

Substituting (3), (4), (6)–(8) into (9)

$$v_{\rm in}(t) = \frac{1}{C_{\rm in}} \left(I_{\rm in} - I_L(t_0)\right)(t - t_0) - \frac{1}{2C_{\rm in}} \frac{V_s - V_{\rm SPM,min}}{L}(t - t_0)^2 + V_s - V_{\rm SPM,min}. \tag{10}$$

Then, substituting (10) into (5)

$$v_{\rm SPM}(t) = -\frac{1}{C_{\rm in}} \left(I_{\rm in} - I_L(t_0)\right)(t - t_0) + \frac{1}{2C_{\rm in}} \frac{V_s - V_{\rm SPM,min}}{L}(t - t_0)^2 + V_{\rm SPM,min}. \tag{11}$$

Since the voltage across SPM equals $V_{Tc,\rm ref}$ at $t = t_1$, by using (11), the time duration $\Delta t_{01} = t_1 - t_0$ can be expressed as

$$\Delta t_{01} = t_1 - t_0 = \frac{I_{\rm in} - I_L(t_0) + I_x}{V_s - V_{\rm SPM,min}} L \tag{12}$$

where $I_x = \sqrt{\left(I_{\rm in} - I_L(t_0)\right)^2 + 2(V_s - V_{\rm SPM,min})\frac{T_d I_{\rm in}}{L}}$.

The time interval $[t_1,\ t_2]$ is determined by the propagation delay of the gate driver T_d. The duration of mode 1, $t_{\rm on}$ is

$$t_{\rm on} = \Delta t_{01} + T_d. \tag{13}$$

2) Mode 2

As shown in Fig. 3(b), mode 2 starts at t_2 and finishes at t_4. At $t = t_2$, the voltage across the SPM and the inductor current reach their peak values. Based on (11), the maximum voltage across the SPM is

$$V_{\rm SPM,max} = -\frac{1}{C_{\rm in}} \left[I_{\rm in} - I_L(t_0)\right] t_{\rm on} + \frac{1}{2\,C_{\rm in}} \frac{V_s - V_{\rm SPM,min}}{L} t_{\rm on}^2 + V_{\rm SPM,min}. \tag{14}$$

Based on (4), the maximum inductor current $I_{L,\rm max}$ is

$$I_{L,\rm max} = I_L(t_0) + \frac{V_s - v_{\rm SPM}(t_0)}{L} t_{\rm on}. \tag{15}$$

$C_{\rm in}$ is being charged by the input current $I_{\rm in}$. The change of charge stored in $C_{\rm in}$ over mode 2, $\Delta Q_{\rm cin}|_{t_{\rm off}}$, can be expressed as

$$\Delta Q_{\rm cin}|_{t_{\rm off}} = I_{\rm in} t_{\rm off} \tag{16}$$

where $t_{\rm off}$ is the time duration of mode 2.

$t_{\rm off}$ is composed of two subintervals, including $\Delta t_{23} = t_3 - t_2$ and $\Delta t_{34} = t_4 - t_3$. For Δt_{23}, the change of charge

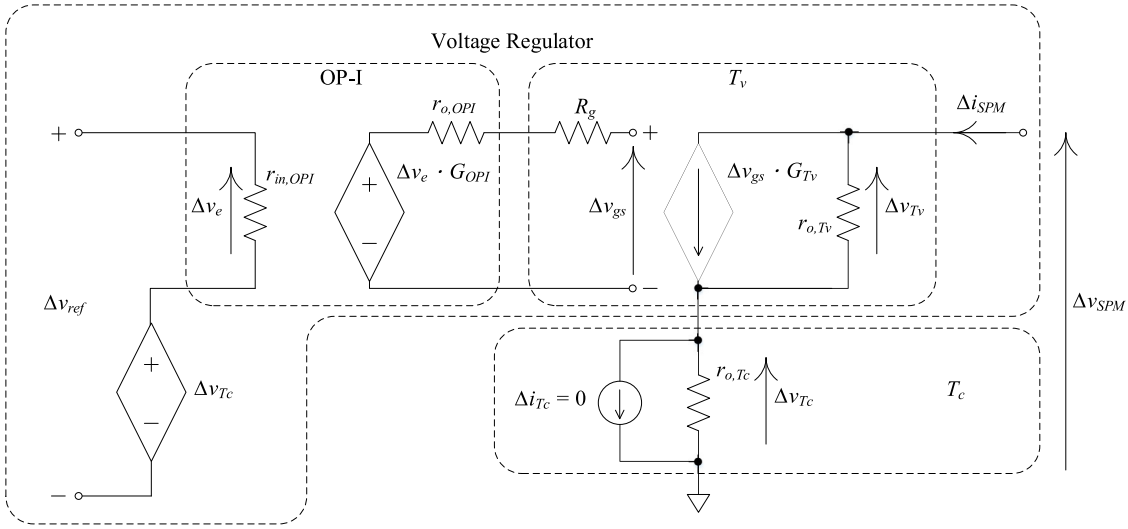


Fig. 4. Low-frequency model of the cascode structure.

stored in $C_{\rm in}$, $\Delta Q_{\rm cin}|_{t_{23}}$, is

$$\begin{aligned}\Delta Q_{\rm cin}|_{t_{23}} &= I_{\rm in}\ \Delta t_{23} \\ &= C_{\rm in}\ (V_{\rm SPM,max} - V_{Tc,\rm ref}).\end{aligned} \tag{17}$$

Based on (17), Δt_{23} can be expressed as

$$\Delta t_{23}\ =\ \frac{C_{\rm in}\ (V_{\rm SPM,max} - V_{Tc,\rm ref})}{I_{\rm in}}. \tag{18}$$

Since the time interval $[t_3, t_4]$ is determined by the gate drive propagation delay T_d. The duration of mode 2, $t_{\rm off}$, is

$$t_{\rm off}\ =\ \Delta t_{23}\ +\ T_d. \tag{19}$$

By combining (13) and (19), the switching frequency $f_{\rm sw}$ of the converter is

$$f_{\rm sw}\frac{1}{t_{\rm sw}} = \frac{1}{t_{\rm on} + t_{\rm off}} \tag{20}$$

and the duty cycle $d_{\rm on}$ is

$$d_{\rm on} = \frac{t_{\rm on}}{t_{\rm on} + t_{\rm off}}. \tag{21}$$

The main switch $\rm S_1$ is OFF around the zero crossings. There is no current flowing through the flyback inductor, i.e., $i_L\ =\ 0$. The voltage across the SPM over the time interval is expressed as

$$\begin{aligned}v_{\rm SPM}(t) &= V_{s,\rm Peak}\sin\omega t - v_{\rm in}(t) \\ &= V_{s,\rm Peak}\sin\omega t - \frac{1}{C_{\rm in}}\int_0^t i_{\rm in}(\tau)d\tau \\ &= V_{s,\rm Peak}\sin\omega t - \frac{I_{\rm in}(1-\cos\omega t)}{\omega C_{\rm in}}\end{aligned} \tag{22}$$

where $V_{s,\rm Peak}$ and $I_{\rm in,Peak}$ are the peak values of the rectified supply voltage and current, respectively, and ω is the angular line frequency.

By differentiating (22), the time $t_{VT,\rm Peak}$, at which v_T is maximum, is

$$t_{VT,\rm Peak}\ =\ \frac{1}{\omega}\tan^{-1}\left(\frac{V_{s,\rm Peak}\ C_{\rm in}}{I_{\rm in,Peak}}\right). \tag{23}$$

Thus, the value of the peak voltage across SPM, $V_{\rm SPM,Peak}$, can be determined by subtituting (23) into (22) with $v_{\rm SPM}(t_{VT,\rm Peak})\ =\ V_{\rm SPM,Peak}$. The voltage across the SPM is maximum when the input current is small, i.e., in the vicinity of the zero crossings of the supply voltage, as shown in Fig. 3(a). If a single SPD is used, it is necessary to shape the input current and withstand high-voltage stress. Modern power devices are generally designed and optimized for switching operations. Thus, selection of a suitable power device that can meet the above objectives is limited. The proposed cascode structure utilizes a low-voltage device of low saturation voltage to control the input current and a high-voltage device to share major voltage stress. The high-voltage device is dominantly in switching operation.

A power loss comparison between a single SPD and SPM can be studied by considering two time intervals t_a and t_b, as shown in Fig. 3(a). Within the time interval t_a, the voltage across a single SPD or the voltage across the SPM is unregulated and is determined by (22). Within the time interval t_b, the voltage across the single SPD or the voltage across T_c in the SPM is regulated at $V_{Tc,\rm ref}$. Thus, the difference of the power dissipations of the two methods is the conduction loss of the high-voltage device.

IV. Output Impedance of the SPM

The output impedance of the cascode structure shown in Fig. 1 is studied. Fig. 4 shows the low-frequency small-signal model of the SPM. For the sake of simplicity, the driving signal to T_c is assumed to be constant. This is valid as the variation of the current through the SPM, i.e., i_{Tc} (or equivalently the input current of the PFC $i_{\rm in}$) is much slower than the variation of the voltage

across the SPM. Thus, the variation of the output current source in T_c is neglected, that is, $\Delta i_{Tc} = 0$. The parameters $r_{\text{in,OPI}}$, $r_{o,\text{OPI}}$, and G_{OPI} are the input resistance, output resistance, and voltage transfer gain of OP-I, respectively. R_g is the gate resistor for driving T_v. G_{Tv} and $r_{o,Tv}$ are the transconductance and output impedance of T_v, respectively. $r_{o,Tc}$ is the output impedance of T_c. Thus, the variation of the voltage across SPM is Δv_{SPM} and the variation of the current through the SPM is Δi_{SPM}. The output impedance of SPM $R_{o,\text{SPM}}$ can be expressed as

$$\begin{aligned} R_{o,\text{SPM}} &= \frac{\Delta v_{\text{SPM}}}{\Delta i_{\text{SPM}}} \\ &= \frac{\Delta v_{Tc} + \Delta v_{Tv}}{\Delta i_{\text{SPM}}} \\ &= \frac{r_{o,Tc} G_{\text{OPI}}\, G_{Tv} r_{o,Tv} \Delta i_{\text{SPM}} + r_{o,Tv} \Delta i_{\text{SPM}} + r_{o,Tc} \Delta i_{\text{SPM}}}{\Delta i_{\text{SPM}}} \\ &= (r_{o,Tc}\, G_{\text{OPI}}\, G_{Tv} + 1)\, r_{o,Tv} + r_{o,Tc} \end{aligned} \tag{24}$$

where $r_{o,Tc} G_{\text{OPI}} G_{Tv}$ is the dominant term in the above expression. Hence, $R_{o,\text{SPM}} >> r_{o,Tc}$. In other words, the current through the SPM is then less affected by the variation of the voltage across the SPM. The performance is equivalent to a single SPD with high Early voltage. More importantly, a low-voltage device for T_c with high Early voltage can be used to control the current.

V. Design Procedures

The values of major components in the converter and the SPM are designed as follows.

A. Flyback Converter

The values of the input capacitor C_{in} and inductor L are designed by the following parameters.

T_d	Propagation delay of the gate driver.
$V_{\text{SPM,sat}}$	Saturation voltage of the SPM.
$V_{\text{SPM,min}}$	Minimum voltage across the SPM.
$V_{Tc,\text{ref}}$	Reference voltage for the SPM.
$V_{\text{ac,max}}$	Peak value of the supply voltage under high-line condition, i.e., 265 Vrms.
V_o	Rated average output voltage of the PFC.
P_o	Rated power of the PFC.
$I_{\text{ac,min}}$	Peak value of the supply current at the rated power and low-line condition.
$f_{\text{sw. min}}$	Switching frequency when the supply current is maximum at the high-line condition.

1) Input Capacitor C_{in}: In order to ensure that the SPM operates in the linear region over the operating range

$$V_{\text{SPM,min}} > V_{\text{SPM,sat}}. \tag{25}$$

Based on (6), as the voltage across the SPM at the beginning of a switching cycle is close to its minimum value $V_{\text{SPM,min}}$

$$V_{\text{SPM,min}} \approx V_{Tc,\text{ref}} - \frac{I_{\text{ac,min}}}{C_{\text{in}}} T_d. \tag{26}$$

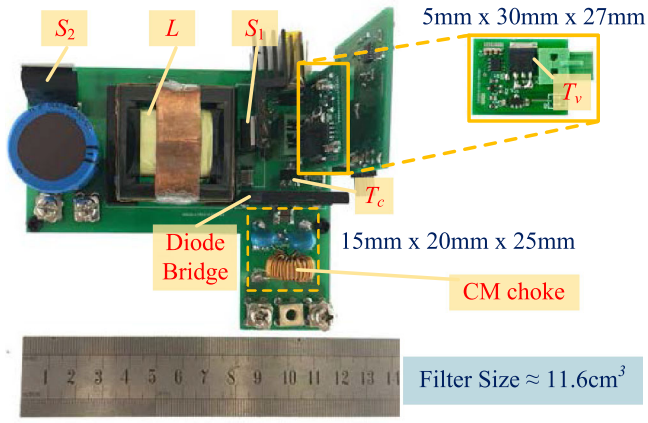


Fig. 5. Hardware prototype with the key components labeled.

By substituting (26) into (25)

$$C_{\text{in}} > \frac{I_{\text{ac,min}}\, T_d}{V_{Tc,\text{ref}} - V_{\text{SPM,sat}}}. \tag{27}$$

2) Magnetizing Inductance L: The flyback converter is designed to operate in CCM. The value of L is determined by considering the operation at the peak input current under the high-line condition. The peak inductor current I_P at the rated power and high-line condition is

$$I_p = \frac{4\, P_o}{V_{\text{ac,max}}}. \tag{28}$$

The dc voltage conversion ratio of flyback converter is

$$\frac{V_o}{V_{\text{ac,max}}} = \frac{D_{\text{min}}}{1 - D_{\text{min}}} \frac{N_S}{N_P} \tag{29}$$

where D_{min} is the duty cycle of the main switch when the supply current is maximum under the rated load and high-line condition and N_P and N_S are the number of turns of the primary and secondary windings in the flyback transformer.

D_{min} can be expressed as

$$D_{\text{min}} = t_{\text{on,min}} f_{\text{sw,min}} \tag{30}$$

where $t_{\text{on,min}}$ is the conduction time of the main switch.

By substituting (30) into (29)

$$t_{\text{on,min}} = \frac{V_o}{V_{\text{ac,max}} f_{\text{sw,min}}} \frac{1}{\frac{V_o}{V_{\text{ac,max}}} + \frac{N_S}{N_P}}. \tag{31}$$

Thus, when the converter is in mode 1

$$I_P = \frac{V_{\text{ac,max}}}{L} t_{\text{on,min}}. \tag{32}$$

Based on (28), (29), and (32)

$$L = \frac{V_{\text{ac,max}} V_o}{4\, P_o\, f_{\text{sw,min}} \left(\frac{V_o}{V_{\text{ac,max}}} + \frac{N_S}{N_P} \right)}. \tag{33}$$

B. Series-Pass Module

T_c and T_v in the SPM are designed by considering their operating voltages and currents. The minimum voltage rating of T_c

TABLE I
LIST OF MAJOR COMPONENTS USED IN THE PROTOTYPE

Component	Value / Part Number	Component	Value / Part Number
T_c	FZT853	C_{in}	1μF
T_v	STB45N40DM2AG	C_o	3000μF
L	180μH	Controller	STM32F334C8T6
S_1	8N65M5G4089	S_2	C3D20060

TABLE II
CONTROL PARAMETERS USED IN THE PROTOTYPE

Parameters of the proposed system	Value
Proportional gain of the controller PI-2, K_{P2}	0.01
Scaling factor for v_s sensing, K	1/175.1
Proportional gain of the controller PI-1, K_{P1}	0.9
Integral gain of the controller PI-1, K_I	0.005

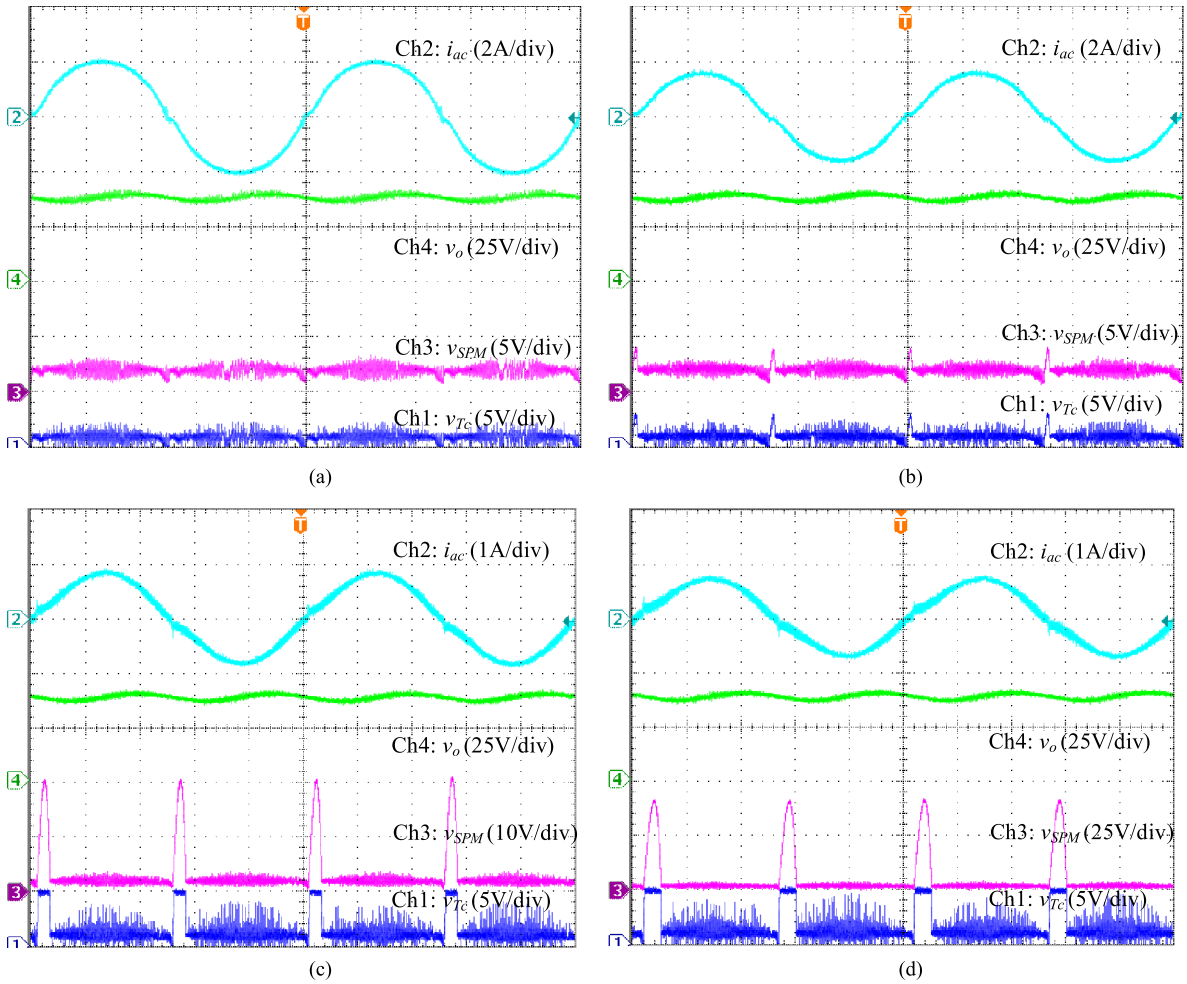


Fig. 6. Steady-state waveform with the output power of 100 W (timebase: 4 ms/div). (a) v_s = 85 Vrms. (b) v_s = 110 Vrms. (c) v_s = 220 Vrms. (d) v_s = 265 Vrms.

equals $V_{\rm ref}$, as the voltage across T_c is regulated by controlling the biasing condition of T_v. The minimum current rating of T_c equals $I_{ac,\min}$, which is the peak current through SPM under the low-line condition. Moreover, in order to reduce the input current ripple of the PFC, T_c with high Early voltage is chosen.

The minimum voltage rating of T_v equals $V_{ac,\max}$-the worst-case condition when the value of v_s is maximum and the voltage across $C_{\rm in}$ is zero. Similar to the design for T_c, the minimum current rating of T_v equals $I_{ac,\min}$. To reduce conduction loss, the ON-state resistance of T_v should be chosen to be small.

VI. Experimental Verifications

A 100-W 85–265-Vac/36-Vdc prototype with the SPM has been built. The converter is designed to operate in CCM for reducing current stress and losses, as discussed in [36] and [37]. Fig. 5 shows the prototype with the part numbers or values of the major components listed in Table I. The control parameters used in the prototype are given in Table II. A microcontroller, STMicroelectronics STM32F334C8T6, is used to control the PFC. The filtering performance is studied by operating the prototype without additional input filter. The steady-state performances, conducted EMI, transient responses, and performance comparison with the PFC using a single SPD are reported.

A. Steady-State Operations

Fig. 6(a)–(d) shows the steady-state waveforms of $i_{\rm ac}$, v_o, $v_{\rm SPM}$, and v_{Tc} under the full-load condition of 100 W with v_s equal to 85, 110, 220, and 265 Vrms, respectively. With $v_s = 85$ Vrms and 110 Vrms, the voltage stress across the SPM is less than 3 V. However, with $v_s = 220$ Vrms and 265 Vrms, the peak voltages across SPM are 20 and 40 V, respectively. Nevertheless, the voltage across T_c can still be maintained to be lower than 5 V, confirming the function of regulating the voltage across T_c with the cascode structure. Thus, a low-voltage device with high Early voltage can be used for T_c.

Fig. 7 shows the switching frequency versus the instantaneous value of the supply voltage. With the supply voltage varying from 10 to 375 V, the switching frequency varies from 150 to 770 kHz.

Fig. 8 shows the detailed waveforms of the prototype when the supply voltage is maximum. The flyback converter is in CCM. The measured waveforms are in close agreement with the theoretical ones in Fig. 3(b). The input current $i_{\rm ac}$ contains less harmonics, even if the input current of the flyback converter is pulsating and the voltage across the SPM contains high-frequency ripples, confirming that the SPM exhibits high-output impedance.

Fig. 9 shows the measured input power factors under different supply voltages with the load varying from 25% to 100% of the rated condition. With the supply voltage of 85 and 110 Vrms, the input power factor can be maintained around 0.99 from 25% to 100% of the rated load. With the supply voltage of 220 and 265 Vrms, the input power factor is high under the heavy-load condition. However, it reduces under the light-load condition,

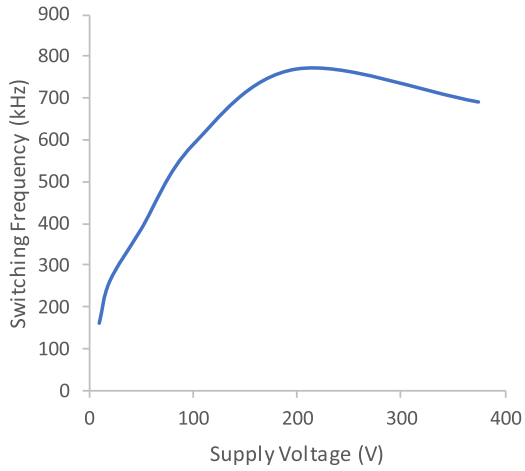


Fig. 7. Relationship between the switching frequency and supply voltage.

because the input current becomes very small and the tracking capability of the error amplifier K_{P2} reduces. Nevertheless, the input power factor can still be maintained higher than 0.91.

Fig. 10 shows the measured THD$_i$ under different supply voltages and loading conditions. Under the rated load condition, the THD$_i$ is around 6% and increases with the decrease of the loading condition. It is generally lower under low-line condition, where the input current is high and its distortion is low.

Fig. 11 (a) and (b) compares the THD$_i$ spectra with the limit line defined in EN61000-3-2 [2] under the supply voltages higher or equal to 220 Vrms at the rated load condition for Class D equipment. Results show that the spectra are sufficiently lower than the limits, which confirm the harmonic rejection function of the proposed technique.

Fig. 12 shows the measured power conversion efficiency of the prototype (with the EMI filter shown in Fig. 16 included) operating under different supply voltages and loading conditions. The efficiency varies between 81% and 88%. Fig. 13 shows the power dissipation measurement of the SPM under different loading conditions. The power dissipation is less than 1.2 W at the full-load condition. With the reduced loading at high supply voltage (220 and 265 Vrms), the power dissipation across the SPM increases. Further discussion on this issue will be discussed.

Fig. 14 shows the temperature distribution of the components at the full-load condition (100 W) with $v_s = 85$ Vrms. The major lossy components are diode bridge, main switch S_1, flyback transformer, and output rectifier S_2. T_c and T_v do not have high-power dissipations.

B. Conducted EMI

Based on the EMC standard EN55022 Information technology equipment—radio disturbance characteristics—limits and methods of measurement [3] Class B ITE, the conducted EMI of the prototype under different supply voltages is measured. The results are shown in Fig. 15. The measured EMI is above the limit line. Therefore, a common-mode (CM) choke and

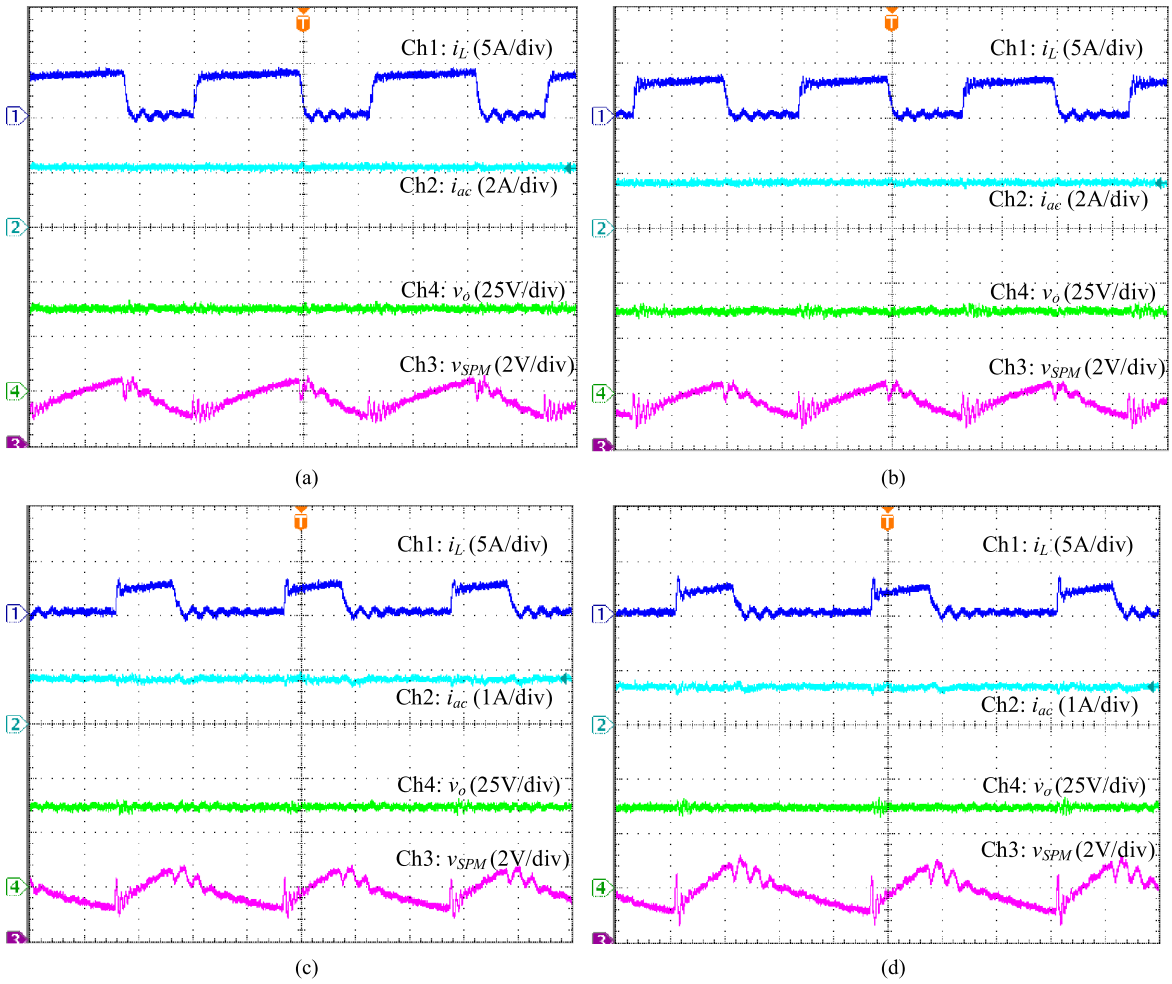


Fig. 8. Detailed waveforms (timebase: 4 μs/div). (a) v_s = 85 Vrms. (b) v_s = 110 Vrms. (c) v_s = 220 Vrms. (d) v_s = 265 Vrms.

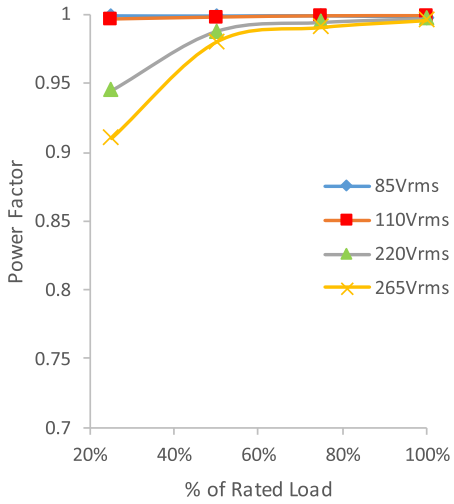


Fig. 9. Measured input power factor under different supply voltages and loading conditions.

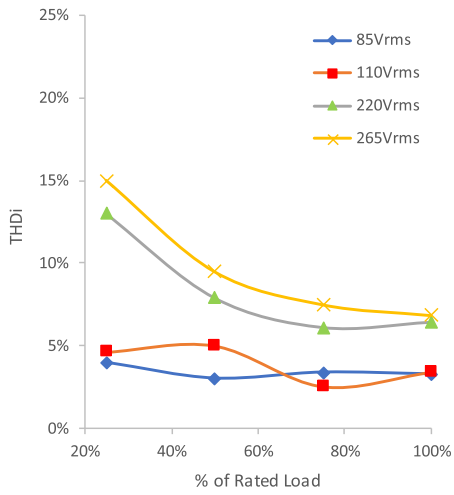


Fig. 10. Measured THD$_i$ under different supply voltages and loading conditions.

a pair of Y capacitors are connected to the input side, and a capacitor is connected between the source pin of S_1 and positive terminal of output winding. Moreover, to further suppress the differential-mode noise within the range of switching frequency, i.e., below 800 kHz, a chip capacitor is connected between live and neutral. The above passive input filter is shown in Fig. 5 and the connection is shown in Fig. 16.

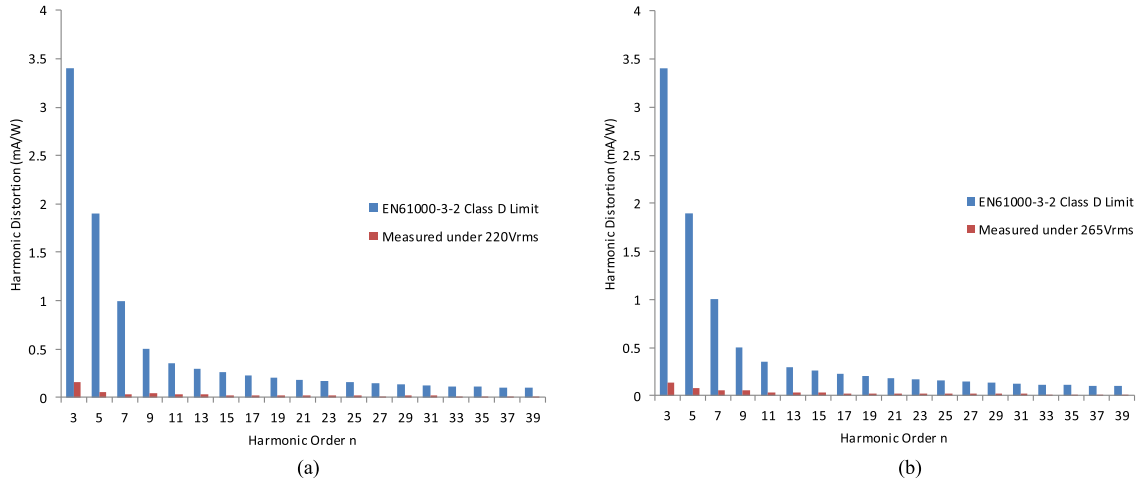


Fig. 11. Comparisons with EN61000-3-2 under different line voltages. (a) v_s = 220 Vrms. (b) v_s = 265 Vrms.

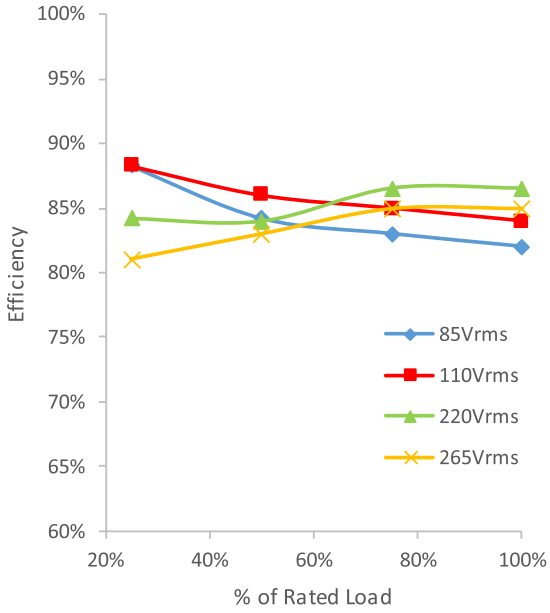


Fig. 12. Measured efficiency.

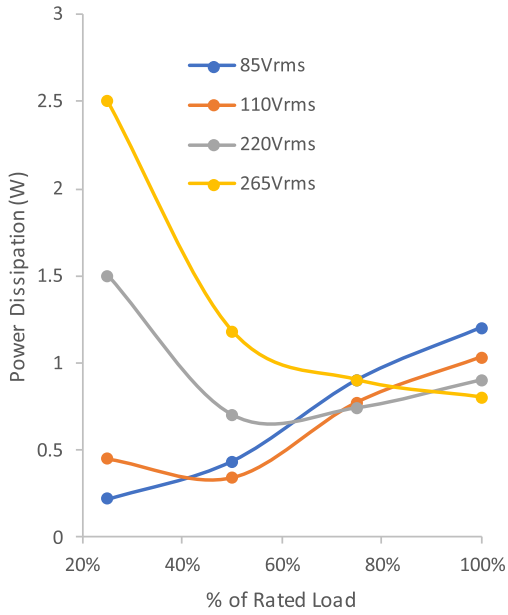


Fig. 13. Measured power dissipations on the SPM.

Fig. 17(a)–(d) shows the conducted EMI measurement results. All measurement results are found to be lower than the limit.

C. Transient Responses

Fig. 18(a)–(d) shows the dynamic responses when the load is switched between 50% and 100% of the rated power. Results show that power factor correction can still be maintained during the transient periods. More importantly, the voltage across T_c is still regulated at a value lower than 5 V, even if the voltage across the SPM is high.

D. Comparisons With a Single SPD

The THD_i of the prototype is compared with the THD_i of the PFC using a single SPD. The SPD is 2SC4140 [38]. Fig. 19

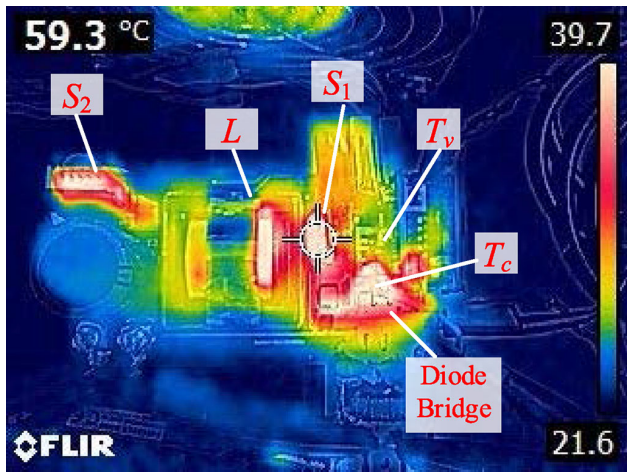


Fig. 14. Temperature distribution of the components.

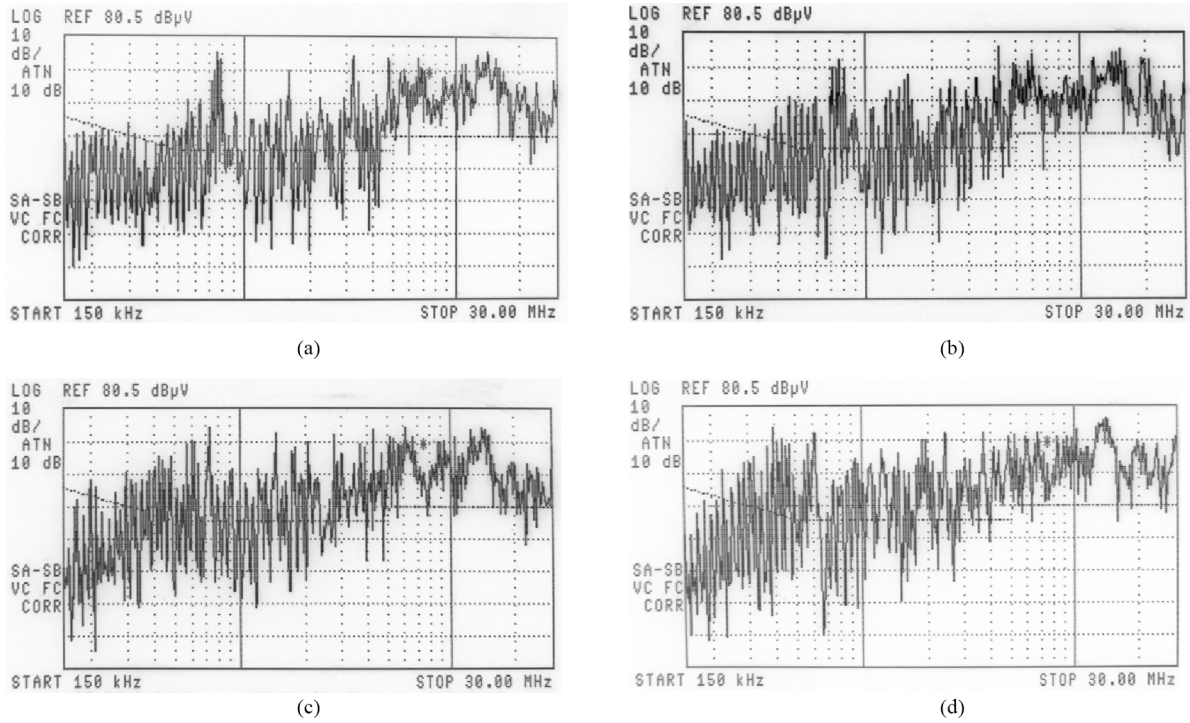


Fig. 15. Conducted EMI under different supply voltages (without added input filter). (a) 85 Vrms. (b) 110 Vrms. (c) 220 Vrms. (d) 265 Vrms.

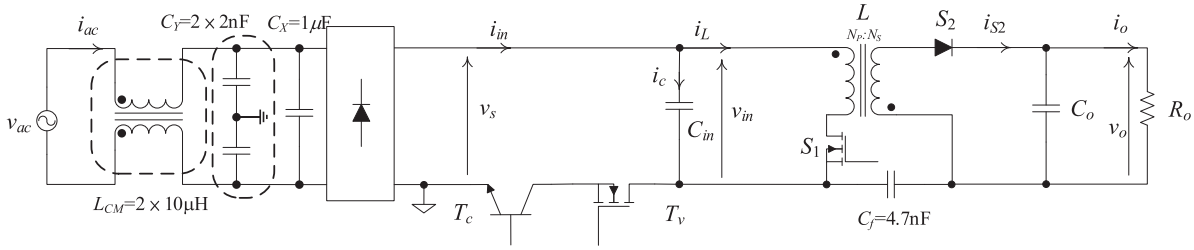


Fig. 16. Architecture of the PFC with a passive filter added.

shows the measured THD_i and efficiency. $V_{Tc,\text{ref}}$ is set at 1 V in both cases. The efficiency with the SPM is a little bit lower than that with a single SPD. However, the SPM improves the THD_i and effectively handles high-voltage stress under small input current, confirming the merit of the cascode structure in profiling the input current.

E. Comparisons With a Conventional Flyback Converter

A commercially available 50-W flyback ac/dc evaluation board, STMicroelectronics STEVAL-ISA142V1 [39], is chosen to compare with the proposed prototype. Fig. 20 shows the pictures and dimensions of the evaluation board. The physical volume of the input filtering section of the proposed prototype (see Fig. 5) is 5 mm × 30 mm × 27 mm + 15 mm × 20 mm × 25 mm = 11.6 cm^3 and that of the evaluation board is 50 mm × 30 mm × 27 mm = 40.7 cm^3. Thus, the physical size of the input filter in the prototype is much smaller.

Regarding the power loss of the input filter section, a comparison is made. For the sake of comparison, the proposed system is also operated at the same output power of 50 W. Fig. 21(a) and (b) shows the temperature distributions of the evaluation board and the proposed prototype operating at the output load of 50 W and with the supply voltage of 85 Vrms. The CM choke of the evaluation board has the temperature rise of 13.4 °C, while the proposed SPM has the temperature rise of 20 °C and the CM choke has negligible temperature rise. The temperature distributions show the hot spots in the converter. Fig. 22 shows a comparison between the power dissipation of the passive input filter on the evaluation board and the SPM under the load condition of 50 W and different supply voltages.

For the sake of fairness, the power dissipations of the passive filter on the board and the SPM are compared. It is due to the following reasons.

1) The prime function of the proposed power semiconductor filter is to perform input filtering of the flyback ac/dc converter. It is more appropriate to emphasize on studying its

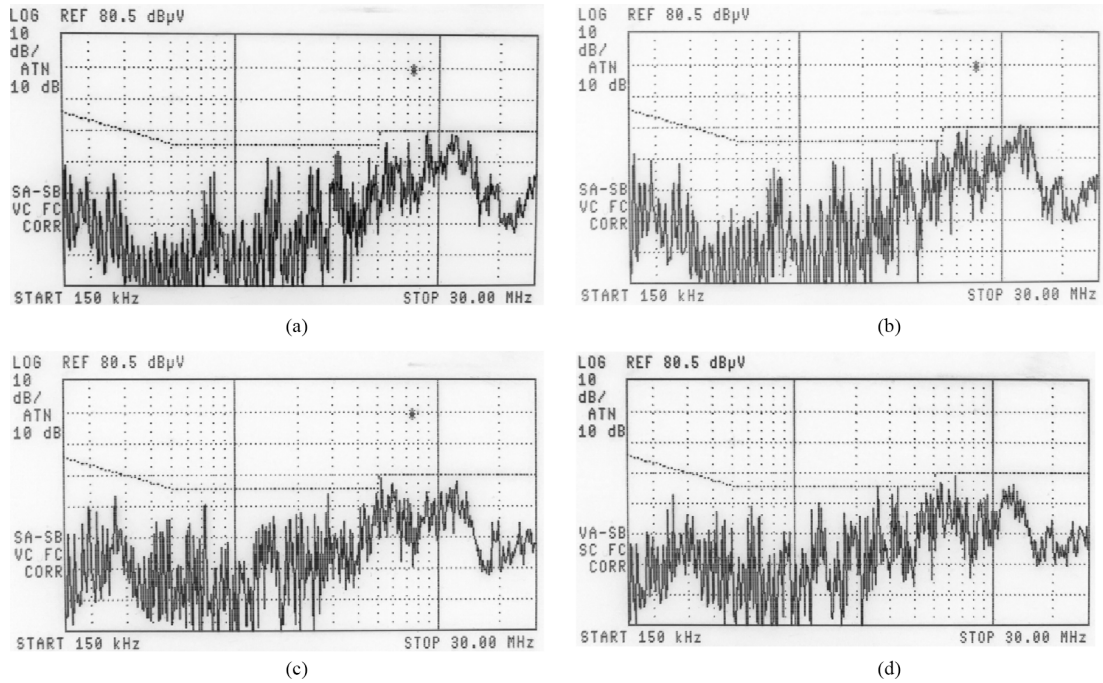


Fig. 17. Conductive EMI with the added passive filter in Fig. 16. (a) 85 Vrms. (b) 110 Vrms. (c) 220 Vrms. (d) 265 Vrms.

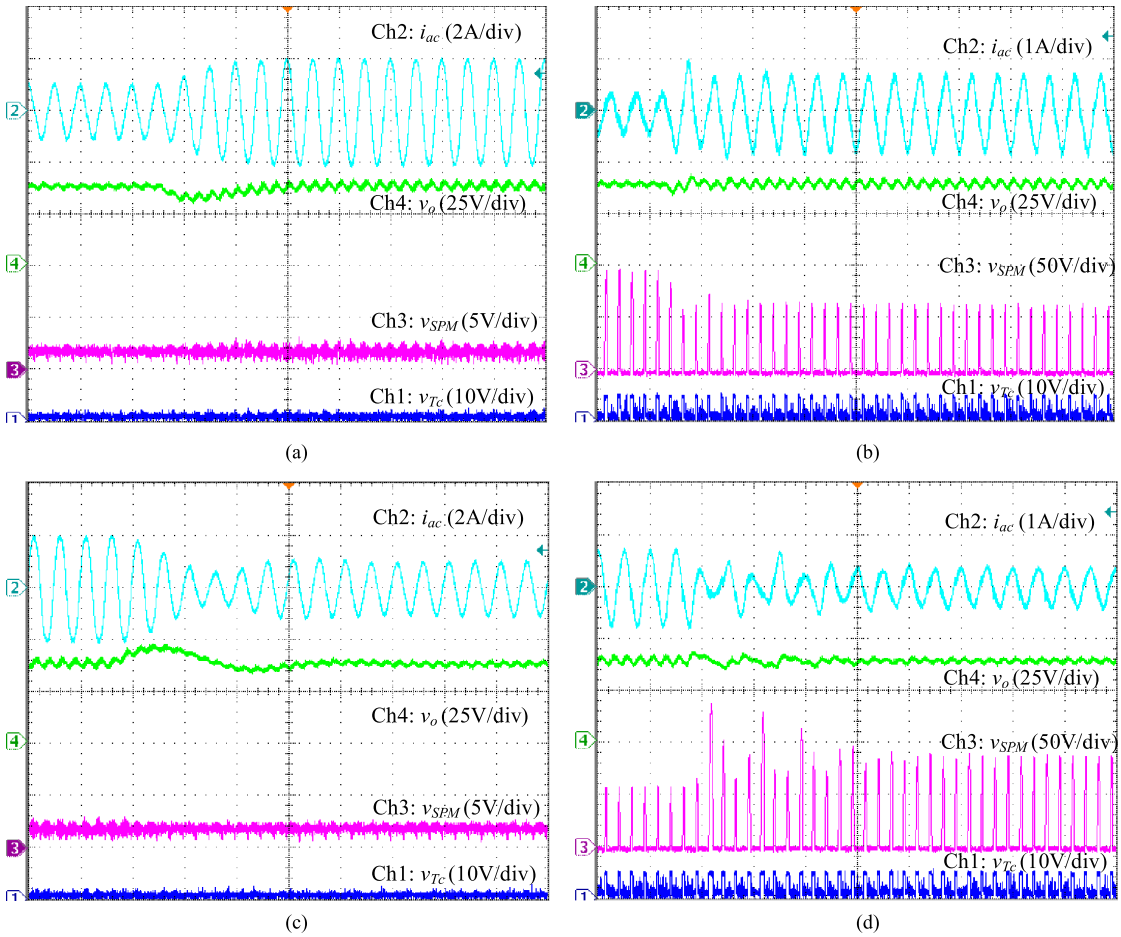


Fig. 18. Dynamic responses. (a) v_s = 85 Vrms, from 50% to 100% load. (b) v_s = 265 Vrms, from 50% to 100% load. (c) v_s = 85 Vrms, from 100% to 50% load. (d) v_s = 265 Vrms, from 100% to 50% load.

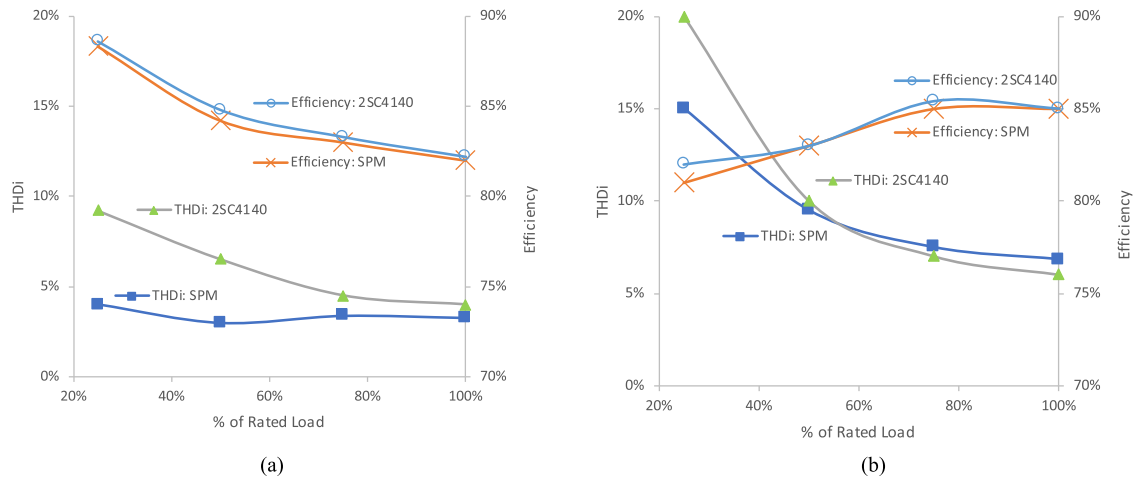


Fig. 19. Measured THD$_i$ and efficiency. (a) $v_s = 85$ Vrms. (b) $v_s = 265$ Vrms.

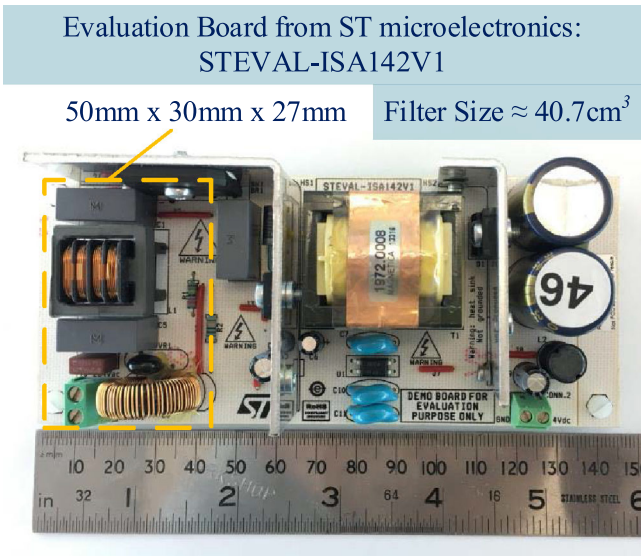


Fig. 20. Picture of the evaluation board.

performance characteristics and benchmarking its power loss with the passive filter.

2) The total power loss of the whole converter consists of the power dissipation of the input filter and that of the power conversion stage, i.e., the flyback converter. If the power losses of the two converters are compared, it would be difficult to make a fair comparison on the performance of the two types of filtering techniques. Moreover, there are many factors that might affect the efficiency of the power conversion stage.

The power loss of the SPM is lower than that of the passive filter when the supply voltage is low. It will increase as the supply voltage increases. Conversely, the power loss of the passive filter decreases as the supply voltage increases. The phenomena can be explained by the following simplified models.

Fig. 23 shows the structure of the input filter section of the evaluation board. The main lossy components are the inductive components L_1 and L_3. For the sake of simplicity, their total power loss $P_{P,T}$ can be approximated by

$$P_{P,T} = {I_{\rm ac}}^2 \, (2\, R_{L1} + R_{L3}) \tag{34}$$

where $I_{\rm ac}$ is the RMS value of the input current, and R_{L1} and R_{L3} are the dc resistances of each winding in L_1 and L_3, respectively.

The power loss of the SPM $P_{\rm SPM}$ can be approximated by

$$P_{\rm SPM} = I_{\rm ac}\, V_{\rm SPM} \tag{35}$$

where $V_{\rm SPM}$ is the voltage across the SPM.

By comparing (34) and (35), it can be concluded that under the low-line condition

$$P_{\rm SPM} \le P_{P,T} \tag{36}$$

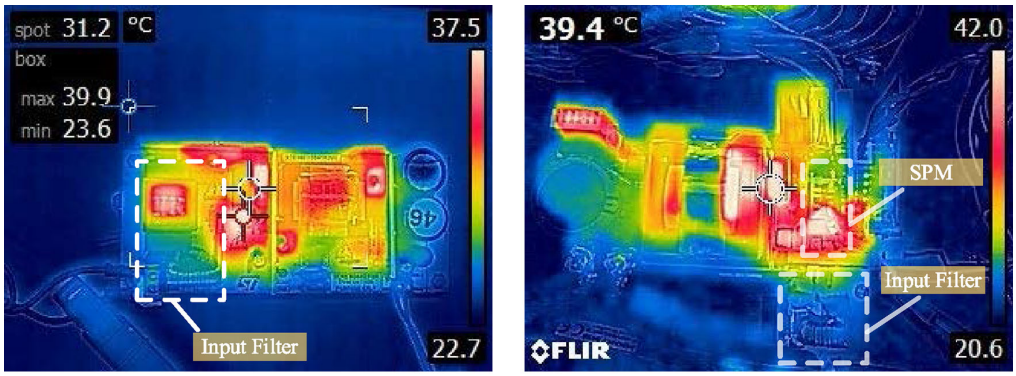
if

$$\begin{aligned} V_{\rm SPM} &\le I_{\rm ac}\, (2\, R_{L1} + R_{L3}) \\ &= \frac{P_{\rm ac}}{V_{\rm ac}}\, (2\, R_{L1} + R_{L3}) \end{aligned} \tag{37}$$

where $P_{\rm ac}$ is the input power of the converter and $V_{\rm ac}$ is the RMS value of the supply voltage.

The values of R_{L1} and R_{L3} are measured to be 0.8 and 0.4 Ω, respectively, and the value of $V_{\rm SPM}$ is regulated around 1 V at low-line condition. Thus, based on (37), when the output power is 50 W, $P_{\rm SPM} < P_{P,T}$, if the supply voltage is less than 100 V. The calculation is based on the assumption that the flyback converter has energy efficiency of 100%. The above results are in close agreement with the experimental results in Fig. 22.

Finally, Figs. 24 and 25 show the comparisons on their measured THD$_i$ and input power factor. Results show that the proposed method has a lower THD$_i$ and a higher power factor.



(a) (b)

Fig. 21. Comparison of the temperature distribution with the supply voltage of 85 Vrms at the output power of 50 W. (a) Evaluation board. (b) Proposed prototype.

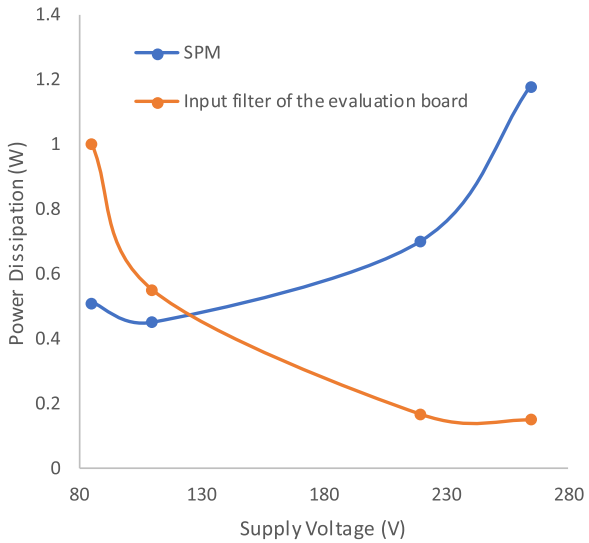


Fig. 22. Power dissipation of the SPM in the proposed prototype and passive input filter in evaluation board.

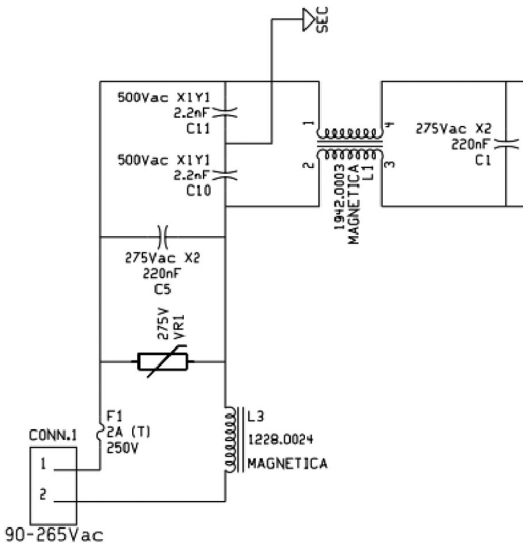


Fig. 23. Input filter section of the evaluation board [39].

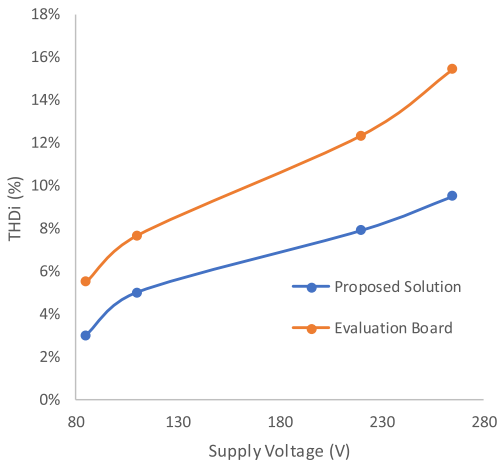


Fig. 24. Comparison of measured THD_i.

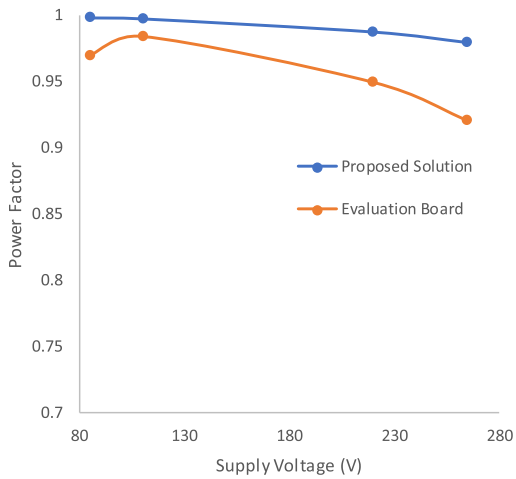


Fig. 25. Comparison of power factor.

VII. Conclusion

A flyback PFC using an SPM to shape the input current waveform and an input capacitor to absorb the high-frequency pulsating current generated by the flyback converter has been

presented. The SPM consists of two power devices, one high-voltage device of low ON-state resistance and one low-voltage device of high Early voltage, in a cascode structure. The high-voltage device is used to regulate the voltage across the low-voltage device at the desired operating point. The low-voltage device is used to regulate the current through the SPM. The following issues can be noted.

1) The proposed method is applicable for isolated and nonisolated converters operating in both CCM and discontinuous-conduction mode.
2) The SPM can be considered as a low-frequency controllable current source and the ripple current generated by the flyback converter is absorbed by the input capacitor.
3) The waveform of the input current is programmed by changing the control signal to the low-voltage device.
4) The proposed method can be applied to typical flyback PFC readily without significant hardware changes.
5) The conventional flyback PFC operating in discontinuous-conduction mode does not require current loop, while the proposed architecture requires an additional feedback loop. However, the complexity is justified by the input filtering performance. It is expected that the controller can be integrated to make the overall implementation be elegant.
6) Passive filters occupy considerable space and are costly, as compared to the other power components in the converter. Since the proposed input filtering technique is semiconductor-based, it is amenable to monolithic integration. It is expected that the semiconductor device and associated control devices for input filtering can be integrated together with the switching devices and controller for the flyback ac/dc converter, so as to reduce the cost and increase the power density of the converter. Nevertheless, the two power devices in the SPM are currently of different types. Their integration will have some technical barriers. Thus, further research will be dedicated to the design and implementation aspects.

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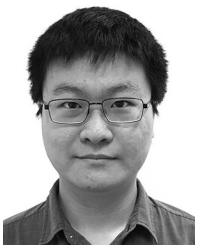

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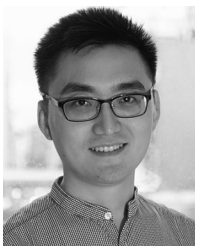
Mr. Tung received the HKIE Outstanding Paper Award for Young Engineers/Researchers, Hong Kong Institution of Engineers, for his research outputs on active filtering techniques for switching mode power supply in 2015.



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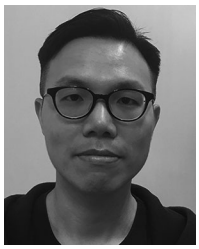

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