Flexible PCB-Based 3-D Integrated SiC Half-Bridge Power Module With Three-Sided Cooling Using Ultralow Inductive Hybrid Packaging Structure

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***Abstract*—Silicon carbide (SiC) devices are capable of high switching speeds and also enable high switching frequency in power electronic converters. However, this feature poses substantial challenges to packaging, especially limiting the loop inductance. The traditional wire-bonding packaged power module has large parasitic inductance, which will cause voltage overshoot, oscillation, parasitic turn-on, and EMI issues. In order to reduce the parasitic inductance, this paper proposes a flexible printed circuit board (FPCB) based full SiC half-bridge power module with a novel low inductive hybrid packaging structure and three-dimensional (3-D) integration method. This hybrid packaging structure has an ultrathin FPCB substrate stacked on a direct bonding copper (DBC) substrate, which forms a multilayer 3-D power loop. The SiC chips are soldered on the DBC substrate for good thermal dissipation through a cavity in the FPCB substrate. After power loop optimization, the power loop inductance of a 1200-V/120-A SiC power module is only 0.79 nH. The power module consists of three submodules, which are connected by the bendable FPCB substrate. The bendable power module enables maximum utilization of 3-D space. The gate drive, decoupling capacitors, and dc-link capacitors are also integrated and 3D-structured using rigid-flexible PCBs. Moreover, the cooling system is a high-efficiency three-sided cooling structure for the bendable power module. The simulation results show that the three-sided cooling structure reduces the heatsink volume by 50%. Applying this method, the converter can be designed as a system-in-package and a 3D-structured compact system. The power density of a 20-kW three-phase inverter will reach 19.3 kW/L based on this power module. In this paper, the 1200-V/120-A power module fabrication and assembly processes are given. Finally, the static and dynamic experimental comparisons are done for a commercial power module and the proposed power module. The experiment results show that the voltage overshoot of the proposed module**

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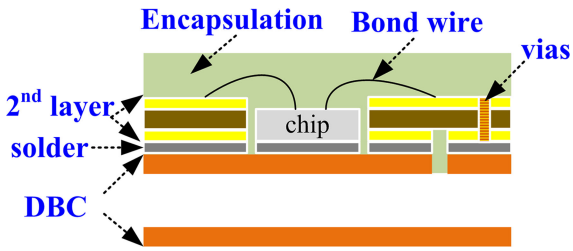

Fig. 1. Illustration of a hybrid packaging structure [27].

ductance about 15–30 nH. This requires the need to decrease the switching speed and add additional snubber circuit to protect the device [12].

In order to reduce the parasitic inductance, some new packaging structures and integration methods have been proposed. The packaging structures can be mainly divided into three types: wire-bonding structure, planar structure, and hybrid structure. The wire-bonding structure usually solders chips to a direct bonding copper (DBC) or other substrate, and the top pad of the chip is connected by bonding wires. The majority of Si MOSFET and IGBT modules are based on this technology. It is a two-dimensional (2-D) structure, and this structure has strong limitations with regards to parasitic control. But its advantages of maturity, simplicity, and low cost attract the attention of manufacturers [13]. An improved wire-bonded structure has been proposed by Chen *et al.* for a 1200-V/60-A SiC power module in 2013 [14]. This module adopted laminated busbar leadframe in a 2-D wire-bonded multichip SiC module to enhance the symmetrical Kelvin source connection for each switching device. However, this module has around 15-nH parasitic inductance. Planar packaging structure eliminates the bonding wires, such as the metal postinterconnect parallel plate [15], the dimple-array interconnect [16], the flip-chip on flex [17]–[19], the embedded power [20], and the power overlay [21], [22]. The planar structures bring the benefits of a smaller module footprint, lower parasitic impedances, and the possibility of double-sided cooling for the semiconductor devices [23]. However, it has complex fabrication processes. Liang *et al.* [24] proposed a 1200-V/200-A planar structure SiC power module, which has total commutation parasitic inductance of 13.58 nH. A flexible epoxy-resin substrate based vertical structure SiC power module is developed by Zhao *et al.* with a 1.3 nH power loop inductance [25]. This substrate has better thermal-stress management and lower cost. A 400-A, 1200-V SiC power module with 1 nH commutation inductance has been proposed by SEMIKRON, which uses a two-layer flexible board sintering on top of chips [26].

As a combination of these two technologies, the hybrid module has the planar structure to achieve the same footprint and volume density, and accomplishes the device top-side interconnections through wire-bonding to simplify fabrication and improve reliability. Thus, it does not require double-side solderable devices [23]. Hybrid packaging structure adopts benefits from both wire bonding and planar structure with a significant reduction of parasitic inductance. Fig. 1 shows the basic concept of the hybrid packaging structure. This concept utilizes multilayer substrates [DBC or printed circuit board (PCB) stacked on another DBC] and vias, which form a three-dimensional (3-D) current commutation loop to reduce parasitic inductance. The chips are placed on the bottom DBC for better thermal performance and vias are used connection between different layers. In [28], a novel hybrid packaging structure for high-temperature SiC power modules with 16 nH power loop inductance is proposed. Literature [23] designed a 1200 V/10 A phase-leg SiC module based on PCB stacked on DBC hybrid structure which has only 3.8 nH parasitic inductance. However, the power loop is not well designed into an overlapped 3-D loop to increase the mutual inductance, and the leadframe of power terminals still have large parasitic inductance. Literature [29] proposed a smaller 1200 V/24 A power module with an improved PCB stacked on DBC hybrid structure and the parasitic inductance can be reduced to 3.38 nH. But the power loop structure is not optimized. Literature [30] developed a 1.2 kV/100 A full SiC module based on DBC plus DBC structure in which the parasitic inductance was reduced to only 6.3 nH. However, the inductance of leadframe is still very large. It can be seen that the existing hybrid structure packaged high current power module has more than 5 nH of power loop inductance. If the terminal inductances are also included, the parasitic inductance will be even higher. Literature [31] introduced a wire-bonding SiC power module with a multilayer DBC substrate, which reduces the power loop stray inductance to 1.15 nH. However, the chips are soldered on top of the multilayer DBC which causes the thermal resistance to increase. This paper will introduce a new flexible PCB (FPCB) based 3-D hybrid ultra-low parasitic full SiC integrated power module, with the power loop inductance less than 1 nH [27]. Further, the terminal inductance is restricted to only 1.6 nH. The 2nd layer substrate is an ultra-thin FPCB different from the traditional hybrid structure, and the chips are placed on the top of the bottom DBC layer for high thermal performance. The parasitic inductance can be reduced extraordinarily. Meanwhile, a high current power module can be designed into three-sided cooling for the bendable FPCB connection between the submodules. The integrated converter system can realize high space utilization for the 3D-structured system-in-package design.

The organization of the paper is as follows. In Section II, the FPCB is introduced into the hybrid packaging structure and the mutual cancellation effect to obtain an optimized low inductive hybrid structure is used. In Section III, a 3-D high power density 1200-V/120-A full SiC power module is presented. Section IV provides the integration method and thermal management of this power module. The power module fabrication processes and experimental results are presented in Sections V and VI. Finally, conclusions are drawn on the efficacy of the presented work.

II. Low Inductive Hybrid Packaging Structure Design

A. Mutual Inductance Cancellation Principle

In the traditional 2-D wire-bonding structure, the inductance can be decreased by reducing the power loop length. However, this method has an inductance reduction limitation where the minimum distance between the chips (SiC dies) depends on the insulation and thermal dissipation requirements. In order to further reduce the parasitic inductance, the multilayer 3-D power

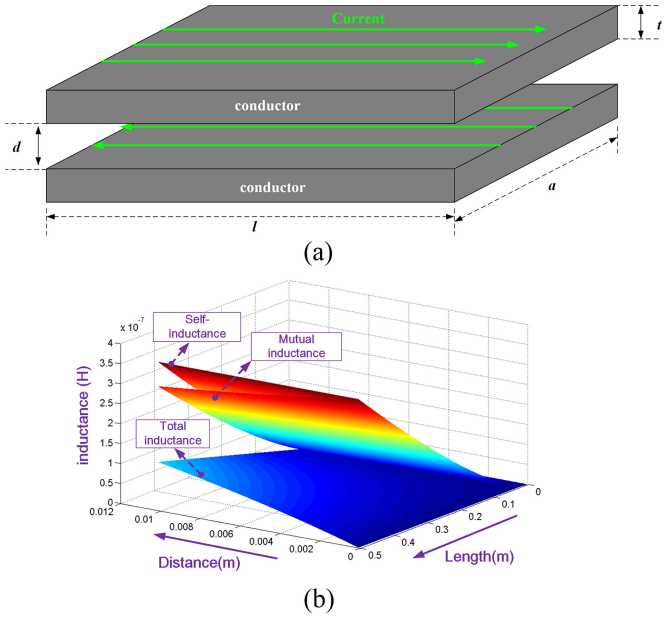

Fig. 2. Illustration of mutual inductance cancellation effect.

loop can be used. This can be easily achieved in a multilayer hybrid packaging structure.

Furthermore, this method can utilize the mutual inductance cancellation effect to reduce the parasitic inductance significantly, as shown in Fig. 2. This technology has been widely used in the laminated busbar design [32]. The inductance of two conductors with opposite current can be obtained using the following formula [33]:

$$L = \frac{u_0 l}{2\pi}\ln\left(\frac{2l}{t+a}+\frac{1}{2}\right) - \frac{u_0 l}{2\pi}\left[\ln\frac{2l}{d}+\frac{1}{2}-2\frac{d}{a}\tan^{-1}\frac{a}{d} - \frac{1}{2}\left(1-\frac{d^2}{a^2}\right)\ln\left(1+\frac{a^2}{d^2}\right)\right] \quad (1)$$

where l is the conductor length, a is the conductor width, t is the conductor thickness, and d is the distance between two conductors. The formula (1) indicates that the equivalent inductance equals to the self-inductance (first part) minus the mutual inductance (second part), and the parasitic inductance can be reduced by increasing the mutual inductance. Fig. 2(b) depicts the l and d influence to the parasitic inductance. Since the conductor thickness t and width w will be constant at a certain current and frequency, the influences of t and w will not be discussed. While l and d increase, the total inductance will increase. Besides, the inductance is more sensitive to the distance d between two conductors. Hence, in order to obtain the lowest inductance hybrid power module, it should follow these three principles: 1) opposite current loop to form mutual inductance; 2) reduce the insulation thickness to enforce the mutual inductance effect; and 3) reduce the power loop length to reduce total inductance.

In order to reduce the distance d, the thickness of the second layer substrate can be changed to a thinner substrate with high dielectric breakdown strength material. Table I gives three possible candidates. It can be seen that the FPCB has the highest dielectric breakdown strength about 10 times higher than DBC. Based on the Fig. 2(b), the 2nd layer substrate uses the thinnest

TABLE I
CHARACTERISTIC COMPARISON OF THREE DIFFERENT TYPES OF SUBSTRATES

Physical Property	PCB	DBC	FPCB
Insulation material	FR4	Ceramic	Polyimide (PI)
Substrate thickness (mm)	0.4-2	0.3-1	0.012-0.065
Operation temperature (ºC)	< 200	> 850	-200-300
Dielectric breakdown strength (kV/mm)	~14	10~35	100-300
Thermal conductivity (W/mK)	0.2	20-330	0.1-0.35

FPCB can achieve the lowest parasitic inductance in the hybrid structure, and this paper will propose a high power density 3-D hybrid full SiC power module based on FPCB.

B. Power Loop Optimization

Considering the thermal performance as mentioned in Section I, the chips are placed on the DBC layer. Meanwhile, the power loop has mutual inductance cancellation effect. Four possible hybrid packaging structures are presented in Fig. 3. The power loops have opposite current direction and mutual inductance cancellation. The parasitic inductance of these four hybrid structures are simulated in Ansys Q3D, and the results are given in Table II.

The power loop of Structure 1 [see Fig. 3(a) and (b)] has good overlap between the top and bottom layers of the FPCB, and therefore the mutual inductance cancellation effect is good. However, the dc terminal leadframes of Structure 1 are located in the middle of the FPCB. Since these terminals need to be soldered on the FPCB, more soldering area is required. If the soldering area length is 4 mm (one terminal 2 mm), the additional soldering area will increase the self-inductance significantly and the total inductance will increase. The power loop inductance for Structure 1 is 4.87 nH (excluding the terminals) as shown in Table II. The dc input terminal leadframes of Structure 2 [see Fig. 3(c) and (d)] can be directly extended from the FPCB, which can reduce the power loop length. But, because the copper trace of +dc (red) around D_2 and output copper trace (green) are in the same bottom layer of FPCB, the mutual inductance cancellation effect is weak and the mutual inductance is small. Hence, the total inductance is 5.91 nH. The dc terminal leadframes of Structure 3 (this structure is used in [29]) [see Fig. 3(e) and (f)] and Structure 4 [see Fig. 3(g) and (h)] can also be directly extended from the FPCB, and they are nearly the same. The only difference is the direction of the bonding-wires of D_2. As shown in Fig. 3(f) and (h), the length of l_{s4} is longer than l_{s3} that will lead to a higher self-inductance of Structure 4 (8.82 nH) than Structure 3 (7.24 nH). However, the large area (dotted yellow box) of Structure 3 does not have strong mutual inductance cancellation effect, because –dc copper trace on the top layer has not overlapped with the bottom layer in this area and only has weak flux coupling with the bonding wires. Structure 3 has 2.49 nH mutual inductance, which is smaller than Structure 4 (4.51 nH). Hence, although the length of Structure 4 has 1 mm longer than Structure 3, Structure 4 has smaller total parasitic inductance due to the larger mutual inductance.

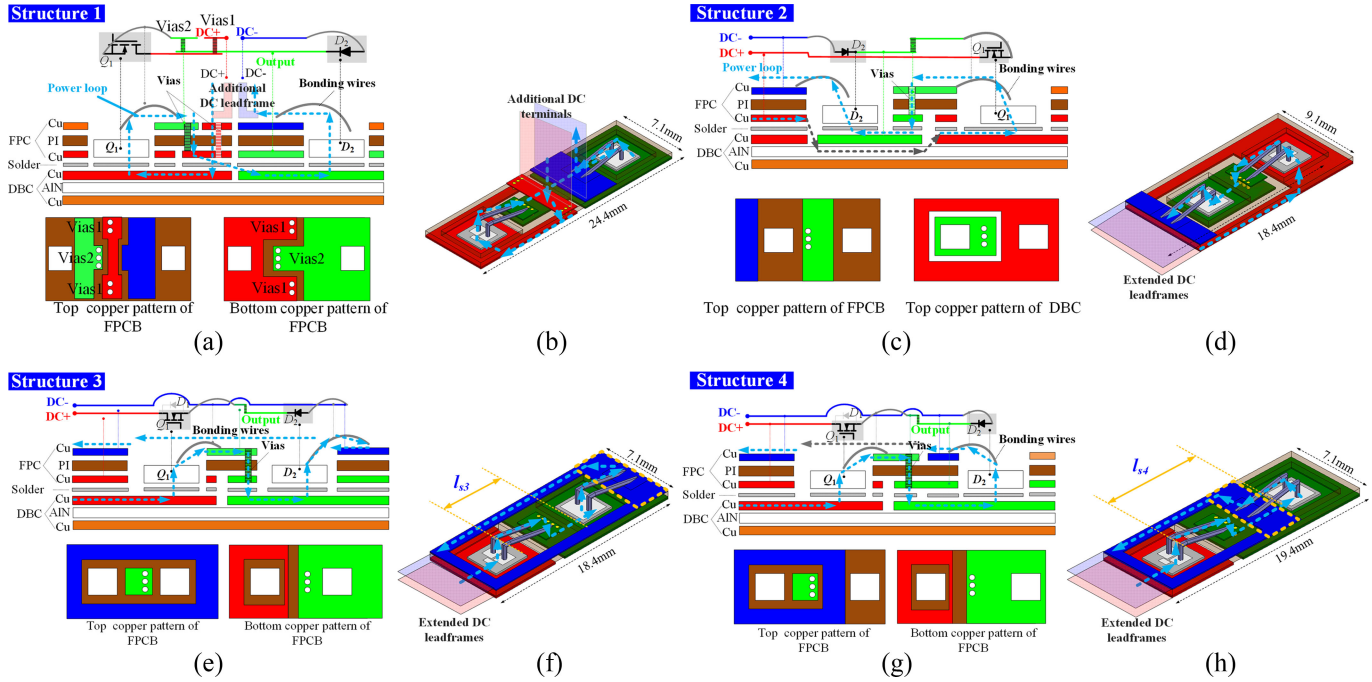

Fig. 3. Possible hybrid packaging structures with mutual inductance cancellation: (a)–(b) structure 1 and simulation model, (c)–(d) structure 2 and simulation model, (e)–(f) structure 3 and simulation model, and (g)–(h) structure 4 and simulation model.

TABLE II
PARASITIC INDUCTANCE COMPARISON OF FOUR STRUCTURES

Type	Self-inductance /nH	Mutual Inductance /nH	Total inductance /nH	DC leadframes connection method
Structure 1	10.9	-6.03	4.87	soldering additional leadframes
Structure 2	8.62	-2.71	5.91	FPCB extended directly
Structure 3	7.24	-2.49	4.75	FPCB extended directly
Structure 4	8.82	-4.51	4.31	FPCB extended directly

As we can see from these structures and simulation results, more copper trace overlap and smaller loop length are possible considering dc terminal leadframes and lower inductance. Therefore, this paper will use hybrid structure 4 to design the 1200-V/120-A 3-D high-density full SiC power module.

III. HIGH POWER DENSITY 3-D SiC POWER MODULE

Based on the hybrid packaging Structure 4, the proposed 1200-A/120-A full SiC half-bridge (HB) power module is depicted as shown in Fig. 4(a). The HB module has six Wolfspeed's CPM2-1200-0080B (1200 V/24 A@100 °C) SiC MOSFET bare dies in parallel and three Wolfspeed's CPW4-1200-S020B (1200 V/20 A) SiC Schottky diode bare dies in parallel for both high-side and low-side switch. The power module has three identical submodules, which are connected by the FPCB. This method can increase the fabrication yield and effectively reduces the DBC warpage increasing reliability. The dc decoupling capacitors are integrated around the devices in each submodule, and the leadframes of dc input and ac output terminals are directly extended from the FPCB. This type of ultrathin FPCB-based laminated dc terminals also has ultralow parasitic inductance. In order to get symmetrical current sharing for multichips parallel, the diode chips are placed in the middle of two paralleled MOSFET chips. Taking Q_3 and Q_4 and D_5 loop as an example, the Q_3 to D_5 current loop (red dotted line) is the same as Q_4 to D_5 (blue dotted line). Additionally, the high-side and low-side chips are symmetrically distributed. These symmetrical layouts can obtain symmetrical parasitic inductance for each device. Moreover, there are two small two-layer FPCBs individually soldered on the DBC, which are used to connect the gate and source pad of the MOSFETs. Only low cost two-layer FPCBs are needed for power loop and gate loop connections, and the gate connections can achieve Kelvin connections. Moreover, the common source inductance caused by the magnetic coupling is almost zero because gate loops are vertical to the power loop [29].

Fig. 4(b) shows the proposed high-density 3-D power module applying the bendable capability of FPCB. Meanwhile, the heatsink and cooling fan can be integrated into the 3-D power module, and the thermal management of the module will be introduced in Section IV. The dimension of the proposed 1200-V/120-A power module with the heatsink is 62 mm × 45.5 mm × 53 mm (0.150 L). The dimension of the commercial 1200-V/120-A power module CAS120M12BM2 (w/o heatsink) is 62 mm × 106 mm × 30 mm (0.197 L) as shown in Fig. 5(a). As it can be seen, although the proposed power module contains heatsink and fan, the volume of the proposed power

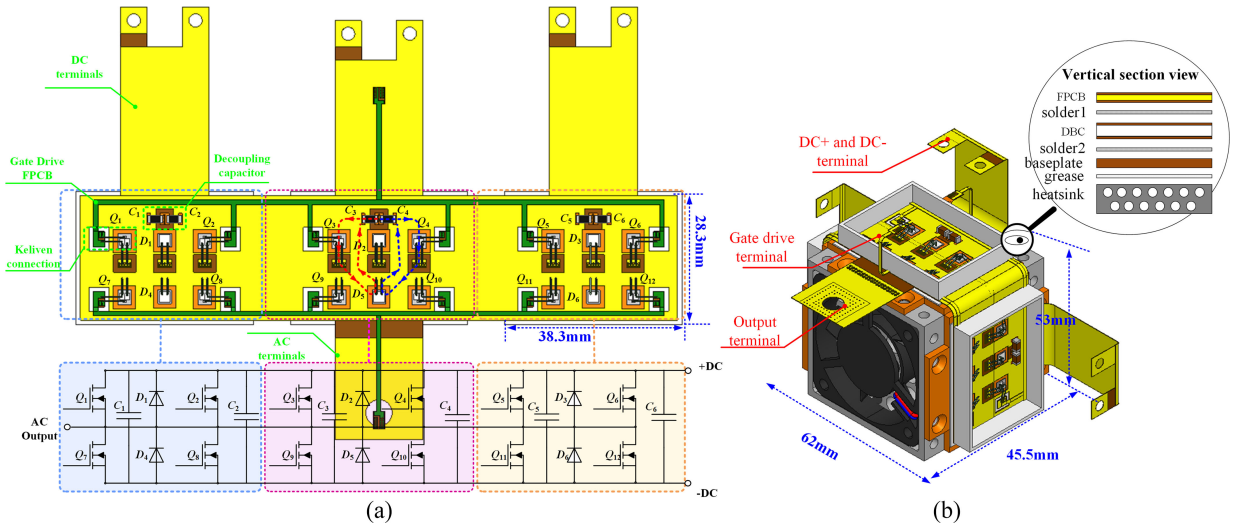

Fig. 4. Proposed power module. (a) Extension view of the proposed 1200-V/120-A full SiC HB power module. (b) 3-D schematic of the proposed 1200-V/120-A full SiC HB power module.

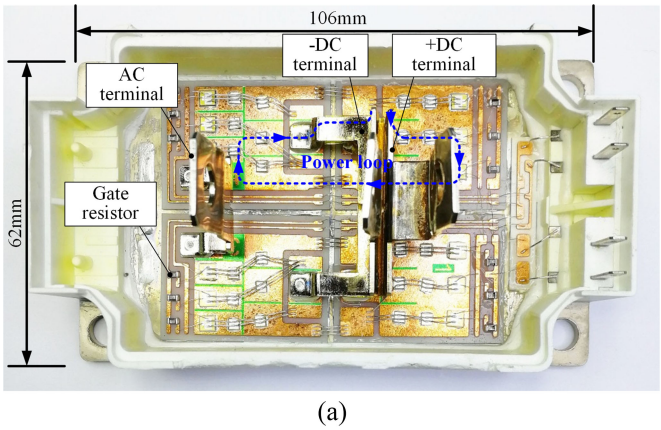

Fig. 5. CAS120M12BM2 power module. (a) Open case and decapsulation. (b) Q3D simulation model.

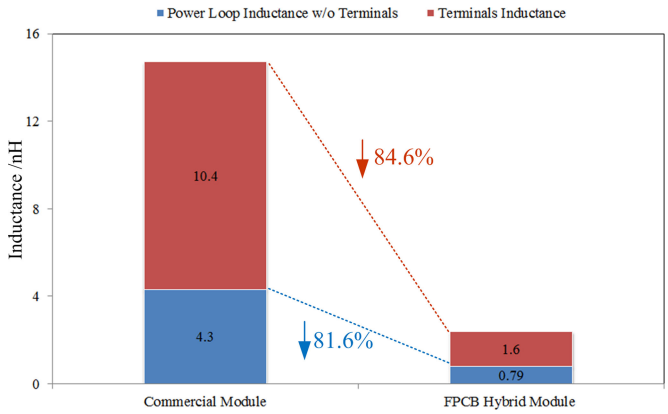

Fig. 6. Inductance simulation results of commercial module and proposed module.

module is smaller than the same power-rated commercial power module. Because the 3-D spaces are efficiently utilized, this design can significantly increase the power density of the power module.

The parasitic inductance of the proposed 1200-V/ 120-A full SiC power module and the commercial 1200-V/120-A full SiC power module (CAS120M12BM2) are extracted in ANSYS Q3D as shown in Figs. 4(a) and 5, respectively. The commercial power module has 6 24-A MOSFET chips paralleled and 12 10-A SBD diode chips paralleled. The dimensions of the copper traces and chip locations of the commercial power module are measured by 3-D imaging scanner after decapsulation. The detailed parasitic inductance can be obtained as shown in Fig. 6. The power loop parasitic inductance of the proposed FPCB-based hybrid power module is only 0.79 nH. The leadframe parasitic inductance of dc terminals is only 1.6 nH, which is 84.6% lower when compared to commercial busbar terminals. The power loop parasitic inductance of the commercial 1200-V/120-A power module CAS120M12BM2 has about 15 nH. The power loop of the commercial power module is depicted as the dotted blue line in Fig. 5(a), which is relatively larger compared to the 3-D power loop of Structure 4.

IV. Integration Method and Thermal Management

A. Power Module Integration

Fig. 7 is the 3-D graph of the air-cooled power module integrated with the heatsink, gate drive, dc-link capacitor bank, and

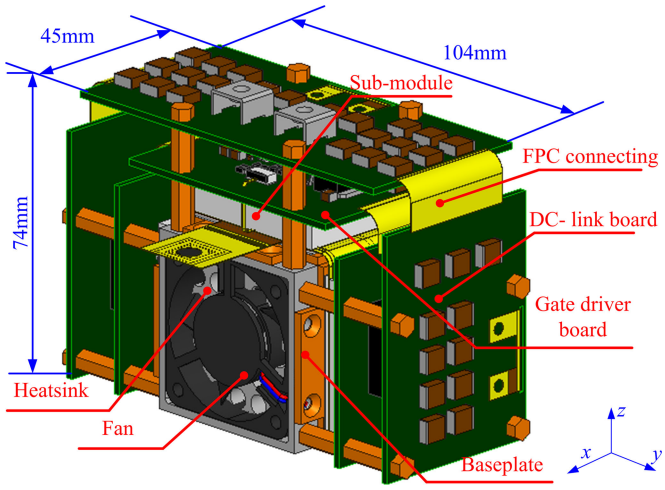

Fig. 7. 3-D view of the highly integrated 1200-V/120-A full SiC HB module.

fan. The power module has three submodules mounted on the three sides of the heatsink, and a 40 mm × 40 mm × 6 mm axial fan is mounted inside the fan-slot of the heatsink. The gate drive board is a rigid-flex PCB with 6-W/30-A HB gate drive capability. The isolated power supplies of the HB gate drivers are mounted on the two sides of the heat-sink at y-direction. The dc-link capacitor board is also a rigid-flexible PCB with 60 × 2.2 μF/500 V MLCC capacitors, and the capacitors are symmetrically connected to the three extended FPCB dc terminals. Due to the high space utilization rate of this 3-D system-in-package integration method, the total volume of the integrated full SiC HB power module system is only 104 mm × 74 mm × 45 mm (0.346L).

B. Thermal Management

Considering fabrication convenience and cost, the aluminum heatsink with round-holes is utilized. The heatsink dimensions are 44.3 mm × 44.3 mm × 45.5 mm to fit the power module. The fan is a commercial axial fan AD4006 (40 mm × 40 mm × 6 mm) from ADDA corporation. The thermal FEA simulation software Flotherm is used to optimize the heatsink instead of complex theoretical calculation. The hole diameter of the heatsink and the hole distribution will be discussed below.

Because a smaller hole will have a larger windage resistance and larger holes will have smaller heat dissipating areas, the hole size should have an optimal value. Fig. 8 gives the simulation results under different hole size at 25 °C ambient temperature, where each MOSFET loss is 4.95 W, and each diode loss is 0.068 W for a 20 kW/20 kHz three-phase inverter. It can be seen that the heatsink with a 5-mm diameter hole has the lowest peak temperature 94.4 °C. Meanwhile, the output air-flow rate increases with the hole diameter due to the reduced windage resistance, as shown in Fig. 9.

The hole distribution is also considered in the design. Figs. 10 and 11 give the simulation results of four types of hole distribution simulation structures varying from 16 to 36 holes (Φ5 mm). It can be seen that the 36 holes structure has the lowest temperature under this condition. This structure has the largest

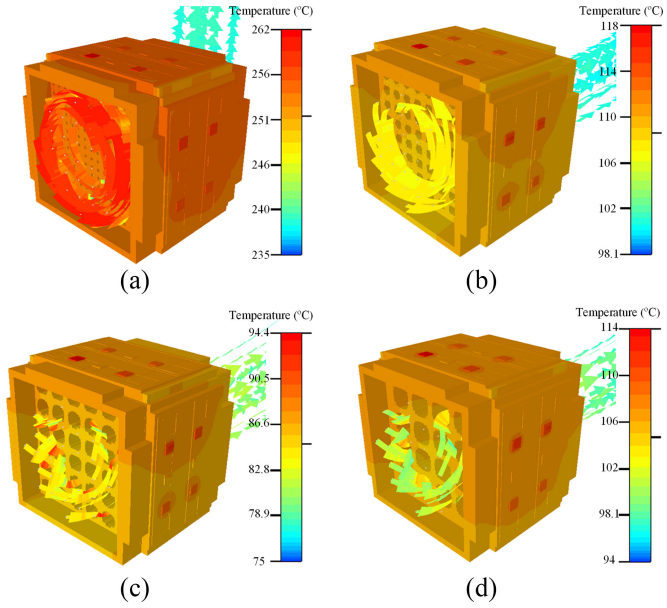

Fig. 8. Hole size simulation results. (a) 1-mm diameter hole. (b) 3-mm diameter hole. (c) 5-mm diameter hole. (d) 7-mm diameter hole.

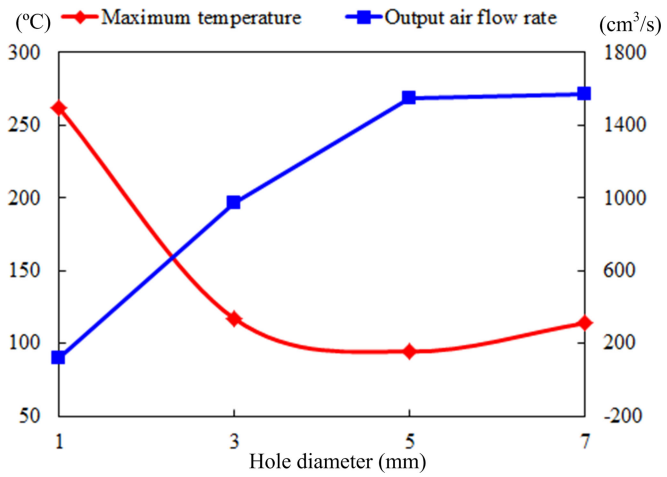

Fig. 9. Maximum temperature and output air flow curves.

hole-area for heat dissipation. Hence, the 36 holes (Φ5 mm) structure heatsink is chosen for this design.

Furthermore, Fig. 12 gives the thermal simulation results using a traditional heatsink for commercial power module and the proposed power module under the unfolded condition. The heatsink has the same shape with Φ5 mm holes. The commercial module needs a 64.3 mm × 24.4 mm × 103.5 mm (0.162L) heatsink to realize 94.9 °C maximum chip temperature as shown in Fig. 12(a). The proposed three-sided cooling heatsink dimensions are 44.3 mm × 44.3 mm × 45.5 mm (0.089L), which is only half of the traditional heatsink for the commercial power module. Fig. 12(b) gives the simulation result of the proposed power module under the unfolded condition, which requires a 24.4 mm × 44.3 mm × 133 mm (0.144L) heatsink to achieve 106 °C maximum chip temperature, which is also two times larger than the proposed 3-D power module.

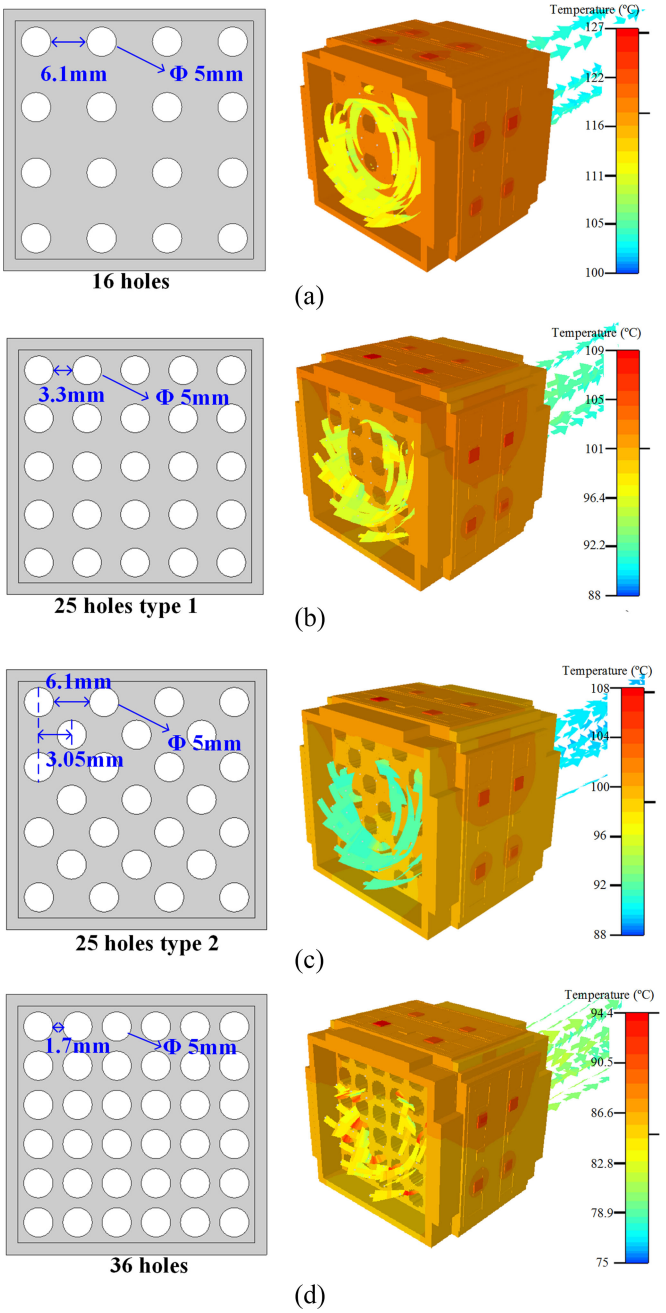

Fig. 10. Heatsink hole distribution simulation models. (a) 16 holes. (b) 25 holes type 1. (c) 25 holes type 2. (d) 36 holes.

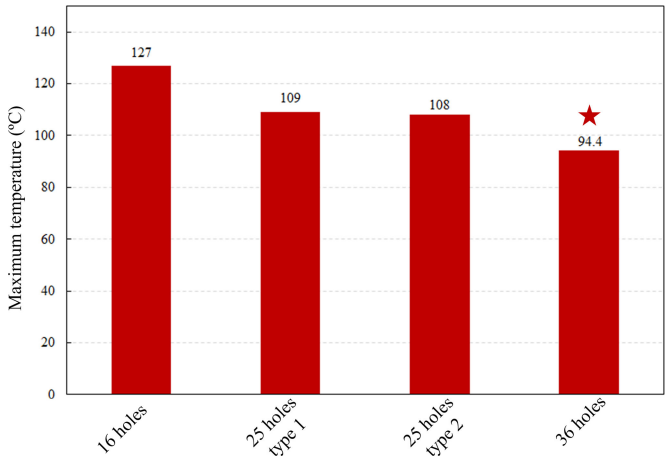

Fig. 11. Highest temperature comparison for different types of heatsink hole distribution.

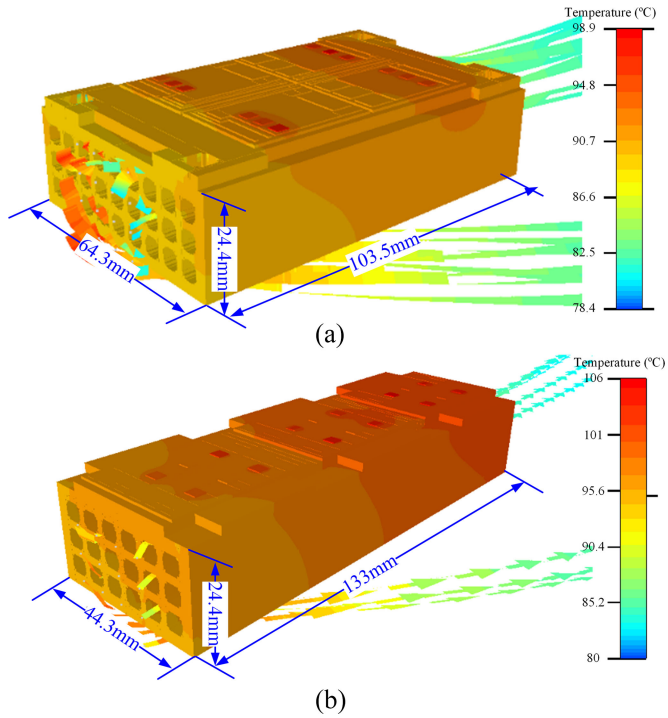

Fig. 12. Traditional heatsink simulation results. (a) Commercial module simulation results. (b) Proposed power module simulation results under the unfolded condition.

V. Power Module Fabrication and Assembly

Fig. 13 shows the fabrication processes of the proposed power module. Table III gives the the packaging material list of this module. First, the AlN DBC substrate is etched by $FeCl_3$ and the FPCBs are fabricated by Vendor. Then, the $Pb_{37}Sn_{63}$ solder paste is stencil printed on the DBC substrates. Here, the cheap low-temperature solders are used to verify the proposed 3-D hybrid structure for the full SiC power module. The FPCBs, decoupling capacitors, and SiC chips are aligned and placed on the DBC substrates. After that, all components are soldered with a steel fixture through vacuum reflow soldering. Afterward, Al bonding wires are bonded between SiC chips and FPCBs as shown in Fig. 13(d). Finally, DBCs are soldered on the Ni-plated copper baseplates with low temperature $Sn_{42}Bi_{58}$ solder paste, and the power module is housed by a 3-D printed PPS case and encapsulated with epoxy. It can be seen that the fabrication steps are nearly the same as the traditional wire-bonding module and easy to realize.

Fig. 14 shows the proposed high-density power module assembly processes. Since the FPCB is flexible and bendable, the power module can be mounted on the three faces of the aluminum heatsink, as shown in Fig. 14(a). This method increases the space utilization ratio and improves the thermal

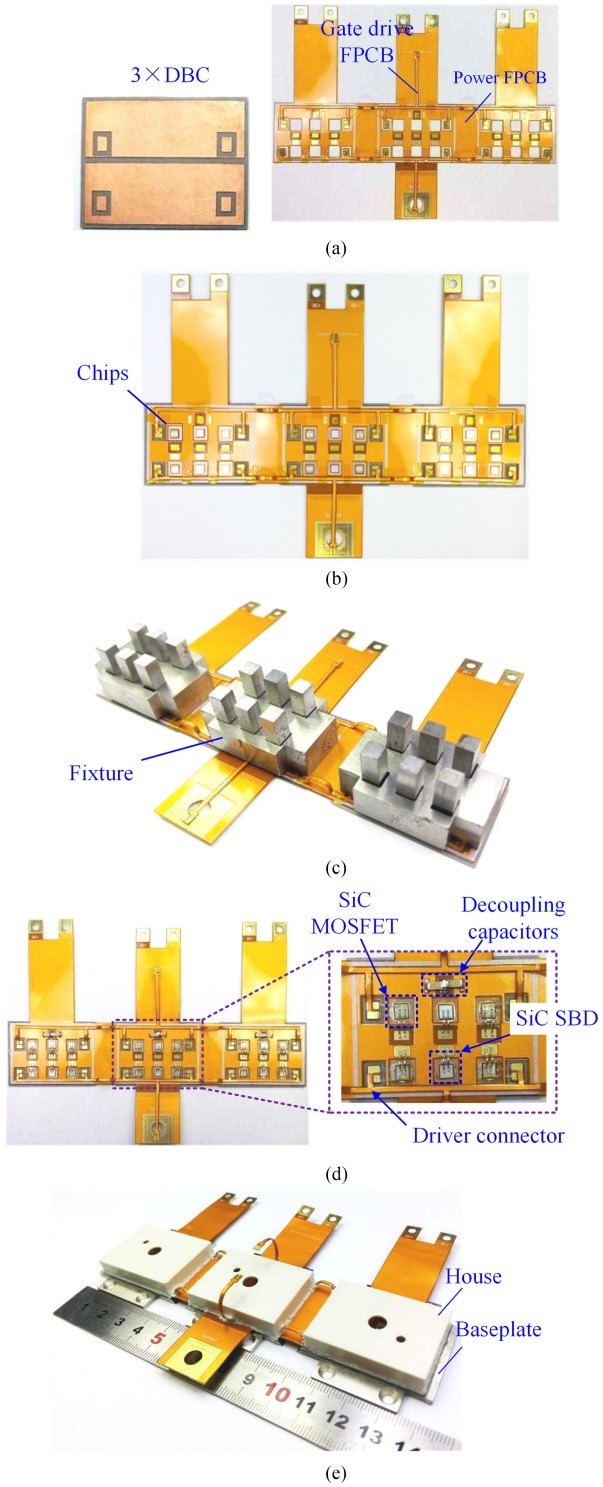

Fig. 13. Module fabrication processes. (a) Etched DBC and fabricated FPC board. (b) Placed chips and FPCB. (c) FPC boards and chips soldering. (d) Wire-bonding. (e) Baseplate soldering, housing, and encapsulation.

performance. Meanwhile, the power terminals and gate drive terminals are FPCB. The rigid-flexible gate driver board and rigid-flexible dc-link board are mounted on the top of the power module, as shown in Fig. 14(b) and (c). As shown in Fig. 14(d), the air-cooled fan is mounted inside the heatsink. The dimensions of the air-cooled system integrated 1200-V/120-A full SiC power module are 104 mm × 74 mm × 45 mm (0.346L), and its power density reaches 19.3 kW/L for a 20 kW three-phase inverter. The 3-D model of the 20-kW three-phase inverter is depicted in Fig. 15. Three integrated HB modules are horizontally arranged and connected by a laminated busbar. The volume of the 20-kW three-phase inverter is only 1.038 L and the power density can reach 19.3 kW/L.

VI. Experimental Results

A. Static Characteristics

The static characteristics are measured by Keysight B1505A power device analyzer at 25 °C. Fig. 16 gives the measurement results. Fig. 16(a) depicts the *I–V* curve, (b) shows the transfer characteristic curve, and (c) gives the on-resistance curve. As shown in the results, the static curves of the proposed module are similar to the commercial module. The difference is caused by the chips' characteristics. The on-resistance of the lab-level fabricated module is 15.2 mΩ at 120 A (typical value of commercial module is 13 mΩ), which is close to the commercial module.

B. Dynamic Characteristics

In order to compare the dynamic characterizations of the FPCB-based hybrid structure SiC power module with the commercial SiC power module (CAS120M12BM2), the same double pulse set-ups are designed for them as shown in Fig. 17. There are several groups of decoupling capacitors adding in the DPT setup for exact $V_{\rm ds}$ measurement and switching loss measurement. The power loops of DPT test boards are designed the same and the gate drive uses the same driver board, which is utilized in the integrated power module. The proposed power module without housing and epoxy encapsulation is used for testing. The chip voltage can be measured directly. The drain-source current is measured by the T&M research SSDN-10 (0.1 Ω and 2 GHz bandwidth) shunt resistor. The waveforms are captured by Lecroy WaveSurfer 10 oscilloscope with 1 GHz bandwidth. The gate-source and drain-source voltage are measured by 500 MHz PP018 passive probe with low ground lead inductance BNC or spring probe tip. It should be noted that the $V_{\rm ds}$ of commercial module is measured at the terminals. The measured $V_{\rm ds}$ will be smaller than the actual drain-source voltage because about half of the power module inductance is in the voltage measuring loop [34]. The $V_{\rm ds}$ of the proposed FPCB-based hybrid power module is measured near the chip using the spring probe tip as shown in Fig. 17(a).

The large $C_{\rm dc}$ and C_{dec1} decoupling capacitors are used to eliminate the parasitic inductance L_2 and $L_{\rm dc}+L_1$ influences caused by the power supply connection wire and the $C_{\rm dc}$ to C_{dec1} PCB copper trace. Although the power loop is designed carefully, the current shunt will induce additional inductance around 9 nH Ls. The 9 nH inductance cannot be neglected compared to the 2.4 nH $L_{\rm lead}+L_{\rm module}$ of the proposed module. Otherwise, the voltage overshoot will be mainly caused by L_s. Therefore, an additional group of decoupling capacitors C_{dec2}

TABLE III
BILL-OF-MATERIALS FOR THE PROPOSED SiC POWER MODULE

Part	Material	Specification
Switch	Wolfspeed SiC MOSFET	1200V/24A, CPM2-1200-0080B×12; Top pads: G & S, Al metalized; Bottom pad: D, Ni/Ag metalized
Diode	Wolfspeed SiC SBD	1200V/20A, CPW4-1200-S020B×6; Top pad: A, Al metalized; Bottom pad: K, Ni/Ag metalized
Bonding wire for drive connection	Al	Dia: 1mil; 5 wires in parallel for each die
Bonding wire for power connection	Al	Dia: 16mil; 2 wires in parallel for each die
Die and FPCB attach solder	Sn_{37}-Pb_{63}	Liquidus point:183/ °C
Baseplate attach solder	Sn_{42}-Bi_{58}	Liquidus point:138/ °C
Gate drive and power FPCB	Cu & Polyimide	2 oz copper; Immersion gold pad; 0.065mm in thickness polyimide with 100kV/mm dielectric strength
Substrate	AlN DBC	0.38mm Cu/0.6mm ceramic/0.38mm Cu
Baseplate	Cu	2mm in thickness
Fixture	Steel	10mm in thickness
Housing	PPS	Max. long-term service temp:260 °C
Encapsulation	*Qgel* 310	Dosage 60 ml

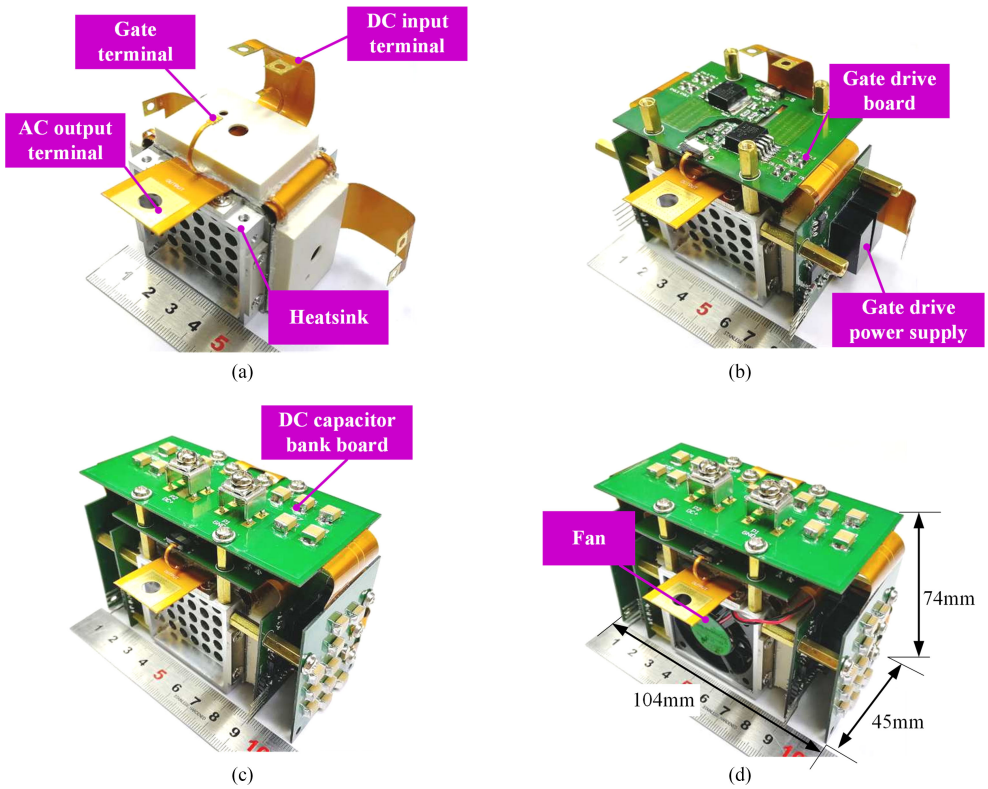

Fig. 14. Air-cooled integrated 1200-V/120-A full SiC power module. (a) Heatsink integration. (b) Gate drive board integration. (c) DC-link board integration. (d) Air-cooled fan integration.

(14×2.2 μF) is inserted between the current shunt and power module to eliminate the overshoot affected by L_s for V_{ds} measurement, as shown in Fig. 18. Meanwhile, the proposed power module has been tested under both 60 nF C_{dec} integrated inside the power module and not integrated.

Fig. 19 shows the turn-off experimental results of the commercial power module and the FPCB-based power module. Because of the C_{dec2}, the load current is measured instead of the shunt current. It should be noted that the commercial module has integrated 12 10-Ω gate resistors [see Fig. 5(a)] for SiC MOSFET paralleling for the asymmetrical gate loop. Otherwise, the power module will not operate normally. In order to get the same turn-on 2.8 Ω and turn-off 2.25 Ω gate resistor as FPCB-based power module is, the external turn-on and turn-off gate resistor of commercial power module are 1.1 and 0.55 Ω. The voltage spike of the commercial power module is 499 V at turn-off, as shown in Fig. 19(a). As mentioned previously that the commercial module V_{ds} is measured at the terminals and about

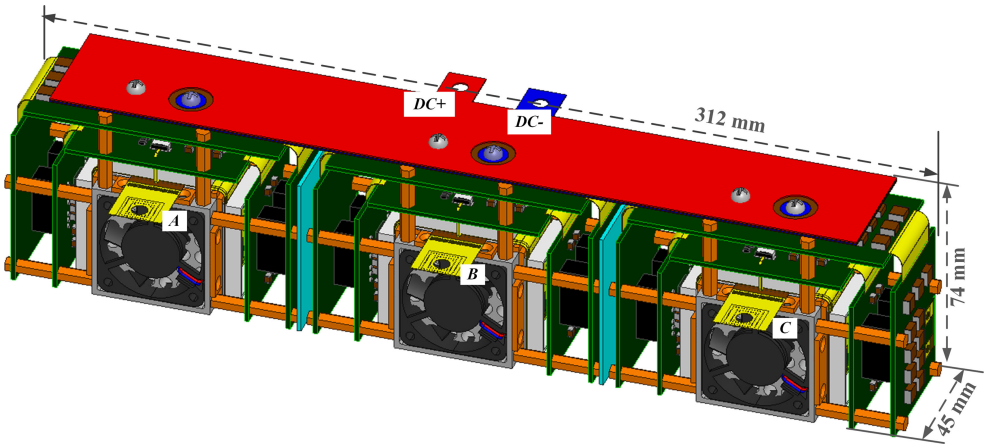

Fig. 15. 3-D model of the 20-kW three-phase inverter.

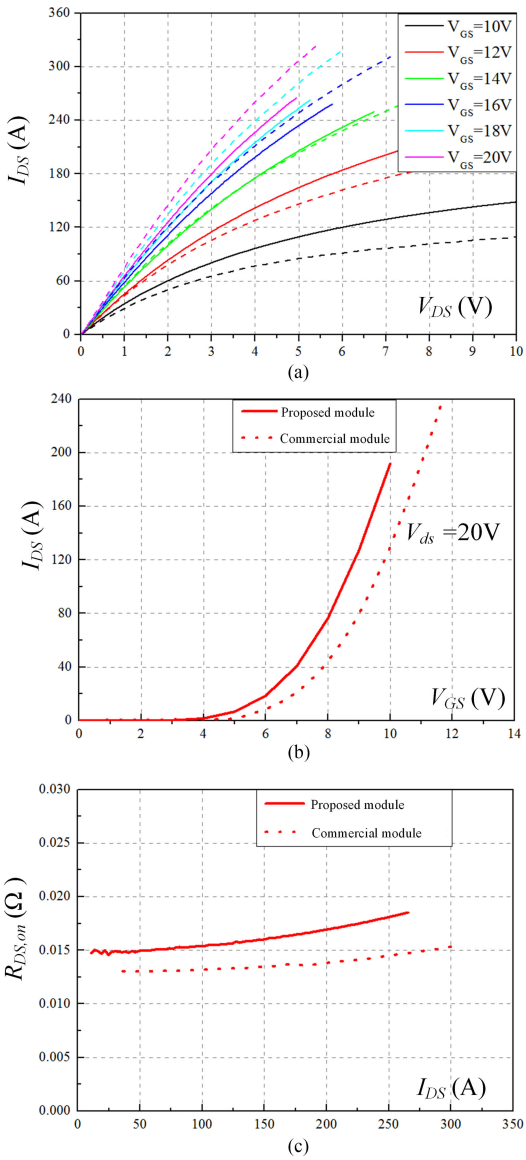

Fig. 16. Static characteristics of the proposed power module and commercial power module at 25 °C. (a) *I–V* curve. (b) Transfer characteristic curve. (c) On-resistance curve.

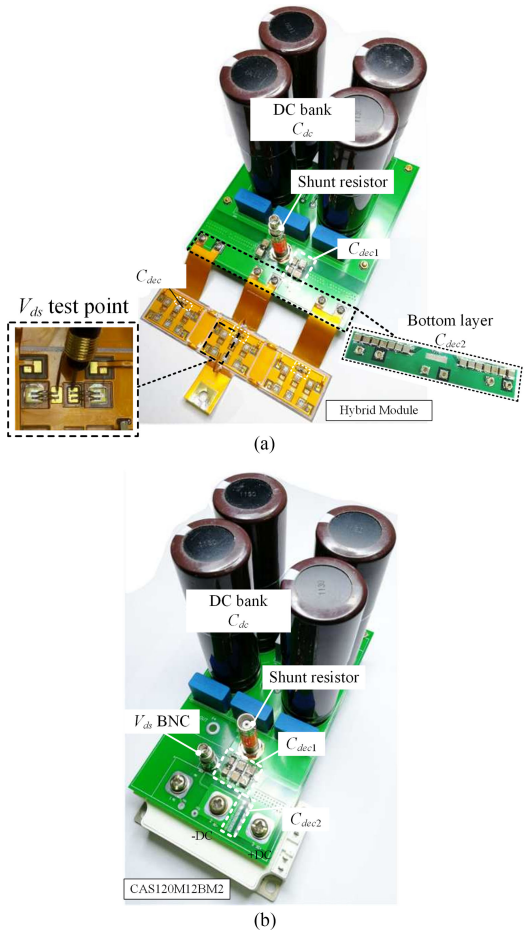

Fig. 17. Double pulse test PCBs for two modules. (a) Tester PCB for FPC module. (b) Tester PCB for CAS120M12BM2.

half of the power module inductance influence is measured, the actual drain-source voltage will be 558 V as the simulation prediction result shown in Fig. 20. The FPCB-based power module is only 440 V and the voltage spike is reduced to 427 V with integrated decoupling capacitors as shown in Fig. 19(b) and (c). The voltage overshoot is only 17% of the commercial module.

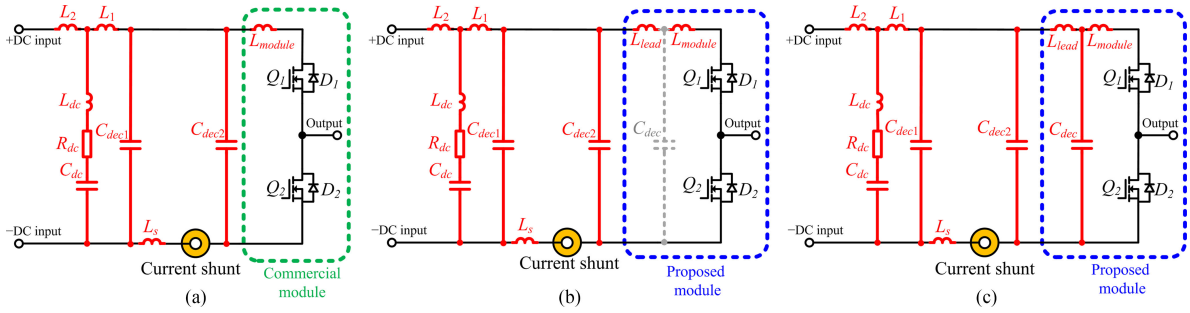

Fig. 18. Experimental comparison circuits of parasitic inductance influence for voltage overshoot of commercial power module and proposed power module. (a) Adding C_{dec2} for commercial power module. (b) Adding a large C_{dec2} for proposed power module without C_{dec}. (c) Adding C_{dec2} with C_{dec}.

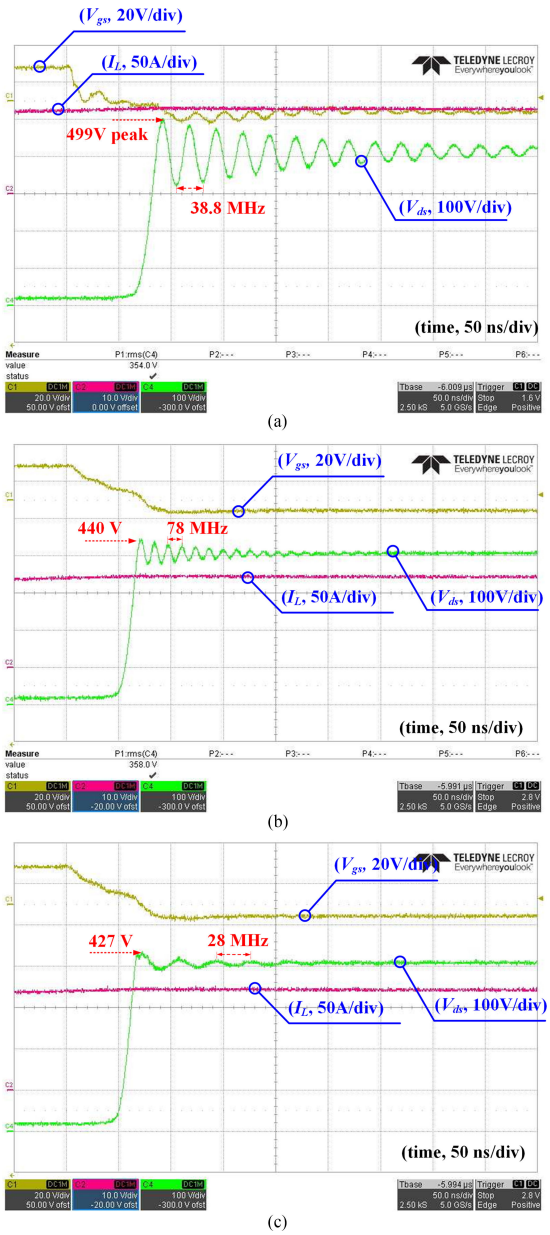

Fig. 19. Turn-off waveforms of the commercial and the proposed modules at 400-V/120-A with gate resistor $R_{g,\text{off}} = 2.25\,\Omega$. (a) Commercial module turn-off waveforms with C_{dec2}. (b) Proposed module turn-off waveforms with C_{dec2} and without C_{dec}. (c) Proposed module turn-off waveforms with C_{dec2} and C_{dec}.

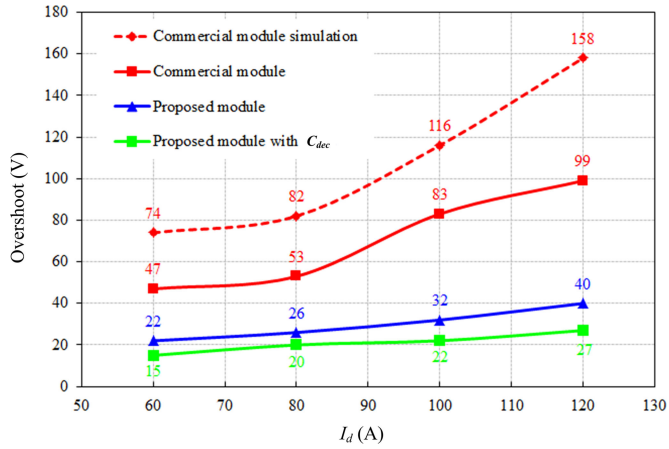

Fig. 20. Drain-source voltage overshoot measurement results under different turn-off currents.

Besides, the parasitic inductance can be calculated according to the following equation:

$$f = \frac{1}{2\pi\sqrt{L \cdot C_{\text{oss}}}} \tag{2}$$

where f is the V_{ds} overshoot resonant frequency and C_{oss} is the output capacitor of the power module. C_{oss} of the commercial module is 1010 pF reading from datasheet C–V curve at 400 V. C_{oss} of the FPCB module is 1499 pF, which forms by six MOSFETs (6 × 95 pF from datasheet C–V curve) paralleled with three SBDs (3 × 93 pF) and the parasitic capacitance induced by the overlapped area of the output layer and –dc layer of FPCB (650 pF from simulation). It should be noted that although the overshoot of the commercial module is not actual, the oscillation frequency will not change and is the same as actual, which can be used to calculate the inductance. The parasitic inductance of the commercial power module can be obtained as 16.7 nH at 38.8 MHz oscillation as shown in Fig. 19(a). The FPCB-based module can be calculated as 2.8 nH at 78 MHz oscillation as shown in Fig. 19(b). Moreover, because the precision of the probe and scope is not enough, the 146 MHz resonant caused by C_{oss} and 0.79 nH power loop inductance cannot be captured clearly in Fig. 19(c) and only a low-frequency oscillation caused by the C_{dec} can be observed. It can be seen that the test circuit induced only around 1 nH inductance for the module terminal connections. Besides, the inductance reduction of FPCB-based

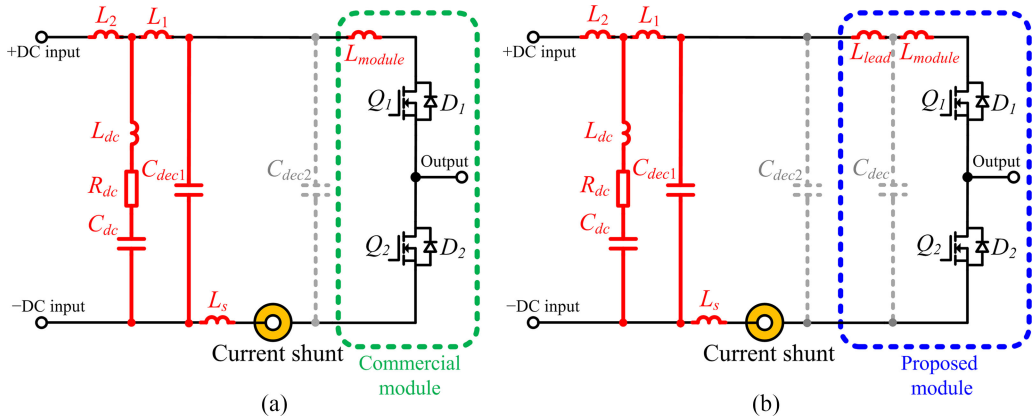

Fig. 21. Experimental comparison circuits of switching losses for commercial power module and proposed power module. (a) Without C_{dec2} for commercial power module. (b) Without C_{dec2} and C_{dec} for proposed power module.

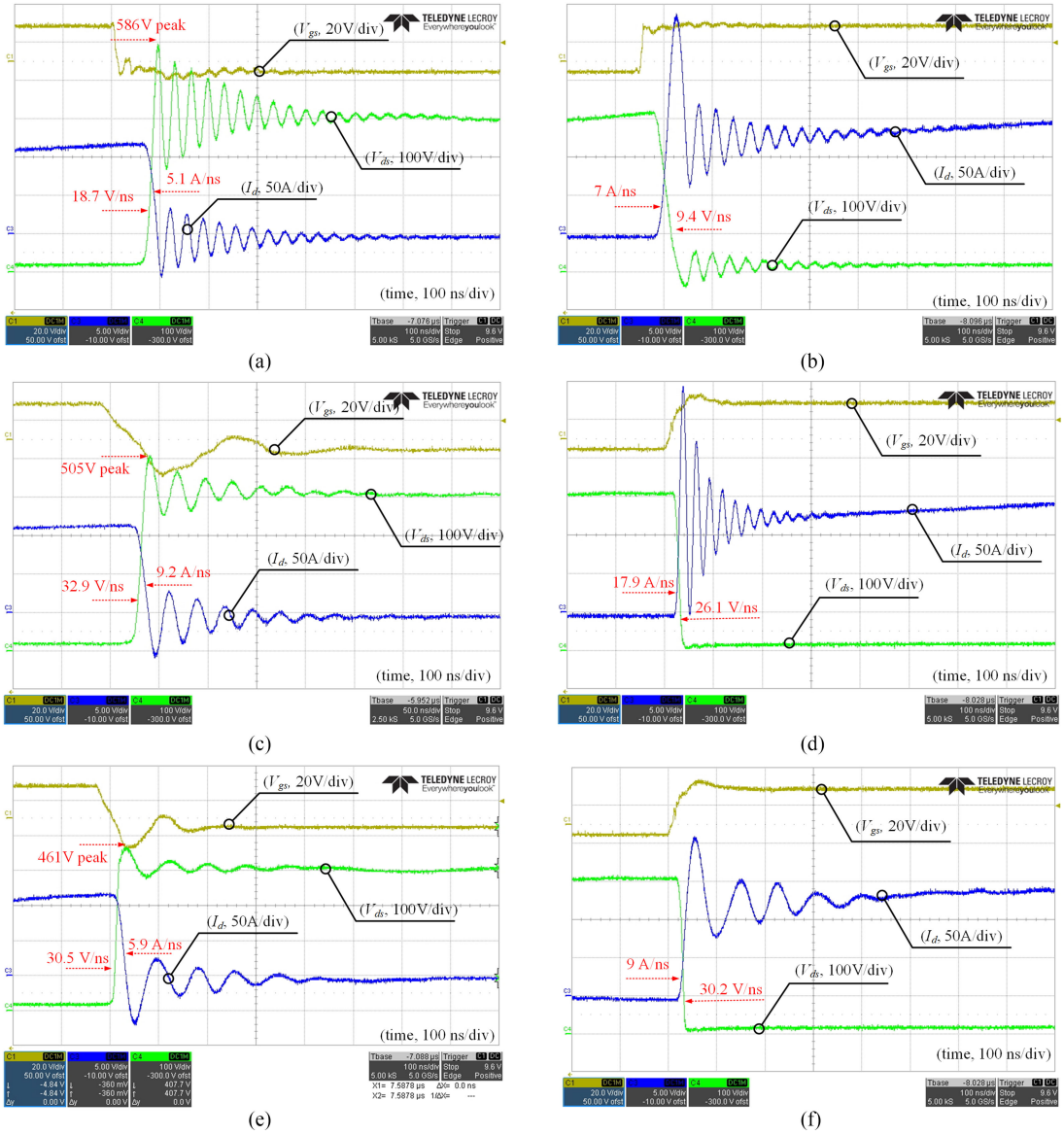

Fig. 22. Switching waveforms of commercial module and FPCB-based module under zero external gate resistor and 400-V/120-A condition. (a) Turn-off waveforms of commercial module. (b) Turn-on waveforms of commercial module. (c) Turn-off waveforms of proposed module without C_{dec}. (d) Turn-on waveforms of proposed module without C_{dec}. (e) Turn-off waveforms of proposed module with C_{dec}. (f) Turn-on waveforms of proposed module with C_{dec}.

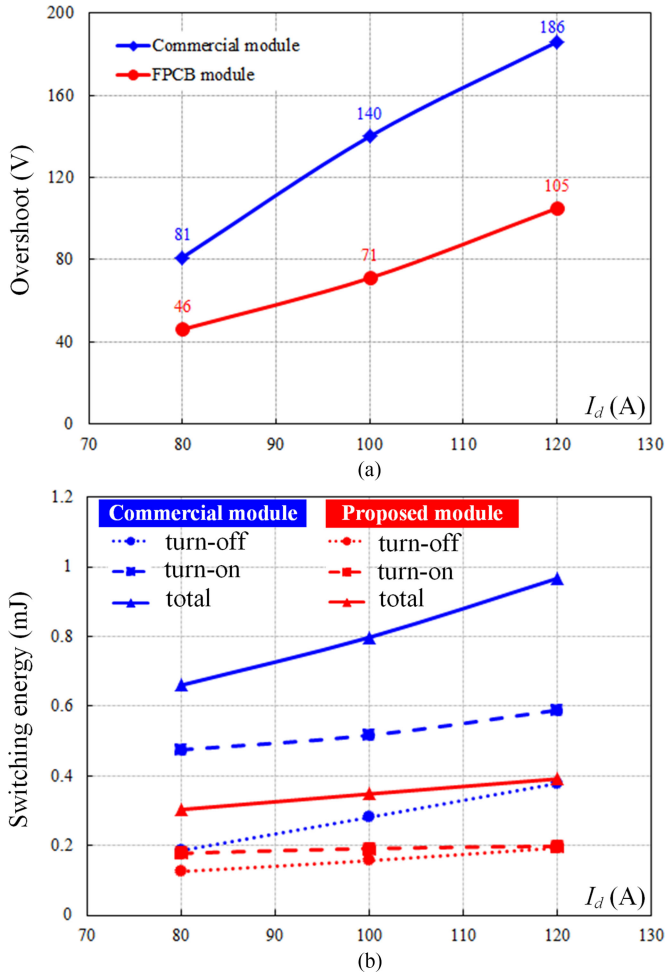

Fig. 23. Voltage overshoot and switching energy comparison results under different currents for the commercial module and proposed module. (a) Voltage overshoot curve. (b) Switching energy curve.

module is 13.9 nH compared to the commercial module, which is the same as the simulation result. Fig. 20 depicts the V_{ds} overshoots under different turn-off currents. It shows that the proposed power module has lower overshoots than commercial module under different turn-off currents.

Moreover, the switching loss of these two modules are measured based on the test circuits shown in Fig. 21, in which the C_{dec2} and C_{dec} are removed to get the actual drain current. The current shunt resistor from T&M research SSDN-10 is used to measure the drain current. The switching loss comparison of the commercial module and the FPCB-based module are tested at the fastest switching condition with zero external gate resistor. Fig. 22 gives the switching waveforms at 400-V/120-A condition. The voltage rise time of the commercial module is 17.1 ns, the current fall time is 18.8 ns, and voltage spike is 586 V at turn-OFF. The turn-OFF *dv/dt* and *di/dt* are 18.47 V/ns and 5.1 A/ns. The voltage fall time of the commercial module is 34 ns and current rise time is 13.7 ns during switch turning ON. The turn-ON *dv/dt* and *di/dt* are 9.4 V/ns and 7 A/ns, whereas the voltage rise time of the proposed FPCB-based hybrid packaged module without C_{dec} is 9.7 ns, the current fall time is 10.5 ns, and voltage spike is 505 V. The *dv/dt* and *di/dt* are 32.9 V/ns and 9.2 A/ns. The voltage fall time of the proposed module is 12.3 ns and current rise time is 5.36 ns at turn-ON. The turn-ON *dv/dt* and *di/dt* are 26.1 V/ns and 17.9 A/ns. It can be seen that the proposed power module is 1.8 times faster than commercial module under the fastest switching potential and the switching loss reduce about 60% as shown in Fig. 23(b). When adding the C_{dec}, the voltage rise time is 10.5 ns and fall time is 10.6 ns, *dv/dt* reaches 30.5 V/ns and 30.2 V/ns in the conditions that switch turns OFF and turns ON, respectively, and voltage spike reduces to 461 V as shown in Fig. 22(e) and (f). After adding the decoupling capacitor, the *dv/dt* is reduced only by a small value of 0.3 V/ns.

Fig. 23 depicts the voltage overshoot and switching energy comparison results without C_{dec}. The V_{DS} overshoot of the FPCB module reduces about 45% compared to the commercial power module as shown in Fig. 23(a). The voltage overshoot of the proposed power module will reduce much more in comparison to the actual voltage overshoot of the commercial power module. The turn-ON switching energy reduces by about 0.4 mJ and turn-OFF switching energy can decrease by about 0.2 mJ at 120 A. The total switching energy is only 40% of the commercial module.

VII. Conclusion

An FPCB-based 3-D low inductive high-density integrated hybrid SiC HB power module has been developed and fabricated. The power loop parasitic inductance is 0.79 nH for a 1200-V/120-A power module because of the integrated decoupling capacitors and the optimized mutual inductance canceled 3-D power loop design. In addition, the inductance of the laminated FPCB-based dc leadframe is as low as 1.6 nH. Moreover, the power module is designed into three submodules and connected by a bendable FPCB substrate. The 3-D space has been fully utilized based on the bendable power module. The gate drive, decoupling capacitors, and dc-link capacitors can be integrated and 3D-structured using rigid-flexible PCB. Meanwhile, a high-efficiency three-sided cooling structure is designed for the bendable power module. The 3-D thermal dissipation method reduces the heatsink volume about one half and is also verified in the thermal simulation. The power density of the power module reaches 19.3 kW/L for a 20-kW three-phase inverter. Besides, the proposed 1200-V/120-A power module can be easily fabricated based on the traditional wire-bonding technology. The static and dynamic tests are compared between commercial and proposed module. The experimental results show that the proposed module has 5.8 times lower voltage overshoot, 1.8 times faster switching time, and the switching loss can reduce by about 60%.

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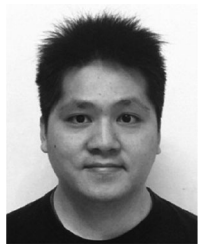

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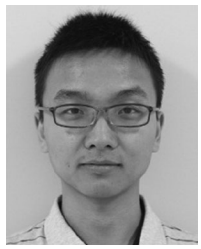

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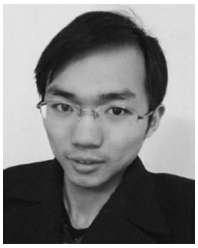

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