Design and Control of Unidirectional DC–DC Modular Multilevel Converter for Offshore DC Collection Point: Theoretical Analysis and Experimental Validation

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***Abstract*—This paper presents the design and control of an advanced unidirectional dc–dc modular multilevel converter (MMC), which enables the integration of off-shore windfarms with the high-voltage direct current (HVdc) transmission system. The proposed converter consists of a single-phase MMC inverter, coupled with series-connected rectifier modules through a medium frequency transformer of multiple secondary windings. The modularity feature of the proposed converter enables scalability for different voltage levels. In addition to the galvanic isolation, the transformer also provides stepping gain to the output voltage. The proposed converter shows superior performance in terms of efficiency, losses, and devices utilization, when compared with the most competitive unidirectional cascaded dc–dc converters such as input series output series and input parallel output series. Furthermore, unlike the conventional *d-q* control method, which involves multiple transformations, this paper employs a simple proportional resonant control strategy that directly acts on the ac output of the MMC, under the stationary reference frame. The analytical design along with the simulation and experimentally validated results, confirmed the excellent performance of the proposed converter.**

***Index Terms*—DC collection point, dc–dc converter, generalized stationary frame regulators, modular multilevel converter (MMC), off-shore windfarm, unidirectional dc–dc converters.**

I. Introduction

HIGH-voltage direct current (HVdc) transmission system is a well-established and proven technology for delivering large-scale energy over a long distance with less

Manuscript received January 13, 2018; revised April 2, 2018 and June 21, 2018; accepted August 8, 2018. Date of publication August 21, 2018; date of current version April 20, 2019. This work was supported by SP Energy Networks through the Network Innovation Allowance Project No. RES/0560/7466/002. Recommended for publication by Associate Editor Y. Xue. *(Corresponding author: He Liu.)*

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loss. However, a large core is required for thermal dissipation, limiting the whole system power density and large-scale applications. In addition, more recently improved soft switching range was achieved by additional active switches [13]–[15]. However, the added switches complicate the control and increase the switching losses, especially for a larger-scale system.

Modular multilevel converters (MMC) based on dc collection point for HVdc system have received great attention in the recent years due to their manifold advantages including modularity, straightforward scalability, high-quality output voltage with low harmonic distortion, etc. A dual active MMC-based dc–dc converter linked by a medium frequency transformer, functioning as dc collection point in the HVDC system is proposed in [16]–[19]. Another variation of the MMC or else known as alternate arm converter has been also reported in [20]. These converters feature bidirectional power flow and mostly operate with medium frequency aiming to reduce the switching losses and the size/volume. However, bidirectional power transmission capability is unnecessary for the proposed offshore windfarm dc collection point, as it contributes to more switching losses and increases the control complicity.

Other variations of high-voltage dc–dc converters have been also reported in [21]–[23], where in [22], an *LCL*-based dc–dc converter is developed using thyristor technology. While it has the capability of bidirectional power flow and dc fault clearance on both sides of the converter; however, the conversion ratio of such a converter is limited, which makes it improper for a large-scale HVdc system. Denniston *et al.* [23] introduced a multimodule high-gain and high-voltage transformerless dc–dc converter using a single-switch and a single-inductor. However, due to the absence of the transformer, this converter lacks electrical isolation feature. On the other hand, a high-efficiency, step-up resonant dc–dc converter for offshore wind farm HVdc system is studied in [24]. The soft-switching technique is applied for all switches in the converter, therefore, the high switching frequency can be used resulting in a smaller volume and weight with lower switching losses. Nevertheless, the lack of modularity not only limits the system from flexible scalability, but also increases control complexity and manufacturing cost.

The work in this paper is aimed at alleviating the abovementioned issues by proposing a unidirectional high voltage (HV) modular dc–dc converter, employing MMC at the primary side of a medium frequency transformer. It is noted that the medium voltage obtained from the medium voltage dc–dc converter as shown in Fig. 1 is normally in the range of 10 to 50 kV or even higher, depends on the technology and the layout of the offshore wind farms. In such medium voltage range, the employed MMC at the primary side of the proposed converter will not require a large number of submodules (SMs), which in turns, significantly reduces the cost and losses, hence higher efficiency. Furthermore, due to modular design of MMC, the number of SMs can be flexibly changed to meet different input voltage levels requirement. Meanwhile, the dc voltage is collected at the secondary side through series-connected diode-bridge rectifier modules. Due to the use of diode bridge rectifier modules at the secondary side, the control system is not required. From the compassion in Section IV, the proposed converter shows a

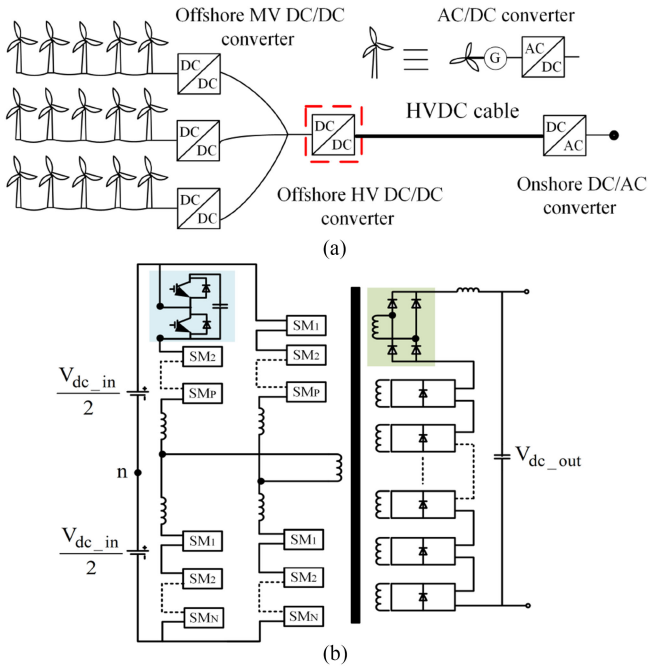


Fig. 1. (a) Typical schematic diagram of off-shore HVdc transmission system and (b) using the proposed high voltage (HV) dc–dc converter functioned as dc collection point (red dashed line).

superior performance in terms of efficiency, losses, and devices utilization, when compared with the most competitive unidirectional cascaded input series output series (ISOS) and IPOS converters, which makes it more attractive for this particular application. A control method based on proportional resonant (PR) strategy is employed for the proposed converter. It should be noted that the proposed converter is just intended for the HV dc collection point (HV dc–dc converter) as shown in Fig. 1 (red dashed line).

The rest of the paper is organized as follows: Section II describes the circuit configuration of the proposed dc–dc converter and its operating principle. The power balance analysis of the MMC at the primary side is presented in Section III. Section IV details the losses calculation of the proposed converter and its medium frequency transformer. A comparison between the proposed converter and the most competitive unidirectional topology based on SAB dc–dc converters with ISOS and IPOS is also presented in Section IV. A simple control strategy based on the stationary reference frame, using PR controller is derived in Section V. Section VI illustrates selected simulation and experimentally validated results. Finally, the work is concluded in Section VII.

II. Proposed DC–DC Converter Based System

A. Structure of the Proposed Converter

Fig. 1 shows a simplified schematic diagram of a typical HVdc offshore windfarm using the proposed modular dc–dc converter, functioning as HV dc collection point (red dashed line in Fig. 1), where a single-phase (two-leg) MMC inverter producing a controllable ac voltage is connected at the primary

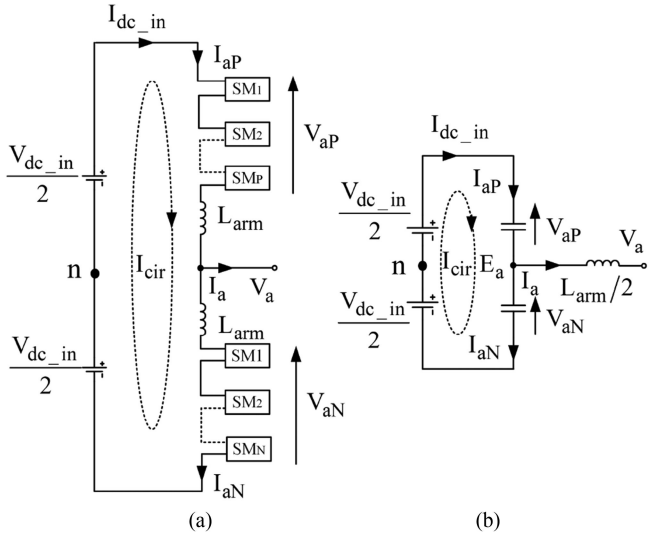


Fig. 2. (a) Schematic diagram of the one-leg MMC and (b) its equivalent circuit.

side of a medium frequency (400 Hz) transformer. The dc output voltage is obtained through series-connected full-bridge rectifier modules at the multiwinding secondary side of the transformer. It is worth noting that the design is fully modular at both sides and can be easily expanded as required by simply adding more modules. The dc output voltage is controlled via controlling the ac voltage of the MMC at the primary side and a PR regulator is employed in this paper to perform the overall control of the converter.

B. Mathematical Model of the Proposed Converter

Fig. 2 shows the equivalent circuit of one-leg (Phase A) of the MMC, where $V_{\mathrm{dc\_in}}$ and $I_{\mathrm{dc\_in}}$ are the converter's dc input voltage and current, respectively. V_{ap} and V_{aN} are the upper and lower arm voltages of the cascede SMs of Phase A leg, respectively. I_{aP} and I_{aN} are the current of the upper and lower arms, respectively. E_a is the equivalent output phase voltage as shown in Fig. 2(b) and V_a is output ac voltage, respectively. I_{cir} and I_a are circulating current and ouput ac current, respectively.

From Fig. 2, the upper and lower arm currents of Phase A leg can be expressed as

$$I_{aP} = I_a/2 + I_{\mathrm{cir}} \tag{1}$$

$$I_{aN} = -I_a/2 + I_{\mathrm{cir}} \tag{2}$$

where the circulating current, I_{cir}, is flowing through both the upper and lower amrs.

It should be noted that the circulating current has no effect on the ouptut phase current and can be expressed as

$$I_{\mathrm{cir}} = (I_{aP} + I_{aN})/2\,. \tag{3}$$

With reference to (1) and (2), the equation of output ac current I_a can be expressed in terms of upper and lower arm currents as

$$I_a = I_{aP} - I_{aN}\,. \tag{4}$$

Considering *n* as the neutral point, applying the Kirchhoff voltage laws (KVL) for the schematic diagram of one-leg MMC as shown in Fig. 2(a), the upper and lower voltages can be derived as

$$V_{aP} = \frac{V_{\mathrm{dc}}}{2} - V_a - L_{\mathrm{arm}}\frac{dI_{aP}}{dt} \tag{5}$$

$$V_{aN} = \frac{V_{\mathrm{dc}}}{2} + V_a - L_{\mathrm{arm}}\frac{dI_{aN}}{dt}. \tag{6}$$

Combining (5) and (6), the output phase voltage V_a can be expressed as

$$V_a = \frac{1}{2}\,(V_{aN} - V_{aP}) - \frac{1}{2}L_{\mathrm{arm}}\frac{d\,(I_{aN} - I_{aP})}{dt}. \tag{7}$$

Substituting (4) into (7), the equivalent output phase voltage E_a can be given by

$$E_a = \frac{1}{2}\,(V_{aN} - V_{aP}) = V_a + \frac{1}{2}L_{\mathrm{arm}}\frac{dI_a}{dt}. \tag{8}$$

Therefore, the mathmatical model of the one-leg MMC can be derived by rearranging (8) as

$$\frac{1}{2}L_{\mathrm{arm}}\,\frac{dI_a}{dt} = E_a - V_a. \tag{9}$$

According to (9), the equivalent circuit of Phase A can be expressed as Fig. 2(b).

Similarly, the mathmatical model of the second leg of MMC (i.e., phase B), can be given by

$$\frac{1}{2}L_{\mathrm{arm}}\,\frac{dI_b}{dt} = E_b - V_b \tag{10}$$

where E_b and V_b are the equivalent output phase voltage and output ac voltage of Phase B, respectively, and I_b is the ouptut ac current of Phase B.

Combining (9) and (10), the mathmatical model of single phase (two-leg) MMC can be expressed as

$$\frac{1}{2}L_{\mathrm{arm}}\frac{dI_a}{dt} - \frac{1}{2}L_{\mathrm{arm}}\,\frac{dI_b}{dt} = (E_a - E_b) - (V_a - V_b)\,. \tag{11}$$

For simplicity, let

$$E_{ab} = E_a - E_b \tag{12}$$

$$V_{ab} = V_a - V_b. \tag{13}$$

Hence, (11) can be rewritten as

$$\frac{1}{2}L_{\mathrm{arm}}\,\frac{d(I_a - I_{b)}}{dt} = E_{ab} - V_{ab}. \tag{14}$$

For a single phase (two-leg) MMC, the relationship between the output current of Phase A and B can be expressed as

$$I_P = I_a\ = -I_b \tag{15}$$

where I_P is the transformer primary current of the proposed converter.

Substituting (15) into (14), yields

$$L_{\mathrm{arm}}\,\frac{dI_P}{dt} = E_{ab} - V_{ab} \tag{16}$$

where E_{ab} and V_{ab} can be considered as the equivalent primary voltage and primary terminal voltage of the transformer, respectively.

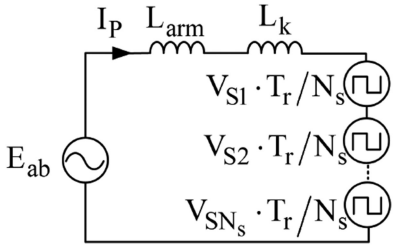


Fig. 3. Equivalent circuit of the proposed converter referred to primary side.

From Fig. 1, the secondary side of the transformer is made of a combination of individual and isolated rectifier modules. This can be regarded as a series connection of voltage sources $(V_{s1}, V_{s2}, \ldots, V_{s(N_s)})$. Therefore, the total equivalent voltage at the secondary side of the transformer V_s, can be expressed as

$$V_s = V_{s1} + V_{s2} + \cdots + V_{s(N_s)} \tag{17}$$

where N_s is the number of rectifier modules at the secondary side of the transformer.

If the equivelant primary-to-secondary winding turns ratio is R_t and the turns ratio of primary to each individual secondary winding is T_r, the equivelant secondary volatge V_s when it is referred to the primary side can then be given by

$$V_{ab} = V_s\ R_t = V_{s1}\ \frac{T_r}{N_s} + V_{s2}\frac{T_r}{N_s} + \cdots + V_{s(N_s)}\frac{T_r}{N_s}. \tag{18}$$

Substituting (16) into (18), and with the transformer's leakage inductance L_k referred to the primary side, the primary referred equivalent circuit of the proposed converter converter can be expressed by (19) and schematically represented by Fig. 3

$$(L_{\text{arm}} + L_k)\ \frac{dI_p}{dt} = E_{ab}\ - V_s R_t. \tag{19}$$

C. Voltage and Current Key-Waveforms of the Proposed Converter

For the sake of simplicity and easy understanding, the following are assumed for the MMC at the primary side: 1) The SMs' capacitor voltages are balanced and ripple-free; 2) the converter is operating with a unity modulation index; and 3) high number of SMs, resulting in a very close to sinusoidal ac output waveform. Furthermore, the well-known carrier-phase-shift pulsewidth modulation (CPS-PWM) [25] technique is used in this work to modulate the MMC.

With the above assumptions, the ideal primary and secondary referred voltage waveforms of the proposed converter can be represented as in Fig. 4, where the power is transferred from $V_{\text{dc\_in}}$ to $V_{\text{dc\_out}}$, i.e., unidirectional power flow. As discussed in Section II-B above, V_S is the equivalent secondary ac voltage, which is equal to $V_S = V_{S1} + V_{S2} + \cdots + V_{S(N_s)}$ and φ is the phase shift angle by which the primary equivalent ac voltage, E_{ab}, leads the secondary equivalent ac voltage, V_S.

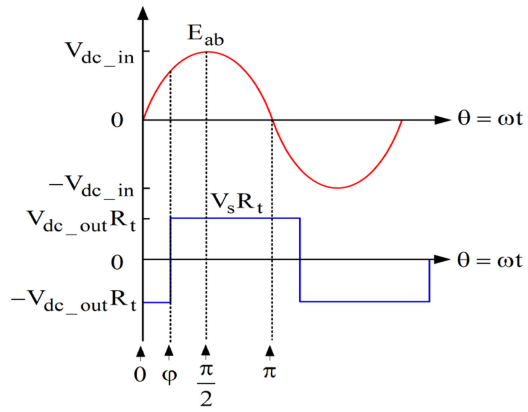


Fig. 4. Typical voltage and current key waveforms of the equivalent circuit of the proposed converter with all voltages are referred to primary.

D. Output Power of the Proposed Converter

It should be noted that in the analysis below takes the following two assumptions into account: 1) the ac output waveform is symmetrical and, therefore, only half of the cycle is considered for the output power derivation and 2) for simplicity, the peak value of E_{ab} and V_S are equal to $V_{\text{dc\_in}}$, and $V_{\text{dc\_out}}$, respectively (i.e., ignoring any voltage drop across the circuit components).

From Fig. 4, the output power can be derived based on the following operational intervals.

Interval 1 ($0 \le \theta < \varphi$) : As it can be noticed from Fig. 4, during this interval $V_S(\theta)$ is equal to the $-V_{\text{dc\_out}}$, and its primary refered voltage is $-V_{\text{dc\_out}}R_t$. Therefore, $E_{ab}(\theta)$ and $I_P(\theta)$ can be expressed as

$$E_{ab}\ (\theta)\ = V_{\text{dc\_in}}\ \sin(\theta) \tag{20}$$

$$I_P\ (\theta)\ = I_P\ (0) + \frac{1}{\omega L}\int_0^{\theta}\left[E_{ab}\ (\theta) - R_t V_S\ (\theta)\right] d\theta \tag{21}$$

replacing $V_S(\theta)$ by $-V_{\text{dc\_out}}$ and substituting (20) into (21), yields

$$I_P\ (\theta) = I_P\ (0) + \frac{1}{\omega L}\left[2V_{\text{dc\_in}}\sin\left(\frac{\theta}{2}\right)^2 + R_t V_{\text{dc\_out}}\theta\right]. \tag{22}$$

According to (22), when $\theta = \varphi$, one can get

$$I_P\ (\varphi) = I_P\ (0) + \frac{1}{\omega L}\left(V_{\text{dc\_in}} - V_{\text{dc\_in}}\cos\varphi + V_{\text{dc\_out}}R_t\varphi\right). \tag{23}$$

According to $V_S(\theta)$ and (22), the output energy during this interval can be obtained by

$$E_1 = \int_0^{\varphi} V_S\ (\theta) * I_P\ (\theta)\, d\theta = -\frac{{R_t}^2 {V_{\text{dc\_out}}}^2 \varphi^2}{2\omega L} - V_{\text{dc\_out}}R_t\varphi I_P\ (0) - \frac{R_t V_{\text{dc\_in}} V_{\text{dc\_out}}\left[\varphi - \sin(\theta)\right]}{\omega L}. \tag{24}$$

Interval 2 ($\varphi \le \theta < \pi$) : During this interval, $V_S(\theta)$ is equal to $V_{\text{dc\_out}}$ and $E_{ab}(\theta)$ remains equal to $V_{\text{dc\_in}}\sin(\theta)$, therefore,

$I_P(\theta)$ can be expressed as

$$I_P\ (\theta) = I_P\ (\varphi) + \frac{1}{\omega L}\int_{\varphi}^{\theta} [E_{ab}\,(\theta) - R_t V_S\,(\theta)]d\theta. \quad (25)$$

Substituting $V_S\ (\theta) = V_{\mathrm{dc\_out}}, E_{ab}(\theta) = V_{\mathrm{dc\_in}}\ \sin(\theta)$ and (23) into $I_P(\theta)$ with (25) yields

$$I_P\ (\theta) = I_P\ (0) + \frac{1}{\omega L}\left[V_{\mathrm{dc\_in}} - V_{\mathrm{dc\_in}}\cos\varphi - R_t V_{\mathrm{dc\_out}}\theta + 2R_t V_{\mathrm{dc\_out}}\varphi\right]. \quad (26)$$

From (26), at $\theta = \pi$, one can get

$$I_P\ (\pi) = I_P\ (0) + \frac{1}{\omega L}\left[2V_{\mathrm{dc\_in}} - \pi R_t V_{\mathrm{dc\_out}} + 2R_t V_{\mathrm{dc\_out}}\right]. \quad (27)$$

Similarly, the transferred energy during this interval is given by

$$E_2 = \int_{\varphi}^{\pi} V_S\,(\theta) * I_P\,(\theta)\,d\theta = -\frac{R_t V_{\mathrm{dc\_out}}}{2\omega L}\left[\begin{pmatrix} 2V_{\mathrm{dc\_in}}\varphi - 2\pi V_{\mathrm{dc\_in}} - 2V_{\mathrm{dc\_in}}\sin(\theta) + \pi^2 R_t V_{\mathrm{dc\_out}} \\ + 3R_t V_{\mathrm{dc\_out}}\varphi^2 - 2\pi L I_P\,(0) + 2L\varphi I_P\,(0) \\ - 4\pi R_t V_{\mathrm{dc\_out}}\varphi \end{pmatrix}\right]. \quad (28)$$

Therefore, from (24) and (28), the ouput power of the proposed converter can be calcultaed as

$$P_{\mathrm{out}} = \frac{E_1 + E_2}{\pi}. \quad (29)$$

Owing to the half-cycle symmetry, $I_P\ (0) = -I_P\ (\pi)$. Therefore, according to (27), the initial current $I_P(0)$ can be calculated as

$$I_P\ (0) = \frac{2V_{\mathrm{dc\_in}} - \pi R_t V_{\mathrm{dc\_out}} + 2R_t V_{\mathrm{dc\_out}}\varphi}{2\omega L}. \quad (30)$$

Therefore, the ouput power of the proposed converter at any phase shift angle, φ, can be expressed by

$$P_{\mathrm{out}}\ (\varphi) = \frac{2GV_{\mathrm{dc\_in}}^2 \sin(\varphi)}{\pi\omega L} \quad (31)$$

where G is defined as the primary-referred dc voltage gain of the proposed converter that is equal to $\mathrm{G} = \frac{V_{\mathrm{dc\_out}} R_t}{V_{\mathrm{dc\_in}}}$, which is often known as the dc conversion ratio [26].

E. Output Power Characteristics of the Proposed Converter

Similar to the conventional SAB dc–dc converter [27], pahse shift angle φ is the point where the primary current, I_P, crosses the zero, which means $I_P\ (\varphi) = 0$. Using this relationship ($I_P\ (\varphi) = 0$) gets

$$G = \frac{2\cos(\varphi)}{\pi}. \quad (32)$$

Substituting (32) into (31), yields

$$P_{\mathrm{out}}\,(\varphi) = \frac{4V_{\mathrm{dc\_in}}^2 \sin(\varphi)\cos(\varphi)}{\pi^2\omega L}. \quad (33)$$

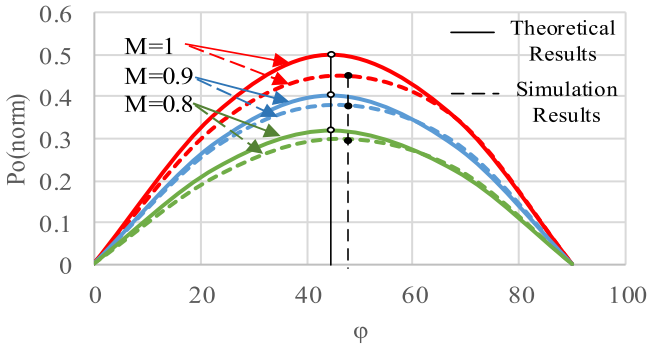


Fig. 5. Normalized output power versus pahse shift angle φ of the proposed converter.

It should be noted that (33) is derived based on the assumption of the modulation index $M = 1$, which corresponds to the maximum power transfer capability of the proposed converter.

For simplicity, the ouput power is normalized to a base power of $P_b = \frac{4V_{\mathrm{dc\_in}}^2}{\pi^2\omega L}$, which results in

$$P_{\mathrm{out\_norm}}\ (\varphi) = M^2 \sin(\varphi)\cos(\varphi) \quad (34)$$

where modulation index $M \in [0, 1]$ is introduced in oder to get the generalized equation of the ouput power.

Fig. 5 illustrates the variation of the normalized power of (34) with respect to phase shift angle φ (noting that the solid line represents theoretical results and dashed line represents simulation results based on parameters in Table V). Furthermore, it is also clear from the same figure that the power transfer capability of the proposed converter is influenced by the modulation index *M*, and the phase shift angle φ, where the highest power is achieved with a unity modulation index. In theory, the maximum output power occurs at the point of $\frac{dP_{\mathrm{out\_norm}}(\varphi)}{d\varphi} = 0$, for which $\varphi = \frac{\pi}{4}$. However, when taking losses of circuit and primary ac voltage (nonideal sinusoidal) into considersion, the maximum output power point will deviate from $\varphi = \frac{\pi}{4}$ as shown in Fig. 5.

III. Power Balance of the Proposed Converter

One of the most challenging aspects of MMC is how to keep the SM capacitors voltage controlled. Therefore, it is very important to analyze and understand the stored energy and the power flow between the SMs and/or the converter arms [28], [29]. To simplify the analysis, the following are assumed: 1) the converter's arm inductance is neglected; 2) only the fundamental component of the MMC ac voltage is considered; and 3) only one-leg of MMC converter is considered as example. Therefore, the output ac current and voltage of Phase A can be approximately expressed as

$$V_a = \hat{V}_m\ \sin(\omega t) \quad (35)$$

$$I_a = \hat{I}_m\ \sin(\omega t - \emptyset) \quad (36)$$

where V_a and $\hat{V}_m$ are the instantaneous output ac voltage and its peak value, respectively; I_a and $\hat{I}_m$ are the instantaneous output ac current and its peak value, respectively.

The equivalent circuit of a balanced one-leg MMC is shown in Fig. 6(a), where the upper and lower SMs are modeled as a

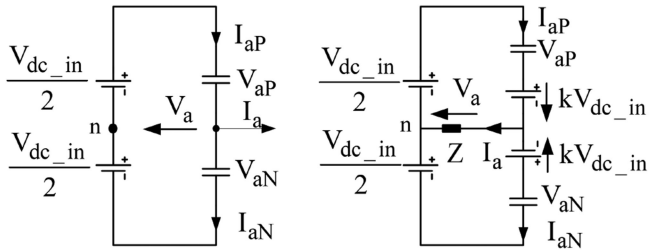


Fig. 6. Equivalent circuit of one-leg MMC. (a) Balanced energy condition. (b) Unbalanced energy condition.

voltage source. Furthermore, an unbalanced energy across the upper and lower arm causing a dc offset to the output ac voltage, is presented by a dc source denoted by $kV_{\mathrm{dc\_in}}$ (i.e., k is defined as unbalance factor, $k \in [-0.1, 0.1]$) in the upper and lower arms as shown in Fig. 6(b).

Therefore, applying KVL, the upper and lower arms voltages can, respectively, be defined by

$$V_{aP} = \frac{V_{\mathrm{dc\_in}}}{2} - \hat{V}_m \sin\omega t + kV_{\mathrm{dc\_in}} \tag{37}$$

$$V_{aN} = \frac{V_{\mathrm{dc\_in}}}{2} + \hat{V}_m \sin\omega t - kV_{\mathrm{dc\_in}}. \tag{38}$$

Let M be the modulation index of the MMC output ac voltage. Therefore, the peak output voltage of one-leg can be then given by

$$\hat{V}_m = \frac{1}{2} MV_{\mathrm{dc\_in}}. \tag{39}$$

Rearranging (39), the input dc voltage can be expressed as

$$V_{\mathrm{dc\_in}} = \frac{2\hat{V}_m}{M}. \tag{40}$$

Substituting (40) into (37) and (38) yields

$$V_{aP} = \frac{\hat{V}_m}{M} - \hat{V}_m \sin\omega t + k\frac{2\hat{V}_m}{M} \tag{41}$$

$$V_{aN} = \frac{\hat{V}_m}{M} + \hat{V}_m \sin\omega t - k\frac{2\hat{V}_m}{M}. \tag{42}$$

It is well known that dc voltage offset will produce a dc current, denoted by I_{ki} in the upper and lower arms, which is caused by the effect of the unbalanced energy. From Fig. 6(b), the upper and lower arms currents can be defined as

$$I_{aP} = I_{\mathrm{dc\_in}} + \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) - I_{ki} \tag{43}$$

$$I_{aN} = I_{\mathrm{dc\_in}} - \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) + I_{ki}. \tag{44}$$

As the introduced unbalanced voltage sources are only dc, consequently, the resultant currents are dc as well. Furthermore, this current flow through the load impedance, which is naturally inductive, however only the resistive part of the impedance needs to be considered as the current is a dc. Therefore, the unbalance dc current I_{ki} in the circuit can therefore be calculated by

$$I_{ki} = \frac{kV_{\mathrm{dc\_in}}}{R} \tag{45}$$

where R is the load resistance.

Neglecting the power losses in the circuit, the power flowing from dc side is equal to the power consumed at the ac side of MMC. Hence

$$P_{\mathrm{dc}} = P_{\mathrm{ac}} = V_{\mathrm{dc\_in}}\, I_{\mathrm{dc\_in}} = \frac{1}{2}\hat{V}_m\, \hat{I}_m \cos\emptyset + 2I_{ki} \cdot kV_{\mathrm{dc\_in}} \tag{46}$$

where V_{dc} and I_{dc} are the input dc voltage and current, respectively; $\cos\emptyset$ is the power factor. It is important to note that the consumed power, $2I_{ki} \cdot kV_{\mathrm{dc}}$ is caused by biased dc on the ac load.

By substituting $\hat{V}_m$ of (39) and I_{ki} of (45) into (46), the input dc current can be obtained by

$$I_{\mathrm{dc\_in}} = \frac{1}{4}\, M\hat{I}_m \cos\emptyset + \frac{4k^2\hat{V}_m}{R \cdot M}. \tag{47}$$

Now, substituting (39), (45), and (47) into (43) and (44) yields

$$I_{aP} = \frac{1}{4}\, M\hat{I}_m \cos\emptyset + \frac{4k^2\hat{V}_m}{R \cdot M} + \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) - \frac{2k\hat{V}_m}{M} \tag{48}$$

$$I_{aN} = \frac{1}{4}\, M\hat{I}_m \cos\emptyset + \frac{4k^2\hat{V}_m}{R \cdot M} - \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) + \frac{2k\hat{V}_m}{M}. \tag{49}$$

From the above analysis, the instantaneous power of the upper and lower arms is expressed by

$$P_{aP} = V_{aP} \times I_{aP} = \left(\frac{\hat{V}_m}{M} - \hat{V}_m \sin\omega t + k\frac{2\hat{V}_m}{M}\right) \left[\frac{1}{4}M\hat{I}_m \cos\emptyset + \frac{4k^2\hat{V}_m}{R \cdot M} + \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) - \frac{2k\hat{V}_m}{M}\right] \tag{50}$$

$$P_{aN} = V_{aN} \times I_{aN} = \left(\frac{\hat{V}_m}{M} + \hat{V}_m \sin\omega t - k\frac{2\hat{V}_m}{M}\right) \left[\frac{1}{4}M\hat{I}_m \cos\emptyset + \frac{4k^2\hat{V}_m}{R \cdot M} - \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) + \frac{2k\hat{V}_m}{M}\right]. \tag{51}$$

By integrating (50) and (51) over one fundamental period, one can obtain the energy variation in the upper and lower arms as follows:

$$E_{aP} = \int_0^{2\pi} P_{aP}\, dt = \frac{\pi\hat{V}_m}{R}\left(\frac{16\hat{V}_m k^3}{M^2} + k\hat{I}_m R\cos\emptyset - \frac{4\hat{V}_m k}{M^2}\right) \tag{52}$$

$$E_{aN} = \int_0^{2\pi} P_{aN}\, dt = -\frac{\pi\hat{V}_m}{R}\left(\frac{16\hat{V}_m k^3}{M^2} + k\hat{I}_m R\cos\emptyset - \frac{4\hat{V}_m k}{M^2}\right). \tag{53}$$

Equations (52) and (53) describe the effect of the unbalance factor k on the arm energy, where in the case of $k = 0$, the average energy transferred to the upper and lower arms over one cycle is zero, i.e., $E_{aP} = E_{aN} = 0$. However, when $k \neq 0$, although the transferred energy in one cycle between upper and lower arms remains zero, i.e., $E_{aP} + E_{aN} = 0$; but there will be an unbalanced energy, i.e., $E_{aP} = E_{aN} \neq 0$, which causes deviations in SMs capacitor voltage and therefore energy exchange between the upper and lower arms is necessary to balance. Furthermore, as the circulating current influences the charging and discharging of SM capacitors, therefore it is mandatory to control the circulating current to achieve voltage balance. A voltage balance control strategy, which includes SM voltage control and arm average voltage control, is employed for the proposed converter. Since this control method has been well-documented [30], therefore, no further details are given here.

IV. Losses Calculation and Topological Comparison

It is very important to demonstrate the superiority of the proposed converter compared to its competitive unidirectional dc–dc converters. For such applications, high output voltage is required, therefore, cascaded topologies such as ISOS and IPOS as shown in Fig. 7 are selected for comparison with the proposed converter.

To simplify the analysis, it should be noted that 1) only the fundamental component of the ac output current of the converter is considered for the power loss calculation and 2) the power is equally shared between the SAB-based SMs in the unidirectional cascaded converters. Furthermore, because of the current flown characteristics of unidirectional cascaded dc–dc converters (e.g., ISOS/IPOS) has been well introduced and analyzed in [7] and [8], hence we just take the proposed converter as an example to derive its losses calculation method.

A. Losses Calculation of the Proposed Converter

Since the proposed converter is a unidirectional, therefore, the losses are calculated only when the MMC operates as an inverter, however, it should be noted that in both modes (i.e., rectifier/inverter), the calculation process is the same. Furthermore, only the fundamental component of the ac output voltage of the MMC is considered in the power loss calculation.

Since CPS-PWM is utilized to control the switches of the proposed MMC converter, therefore, the duty cycle $\tau(t)$ of all switches is defined by

$$\tau\ (t) = \frac{1 + M \sin(\omega t)}{2} \tag{54}$$

where M is the modulation index, and ω is the fundamental angular frequency of the ac output waveform.

Table I lists the possible operating modes of the MMC's SM where the currents directions are schematically presented in Fig. 8 [28]. Taking the upper arm of Phase A as an example, each SM is either inserted or by-passed, making the voltage of Phase A either increased or decreased by an SM capacitor voltage, V_c, respectively. When the modulation signal is greater

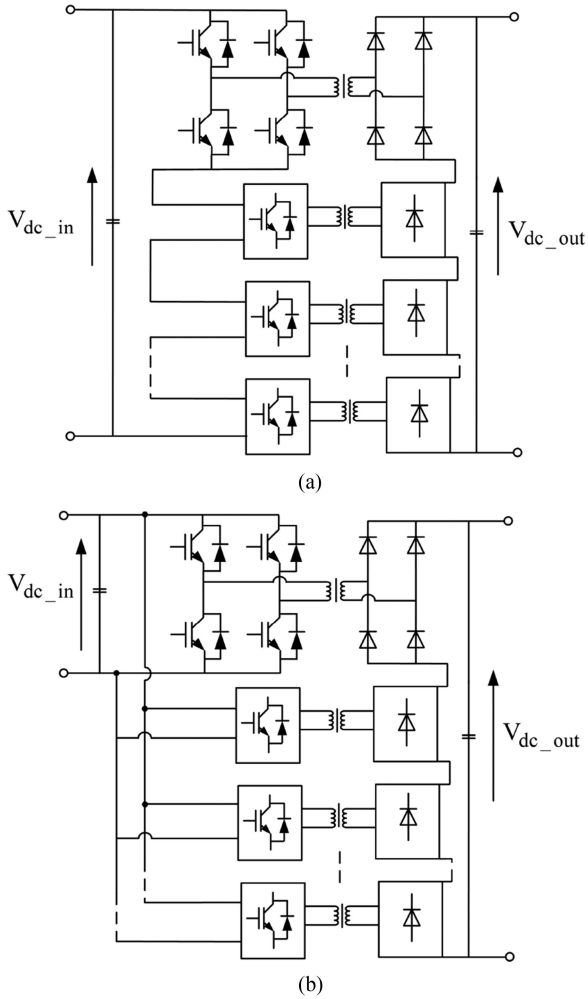


Fig. 7. Unidirectional cascaded dc–dc converters. (a) ISOS. (b) IPOS.

TABLE I
SM States of MMC

states	T_1	T_2	I_{sm}	V_{sm}	submodule
1	ON	OFF	> 0	V_c	Inserted (charging)
2	ON	OFF	< 0	V_c	Inserted (discharging)
3	OFF	ON	> 0	0	By-passed
4	OFF	ON	< 0	0	By-passed

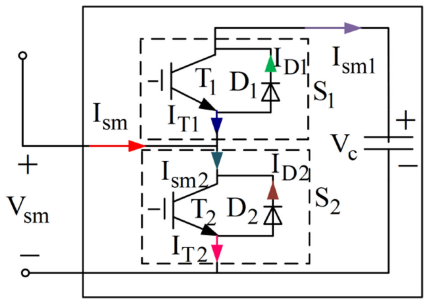


Fig. 8. Current definition of a SM of MMC.

than the carrier signal, T_2 is turned ON and T_1 is turned OFF, which means SM is by-passed. However, on the other hand, when the modulation signal is less than the carrier signal, T_2 is turned OFF and T_1 is turned ON, which means SM is inserted in the circuit. Therefore, if the carrier cycle is T_c, then the conduction time of T_2 when the SM is by-passed is equal to $\tau(t) \cdot T_c$ according to the derived duty cycle in (54). On the other hand, the conduction time of T_1 equals to $[1-\tau(t)] \cdot T_c$, when the SM is inserted. Therefore, based on above analysis, the current flowing through the upper and lower IGBT modules, S_1 and S_2, respectively can be expressed as

$$I_{\mathrm{sm1}} = [1-\tau(t)] * I_{aP}(t) \tag{55}$$

$$I_{\mathrm{sm2}} = \tau(t) * I_{aP}(t) \tag{56}$$

where $I_{aP}(t)$ is the upper arm current of Phase A.

From the operation principle of the MMC, in the normal circumstances, the input dc current, $I_{\mathrm{dc\_in}}$ would be evenly distributed between the two legs, and the ac output currents of each phase are evenly distributed between the upper and the lower arms. Therefore, the upper arm current of Phase A can be expressed as

$$I_{aP}\ (t) = \frac{I_{\mathrm{dc\_in}}}{2} + \frac{1}{2}\hat{I}_a \sin(\omega t - \delta). \tag{57}$$

Substituting (54) and (57) into (55) and (56) yields

$$I_{\mathrm{sm1}} = \frac{1-M\sin(\omega t)}{2} * \left[\frac{I_{\mathrm{dc\_in}}}{2} + \frac{1}{2}\hat{I}_a \sin(\omega t - \delta)\right] \tag{58}$$

$$I_{\mathrm{sm2}} = \frac{1+M\sin(\omega t)}{2} * \left[\frac{I_{\mathrm{dc\_in}}}{2} + \frac{1}{2}\hat{I}_a \sin(\omega t - \delta)\right]. \tag{59}$$

From (58) and (59), the effective and average values of the currents flowing through the switches and diodes of SM can be derived as follows.

1) *The average current flowing through diode D_1 is*

$$I_{\mathrm{D1\_avg}} = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} I_{\mathrm{sm1}}\, d\omega t. \tag{60}$$

Substituting (58) into (60) yields

$$I_{\mathrm{D1\_avg}} = \frac{1}{2\pi}\left[\frac{\hat{I}_a}{2} + \frac{\pi I_{\mathrm{dc\_in}}}{4} - \frac{I_{\mathrm{dc\_in}} M\cos(\delta)}{2} - \frac{\pi \hat{I}_a M\cos(\delta)}{8}\right]. \tag{61}$$

2) *The square of effective current flowing through diode D_1 is*

$${I_{\mathrm{D1\_rms}}}^2 = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} {I_{\mathrm{sm1}}}^2 d\omega t. \tag{62}$$

Substituting (58) into (62) yields

$$\begin{aligned}{I_{\mathrm{D1\_rms}}}^2 = \frac{1}{2\pi}\Bigg[&\frac{\hat{I}_a I_{\mathrm{dc\_in}}}{4} + \frac{\pi \hat{I}_a^2}{32} + \frac{\pi {I_{\mathrm{dc\_in}}}^2}{36} + \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2}{8} \\ &- \frac{a^2 M\cos(\delta)}{6} - \frac{{I_{\mathrm{dc\_in}}}^2 M\cos(\delta)}{4} + \frac{\pi \hat{I}_a^2 M^2}{64} \\ &+ \frac{\pi {I_{\mathrm{dc\_in}}}^2 M^2}{32} + \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2\cos(2\delta)}{24} \\ &+ \frac{\pi \hat{I}_a^2 M^2\cos(2\delta)}{128} + \frac{\pi \hat{I}_a I_{\mathrm{dc\_in}} M\cos(\delta)}{8}\Bigg].\end{aligned} \tag{63}$$

3) *The average current flowing through switch T_1 is*

$$I_{\mathrm{T1\_avg}} = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} I_{\mathrm{sm1}}\, d\omega t. \tag{64}$$

Substituting (58) into (64) yields

$$I_{\mathrm{T1\_avg}} = -\frac{1}{2\pi}\left[\frac{\hat{I}_a}{2} - \frac{\pi I_{\mathrm{dc\_in}}}{4} - \frac{I_{\mathrm{dc\_in}} M\cos(\delta)}{2} + \frac{\pi \hat{I}_a M\cos(\delta)}{8}\right]. \tag{65}$$

4) *The square of effective current flowing through switch T_1 is*

$${I_{\mathrm{T1\_rms}}}^2 = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} {I_{\mathrm{sm1}}}^2 d\omega t. \tag{66}$$

Substituting (58) into (66) yields

$$\begin{aligned}{I_{\mathrm{T1\_rms}}}^2 = \frac{1}{2\pi}\Bigg[&\frac{\pi \hat{I}_a^2}{32} - \frac{\hat{I}_a I_{\mathrm{dc\_in}}}{4} + \frac{\pi {I_{\mathrm{dc\_in}}}^2}{16} - \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2}{8} \\ &+ \frac{\hat{I}_a^2 M\cos(\delta)}{6} + \frac{{I_{\mathrm{dc\_in}}}^2 M\cos(\delta)}{4} + \frac{\pi \hat{I}_a^2 M^2}{64} \\ &+ \frac{\pi {I_{\mathrm{dc\_in}}}^2 M^2}{32} - \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2\cos(2\delta)}{24} \\ &+ \frac{\pi \hat{I}_a^2 M^2\cos(2\delta)}{128} - \frac{\pi \hat{I}_a I_{\mathrm{dc\_in}} M\cos(\delta)}{8}\Bigg].\end{aligned} \tag{67}$$

5) *The average current flowing through switch T_2 is*

$$I_{\mathrm{T2\_avg}} = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} I_{\mathrm{sm2}}\, d\omega t. \tag{68}$$

Substituting (59) into (68) yields

$$I_{\mathrm{T2\_avg}} = \frac{1}{2\pi}\left[\frac{\hat{I}_a}{2} + \frac{\pi I_{\mathrm{dc\_in}}}{4} + \frac{I_{\mathrm{dc\_in}} M\cos(\delta)}{2} + \frac{\pi \hat{I}_a M\cos(\delta)}{8}\right]. \tag{69}$$

6) *The square of effective current flowing through switch T_2 is*

$$I_{\mathrm{T2\_rms}}{}^2 = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} I_{\mathrm{sm2}}{}^2 d\omega t. \tag{70}$$

Substituting (59) into (70) yields

$$\begin{aligned} I_{\mathrm{T2\_rms}}{}^2 = \frac{1}{2\pi}\Bigg[&\frac{\hat{I}_a I_{\mathrm{dc\_in}}}{4} + \frac{\pi \hat{I}_a^2}{32} + \frac{\pi I_{\mathrm{dc\_in}}{}^2}{16} + \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2}{18} \\ &+ \frac{\hat{I}_a^2 M\cos(\delta)}{6} + \frac{I_{\mathrm{dc\_in}}{}^2 M\cos(\delta)}{4} + \frac{\pi \hat{I}_a^2 M^2}{64} \\ &+ \frac{\pi I_{\mathrm{dc\_in}}{}^2 M^2}{32} + \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2\cos(2\delta)}{224} \\ &+ \frac{\pi \hat{I}_a^2 M^2\cos(2\delta)}{128} + \frac{\pi \hat{I}_a I_{\mathrm{dc\_in}} M\cos(\delta)}{8}\Bigg]. \end{aligned} \tag{71}$$

7) *The average current flowing through diode D_2 is*

$$I_{\mathrm{D2\_avg}} = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} I_{\mathrm{sm2}} d\omega t. \tag{72}$$

Substituting (59) into (72) yields

$$\begin{aligned} I_{\mathrm{D2\_avg}} = -\frac{1}{2\pi}\Bigg[&\frac{\hat{I}_a}{2} - \frac{\pi I_{\mathrm{dc\_in}}}{4} + \frac{I_{\mathrm{dc\_in}} M\cos(\delta)}{2} \\ &- \frac{\pi \hat{I}_a M\cos(\delta)}{8}\Bigg]. \end{aligned} \tag{73}$$

8) *The square of effective current flowing through diode D_2 is*

$$I_{\mathrm{D2\_rms}}{}^2 = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} I_{\mathrm{sm2}}{}^2 d\omega t. \tag{74}$$

Substituting (59) into (74) yields

$$\begin{aligned} I_{\mathrm{D2\_rms}}{}^2 = \frac{1}{2\pi}\Bigg[&\frac{\pi \hat{I}_a^2}{32} - \frac{\hat{I}_a I_{\mathrm{dc\_in}}}{4} + \frac{\pi I_{\mathrm{dc\_in}}{}^2}{16} - \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2}{8} \\ &- \frac{\hat{I}_a^2 M\cos(\delta)}{6} - \frac{I_{\mathrm{dc\_in}}{}^2 M\cos(\delta)}{4} + \frac{\pi \hat{I}_a^2 M^2}{64} \\ &+ \frac{\pi I_{\mathrm{dc\_in}}{}^2 M^2}{32} - \frac{\hat{I}_a I_{\mathrm{dc\_in}} M^2\cos(2\delta)}{24} \\ &+ \frac{\pi \hat{I}_a^2 M^2\cos(2\delta)}{128} + \frac{\pi \hat{I}_a I_{\mathrm{dc\_in}} M\cos(\delta)}{8}\Bigg]. \end{aligned} \tag{75}$$

The conduction losses are calculated over one fundamental ac period using the above-derived average/effective currents, using

$$P_{\mathrm{D\_con}} = I_{\mathrm{D\_avg}}\, V_{D\_0} + r_{D\_0} I_{\mathrm{D\_rms}}^2 \tag{76}$$

$$P_{\mathrm{T\_con}} = I_{\mathrm{T\_avg}}\, V_{T\_0} + r_{T\_0} I_{\mathrm{T\_rms}}^2 \tag{77}$$

where $P_{\mathrm{D\_con}}$ and $P_{\mathrm{T\_con}}$ are the SM's diode and switch conduction losses, respectively, within one fundamental ac period, V_{D_0} and V_{T_0} are the threshold voltages of the diode and the switch, respectively, and r_{D_0} and r_{T_0} are the forward conduction resistance of the diode and the switch, respectively. It is worth noting that the blocking state losses are much small compared with the conduction losses, hence are ignored in this analysis.

According to [31], the turn-ON/OFF switching losses are approximately proportional with the average current flowing through the switch; therefore, the switching losses over one fundamental ac period can be calculated by

$$P_{\mathrm{sw}} = f\left(E_{\mathrm{on}} + E_{\mathrm{off}}\right)\frac{V_c I_{\mathrm{T\_avg}}}{V_{\mathrm{T\_ref}} I_{\mathrm{T\_avg}}} \tag{78}$$

$$P_{\mathrm{rec}} = f E_{\mathrm{rec}}\frac{V_c I_{\mathrm{D\_avg}}}{V_{\mathrm{D\_ref}} I_{\mathrm{D\_avg}}} \tag{79}$$

where f is the switching frequency; E_{on} and E_{off} are the switch's turn-ON and turn-OFF energy losses, respectively, $V_{\mathrm{T\_ref}}$ and $I_{\mathrm{T\_ref}}$ are the switch's reference voltage and current, respectively, E_{rec} is the reverse recovery energy losses of diode, and $V_{\mathrm{D\_ref}}$ and $I_{\mathrm{D\_ref}}$ are the diode's reference voltage and current, respectively. The values of E_{on}, E_{off}, $V_{\mathrm{T\_ref}}$, $I_{\mathrm{T\_avg}}$, E_{rec}, $V_{\mathrm{D\_ref}}$, and $I_{\mathrm{D\_ref}}$ can be obtained from the datasheet of the particular device. Similarly, the losses of diode bridge rectifier modules at the secondary side can also be calculated using (76) and (79).

B. Losses Evaluation of the Medium Frequency Transformer

In general, there are two types of losses in a transformer, copper losses and core losses. Copper losses are essentially caused by the conductor resistivity; and with the skin and proximity effects, these losses are increased with the frequency. However, using Litz wires greatly reduces these effects and therefore for this approximate analysis, the skin and proximity effects will not be considered. Hence, the copper losses, P_{copper}, is defined as

$$P_{\mathrm{copper}} = R I_{\mathrm{rms}}^2 \tag{80}$$

where *R* is the equivalent resistance of the transformer windings and I_{rms} is the effective current flowing through these windings.

The core losses are proportionally influenced by the maximum flux density, which is an important factor in designing a transformer. However, for a given magnetic flux, the flux density is solely determined by the core cross-sectional area. In general, the Steinmetz equation [32] is used to predict the core losses, which can be expressed as follows:

$$P_{\mathrm{core}} = k V_{\mathrm{core}} f^{\alpha} B_{pk}^{\beta} \tag{81}$$

where P_{core} and V_{core} are the core losses and core volume, respectively; B_{pk} is the peak core flux density and the coefficients K, α, and β are given by the properties of the core material. f is the ac frequency of the system.

C. Comparison Between the Proposed Converter and Unidirectional Cascaded ISOS and IPOS Converters

The proposed converter aims to reduce the complexity and the losses of the dc collecting point converters of the off-shore wind farms. Therefore, it is very important to evaluate its performance against other available unidirectional dc–dc converter

TABLE II
SYSTEM PARAMETERS OF THE DC–DC CONVERTERS

Items	Proposed Converter	Conventional Unidirectional ISOS Converters	Conventional Unidirectional IPOS Converters
Rated power	10 MW		
Input DC voltage	15 kV		
Output DC voltage	140 kV		
Total number of IGBT modules at the primary side	112 (28*4)	56 (14*4)	784 (14*4*14)
Primary rated IGBT module voltage	1.07 kV		
Total number of Diode modules at the secondary side	112 (14*8)		
Primary rated submodule voltage	1.07 kV		
Secondary rated diode voltage	5 kV		
Modulation method	Sinusoidal pulse width modulation (SPWM)		
carrier-reference frequency ratio (R_c)	$R_c = f_M/f_c$ =5		
AC frequency (f_C)	400 Hz		
Switching frequency (f_M)	2k Hz		

topologies. As the natural requirement of such a converter is to boost the voltage at the output side, hence, the proposed converter is compared with the unidirectional multimodel, SAB dc–dc converters with ISOS and IPOS configurations, reported in [5], [7], and [8].

Table II presents the parameters of the proposed converter and the two SAB converter systems. For a sensible comparison, both converters are rated at the same power as the proposed converter. Moreover, the three topologies utilize the same diode-bridge rectifier modules (i.e., unidirectional), connected in series at the secondary side. In this paper, 14 diode-bridge rectifier modules are cascaded in series to produce an output dc voltage of 140 kV. It should be noted that each valve of the diode-bridge rectifier module consists of two diodes in series [33], with a voltage blocking capability of 5 kV, each. Furthermore, the unidirectional ISOS and IPOS dc–dc converters are designed with the same requirement as of the proposed converter (i.e., blocking voltage capability of each SAB-based SM at primary side is 1.07 kV). This necessitates a total of 56 IGBT modules for ISOS converter and 784 IGBT modules for IPOS converter at primary side as opposed to 112 IGBT modules for the proposed converter. However, it should be noted that for the conventional ISOS and IPOS converters, the number of converter modules on the primary and the secondary sides is dependent on each other. If higher voltage is required at the output side, then the same number of converter modules must be added at both side with their associated transformers, hence losses and complexity. However, with the proposed converter, these are independent of each other, where more rectifier modules can be added at the secondary side without increasing the number of IGBT modules at the primary side.

For a fair comparison, all three topologies are modulated utilizing sinusoidal PWM (SPWM) with the same carrier-reference frequency ratio, denoted by R_c (i.e., $R_c = f_C/f_M$, where f_C and f_M are frequency of the triangular carrier and reference waveform, respectively, and 400 Hz is selected as the ac fundamental frequency of all these three dc–dc converters.

TABLE III
PARAMETERS OF IGBT/DIODE

IGBT/Diode Code	Rated Voltage	Rated Current
FZ1200R12HE4	1.2 kV	1.2 kA
FZ1600R12HP4	1.2 kV	1.6 kA
FZ400R12KE4	1.2 kV	0.4 kA
D1131SH	6.5 kV	1.1 kA

The losses of topologies are also evaluated based on the analysis presented in Section IV to estimate the efficiency of the topologies across the whole range of the output power. For this purpose, the suitable IGBTs and diodes for topologies must be selected. As above mentioned, for a sensible comparison, all three unidirectional converters are rated at the same power and input–output dc voltage as shown in Table II. However, due to the different configurations at the primary side of the topologies, the current stress of every single IGBT module is different. Therefore, according to different current stresses, FZ1200R12HE4 IGBT modules [34] were considered for the primary IGBT modules of the proposed converter; FZ1600R12HP4 and FZ400R12KE4 IGBT modules [34] were considered for the primary IGBT modules of unidirectional cascaded ISOS and IPOS converters, respectively. Meanwhile, due to the similar configuration at the secondary side of all three topologies, D1131SH diodes [35] are selected for all of them. Table III shows the parameters of selected IGBTs/diode.

The losses of the medium frequency transformer are calculated based on the parameters tabulated in Table IV, which are reported in [36]. The power losses and efficiency of the different topologies are illustrated in Figs. 9 and 10, respectively. As expected, the proposed converter shows a better performance in many aspects compared with unidirectional ISOS and IPOS, especially, in terms of losses and components utilization. From Fig. 9(a), it can be observed that the total losses of the proposed converter are much smaller than the ISOS converter but slightly bigger than the IPOS converter. However, the number of employed IGBT module of the IPOS converter is much bigger than the proposed converter and ISOS converter as shown in Fig. 9(b), which would complicate the control system, hence decrease the reliability.

V. OVERALL CONTROL OF THE PROPOSED CONVERTER

A. Implementation of the Closed-Loop Control

The MMC converter in the proposed configuration operates as a voltage source to produce constant amplitude and frequency ac voltage to control the output voltage and current produced by the cascaded diode bridge rectifiers to facilitate the employment of the HVdc transmission lines. Therefore, this section employed a stationary frame regulator, the PR regulator, which achieves the

TABLE IV
PARAMETERS OF THE MEDIUM FREQUENCY TRANSFORMERS

Items	Transformer for proposed Converter	Transformer for unidirectional ISOS Converters	Transformer for unidirectional IPOS Converters
Required transformer numbers	1	14	14
Rated power	10 MW	0.8 MW	0.8 MW
Rated frequency	400 Hz	400 Hz	400 Hz
Rated primary voltage	10 kV	1.1 kV	10 kV
Rated secondary voltage	140 kV	10 kV	10 kV
Primary equivalent resistance	5.2 mΩ	0.66 mΩ	54.29 mΩ
Secondary equivalent resistance	580 mΩ	54.29 mΩ	54.29 mΩ
Core material	Magnetic alloy 2605SA1 [35]		
Core coefficients for Steinmetz Equation	$k = 1.4$, $\alpha = 1.47$, $\beta = 1.52$		
Saturated flux density	1.56 T		
Core volume	0.21 m^3	0.033 m^3	0.033 m^3

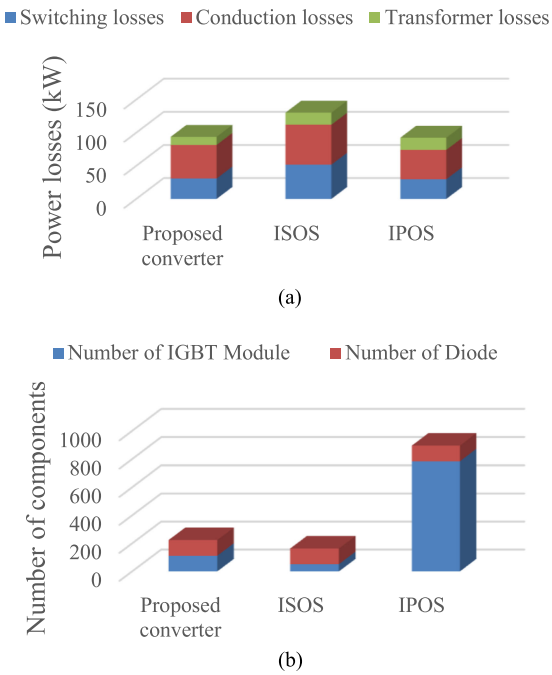


Fig. 9. (a) Distribution of the power losses. (b) Number of employed IGBT/diode of the proposed converter, ISOS and IPOS converters for operation at rated power 10 MW.

same transient and steady-state performance as a synchronous frame PI regulator [37]. The proposed regulator is applicable to the single-phase system. Considering single-phase MMC as an example, the implementation of the employed closed-loop control is illustrated in Fig. 11. It is realized by multiplying the transfer functions of the conventional proportional integral (PI_1 and PI_2) regulators with the sin and cos reference signals. This

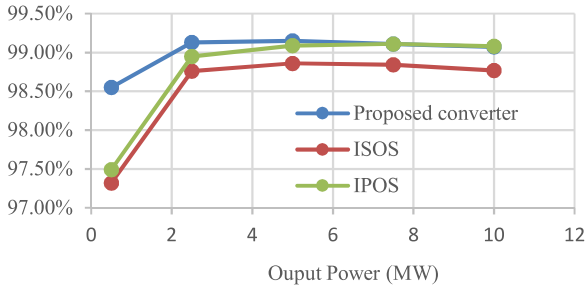


Fig. 10. Efficiency of the proposed converter (blue line), ISOS (red line), and IPOS (green line) converters based on different rated power.

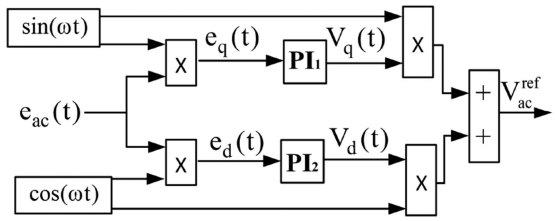


Fig. 11. Block diagram of implementation of the close-loop control.

is applicable for both, steady-state and transient operations as the PI regulator operates under the *d-q* synchronous rotating reference frame [37]. It is worth noting that there is no Park transformation or any other transformations between the stationary and rotating reference frame involved. Equation (82) describes the implementation of the employed control method, which is schematically depicted in Fig. 11

$$V_{\mathrm{ac}}^{\mathrm{ref}}(\mathrm{t}) = \{[e_{\mathrm{ac}}(t)\cdot\sin(\omega t)] * h_{\mathrm{dc}}(t)\}\cdot\sin(\omega t) + \{[e_{\mathrm{ac}}(t)\cdot\cos(\omega t)] * h_{\mathrm{dc}}(t)\}\cdot\cos(\omega t) \quad (82)$$

where $e_{\mathrm{ac}}(t)$ is the input ac error signal, $h_{\mathrm{dc}}(t)$ represents the unit impulse response under time domain of PI regulator, and $'*'$ donates the convolution product. The output of this control loop $V_{\mathrm{ac}}^{\mathrm{ref}}(t)$ is used as a modulating signal to drive the power switches.

Actually, after multiplying with reference signal, sine and cos, the error signal $e_{\mathrm{ac}}(t)$ is converted into a dc and ac components with two times the fundamental frequency. This is then fed into the PI regulators, which perform the integration to get the steady-state error and also work as a low-pass filter to extract out the dc signal to achieve a zero steady-state error in the stationary reference frame. Applying Laplace transform to (82) yields

$$V_{\mathrm{ac}}^{\mathrm{ref}}(s) = \frac{1}{2}\left[H_{\mathrm{dc}}(s+j\omega) + H_{\mathrm{dc}}(s-j\omega)\right]e_{\mathrm{ac}}(s). \quad (83)$$

For the conventional PI controller, the Laplace transform of a unity impulse response can be described by the following equation:

$$H_{\mathrm{dc}}(s) = k_p + \frac{k_i}{s}. \quad (84)$$

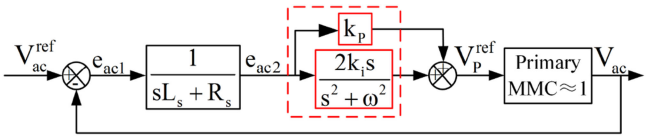


Fig. 12. Simplified close-loop control block diagram for the primary MMC of the proposed dc–dc converter.

By substituting (84) into (83), the transfer function of the control system with derived generalized integrator can be given as

$$V_{\mathrm{ac}}^{\mathrm{ref}}\ (s) = \left(k_p + \frac{k_i \cdot s}{s^2 + \omega^2}\right) e_{\mathrm{ac}}\ (s) \tag{85}$$

where k_p is the proportional constant, which is used to improve the transient response of the control system, k_i is the integral constant, and ω is the resonant frequency of the derived integrator. Therefore, the infinity gain can be achieved when $s = j\omega$.

B. Theoretical Verification of the Derived Generalized Integrator

To simplify the theoretical verification, the proposed converter is approximated as an MMC with a simple *RL* load (L_s and R_s), where the MMC is represented by a unit gain. Fig. 12 shows the resultant simplified control system (i.e., in *S*-domain). Since the proposed converter is controlled via the primary MMC only, therefore, the ac voltage is fed back from the primary side of the transformer and compared with its reference value, $V_{\mathrm{ac}}^{\mathrm{ref}}$. Then, the resultant ac voltage error, e_{ac1}, is divided by the equivalent load (L_s and R_s) in the circuit to get the ac current error e_{ac2}, which is used as an input to the generalized integrator, $H(s)$. The output of the $H(s)$ functions as the reference signal of the primary ac voltage. According to Fig. 12, the transfer function of the MMC voltage controller from $V_{\mathrm{ac}}^{\mathrm{ref}}(s)$ to $V_{\mathrm{ac}}(s)$ can be expressed as

$$\frac{V_{\mathrm{ac}}}{V_{\mathrm{ac}}^{\mathrm{ref}}} = \frac{H\ (s)}{H\ (s) + (sL_s + R_s)} \tag{86}$$

where $V_{\mathrm{ac}}(s)$ and $V_{\mathrm{ac}}^{\mathrm{ref}}(s)$ are the output and the reference voltages of the MMC, respectively, and $H(\mathrm{s})$ is the transfer function of the generalized integrator, which is given by

$$H\ (s) = k_p\ + \frac{2k_i \cdot s}{s^2 + \omega^2} \tag{87}$$

where ω is set to the fundamental frequency.

Substituting $s = j\omega$ into (87) yields

$$H\ (s) = k_p\ + \frac{2k_i \cdot s}{(j\omega)^2 + \omega^2} \rightarrow +\infty. \tag{88}$$

Substituting (88) into (86) yields the characteristics of the proposed controller at the fundamental frequency ω

$$\frac{V_{\mathrm{ac}}\ (j\omega)}{V_{\mathrm{ac}}^{\mathrm{ref}}\ (j\omega)} = 1. \tag{89}$$

In order to get a pure sinusoidal V_{ac} without harmonic distortion, the input voltage reference $V_{\mathrm{ac}}^{\mathrm{ref}}$ is set to the fundamental frequency component only. Furthermore, (89) reveals that the actual output voltage $V_{\mathrm{ac}}(j\omega)$ exactly matches its reference value, $V_{\mathrm{ac}}^{\mathrm{ref}}(j\omega)$. This confirms that the proposed voltage controller can successfully achieve zero steady-state error at the fundamental frequency.

TABLE V
PARAMETERS OF THE SIMULATED SYSTEM

Parameter	Value
Rated power	10 MW
Input DC voltage	15 kV
Output DC voltage	140 kV
Output load resistor	2000 Ω
Number of MMC's SMs per arm	14
Number of diode-bridge rectifier modules	14
Transformer ratio	1:14
SM capacitor of MMC	2.2 mF
Arm Inductor	1 mH
Output capacitor	3 mF
Output inductor	1 mH
Switching frequency	2 kHz
AC fundamental frequency	400 Hz

VI. Simulation and Experimental Results

A. Simulation Results

A simulation model of the proposed converter rated at 10 MW/140 kV is developed with the tabulated parameters in Table V using MATLAB/SIMULINK to validate the feasibility and the effectiveness of the proposed system and its control system performance. In this paper, the MMC at the primary side is constructed using 14 half-bridge SMs per arm and there are 14 series-connected diode-bridge rectifier modules at the secondary side of the transformer. Furthermore, the medium frequency transformer with turn ratios of $W_p : W_{s1} : W_{s2} : \cdots : W_{s14} = 1 : 1 : 1 : \cdots : 1$ is chosen, where W_p and W_{s1} to W_{s14} are the primary winding and the corresponding secondary winding-1 to winding-14, respectively. However, different turns ratio can be also considered for different stepping gains if required.

The steady-state voltage and current of the proposed converter, operating at 400 Hz is depicted in Fig. 13. Since the proposed converter uses MMC at the primary side and diode bridge rectifier modules at the secondary side, the resultant primary terminal voltage, V_{ab}, and secondary voltages are shaped as multilevel and square waveforms (taking V_{s1} and V_{s2} as example), respectively.

To demonstrate the effect of unbalance phenomena between the MMC arms, Figs. 14 and 15 show the voltage, current, and instantaneous power of the upper and lower arms for both, balanced (k = 0) and unbalanced (k = 0.08) cases, respectively. Fig. 15 shows that the upper arm voltage is charged to a higher-level due to the introduced positive unbalanced factor. Meanwhile, the arm current and the instantaneous power flow become unbalanced, which will seriously influence the converter operation.

The performance of the voltage balance control is demonstrated in Fig. 16, where it can be clearly observed that the capacitor voltages are perfectly controlled, and closed to 1/14 of the input dc voltage (i.e., 15 kV/14).

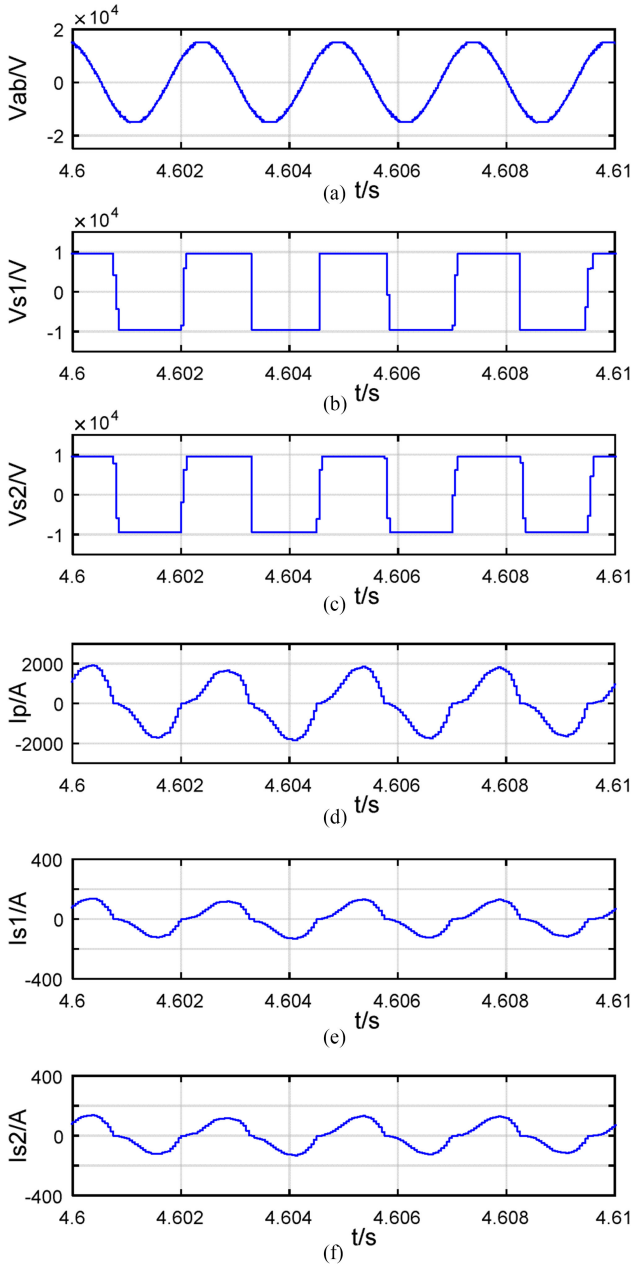


Fig. 13. (a) Transformer primary terminal voltage waveform V_{ab}. (b) Transformer secondary winding-one voltage waveform V_{s1}. (c) Transformer secondary winding-two voltage waveform V_{S2}. (d) Transformer primary current waveform I_P. (e) Transformer secondary winding-one current waveform I_{S1}. (f) Transformer secondary winding-two current waveform I_{S2}.

The output dc voltage of the proposed converter is shown in Fig. 17 and with the given transformer turns ratio in this paper ($W_p : W_{s1} : W_{s2} : \cdots : W_{s14} = 1 : 1 : 1 : \cdots : 1$), the average output dc voltage is maintained around 140 kV.

The performance of the employed control strategy is further investigated and confirmed with a step change in the output load (i.e., 2 to 2.4 kΩ). Fig. 18 shows the dynamic response of the controller when the load changed at $t = 2.5$ s, causing the output current I_{dc2} to decrease from 70 to 60 A; however, the output voltage is perfectly maintained constant, which confirms the effectiveness of the control system.

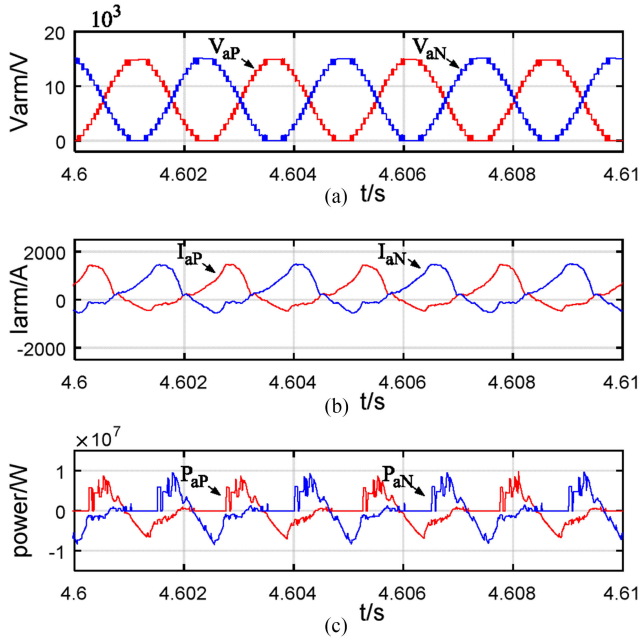


Fig. 14. Primary-side MMC key-waveforms with balanced state k = 0. (a) Upper arm voltage V_{aP} and lower arm voltage V_{aN}. (b) Upper arm current I_{aP} and lower arm current I_{aN}. (c) Upper arm power P_{aP} and lower arm power P_{aN}.

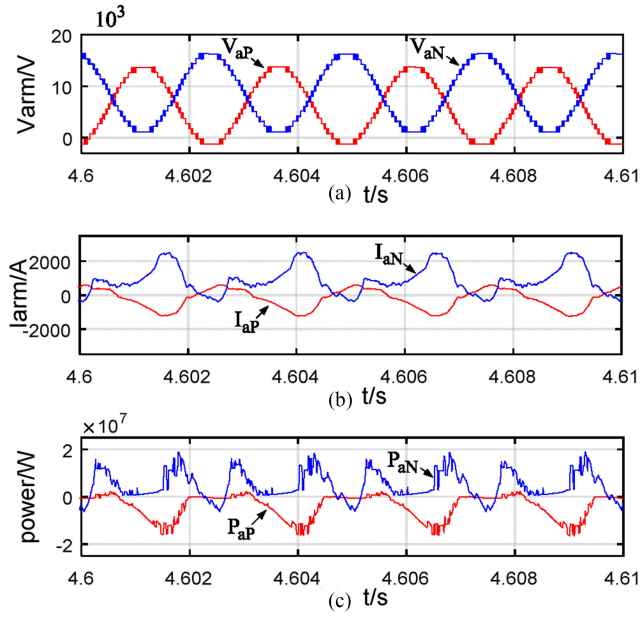


Fig. 15. Primary-side MMC key-waveforms with unbalanced state k = 0.08. (a) Upper arm voltage V_{aP} and lower arm voltage V_{aN}. (b) Upper arm current I_{aP} and lower arm current I_{aN}. (c) Upper arm power P_{aP} and lower arm power P_{aN}.

B. Experimental Validation

Low voltage scaled down laboratory prototype is developed to validate and confirm the simulation and the theoretical studies of the proposed converter and the performance of the control strategies. Table VI summarizes the main parameters of the test-rig. The scaled-down laboratory prototype and its schematic diagram are illustrated in Fig. 19. It is worth noting that the pro-

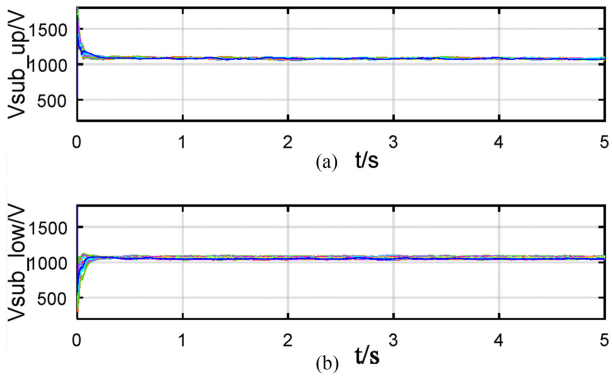


Fig. 16. Upper and lower SM voltages. (a) t/S. (b) t/S.

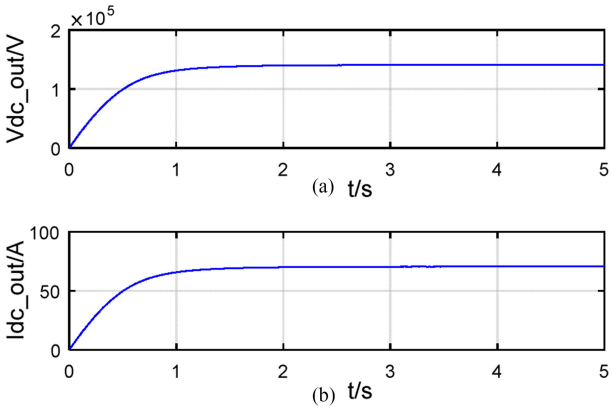


Fig. 17. Output waveforms of the proposed converter under steady-state operation. (a) Output dc voltage. (b) Output dc current.

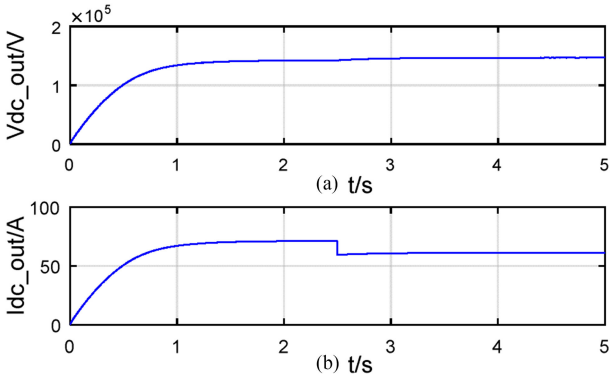
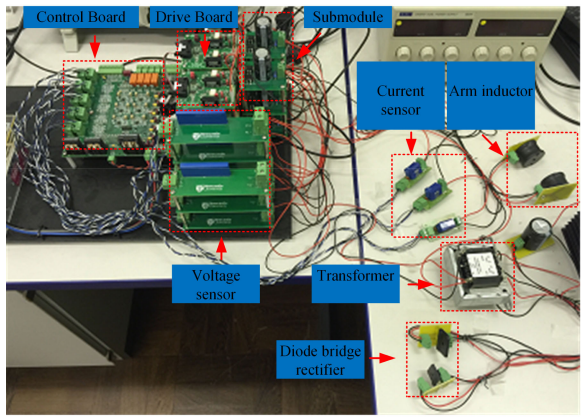


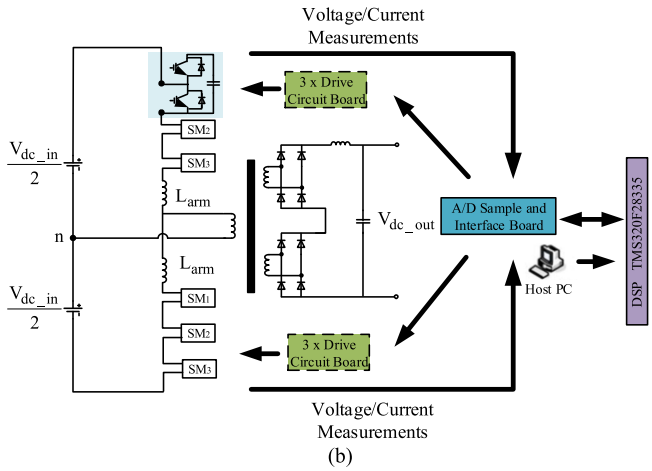
Fig. 18. Output waveforms of the proposed converter under a step change at 2.5 s. (a) Output dc voltage. (b) Output dc current.

TABLE VI
PARAMETERS OF THE EXPERIMENTAL SETUP

Parameter	Value
Rated power	80 W
Input DC voltage	70 V
Output load resistor	20 Ω
Primary side AC peak voltage of transformer	±35 V
Submodule numbers of MMC per arm	3
Submodule numbers of combined converter	2
Transformer ratio	1:1:1
Submodule capacitor of MMC	2.2 mF
Inductance of per arm	1 mH
Output capacitor	3 mF
Output inductor	1 mH
Switching frequency	2000 Hz
AC frequency	400 Hz
Sampling rate (F28335)	20 kHz



(a)



(b)

Fig. 19. (a) Scaled-down laboratory prototype and (b) its schematic diagram.

posed converter is intended for high-voltage high-power applications; therefore, the simulation is presented for close-to-reality systems. However, implementing such a system in the laboratory is not feasible from the safety and the resources point of view; therefore, scaled-down prototype is developed as a proof of concept and to validate the proposed control methods and their effectiveness.

The scaled down prototype is developed with the following considerations.

1) The one-leg MMC is used for the primary side of the test-rig, instead of using single-phase MMC (e.g., two-legs) as shown in the simulation. This will help to reduce the number of SMs (only three SMs) and the control complexity of the test-rig but satisfy the validation of the proposed topology and its control strategy.
2) Likewise, as the proposed converter is modular at both sides, only two diode-bridge rectifier models are considered at the secondary side, which is enough to accom-

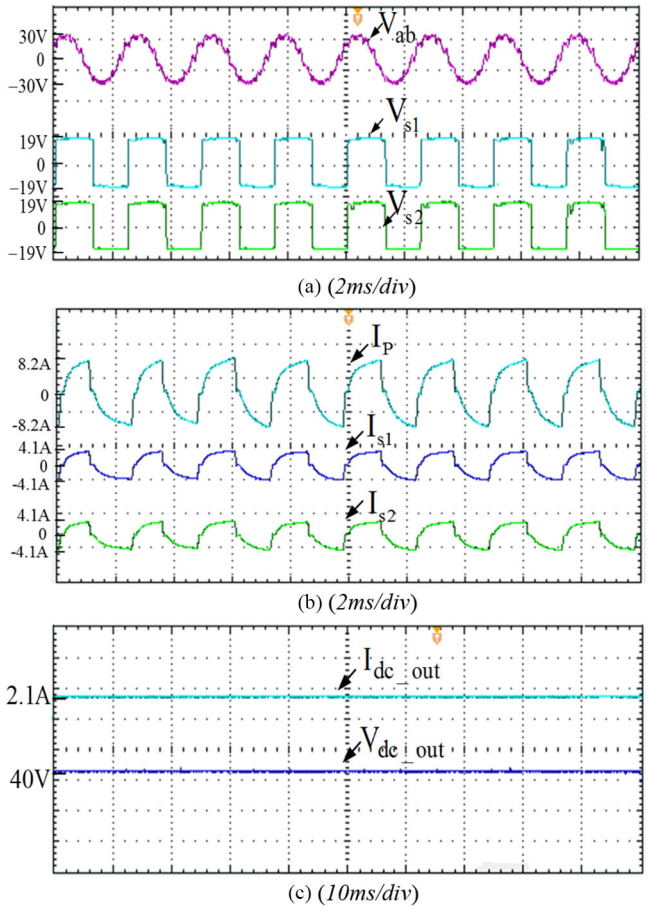


Fig. 20. Under steady state. (a) Transformer primary terminal voltage V_{ab} (40 V/*div*), secondary winding-one voltage V_{s1}, and winding-two voltage V_{s2} (20 V/*div*). (b) Transformer primary current I_P (10 A/*div*), secondary winding-one current I_{s1}, and winding-two current I_{s2} (5 A/*div*). (c) Proposed converter output dc current $I_{\mathrm{dc\_out}}$ (5 A/*div*) and voltage $V_{\mathrm{dc\_out}}$ (40 V/*div*).

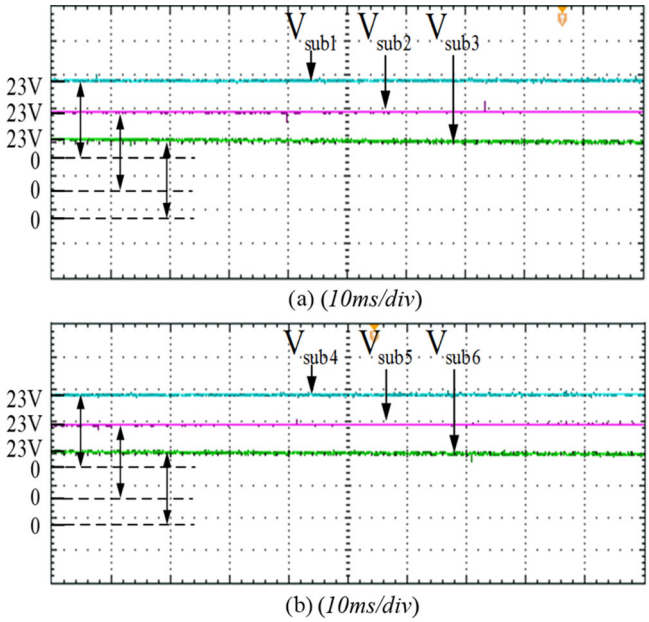


Fig. 21. Under steady state. (a) Upper arm voltages V_{sub1}, V_{sub2}, and V_{sub3} (10 V/*div*). (b) Lower arm SM voltages V_{sub4}, V_{sub5}, and V_{sub6} (10 V/*div*).

modate the requirement of the designed prototype. Once again, due to the modularity feature, this can be easily extended as presented in the simulation, if resources are available.

3) As it can be seen from Fig. 19, the test-rig is developed using the six drive circuit boards, seven voltage sensors, three current sensors, A/D sample-interface board, and TMS320F28335DSP control board. However, in real applications, where a large number of SMs is required, different arrangement maybe needed, which include a higher number of control boards, more sophisticated controllers such as DSP, FPGA, and CPLD to meet these requirements. In general, most of large-scale control systems are built by the company, such as ABB and SIEMENS.

Fig. 20 shows the steady-state performance of the proposed converter. The 400-Hz ac voltages at the primary and secondary side windings are shown in Fig. 20(a), and the corresponding currents at primary and the secondary side windings are depicted in Fig. 20(b). It is worth noting that the peak of secondary currents is just half of the primary one (i.e., $\frac{I_{\mathrm{p\_peak}}}{2} = I_{\mathrm{s1\_peak}} = I_{\mathrm{s2\_peak}} = 4.1$ A), which effectively reduces the current rating of the associated diode bridge rectifier SMs. This can be further reduced if more windings on the secondary side are considered. The root mean square (rms) value of the primary terminal voltage is stepped up by a transformer with turn ratios of $W_p : W_{s1} : W_{s2} = 1 : 1 : 1$ from $V_{\mathrm{ab\_RMS}} = \frac{30\,\mathrm{V}}{\sqrt{2}} = 21\,\mathrm{V}$ to $V_{\mathrm{s\_RMS}} = V_{\mathrm{s1\_RMS}} + V_{\mathrm{s2\_RMS}} = 19\,\mathrm{V} + 19\,\mathrm{V} = 38\,\mathrm{V}$ (noting that the rms value of the square waveform is equal to the peak value). Furthermore, the current and voltage stresses of the diode bridge rectifier modules will be further reduced if higher number of modules is considered. Fig. 20(c) shows the experimental output dc voltage and current waveforms of the proposed converter, which are perfectly smooth and regulated at the required value, confirming the effectiveness of the proposed control system.

Fig. 21 shows the performance of the SM voltage balance control, where it can be seen that the capacitor voltages are well balanced and closed to one-third of the dc input voltage (i.e., 23 V). Meanwhile, the voltage ripple of each SM is relatively small.

The dynamic performance of the system is experimentally validated as well; a step change to the load is applied causing the output power to decrease from 84 to 44 W. This can be clearly seen from Fig. 22, where the primary peak current changes from $I_{\mathrm{p\_peak}} = \pm 8.2$ A (peak value of primary current) to $I_{\mathrm{p\_peak}} = \pm 4.5$ A (peak value of primary current after a step change) as a response to the variations of the output side load. At the same time, primary peak terminal voltage, $V_{\mathrm{ab\_peak}}$, remains controlled at ± 30 V, which effectively demonstrates the excellent performance of the primary voltage control strategy. Consequently, the output dc current quickly decreased from 2.1 to 1.1 A and dc voltage remains at 40 V, as illustrated

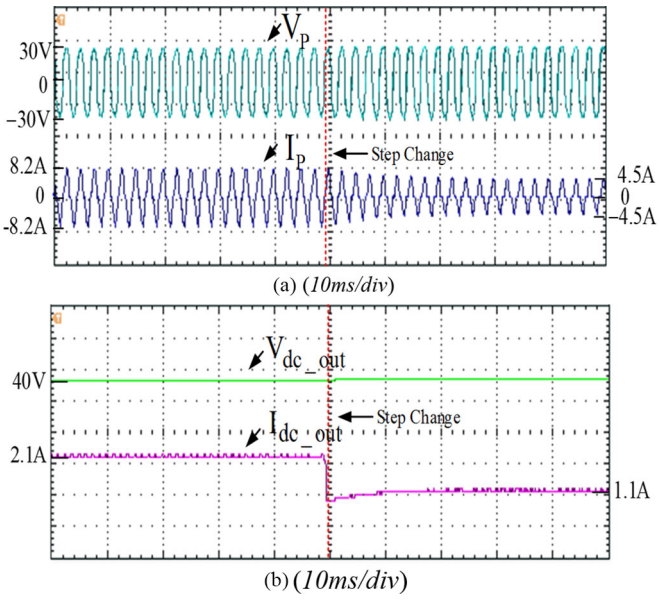


Fig. 22. Dynamic response. (a) Transformer primary terminal voltage V_{ab} (30 V*/div*) and current I_P (10 A*/div*). (b) Proposed converter output dc voltage $V_{\mathrm{dc\_out}}$ (40 V*/div*) and current $I_{\mathrm{dc\_out}}$ (1 A*/div*).

in Fig. 22(b). This further verifies the effectiveness of the proposed system and its control strategy.

VII. Conclusion

A modular unidirectional dc–dc converter based offshore dc collecting point is presented in this paper. The proposed converter utilized the state-of-the-art MMC at the primary side of a medium frequency transformer and cascaded diode-bridge rectifier modules at the secondary side. The converter design features modularity, expandability, galvanic isolation, less losses, lower device voltage and current ratings, and higher efficiency. Detailed theoretical design analysis is presented and parameters that effect the operation of the converter are defined and thoroughly discussed. This includes the energy management between the MMC arms and SMs, power balancing, the power transfer capability of the converter, converter and transformer losses calculation, and comparative study with a competitive circuit topology. As expected, the proposed converter shows superior performance in terms of efficiency, losses, and devices utilization, when compared with the most competitive unidirectional cascaded ISOS and IPOS converters, which makes it more attractive for this particular application. An advanced stationary frame regulator, the PR regulator, which achieves the same transient and steady-state performance as a synchronous frame PI regulator along with other subcontrol loops including SM voltage balance control and circulation current suppression is employed for the proposed converter. The employed control strategy abolishes all complexity associated with the multiple transformations required for the conventional *d-q* synchronous reference frame methods. The employed generalized controller directly acts on the ac single of the primary side, avoiding complex transformation and providing robustness against system variations. The performance of the proposed converter and its control strategy is validated through various simulation and experimentally verified results.

Appendix

1) The parameter of the SM capacitor is determined by [38], [39]

$$C = \Delta E_{\mathrm{arm}} / N \Delta V V_{\mathrm{avg}} \tag{90}$$

where C is the capacitance of the SM capacitor; ΔE_{arm} is the energy variations in the arms; N is SM number per arm; ΔV is voltage ripple of SM capacitor; and V_{avg} is average voltage of SM capacitor.

2) The parameter of the arm inductor is determined by [40], [41]

A. Taking Reducing Fault Current as Criterion:

$$L_{\mathrm{arm}} = \frac{N V_{\mathrm{capacitor}}}{2K} \tag{91}$$

where $K = \frac{dI_{aP}}{dt} = \frac{dI_N}{dt}$; $V_{\mathrm{capacitor}}$ is the SM capacitor voltage; N is the SM number per arm.

B. Taking Suppressing Circulating Current as Criterion:

$$L_{\mathrm{arm}} = \frac{1}{8\omega^2 \cdot C \cdot V_{\mathrm{capacitor}}} \left(\frac{P_s}{3 I_{2\omega}} + V_{\mathrm{dc\_in}} \right) \tag{92}$$

where $I_{2\omega}$ is the allowed value of second-order arm current component; ω is the fundamental angular frequency; C is the SM capacitance; $V_{\mathrm{capacitor}}$ is the SM capacitor voltage;P_s is the apparent power of the converter; and $V_{\mathrm{dc\_in}}$ is the input dc voltage.

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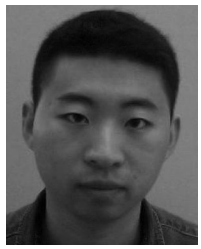

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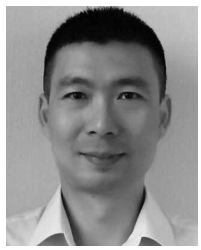

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