Design and Analysis of a Developed Multiport High Step-Up DC–DC Converter With Reduced Device Count and Normalized Peak Inverse Voltage on the Switches/Diodes

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***Abstract*—In this paper, a developed structure is proposed for high step-up nonisolated noncoupled inductor based multiport dc–dc converters. The voltage gain per number of devices of the proposed topology is higher than that of similar topologies. This means that, by using the same number of devices, the proposed topology can generate higher gains than other structures. In other words, the proposed topology utilizes less number of devices for producing the same voltage gain, which leads to less total cost, size, weight, and complexity. Despite high voltage gain, the normalized peak inverse voltage (NPIV) on switches/diodes is low. Higher number of input ports leads to higher gains and lower NPIVs on devices. The load energy can be absorbed and stored in first input unit. Modularity, simple structure, continuous input currents, and low input current ripple are the other profits of proposed topology. Low/medium power applications are suggested for the proposed structure. Proposed topology has been explained and operational modes along with steady-state analysis have been discussed. For better verification, the proposed topology has been compared with several multiport high gain converters. Comparison results confirm the advantages of the proposed topology. Finally, the proper performance of the proposed topology has been validated by experimental results.**

***Index Terms*—DC–DC converter, multiport, nonisolated, number of devices, step-up, voltage gain, normalized peak inverse voltage (NPIV).**

I. Introduction

THE multi-input (MI) dc–dc converters play an important role in hybrid energy systems [1]. These converters are

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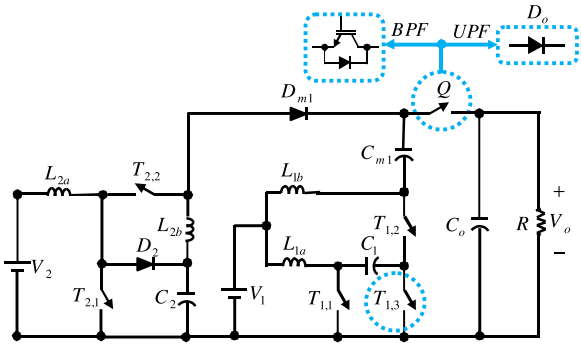

Fig. 1. Proposed basic (dual-input) topology.

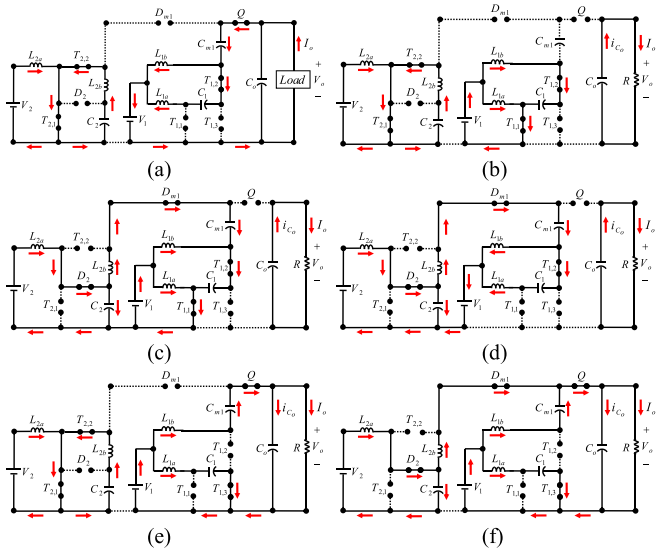

Fig. 2. All possible operational modes of proposed basic topology.

presented in [19] that benefits from continuous input currents. The presented topology is unidirectional and uses high number of capacitors and diodes for achieving higher voltage gains. Another MIHSNINCI-based structure applying conventional boost converters has been presented in [20], in which the input currents are continuous and the energy management capability between the input sources has been provided. In this paper, a modular MPHSNINCI-based topology is proposed in which the input currents are continuous. The energy of higher order input units can be transferred and stored in lower order input units. If the first input source be energy storable one, the bidirectional energy flow capability can be provided for the proposed topology. In such condition, the energy of load can be absorbed and stored in first input source. The voltage gain per number of devices of the proposed topology is higher than that of other similar topologies. Therefore, using the same number of devices, the proposed topology can produce higher gains than other topologies. In other words, the proposed topology utilizes less number of devices for producing the same voltage gain, in comparison with other references. Reduced normalized peak inverse voltage (NPIV) on switches/diodes is another profit of the proposed topology. Aforementioned features make the proposed topology a good candidate for hybrid energy systems and applications.

In the following section, the proposed basic topology is introduced and its operational modes are discussed in Section III. The results of steady-state analysis are presented in Section IV. Extended (MI) form of the proposed topology is introduced in Section V. The proposed topology is compared with some novel structures presented in literature and the results are given in Section VI. Section VII contains the simulation and experimental results. Finally, the paper is concluded in Section VIII.

II. Proposed Basic Topology

The basic (dual-input) form of the proposed topology (see Fig. 1) is composed of four inductors (L_{1a}, L_{1b}, L_{2a}, L_{2b}), four capacitors (C_1, C_2, C_{m1}, C_o), six switches ($T_{1,1}$, $T_{1,2}$, $T_{1,3}$, $T_{2,1}$, $T_{2,2}$, Q), and two diodes (D_{m1}, D_2). The first input source (V_1) can be either storable or nonstorable one. If the V_1 be an energy storable source, it can absorb and store the energy coming from output or second input unit. Otherwise, the $T_{1,3}$ can be replaced by a diode (D_1). In unidirectional power flow applications, the switch Q can be replaced by a diode (D_o). The device count of the proposed basic topology (sum of number of inductors, capacitors, switches, and diodes) is 16. The C_{m1} has been applied to enhance the output voltage and consequently the voltage gain of converter. Also, the interleaved nature of first input unit limits the conduction losses of converter.

III. Operational Modes of the Proposed Basic Topology

The adoption of various switching schemes can lead to six different operational modes in the proposed basic topology (see Fig. 2). As mentioned before, the proposed topology is not bidirectional, but it can transfer the energy of output [like regenerative braking energy in hybrid electric vehicles (HEVs)] to first input unit and V_1 through $T_{1,1}$ and Q (see Fig. 2(a)). As illustrated in Fig. 2(b), the inductors (L_{ia}, L_{ib}) can be charged by the input sources (V_i) and/or capacitors (C_i), through $T_{i,1}$ and $T_{i,2}$ switches. As shown in Fig. 2(c), the energy of second input unit can be delivered to first input unit, through D_{m1}. According to Fig. 2(d), if the V_1 is energy storable one and its state of charge (SoC) is low, the energy of second input unit can charge the V_1 and increase its SoC. Based on Fig. 2(e), the energy of first input unit can be delivered to the load. Also, the energy of both input units can simultaneously flow to the load, as depicted in Fig. 2(f).

According to applied switching scheme [shown in Fig. 3(a)], the switching pattern of $T_{i,1}$ and $T_{i,2}$ ($i = 1, 2$) are the same. Also, Q and $T_{1,3}$ switches have the same switching pattern, which is in complementary manner with $T_{1,1}$ and $T_{1,2}$ switches. So, each input unit of the proposed topology has only two operating modes, first, ($T_{i,1}$, $T_{i,2}$): ON and, second, ($T_{i,1}$, $T_{i,2}$): OFF [see Fig. 3(a)]. The duty cycle of switches are $D_{T_{i,1}} = D_{T_{i,2}} = d_i$ ($i = 1, 2$) and $D_{T_{1,3}} = D_Q = (1 - d_1)$. The same switching pattern and consequently the same duty cycle of ($T_{i,1}$, $T_{i,2}$), and (Q, $T_{1,3}$) switches leads to simplified control of the proposed topology. The applied switching pattern on the proposed basic topology leads to three operational modes, which are as follows:

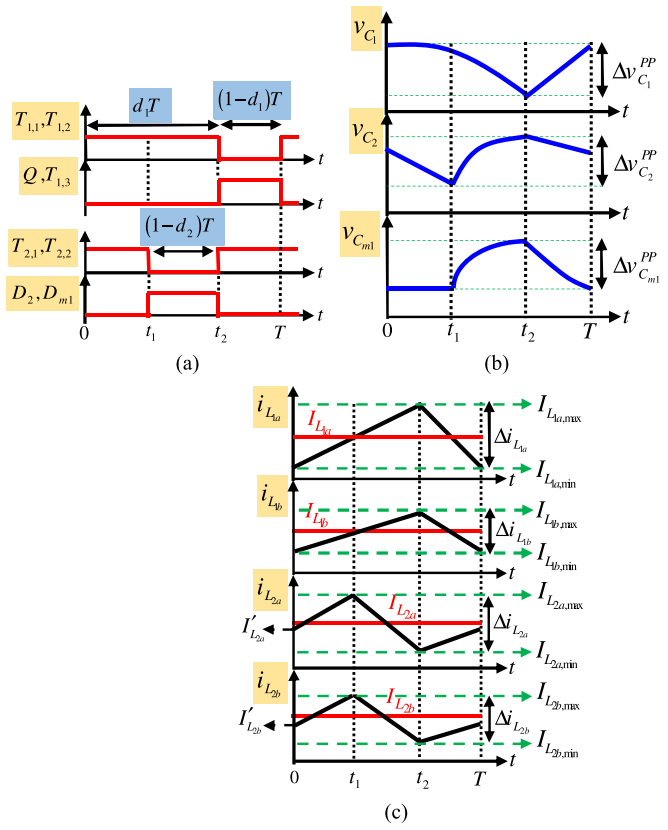

Fig. 3. (a) Applied switching pattern. (b) Voltage waveform of capacitors. (c) Current waveform of inductors.

1) $[0 - t_1]$;
2) $[t_1 - t_2]$;
3) $[t_2 - T]$, where $t_1 = (d_1 + d_2 - 1)\,T$ and $t_2 = d_1 T$.

Since $t_1 > 0$, so $d_1 + d_2 > 1$ should be satisfied. The resulted key waveforms have been presented in Fig. 3(b) and (c).

Mode I-[$\mathbf{0} - t_1$*] [Fig. 2(b)]:* In this mode, the ($T_{1,1}$, $T_{1,2}$, $T_{2,1}$, $T_{2,2}$) conduct, but the ($T_{1,3}$, Q, D_2, D_{m1}) stay nonconducting. So, L_{1a} is charged by V_1 and L_{1b} is charged by (V_1, C_1). Also, L_{2a} and L_{2b} are charged, respectively, from V_2 and C_2. Due to the constant positive voltage on inductors, the current waveforms of (L_{2a}, L_{2b}) increase linearly [see Fig. 3(b)]. In this mode, the output capacitor (C_o) discharges and provides the load power. Thus, its voltage waveform decreases [see Fig. 3(c) and (1)]

$$\begin{aligned} v_{L_{1a}} &= V_1,\ v_{L_{1b}} = V_1 + v_{C_1},\ v_{L_{2a}} = V_2,\ v_{L_{2b}} = v_{C_2} \\ i_{L_{1a}} &= \frac{V_1}{L_{1a}}t + I_{L_{1a,\min}},\ i_{L_{1b}} = \frac{V_1 + v_{C_1}}{L_{1b}}t + I_{L_{1b,\min}} \\ i_{L_{2a}} &= \frac{V_2}{L_{2a}}t + I'_{L_{2a}},\ i_{L_{2b}} = \frac{v_{C_2}}{L_{2b}}t + I'_{L_{2b}}. \end{aligned} \tag{1}$$

Mode II-[$\mathbf{t_1 - t_2}$*] [Fig. 2(c)]:* In this mode, ($T_{2,1}$, $T_{2,2}$) are turned OFF and (D_2, D_{m1}) start to conduct. Consequently, C_2 is charged by (V_2, L_{2a}) and its voltage waveform increases. Also, (V_2, L_{2a}, L_{2b}) charge C_{m1} and increase its voltage. Similar to first mode, L_{1a} is charged by V_1 and L_{1b} is charged by (V_1, C_1). Due to negative constant voltages on L_{2a} and L_{2b}, their current waveforms decrease linearly from peak to minimum value [see Fig. 3(b) and (c)]. Similar to the previous mode, C_o is discharged to provide the load power. The equations of this mode have been presented in (2)

$$\begin{aligned} v_{L_{1a}} &= V_1,\ v_{L_{1b}} = V_1 + v_{C_1},\ v_{L_{2a}} = V_2 - v_{C_2},\ v_{L_{2b}} \\ &= v_{C_1} + v_{C_2} - v_{C_{m1}} \\ i_{L_{1a}} &= \frac{V_1}{L_{1a}}t + i_{L_{1a}}(t_1),\ i_{L_{1b}} = \frac{V_1 + v_{C_1}}{L_{1b}}t + i_{L_{1b}}(t_1) \\ i_{L_{2a}} &= \frac{V_2 - v_{C_2}}{L_{2a}}t + I_{L_{2a,\max}},\ i_{L_{2b}} \\ &= \frac{v_{C_1} + v_{C_2} - v_{C_{m1}}}{L_{2b}}t + I_{L_{2b,\max}}. \end{aligned} \tag{2}$$

Mode III-[$\mathbf{t_2 - T}$*] [Fig. 2(e)]:* In this mode, the ($T_{1,1}$, $T_{1,2}$, D_2, D_{m1}) are turned OFF and the ($T_{2,1}$, $T_{2,2}$, $T_{1,3}$, Q) start to conduct. The energy transfer process in second input unit is exactly the same as first mode. But in first input unit, the energy of (V_1, L_{1b}, C_{m1}) is delivered to the load and output capacitor (C_o) through Q. Also, C_1 is charged by (V_1, L_{1a}) through $T_{1,3}$. During this mode, the voltage on the L_{1a} and L_{1b} are negative, so their current waveforms decrease linearly from peak to minimum value. On the other hand, the positive voltage on L_{2a} and L_{2b} lead to linear increase in their current waveforms [see Fig. 3(b) and (c)]

$$\begin{aligned} v_{L_{1a}} &= V_1 - v_{C_1},\ v_{L_{1b}} = V_1 + v_{C_{m1}} - V_o,\ v_{L_{2a}} \\ &= V_2, v_{L_{2b}} = v_{C_2} \\ i_{L_{1a}} &= \frac{V_1 - v_{C_1}}{L_{1a}}t + I_{L_{1a,\max}},\ i_{L_{1b}} \\ &= \frac{V_1 + v_{C_{m1}} - V_o}{L_{1b}}t + I_{L_{1b,\max}} \\ i_{L_{2a}} &= \frac{V_2}{L_{2a}}t + I_{L_{2a,\min}},\ i_{L_{2b}} = \frac{v_{C_2}}{L_{2b}}t + I_{L_{2b,\min}}. \end{aligned} \tag{3}$$

IV. Steady-State Analysis of the Proposed Basic Topology

It is of interest to keep the operation of the proposed topology in continuous conduction mode (CCM). So, the steady-state analysis are presented only for CCM operation.

A. Relationship Between Output and Input Voltages

The relationship between output and input voltages can be achieved by applying the volt-second principle on the inductors. This principle says that the average voltage on the inductor during steady-state condition is zero. So,

$$\begin{cases} \langle v_{L_{1a}} \rangle = 0 \ \Rightarrow\ v_{C_1} = [1/(1-d_1)]V_1 \\ \langle v_{L_{1b}} \rangle = 0 \ \Rightarrow\ V_o = [1/(1-d_1)]V_1 \\ \qquad\qquad + [d_1/(1-d_1)]v_{C_1} + v_{C_{m1}} \\ \langle v_{L_{2a}} \rangle = 0 \ \Rightarrow\ v_{C_2} = [1/(1-d_2)]V_2 \\ \langle v_{L_{2b}} \rangle = 0 \ \Rightarrow\ v_{C_{m1}} = v_{C_1} + [1/(1-d_2)]v_{C_2}. \end{cases} \tag{4}$$

TABLE I
NPIV ON SWITCHES/DIODES OF PROPOSED BASIC TOPOLOGY

$NPIV_{T_{1,1}} = NPIV_{T_{1,3}} = \frac{v_{C_1}}{V_o} = \left[\frac{1}{1-d_1}\right]\frac{V_1}{V_o}$	$NPIV_{T_{1,2}} = \frac{V_o - v_{C_{m1}}}{V_o} = \left[\frac{1}{(1-d_1)^2}\right]\frac{V_1}{V_o}$
$NPIV_{T_{2,1}} = NPIV_{D_2} = \frac{v_{C_2}}{V_o} = \left[\frac{1}{1-d_2}\right]\frac{V_2}{V_o}$	$NPIV_{T_{2,2}} = \frac{v_{C_{m1}} - v_{C_1} - v_{C_2}}{V_o} = \left[\frac{d_2}{(1-d_2)^2}\right]\frac{V_2}{V_o}$
$NPIV_{D_{m1}} = \frac{V_o}{V_o} = 1$	$NPIV_Q = \frac{V_o + v_{C_1} - v_{C_{m1}}}{V_o} = \left[\frac{2-d_1}{(1-d_1)^2}\right]\frac{V_1}{V_o}$
$ANPIV = \frac{\sum NPIV_{switch/diode}}{N_{switch} + N_{diode}} = \frac{1}{8}\left(\left[\frac{7-4d_1}{(1-d_1)^2}\right]\frac{V_1}{V_o} + \left[\frac{3-d_2}{(1-d_2)^2}\right]\frac{V_2}{V_o}\right)$	

The output voltage (V_o) can be accomplished by simplifying (4), as (5). The $G_{V1,\mathrm{CCM}}$ and $G_{V2,\mathrm{CCM}}$ denoted the voltage gain of first and second input units, during CCM. For identical sources and duty cycles ($V_1 = V_2 = V$, $d_1 = d_2 = d$), the (5) can be rewritten as (6)

$$V_o = \left[\frac{2-d_1}{(1-d_1)^2}\right] V_1 + \left[\frac{1}{(1-d_2)^2}\right] V_2 = (G_{V_1,\mathrm{CCM}})\, V_1 + (G_{V_2,\mathrm{CCM}})\, V_2 \quad (5)$$

$$V_o = \left[(3-d)/(1-d)^2\right] V = (G_{V,\mathrm{CCM}})\, V. \quad (6)$$

B. Normalized Peak Inverse Voltage on Switches/Diodes

The PIV is an important factor that affects the size, cost, and loss of switches/diodes. On the other hand, as the voltage gain of converter increases, the PIV on its switches/diodes increases, too. To make a tradeoff between these two conflicting parameters (voltage gain and PIV), another quantity called NPIV is considered, which is defined mathematically as NPIV $=$ [(PIV)/(V_o)]. The NPIV on the switches/diodes and also the average of NPIV (ANPIV) of the proposed basic topology have been presented in Table I.

The NPIV across semiconductors and also the ANPIV of the proposed basic topology have been plotted for different (d_1, d_2) and the results have been shown in Fig. 4. According to Fig. 4, for different values of (d_1, d_2) and $V_1 = 10$, $V_2 = 15$, the NPIV on ($T_{1,1}$, $T_{1,3}$), $T_{1,2}$, ($T_{2,1}$, $T_{2,3}$), D_2, and Q is less than 20%, 80%, 25%, 85%, and 95%, respectively. The NPIV on D_{m1} is always 1. Also, the ANPIV on semiconductors of the proposed basic topology is always less than 38%.

C. Calculation of Current Ripple of Inductors

According to Fig. 3(b) and (1)–(3), the current ripple of inductors can be found as (7). It is observed that the ripple on the inductor current is directly proportional to input voltage and inversely proportional to inductance and switching frequency.

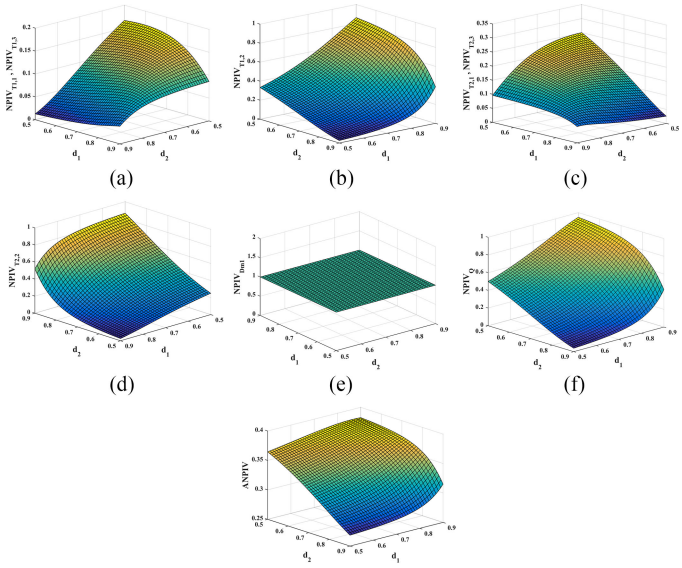

Fig. 4. NPIV on (a) $T_{1,1}$, $T_{1,3}$; (b) $T_{1,2}$; (c) $T_{2,1}$, $T_{2,3}$; (d) D_2; (e) D_{m1}; (f) Q; and (g) ANPIV; versus d_1, d_2 ($V_1 = 10$, $V_2 = 15$).

$$\Delta i_{L_{1a}} = I_{L_{1a,\max}} - I_{L_{1a,\min}} = \frac{d_1 V_1}{L_{1a} f},$$
$$\Delta i_{L_{1b}} = I_{L_{1b,\max}} - I_{L_{1b,\min}} = \frac{(2-d_1)\, d_1 V_1}{(1-d_1)\, L_{1b} f}$$
$$\Delta i_{L_{2a}} = I_{L_{2a,\max}} - I_{L_{2a,\min}} = \frac{d_2 V_2}{L_{2a} f},$$
$$\Delta i_{L_{2b}} = I_{L_{2b,\max}} - I_{L_{2b,\min}} = \frac{d_2 V_2}{(1-d_2)\, L_{2b} f}. \quad (7)$$

D. Calculation of Current Stress Across the Switches/Diodes

The inductor average current can be obtained by applying the ampere-second balance principle on the capacitors. This principle states that the average current of capacitor during steady-state operation is zero. So,

$$\langle i_{C_o} \rangle = 0 \Rightarrow I_{L_{1b}} = [I_o/(1-d_1)],$$
$$\langle i_{C_{m1}} \rangle = 0 \Rightarrow I_{L_{2b}} = [I_o/(1-d_2)]$$
$$\langle i_{C_1} \rangle = 0 \Rightarrow I_{L_{1a}} = \left[I_o/(1-d_1)^2\right],$$
$$\langle i_{C_2} \rangle = 0 \Rightarrow I_{L_{2a}} = \left[I_o/(1-d_2)^2\right]. \quad (8)$$

The peak current value of each inductor can be computed through (9). Using (8) and (9), the current stress of switches/diodes of the proposed basic topology can be

TABLE II
CURRENT STRESS OF SWITCHES/DIODES OF PROPOSED TOPOLOGY

$I_{stress,T_{1,1}} = I_{L_{1a},\max} + I_{L_{1b},\max} + I_{L_{2b},\min}$	$I_{stress,T_{1,3}} = I_{L_{1a},\max}$
$I_{stress,T_{1,2}} = I_{L_{1b},\max} + I_{L_{2b},\min}$	$I_{stress,T_{2,1}} = I_{L_{2a},\max}$
$I_{stress,T_{2,2}} = I_{L_{2b},\max}$	$I_{stress,D_2} = I_{L_{2a},\max}$
$I_{stress,D_{m1}} = I_{L_{2b},\max}$	$I_{stress,Q} = I_{L_{1b},\max}$

computed as Table II

$$\begin{cases} I_{L_{1a},\max} = I_{L_{1a}} + (\Delta i_{L_{1a}}/2) \\ \quad = [I_o/(1-d_1)^2] + [d_1 V_1/2L_{1a}f] I_{L_{1b},\max} \\ \quad = I_{L_{1b}} + (\Delta i_{L_{1b}}/2) \\ \quad = [I_o/(1-d_1)] + [(2-d_1)d_1 V_1/(2(1-d_1)L_{1b}f)] \\ I_{L_{2a},\max} = I_{L_{2a}} + (\Delta i_{L_{2a}}/2) \\ \quad = [I_o/(1-d_2)^2] + [d_2 V_2/2L_{2a}f] \\ I_{L_{2b},\max} = I_{L_{2b}} + (\Delta i_{L_{2b}}/2) \\ \quad = [I_o/(1-d_2)] + [d_2 V_2/2\,(1-d_2)\,L_{2b}f]. \end{cases} \tag{9}$$

Based on (7) and Table II, the current ripple of inductors and current stress of semiconductors can be limited by proper design and selection of inductors and switching frequency.

V. DESIGN GUIDELINES OF INDUCTORS/CAPACITORS

A. Inductor Design

In this study, the operation in CCM mode is the main objective of inductors design. If the average of inductor current be higher than half of its current ripple ($I_L > (\Delta i_L/2)$), CCM operation can be accomplished. So,

$$\begin{cases} I_{L_{1a}} > \frac{\Delta i_{L_{1a}}}{2} \Rightarrow L_{1a} > \frac{(1-d_1)^2 d_1 V_1 R}{2V_o f} \\ \qquad\qquad \Rightarrow \frac{L_{1a} f}{R} > \frac{(1-d_1)^2 d_1 V_1}{2V_o} \\ I_{L_{1b}} > \frac{\Delta i_{L_{1b}}}{2} \Rightarrow L_{1b} > \frac{(2-d_1) d_1 V_1 R}{2V_o f} \\ \qquad\qquad \Rightarrow \frac{L_{1b} f}{R} > \frac{(2-d_1) d_1 V_1}{2V_o} \\ I_{L_{2a}} > \frac{\Delta i_{L_{2a}}}{2} \Rightarrow L_{2a} > \frac{d_2 (1-d_2)^2 V_2 R}{2V_o f} \\ \qquad\qquad \Rightarrow \frac{L_{2a} f}{R} > \frac{d_2 (1-d_2)^2 V_2}{2V_o} \\ I_{L_{2b}} > \frac{\Delta i_{L_{2b}}}{2} \Rightarrow L_{2b} > \frac{d_2 V_2 R}{2V_o f} \Rightarrow \frac{L_{2b} f}{R} > \frac{d_2 V_2}{2V_o}. \end{cases} \tag{10}$$

According to (10), the critical inductance which leads to boundary conduction mode, is directly proportional to resistive load (R) and inversely proportional to switching frequency (f). Fig. 5 presents the DCM/CCM boundary condition of L_{1a}, L_{1b}, L_{2a}, and L_{2b}, for different d_1 and d_2.

B. Capacitor Design

Reaching to limited voltage ripple is the base of design of C_i ($i = 1, 2, m_1, o$) capacitors. Assuming $\Delta v_{C_i}^{\mathrm{PP}}$ and $x_{C_i}^{\%} = (\Delta v_{C_i}^{\mathrm{PP}}/v_{C_i})$, respectively, as peak–peak and percentage of

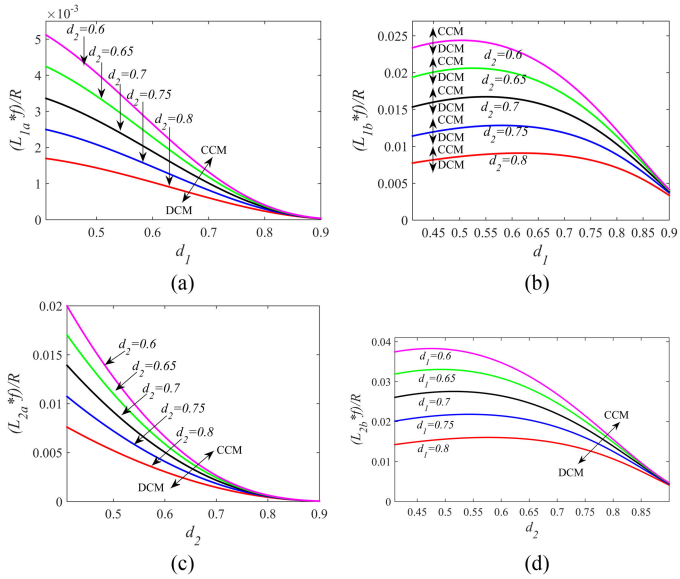

Fig. 5. DCM/CCM boundary condition for (a) L_{1a}, (b) L_{1b}, (c) L_{2a}, (d) L_{2b}, versus d_1, d_2 ($V_1 = 10$, $V_2 = 15$).

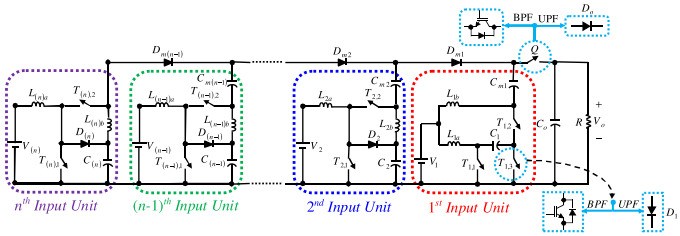

Fig. 6. Proposed extended multi-input topology.

voltage ripple on C_i, the C_i are designed as follows:

$$\begin{aligned} C_1 &\geq \frac{V_o}{Rf\,(1-d_1)\,\Delta v_{C_1}^{PP}} = \frac{V_o}{RfV_1(x_{C_1}^{\%})}, \\ C_2 &\geq \frac{d_2 V_o}{Rf\,(1-d_2)\,\Delta v_{C_2}^{PP}} = \frac{d_2 V_o}{RfV_2(x_{C_2}^{\%})} \\ C_{m1} &\geq \frac{V_o}{Rf\Delta v_{C_{m1}}^{PP}} = \frac{V_o}{Rf(x_{C_{m1}}^{\%} \times v_{C_{m1}})}, \\ C_o &\geq \frac{V_o d_1}{Rf\Delta v_{C_o}^{PP}} = \frac{d_1}{Rf(x_{C_o}^{\%})}. \end{aligned} \tag{11}$$

The load transient requirement should also be considered in C_o design, as (12). The $\Delta I_{o,\mathrm{transient}}$ and $\Delta V_{o,\mathrm{transient}}$, respectively, denotes the load current and voltage variations, during transient response. f_{BW} represents the unity-gain bandwidth of control loop

$$C_o \geq (\Delta I_{o,\mathrm{transient}}/2\pi f_{\mathrm{BW}} \Delta V_{o,\mathrm{transient}}). \tag{12}$$

VI. PROPOSED EXTENDED MULTI-INPUT TOPOLOGY

The extended version of the proposed basic topology has been shown in Fig. 6. According to Table III, the proposed n-input topology utilizes totally $8n$ devices, including switches, diodes, inductors, and capacitors. If an energy storable source

TABLE III
NUMBER OF COMPONENTS OF PROPOSED EXTENDED TOPOLOGY

number of inputs	n	**number of capacitors**	$2n$	
number of sources	n	**number of switches**	***UPF***	***BPF***
			$2n$	$2n$+2
number of inductors	$2n$	**number of diodes**	***UPF***	***BPF***
			$2n$	$2n$-2
Total number of devices (switches+diodes+inductors+capacitors)			$8n$	

TABLE IV
SWITCHING PATTERN AND OPERATIONAL MODES OF PROPOSED n-INPUT (EXTENDED) TOPOLOGY

Mode	Description
1	$T_{i,1}$,$T_{i,2}$ (i=1,2,⋯,n): on – Other switches/diodes: off L_{1a} is charged by V_1. L_{1b} is charged by (V_1,C_1). L_{ia} is charged by V_i. L_{ib} is charged by C_i (i=2,⋯,n). The load is supplied by C_o.
2	$T_{i,1}$,$T_{i,2}$,D_n, $D_{m,(n-1)}$, (i≠n): on – Other switches/diodes: off L_{1a} is charged by V_1. L_{1b} is charged by (V_1,C_1). L_{ia} is charged by V_i. L_{ib} is charged by C_i (i≠1,n).The energy of (V_n,$L_{(n)a}$,$L_{(n)b}$) is delivered to (n-1)th unit through $D_{m,(n-1)}$. C_n is charged by (V_n,$L_{(n)a}$). The load is supplied by C_o.
3	$T_{i,1}$,$T_{i,2}$,D_{n-1}, $D_{m,(n-2)}$, (i≠n-1): on – Other switches/diodes: off L_{1a} is charged by V_1. L_{1b} is charged by (V_1,C_1). L_{ia} is charged by V_i. L_{ib} is charged by C_i (i≠1,n-1).The energy of (V_{n-1},$L_{(n-1)a}$,$L_{(n-1)b}$) is delivered to (n-2)th unit through $D_{m,(n-2)}$. C_{n-1} is charged by (V_{n-1},$L_{(n-1)a}$). The load is supplied by C_o.
⋮	⋮
j	$T_{i,1}$,$T_{i,2}$,D_{n-j+2}, $D_{m,(n-j+1)}$, (i≠n-j+2): on – Other switches/diodes: off L_{1a} is charged by V_1. L_{1b} is charged by (V_1,C_1). L_{ia} is charged by V_i. L_{ib} is charged by C_i (i≠1,n-j+2). The energy of (V_{n-j+2},$L_{(n-j+2)a}$,$L_{(n-j+2)b}$) is delivered to (n-j+1)th unit through $D_{m,(n-j+1)}$. C_{n-j+2} is charged by (V_{n-j+2},$L_{(n-j+2)a}$). The load is supplied by C_o.
⋮	⋮
n	$T_{i,1}$,$T_{i,2}$,D_2, D_{m1} (i≠2): on – Other switches/diodes: off L_{1a} is charged by V_1. L_{1b} is charged by (V_1,C_1). L_{ia} is charged by V_i. L_{ib} is charged by C_i (i≠1,2).The energy of (V_2,L_{2a},L_{2b}) is delivered to 1th unit through D_{m1}. C_2 is charged by (V_2,L_{2a}). The load is supplied by C_o.
***n*+1**	$T_{i,1}$,$T_{i,2}$,$T_{1,3}$, Q (i≠1): on – Other switches/diodes: off L_{ia} is charged by V_i. L_{ib} is charged by C_i (i≠1,2). Energy of (V_1,L_{1a},L_{1b}) is delivered to load through Q. C_1 is charged by (V_1,L_{1a}).

be applied as V_1, it can absorb energy of load or higher order input units. Also, the higher order units can deliver energy to lower order ones.

A. Switching Pattern and Operational Modes

By extending the switching pattern to n-input version, $(n+1)$ operational modes can be achieved, which have been explained in Table IV. In this study, it has been assumed that the V_i sources are nonstorable and the power flow is unidirectional.

B. Relationship Between Output and Input Voltages

By applying volt-second balance principle on inductors, the output voltage relation can be achieved as follows:

$$V_o = \frac{(2-d_1)V_1}{(1-d_1)^2} + \sum_{i=2}^{n} \frac{V_i}{(1-d_i)^2} \xrightarrow[d_1=d_2=\cdots=d_n=d]{V_1=V_2=\cdots=V_n=V}$$

$$V_o = \frac{(n+1-d)V}{(1-d)^2}. \tag{13}$$

C. Calculation of Output Voltage, Voltage Across the Capacitors, and PIV on the Switches/Diodes

The output and capacitor voltages and the PIV on switches/diodes of the proposed topology for 2-, 3-, and 4-input versions have been presented in Table V. Based on Table V, as the number of input units increases, the output voltage (and consequently the gain) of the proposed topology raises too, but the PIV on switches/diodes remain constant. As a result, as the number of inputs increases, not only the voltage gain increases, but also the NPIV on switches/diodes decreases. This feature is considered as one of important merits of proposed MI topology.

The NPIV on switches/diodes of the proposed topology for 2-, 3-, and 4-input versions have been shown in Fig. 7.

Fig. 7 confirms that the NPIV on switches/diodes decreases by increment of number of inputs. For example, the NPIV on $T_{2,2}$ in 2, 3, and 4-input versions of the proposed topology is 12%, 7% and 4%, respectively.

VII. COMPARISON WITH OTHER HIGH STEP-UP MULTI-INPUT TOPOLOGIES

In this section, the proposed topology is compared with novel HSNINCI-based topologies presented in [15]–[20]. The number of devices, voltage boosting capability (voltage gain), and stress on the devices are selected as the comparison factors. General specifications of 2-input and n-input versions of above-mentioned topologies have been presented in Table VI.

The voltage gain of proposed and [15]–[20] topologies (2-input) has been plotted versus different d_1, d_2 (see Fig. 8). Fig. 8 shows that for the same duty cycles, the proposed topology can produce higher voltage gains than other topologies. According to Table VI, the proposed topology has the highest and the topologies in [16] and [18] have the lowest step-up capability among the selected topologies.

Number of devices is an effective parameter on the gain of converter. Table VII and Fig. 9 present the gain of proposed and [16]–[20] topologies in terms of number of devices, where the input sources and duty cycles have been assumed to be identical.

Since [19] presents a double-input topology (not MI one), it has not been considered in Fig. 9. In Fig. 9, the duty cycle has been selected $d = 0.75$, but for any other values, the same results can be obtained, too. Fig. 9(a) shows that for achieving a desirable gain, the proposed topology uses less switches than other references, which can lead to less gate driver circuits and consequently less size, cost, loss, and complexity of converter.

It is seen that the topologies in [16] and [18] use higher number of switches than other topologies. Fig. 9(b) presents the gain versus diode count. Similar to Fig. 9(a), the proposed topology produces higher voltage gain per number of diodes than other topologies. Lower diode count can result in less conduction loss. Fig. 9(c) and (d), respectively, shows the gain versus inductor and capacitor counts.

According to Fig. 9(c) and (d), the proposed topology utilizes less number of inductors and capacitors for generating a desired voltage gain, in comparison with other references. Fig. 9(e) illustrates the gain of proposed and other topologies, in terms of component count. It is observed from Fig. 9(e) that the proposed topology can produce higher gains per number of components

TABLE V
OUTPUT/CAPACITOR VOLTAGES, PIV ON SWITCHES/DIODE OF 2, 3, AND 4-INPUT VERSIONS OF PROPOSED TOPOLOGY

Number of Input units		*n*=2	*n*=3	*n*=4
Voltage across capacitors	v_{C1}	$V_1/(1-d_1)$	$V_1/(1-d_1)$	$V_1/(1-d_1)$
	v_{C2}	$V_2/(1-d_2)$	$V_2/(1-d_2)$	$V_2/(1-d_2)$
	v_{C3}	-	$V_3/(1-d_3)$	$V_3/(1-d_3)$
	v_{C4}	-	-	$V_4/(1-d_4)$
	v_{Cm1}	$[V_1/(1-d_1)]+[V_2/(1-d_2)^2]$	$[V_1/(1-d_1)]+[V_2/(1-d_2)^2]+[V_3/(1-d_3)^2]$	$[V_1/(1-d_1)]+[V_2/(1-d_2)^2]+[V_3/(1-d_3)^2]+[V_4/(1-d_4)^2]$
	v_{Cm2}	-	$[V_3/(1-d_3)^2]$	$[V_3/(1-d_3)^2]+[V_4/(1-d_4)^2]$
	v_{Cm3}	-	-	$[V_4/(1-d_4)^2]$
PIV on switches/diodes	$T_{1,1}=T_{1,3}$ or D_1	$v_{C1}=V_1/(1-d_1)$	$v_{C1}=V_1/(1-d_1)$	$v_{C1}=V_1/(1-d_1)$
	$T_{1,2}$	$V_o-v_{Cm1}=[V_1/(1-d_1)^2]$	$V_o-v_{Cm1}=[V_1/(1-d_1)^2]$	$V_o-v_{Cm1}=[V_1/(1-d_1)^2]$
	$T_{2,1}=D_2$	$v_{C2}=V_2/(1-d_2)$	$v_{C2}=V_2/(1-d_2)$	$v_{C2}=V_2/(1-d_2)$
	$T_{2,2}$	$v_{Cm1}-v_{C1}-v_{C2}=[d_2/(1-d_2)^2]V_2$	$v_{Cm1}-v_{C1}-v_{C2}-v_{Cm2}=[d_2/(1-d_2)^2]V_2$	$v_{Cm1}-v_{C1}-v_{C2}-v_{Cm2}=[d_2/(1-d_2)^2]V_2$
	$T_{3,1}=D_3$	-	$v_{C3}=V_3/(1-d_3)$	$v_{C3}=V_3/(1-d_3)$
	$T_{3,2}$	-	$v_{Cm2}-v_{C3}=[d_3/(1-d_3)^2]V_3$	$v_{Cm2}-v_{C3}-v_{Cm3}=[d_3/(1-d_3)^2]V_3$
	$T_{4,1}=D_4$	-	-	$v_{C4}=V_4/(1-d_4)$
	$T_{4,2}$	-	-	$v_{Cm3}-v_{C4}=[d_4/(1-d_4)^2]V_4$
	D_{m1}	$V_o=[(2-d_1)/(1-d_1)^2]V_1+[1/(1-d_2)^2]V_2$	$V_o-v_{Cm2}=[(2-d_1)/(1-d_1)^2]V_1+[1/(1-d_2)^2]V_2$	$V_o-v_{Cm2}=[(2-d_1)/(1-d_1)^2]V_1+[1/(1-d_2)^2]V_2$
	D_{m2}	-	$v_{Cm1}-v_{C1}=[1/(1-d_2)^2]V_2+[1/(1-d_3)^2]V_3$	$v_{Cm1}-v_{C1}-v_{Cm3}=[1/(1-d_2)^2]V_2+[1/(1-d_3)^2]V_3$
	D_{m3}	-	-	$v_{Cm2}=[1/(1-d_3)^2]V_3+[1/(1-d_4)^2]V_4$
	Q	$V_o-v_{Cm1}+v_{C1}=[(2-d_1)/(1-d_1)^2]V_1$	$V_o-v_{Cm1}+v_{C1}=[(2-d_1)/(1-d_1)^2]V_1$	$V_o-v_{Cm1}+v_{C1}=[(2-d_1)/(1-d_1)^2]V_1$
Output voltage	V_o	$[(2-d_1)/(1-d_1)^2]V_1+[1/(1-d_2)^2]V_2$	$[(2-d_1)/(1-d_1)^2]V_1+[1/(1-d_2)^2]V_2+[1/(1-d_3)^2]V_3$	$[(2-d_1)/(1-d_1)^2]V_1+[1/(1-d_2)^2]V_2+[1/(1-d_3)^2]V_3+[1/(1-d_4)^2]V_4$

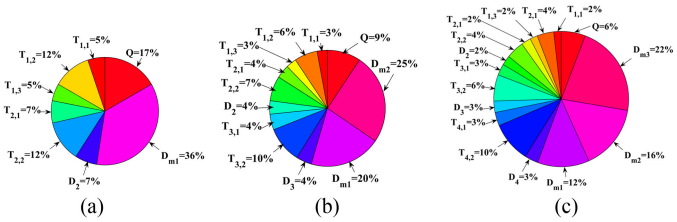

Fig. 7. NPIV on switches/diodes of proposed topology. (a) 2-input. (b) 3-input. (c) 4-input; versions.

than other references. This means that, for reaching a desirable voltage gain, the proposed topology utilizes less components than the other references, which leads to less size, weight, and cost. It can be concluded from Fig. 9(a)–(e) that the proposed topology uses less number of components (switches, diodes, inductors, or capacitors) for generating a desired voltage gain in comparison with other topologies. In other words, using the same number of components, the proposed topology can produce higher voltage gains than other references. Fig. 9 confirms that the voltage gain per number of switches, diodes, inductors, capacitors, and total number of components in the proposed topology is higher than other topologies. In other words, the portion of each component of the proposed topology on producing the voltage gain is higher than other structures. These features can reduce the size, weight, cost, loss, and complexity of the proposed topology. Table VI indicates that the input currents of proposed and [16]–[20] topologies are continuous, but this property has not been provided in [15]. The converters with pulsating input currents are not suitable choices for maximum power point tracking (MPPT)-based applications, like photovoltaic. Also, the bidirectional energy flow capability is an important feature that has been provided only in the proposed topology and the topology in [20]. This property gains more importance, especially in HEVs, where the regenerative braking energy can be absorbed and stored in input sources (battery). The NPIV on switches/diodes and also ANPIV of proposed and [15]–[20] topologies (2-input version and identical input sources and duty cycles) have been investigated and plotted in Table VIII and Fig. 10.

It is observed that for any identical values of duty cycle, the ANPIV of [16]–[20] is constant. The ANPIV for [19] is 31.4%, for [17], [18], and [20] is 50% and for [16] is 62.5% [see Fig. 10(a)]. Also, it seen that the ANPIV on proposed and [15] decrease by increment of duty cycle. Fig. 10(a) shows that the proposed topology has the second least ANPIV on its switching devices (little higher than that of [19]). Fig. 10(b) illustrates the ANPIV against voltage gain of the proposed topology and other references. According to Fig. 10(b), the ANPIV on proposed and [15] topologies decreases, as the gain of converter increases. So, at higher voltage gains, lower ANPIVs will be achieved. For other references [16]–[20], this amount is constant for all voltage gains. Fig. 10(c) presents the ratio of voltage gain to ANPIV for different duty cycle values. According to Fig. 10(c), the ratio of voltage gain to ANPIV of proposed and other references increase by increment of duty cycle. For $d < 0.58$, the proposed topology has the second highest ratio of gain to ANPIV, but for $d > 0.58$, the ratio of gain to ANPIV of the proposed topology is higher than that of other references. This means that, for producing a desired voltage gain, the ANPIV on the proposed

TABLE VI
DESCRIPTION OF 2-INPUT AND *n*-INPUT VERSIONS OF PROPOSED AND [15]–[20] TOPOLOGIES

Parameters		Topology						
		[15]	[16]	[17]	[18]	[19]	[20]	Proposed
2-Input Version	Switches	2	2	3	2	2	5	6
	Diodes	2	2	3	3	5	1	2
	Inductors	2	2	3	2	2	3	4
	Capacitors	2	2	3	4	5	3	4
	Components	8	8	12	11	14	12	16
	V_o	$\frac{d_1 d_2 V_1 + (1-d_1)V_2}{(1-d_1)(1-d_2)}$	$\frac{V_1}{1-d_1}+\frac{V_2}{1-d_2}$	$\frac{V_1}{(1-d_1)^2}+\frac{V_2}{1-d_2}$	$\frac{V_1}{1-d_1}+\frac{V_2}{1-d_2}$	$\frac{3V_1}{1-d_1}+\frac{2V_2}{1-d_2}$	$\frac{(2-d_1)V_1}{(1-d_1)^2}+\frac{V_2}{1-d_2}$	$\frac{(2-d_1)V_1}{(1-d_1)^2}+\frac{V_2}{(1-d_2)^2}$
n-Input Version	Switches	n	n	n+1	n	-	n+3	3n
	Diodes	n	n	n+1	2n-1	-	n-1	n
	Inductors	n	n	n+1	n	-	n+1	2n
	Capacitors	n	n	n+1	2n	-	n+1	2n
	Components	4n	4n	4n+4	6n-1	-	4n+4	8n
Input currents		Pulsating	Continuous	Continuous	Continuous	Continuous	Continuous	Continuous
Bidirectional energy flow		No	No	No	No	No	Yes	Yes
Step-up capability		**	*	***	*	**	***	****

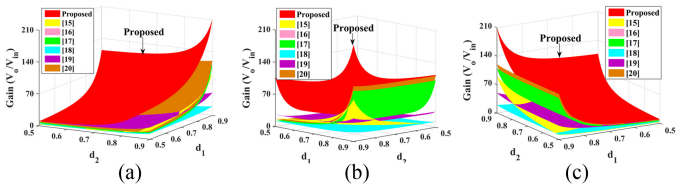

Fig. 8. Voltage gain of proposed and [15]–[20] topologies (2-input) versus different d_1, d_2 (from different views).

TABLE VII
VOLTAGE GAIN IN TERMS OF NUMBER OF DEVICES

Gain in terms of	Topology				
	[16]	[17]	[18]	[20]	Proposed
N_{Switch}	$\frac{N_{Switch}}{1-d}$	$\frac{d+(N_{Switch}-1)(1-d)}{(1-d)^2}$	$\frac{N_{Switch}}{1-d}$	$\frac{1+(N_{Switch}-3)(1-d)}{(1-d)^2}$	$\frac{(\frac{N_{Switch}}{2}-d)}{(1-d)^2}$
N_{Diode}	$\frac{N_{Diode}}{1-d}$	$\frac{d+(N_{Diode}-1)(1-d)}{(1-d)^2}$	$\frac{(N_{Diode}+1)}{2(1-d)}$	$\frac{1+(N_{Diode}-3)(1-d)}{(1-d)^2}$	$\frac{(\frac{N_{Diode}}{2}+2-d)}{(1-d)^2}$
$N_{Inductor}$	$\frac{N_{Inductor}}{1-d}$	$\frac{d+(N_{Inductor}-1)(1-d)}{(1-d)^2}$	$\frac{N_{Inductor}}{1-d}$	$\frac{1+(N_{Inductor}-3)(1-d)}{(1-d)^2}$	$\frac{(\frac{N_{Inductor}}{2}+1-d)}{(1-d)^2}$
$N_{Capacitor}$	$\frac{N_{Capacitor}}{1-d}$	$\frac{d+(N_{Capacitor}-1)(1-d)}{(1-d)^2}$	$\frac{N_{Capacitor}}{2(1-d)}$	$\frac{1+(N_{Capacitor}-3)(1-d)}{(1-d)^2}$	$\frac{(\frac{N_{Capacitor}}{2}+1-d)}{(1-d)^2}$
$N_{Component}$	$\frac{N_{Component}}{4(1-d)}$	$\frac{d+(\frac{N_{Component}}{4}-1)(1-d)}{(1-d)^2}$	$\frac{(N_{Component}+1)}{6(1-d)}$	$\frac{1+(\frac{N_{Component}}{4}-1)(1-d)}{(1-d)^2}$	$\frac{(\frac{N_{Component}}{8}+1-d)}{(1-d)^2}$

topology will be less than the others, which can lead to less cost, size, and losses.

VIII. EXPERIMENTAL RESULTS

The laboratory-scale 2-input version of the proposed topology has been experimentally implemented to confirm its appropriate performance (see Fig. 11). The specification of implemented prototype has been presented in Table IX.

According to (10), $L_{1\mathrm{a,cri}} = 17.82\ \mu$H, $L_{1\mathrm{b,cri}} = 257.4\ \mu$H, $L_{2\mathrm{a,cri}} = 15.01\ \mu$H, and $L_{2\mathrm{b,cri}} = 122.57\ \mu$H are the critical inductances of implemented prototype. In order to guarantee the CCM operation of converter and also to limit inductor peak current and current ripple, which leads to reduction of current stress of switching devices, the ferrite core type inductors with inductances of $L_{1\mathrm{a}} = L_{2\mathrm{a}} = 150\ \mu$H and $L_{1\mathrm{b}} = L_{2\mathrm{b}} = 500\ \mu$H have been selected.

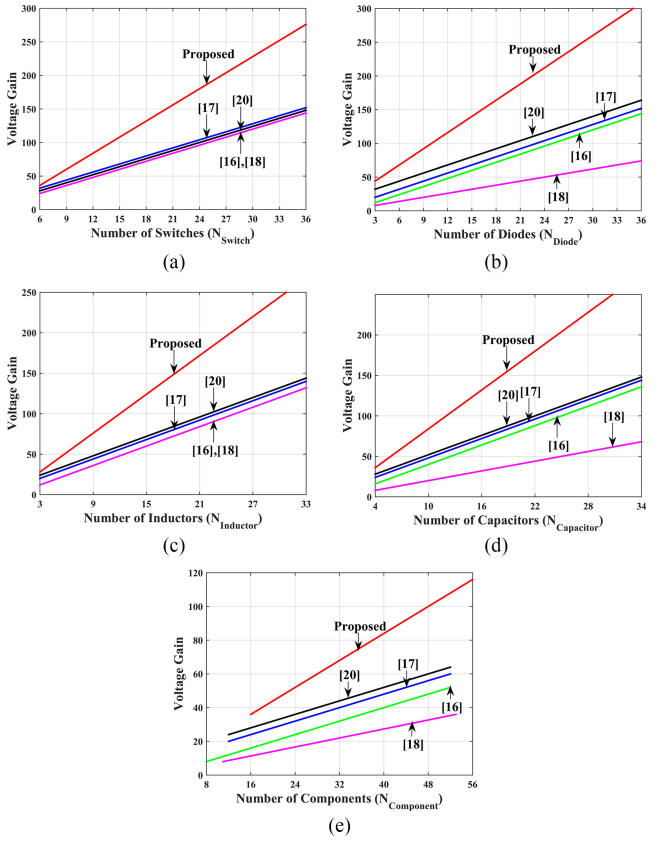

Fig. 9. Gain of proposed and [16]–[18], [20] topologies in terms of number of (a) switches, (b) diodes, (c) inductors, (d) capacitors, and (e) components. ($d = 0.75$).

TABLE VIII
NORMALIZED PEAK INVERSE VOLTAGE (NPIV) ON SWITCHES/DIODES OF PROPOSED AND [15]–[20] TOPOLOGIES (2-INPUT VERSION AND IDENTICAL INPUT SOURCES AND DUTY CYCLES)

Topology	[15]	[16]	[17]	[18]	[19]	[20]	Proposed
NPIV $\left(\frac{PIV}{V_o}\right)$	S_1 $\frac{1-d}{d^2-d+1}$	S_1 0.5	S_1 $\frac{1-d}{2-d}$	S_1 0.5	S_1 0.2	$T_{1,1}$ $\frac{1-d}{3-2d}$	$T_{1,1}$ $\frac{1-d}{3-d}$
			D_1 $\frac{1-d}{2-d}$		S_2 0.2	$T_{1,2}$ $\frac{1}{3-2d}$	$T_{1,2}$ $\frac{1}{3-d}$
	D_1 $\frac{1-d}{d^2-d+1}$	D_1 0.5	S_2 $\frac{1-d}{2-d}$	D_1 0.5	D_1 0.4	$T_{1,3}$ $\frac{1-d}{3-2d}$	$T_{1,3}$ $\frac{1-d}{3-d}$
			D_2 1		D_2 0.4	T_2 $\frac{1-d}{3-2d}$	$T_{2,1}$ $\frac{1-d}{3-d}$
	S_2 $\frac{1}{d^2-d+1}$	S_2 0.5	Q $\frac{d}{2-d}$	S_2 0.5	D_3 0.4		$T_{2,2}$ $\frac{d}{3-d}$
					D_4 0.4	Q $\frac{2-d}{3-2d}$	D_2 $\frac{1-d}{3-d}$
	D_2 $\frac{1}{d^2-d+1}$	D_2 1	D_o $\frac{1}{2-d}$	D_2 0.5	D_o 0.2	D_{m1} 1	Q $\frac{2-d}{3-d}$
				D_3 0.5			D_{m1} 1
Total NPIV	$\frac{4-2d}{d^2-d+1}$	2.5	3	2.5	2.2	3	$\frac{10-5d}{3-d}$
Average NPIV	$\frac{4-2d}{4(d^2-d+1)}$	0.625	0.5	0.5	0.314	0.5	$\frac{10-5d}{8(3-d)}$

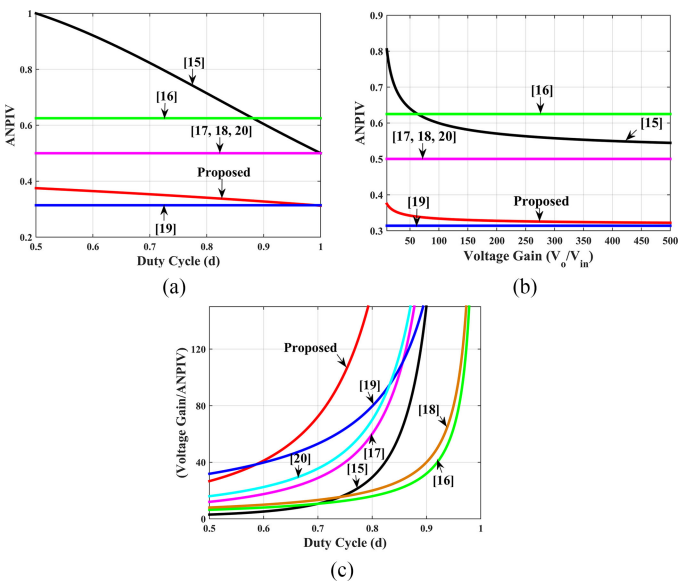

Fig. 10. (a) ANPIV versus duty cycle. (b) ANPIV versus voltage gain. (c) [Voltage gain/ANPIV] versus duty cycle; for proposed and [15]–[20] topologies (assuming 2-input version and identical inputs and duty cycles).

Based on (11) and assuming the maximum voltage ripple on the capacitors to be $x_C = 1.5\%$, the capacitances are achieved as $C_1 \geq 73.65\,\mu$F, $C_2 \geq 71.81\,\mu$F, and $C_{m1} \geq 8.41\,\mu$F. Considering the stresses on the capacitors [presented in (4)], the capacitors are selected as: $C_1 = C_2 = 100\,\mu$F (100 μF, 50 V, Radial Electrolytic Capacitor Nichicon UPW1H101MPD), C_{m1} $= 47\,\mu$F (47 μF, 200 V, Radial Electrolytic Capacitor Nichicon UVZ2D470MHH) and $C_o = 220\,\mu$F (220 μF, 350 V, Radial Electrolytic Capacitor Nichicon UVY2V221MRD).

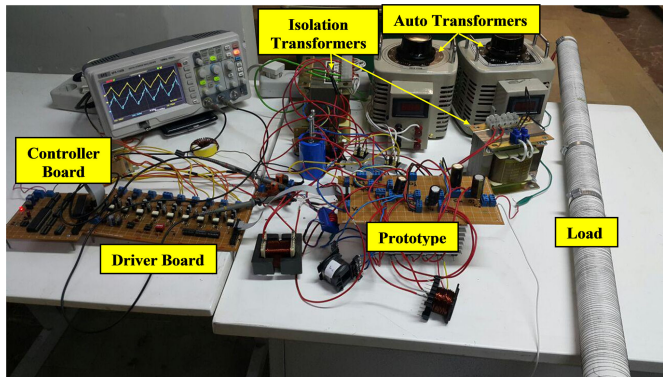

Fig. 11. Laboratory-scale implemented prototype.

TABLE IX
SPECIFICATION OF IMPLEMENTED PROTOTYPE

Parameter	Value	Parameter	Value
V_1	15 [V]	L_{1b}	500 [μH]
V_2	10 [V]	L_{2a}	150 [μH]
d_1	0.7	L_{2b}	500 [μH]
d_2	0.65	C_1	100 [μF]
f	40 [kHz]	C_2	100 [μF]
R	450 [Ω]	C_{m1}	47 [μF]
L_{1a}	150 [μH]	C_o	220 [μF]
V_o	Theoretical	298.299[V]	
	Experimental	293[V]	

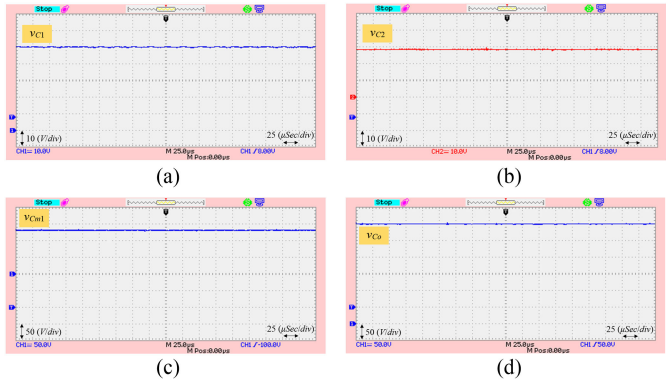

Fig. 12. Voltage waveform on (a) C_1; (b) C_2; (c) C_{m1}; (d) C_o; capacitors.

Based on current stress and PIV on switches/diodes, the ($T_{1,1}$, $T_{1,3}$, $T_{2,1}$, $T_{2,2}$, $T_{2,3}$) switches have been realized by IRF3710 MOSFETs and ($T_{1,2}$, Q) switches have been realized by IRF740 MOSFETs. The D_{m1} diode has been realized by NXP BYV34-400. The switching pulses have been produced by ATmega32 AVR Microcontroller. The LA-55P 715191 has been used as current sensor with sensing ratio of 0.264. The capacitors' voltage waveform has been shown in Fig. 12.

According to Fig. 12, the voltage on C_1, C_2, C_{m1}, and C_o capacitors are about 48, 26, 129, and 293 V, respectively. Since the load and output capacitor have the same voltages. So, $V_o =$

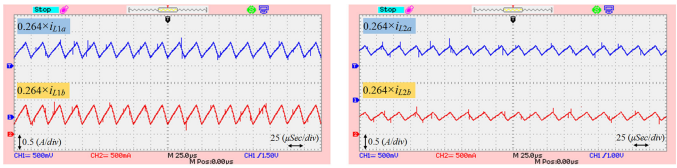

Fig. 13. Current waveform of (a) (L_{1a}, L_{1b}); (b) (L_{2a}, L_{2b}); inductors.

293 V. The output voltage (V_o) is about 19 times higher than $V_1 = 15$ V and 29 times higher than $V_2 = 10$ V, which confirms the high step-up capability of the proposed topology. These values are validated by (4) and (5). The capacitances have been selected in a way that the voltage ripple on them be limited to less than 1%. The inductor currents have been presented in Fig. 13. It is observed that the proper selection of inductances have led to low current ripple of L_{1a}, L_{1b}, L_{2a}, and L_{2b} inductors, which are, respectively, about 1.3, 1.2, 0.8, and 0.46 A [confirmed by (7)]. Also, Fig. 13 shows that peak current values of L_{1a}, L_{1b}, L_{2a}, and L_{2b} inductors are, respectively, about 8.2, 3.34, 6, and 2.4 A [confirmed by (9)]. These low peak values lead to lower current stress of switches/diodes and consequently lower losses.

The current of first and second input sources (i_1, i_2) are, respectively, equal to ($i_{L1a} + i_{L1b}$) and i_{L2b}. Fig. 13 confirms that the current of both input sources are continuous, which is necessary, especially for MPPT-based applications. The average current values of first and second input sources are $I_1 = 8.7$ A and $I_2 = 4.6$ A, respectively. The total input power of the proposed topology ($P_{in} = P_{in1} + P_{in2}$) is about $P_{in} = 176.9$ W ($P_{in1} = 130.6$ W, $P_{in2} = 46.3$ W). The output power of converter is about $P_o = 161.48$ W, which leads to an efficiency of 91.2%. According to Fig. 14, the PIV on $T_{1,1}$, $T_{1,2}$, $T_{1,3}$, $T_{2,1}$, $T_{2,2}$, D_2, Q, and D_{m1} are, respectively, about 49, 165, 49, 27, 54, 27, 215, and 293 V, which are confirmed by Table I.

As seen, the D_{m1} diode has the highest PIV, which is equal to $V_o = 293$ V. The other switches or diodes withstand less voltage than V_o during their OFF mode. The current waveform of switches/diodes have also been presented in Fig. 15.

The $T_{1,1}$ has highest current stress (which is about 14 A). The current stress of $T_{1,1}$, $T_{1,2}$, $T_{1,3}$, $T_{2,1}$, $T_{2,2}$, D_2, Q, and D_{m1} are, respectively, about 14, 5, 9, 9, 2.5, 6.4, 3.3, and 2.2 A. It is observed that all the switches/diodes (except $T_{1,1}$) have low current stresses. The results shown in Fig. 15 are validated by Table II. The efficiency of the proposed topology and the structures presented in [16] and [20] have been plotted and compared across [30–350 W] range of output power in Fig. 16. Fig. 16 shows that the efficiency of the proposed topology remains higher than 85% across the aforementioned range. The efficiency of the proposed topology can be further improved by applying high-tech switches/diodes with less ON-state resistances and forward voltage drops and shorter turn-ON/OFF times. In (ultra) high step-up dc–dc topologies, as the output power increases, the current of low voltage side (input side) increases too, which usually leads to high losses and low efficiencies. This fact can easily be observed in Fig. 16, where the efficiency of the proposed topology and topologies presented in [16] and [20] decreases as the output

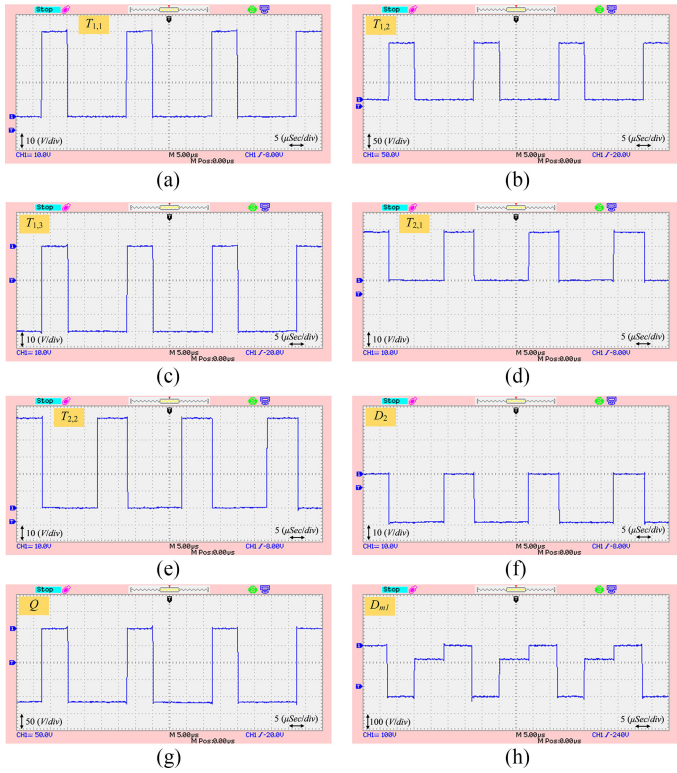

Fig. 14. PIV on (a) $T_{1,1}$, (b) $T_{1,2}$; (c) $T_{1,3}$; (d) $T_{2,1}$, (e) $T_{2,2}$; (f) D_2; (g) Q; (h) D_{m1}.

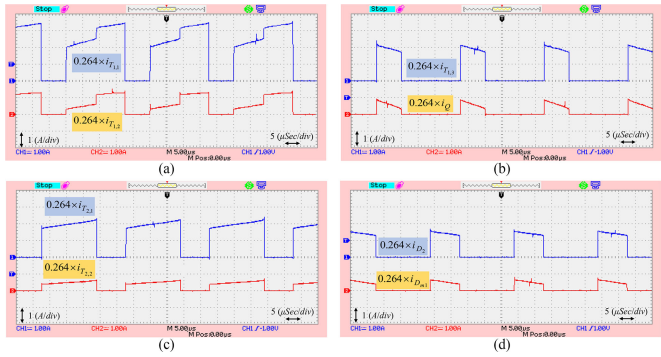

Fig. 15. Current waveform of (a) ($T_{1,1}$, $T_{1,2}$); (b) ($T_{1,3}$, Q); (c) ($T_{2,1}$, $T_{2,2}$); (d) (D_2, D_{m1}).

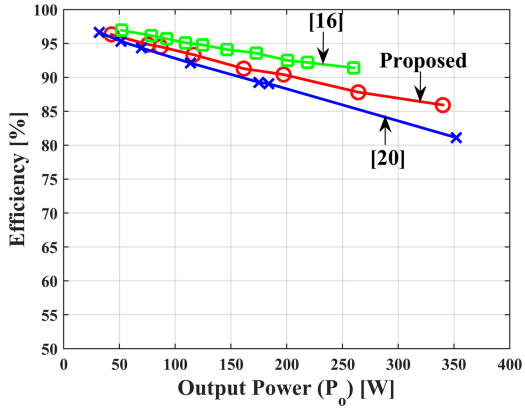

Fig. 16. Efficiency curve of proposed topology across P_o = [30–350 W].

power increases. Therefore, the proposed topology is suggested for low/medium power applications.

IX. Conclusion

In this study, a basic double input high step-up dc–dc topology is proposed and then is extended to *n*-input version. The input currents are continuous. Increment of number of inputs, not only increases the gain of topology, but also decreases the NPIV on switches/diodes. The operational modes of the proposed topology are explained and then steady-state analysis as well as design considerations are presented. For better verification, the proposed topology has been compared with other similar structures. Comparison results show that despite the high voltage gain, the NPIV on switches/diodes of the proposed topology is less than that of other references. For achieving a specified voltage gain, the proposed topology uses less number of devices than other topologies. In other words, application of same number of devices leads to higher voltage gains in the proposed topology than other topologies. So, the portion of each component of the proposed topology on producing the voltage gain is higher than other structures. The double-input version of the proposed topology has been experimentally implemented. For $V_1 = 15$ V, $V_2 = 10$ V, $d_1 = 0.7$, $d_2 = 0.65$, the output voltage and efficiency of the proposed topology are, respectively, about $V_o = 293$ Vand $\eta = 91\%$. Obtained experimental results confirm the validity and effectiveness of the proposed topology.

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