Design Considerations and Development of an Innovative Gate Driver for Medium-Voltage Power Devices With High dv/dt

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***Abstract*—Medium-voltage (MV) silicon carbide (SiC) devices have opened up new areas of applications which were previously dominated by silicon-based IGBTs. From the perspective of a power converter design, the development of MV SiC devices eliminates the need for series connected architectures, control of multilevel converter topologies which are necessary for MV applications, and the inherent reliability issues associated with it. However, when SiC devices are used in these applications, they are exposed to a high peak stress (5–10 kV) and a very high dv/dt (10–100 kV/μs). Using these devices calls for a gate driver with a dc–dc isolation stage that has ultralow coupling capacitance in addition to be able to withstand the high isolation voltage. This paper presents a new MV gate driver design to address these issues while maintaining a minimal footprint for the gate driver. An MV isolation transformer is designed with a low interwinding capacitance, while maintaining the clearance, creepage, as well as insulation standards. A dc isolation test has been performed to validate the integrity of the insulating material. The key features include low input common mode current, and a short-circuit protection scheme specifically designed for 10 kV SiC MOSFETs. The performance of the gate driver is evaluated using double pulse tests and continuous tests. Experimental results validate the advantages of the gate driver and its application for MV SiC devices exhibiting very high dv/dt. The proposed gate driver concept is aimed at providing an efficient and reliable method to drive MV SiC devices.**

***Index Terms*—Boost converter, buck converter, continuous tests, coupling capacitance, double pulse test, dv/dt immunity, gate driver, medium voltage (MV), silicon carbide (SiC) devices.**

I. Introduction

With the advancement of wide bandgap semiconductors, power devices such as silicon carbide metal-oxide-field-effect transistors (SiC-MOSFETs) and silicon carbide insulated-gate-bipolar transistors (SiC-IGBTs) are now available with blocking voltages up to 15 kV [1]. A 4H-SiC n-IGBT with a blocking voltage up to 27.5 kV is demonstrated in [2]. Applications which require a blocking voltage of 1.2–10 kV are primarily dominated by SiC MOSFETs owing to its small ON-state resistance [3]. While gate drivers are commercially available for SiC devices with a blocking voltage range of 650–1700 V, there are a very few commercial gate drivers for 10 kV SiC MOSFETs due to the challenges associated with them [4]. The MV SiC MOSFETs' fast switching transients can result in a dv/dt as high as 100 kV/μs, which imposes a requirement for a very low isolation capacitance in the gate drive circuit [5], [6]. Also, the severe dv/dt stresses reduces the lifetime of the insulation material over time [7].

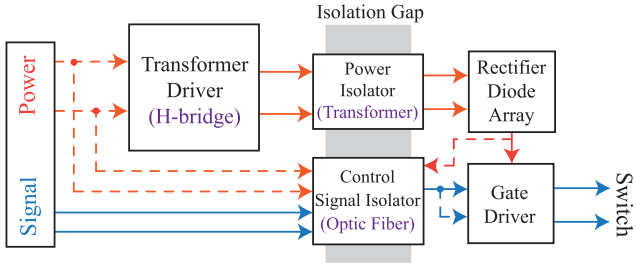

Fig. 1. General schematic of the architecture of a gate driver circuit. The transformer driver provides a high frequency ac signal to the transformer. The power isolation stage can be realized using various methods such as conventional transformers, coreless transformers, power over optics (PoF), etc. The signal isolation is generally done through optcouplers, digital isolators, or optical fibers.

Medium-voltage (MV) gate drivers must provide at least two functions, which includes the signal transmission and the power transmission as shown in Fig. 1. The signal transmission can include signals for pulsewidth modulation, protection, monitoring the health of the devices, etc. For signal transmission, among all the solutions used like optocouplers [8], coreless transformers [9], classical transformers [10], etc., optical fibers seem to be best suited on account of its transmission speed and insulation voltage capability [11]. However, designing the power transmission stage still remains as a challenge basically due to three main reasons, which are as follows:

1) high isolation requirements;

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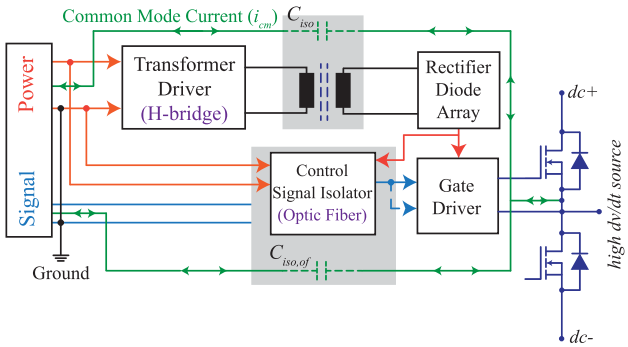

Fig. 2. Schematic representation of the common mode current path for the high side gate driver in a half-bridge configuration. The isolation capacitance of the transformer (C_{iso}) is much higher than the isolation capacitance of the optical fiber ($C_{\text{iso,of}}$). The common mode current through the optical fiber is therefore generally neglected.

2) low coupling capacitance;
3) optimized gate driver footprint.

It becomes necessary to satisfy all these requirements simultaneously, and since the requirements counter one another, it becomes imperative to have an optimum tradeoff between them, with the isolation requirements and the low coupling capacitance being the highest priority ones. The high dv/dt during the turn-ON and turn-OFF of the SiC MOSFETs is a major concern. The high dv/dt leads to the disruption of the control signals due to the common mode (CM) currents that flows through the interwinding capacitance of the isolation transformer as shown in Fig. 2. The magnitude of the CM current (I_{cm}) is directly affected by the dv/dt and isolation capacitance (C_{iso})

$$i_{\text{cm}} = C_{\text{iso}} \frac{dv}{dt}. \tag{1}$$

A number of MV gate drivers have been proposed in the literature [5], [6], [11]–[16]. Several isolated power transformer topology have been studied in [17], where isolation transformers having coupling capacitance less than 1 pF have been demonstrated where an isolation capability of 20 kV is claimed. However, no further analytical explanation has been given for how it can be achieved. In [11], a gate driver for a 15 kV SiC MOSFET is proposed. The gate drivers' power supply is based on a power over fiber (PoF) concept. It offers high CM immunity and has a comparatively smaller footprint. However, due to its very low efficiency (24%), and its maximum power output being limited to 0.5 W, driving MOSFETs with paralleled dies is not possible with this design. In addition, the overcurrent protection functionality with desaturation scheme is not demonstrated. Further, the PoF concept is not very reliable for continuous operation of the converters. In [6], a gate driver is designed to drive 15 kV SiC IGBTs and is based on the conventional transformer method. However, no information on the CM currents is provided. In addition, no short-circuit protection is demonstrated. A gate driver with high CM rejection and a miller clamp is provided in [5]. A flyback-based topology is used for the isolation stage and a coupling capacitance of 2.6 pF has been achieved. The analysis does not give an insight into the size of the transformer. Gate drivers using wireless power transfer have also been studied [13], [14]. These are, however, sensitive to electromagnetic interference and requires larger size for isolation and shielding. A current-loop-based gate driver is proposed in [15]. No experimental results are, however, provided regarding the insulation capabilities of the gate driver. An enhanced short-circuit protection scheme is discussed in [18] where a potential divider is used to maintain the drain-source desat voltage below the reference desat voltage during normal operation. The gate driver used is an intelligent gate driver proposed in [19] where a computer programmable logic device is used for monitoring the temperature and actively driving the gate driver voltage. The power supply used for isolation in the gate driver is the same as in [6]. Also, none of the previous works considers the insulation standards required for operation and testing of the gate drivers.

This paper provides the design and development of an MV gate driver to enable efficient and smooth operation of MV SiC power devices. The MV isolation transformer is the key component for reliable operation of an MV gate driver. The components in the gate driver circuitry, which experiences the MV needs to be properly designed. From the perspective of the gate driver, the MV isolation transformer and the desat (short-circuit) diode experience a MV across them. The optical connection also witness the MV across them, but they are designed to withstand voltages in ranges of 100 kV. The novelty of the design structure hinges on the design and implementation of a robust isolation transformer, which maintains the required insulation requirement, while having a small coupling capacitance and an optimized footprint. Additional features like short-circuit protection scheme (with a single diode and no additional circuitry) is also implemented to built a reliable gate driver which is able to drive 10 kV SiC MOSFETs and shut them OFF during abnormal conditions. A dc isolation, which is multiple time the working voltage is provided for reliable operation of the gate driver over an extended period of time. The performance of the gate driver is evaluated experimentally by conducting double pulse tests and continuous tests on a 10 kV SiC MOSFET from Wolfspeed. The coupling capacitance and the associated CM currents of the gate driver is also measured. The short-circuit protection scheme of the gate driver is also tested by shorting the dc-bus through the 10 kV SiC MOSFET.

The paper is organized as follows. Section II describes the gate driver and the power supply architecture. The dc–dc isolation stage, which includes the isolation transformer design is explained in detail. The short-circuit protection scheme for 10 kV MOSFET is also elaborated upon. A brief idea on the gate driver architecture design is also provided. Section III details the experimental results conducted to validate reliable operation of the MV gate driver. It is followed by conclusions and references.

II. Gate Driver and Power Supply Architecture

The MV isolation and high dv/dt requirements on the gate driver imposes several restrictions on the design of the dc–dc isolation stage. In addition, the selection of components having high immunity to noise and having reliable signal transfer capability, while maintaining a small footprint, is imperative. The overall architecture of the gate driver is shown in Fig. 3.

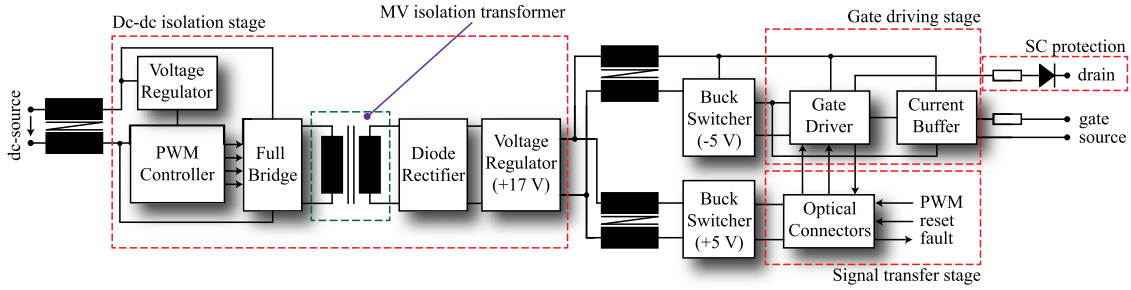

Fig. 3. Overall architecture of the designed gate driver. It includes four main parts: DC–DC isolation stage, signal transfer stage, gate driving stage, and short-circuit protection stage.

A. DC–DC Isolation Stage

The design of the dc–dc isolation stage is perhaps the most important aspect while building an MV gate driver for driving MV SiC devices.

1) Power Supply Topology: The designed power supply utilizes a single active bridge (SAB) topology to deliver power across the isolation stage [20]. In order to reduce the gate driver footprint, an integrated full bridge switch (FDMQ86530L) is used in the primary side of the SAB [21]. This full bridge is driven by a phase shifted full bridge controller (LM5046), which ensures smooth start-up operation in addition to having an in-built undervoltage lockout and overvoltage protection [22]. This IC operates with a user defined switching frequency (100 kHz), which ensures a reasonable temperature rise in the transformer (on account of core losses) while maintaining the minimum size of the transformer. The secondary side of the SAB consists of a diode rectifier (MB110S) for converting the high frequency ac signal to an unregulated dc-stage. The output of the unregulated dc-stage is kept between 17 and 18 V. A linear regulator of 17 V is used thereafter to convert the unregulated dc-voltage to a regulated dc voltage. A -5 V stage for turning OFF the SiC-MOSFET is derived from the regulated $+17$ V power supply, using a buck converter IC. The power supply for the signal stage (optical fiber) is also generated from the regulated $+17$ V supply. The $+17$ V/-5 V gate drive is based on the recommended driving voltages for the Gen3 10 kV SiC MOSFET.

2) Transformer Design: The design of the transformer is based in two major factors which includes achieving a low coupling capacitance between the primary and the secondary and being able to meet the high isolation requirements. In addition to these requirements, it is necessary for the transformer design to meet the clearance and creepage standards as provided in IEC 61800-5-1 [23]. For a working voltage of 7.2–7.6 kV, which is ideally the operating voltage for 10 kV SiC MOSFETs, the clearance requirement is 25 mm for all the pollution levels. The creepage requirement comes to be around 32.5 mm [23], [24]. A clearance of 50 mm is maintained between the open terminals of the designed isolation transformer, and the creepage distance is maintained by the support structure as explained later.

The coupling capacitance between the primary and the secondary winding of the transformer is mainly dependent on the distance between the primary and the secondary windings and the area enclosed by the transformer windings and the core. The dominant part of the capacitive coupling is present through the transformer core [5]. In order to reduce the area enclosed by the windings with the transformer core, a PCB-based planar winding is used. This leads to an increase in the leakage inductance of the transformer, but it greatly helps in the reduction in coupling capacitance. An analytical method for the capacitance estimation is carried out for the designed transformer. The capacitances of the transformer include turn-to-turn capacitance, turn-to-core capacitance, and turn-to-shield capacitance. As seen from Fig. 4(b), the section is divided into eight regions ($R1$–$R8$). The capacitances of regions $R1$–$R4$ can be calculated by the parallel-plate capacitor model and the capacitance of the regions $R5$–$R8$ is calculated by cylindrical capacitor model [25]. The airgap between the core and the PCB is neglected. Fig. 4 shows the winding arrangement in the PCB and the corresponding parasitic capacitances considered for the analysis. The turn-to-turn capacitances for the windings which are on the same layer (C_{12}, C_{23}, C_{45}, C_{56}, C_{78}, and C_{89}) is given by

$$C_{\mathrm{TT,SL}} = 4 \times \frac{\epsilon_0 \epsilon_r t l_1}{w_i} + \frac{2\pi\epsilon_0\epsilon_r t}{\log(r_i + w_c)/r_i} \tag{2}$$

where r_i can be selected appropriately from Fig. 4(b). ϵ_0 is the permittivity of vacuum, ϵ_r is the permittivity of the insulating material (Arlon 85S), and t is the thickness of the PCB. The turn-to-turn capacitances for overlapping turns on adjacent layers (C_{16}, C_{25}, C_{34}, C_{67}, C_{58}, and C_{49}) is given by

$$C_{\mathrm{TT,AL}} = \frac{\epsilon_0 \epsilon_r}{t} \times (4 w_c l_1 + \pi(r_i^2 - (r_i - w_c)^2)) \tag{3}$$

where r_i can be selected appropriately from Fig. 4(b). The overlapping capacitances for nonadjacent layers can be calculated similarly by adjusting the value of t (depending on the distance between the layers, t becomes $2t$ or $3t$).

Similarly, the turn-to-shield capacitance can be be calculated by the parallel plane model

$$C_{\mathrm{TS}} = \frac{2\epsilon_0\epsilon_r}{t}(12 w_c l_1 + \pi(2r_3^2 + r_2^2 + r_1^2 - 2(r_3 - w_c)^2 - (r_2 - w_c)^2 - (r_1 - w_c)^2)). \tag{4}$$

The total turn-to-core capacitance (primary to core and secondary to core) is calculated by

$$C_{\mathrm{TC}} = \frac{12\epsilon_0\epsilon_r t l_1}{w_i} + \frac{6\pi\epsilon_0\epsilon_r t}{\log(r_1 - w_c)/(r_1 - w_c - w_i)}. \tag{5}$$

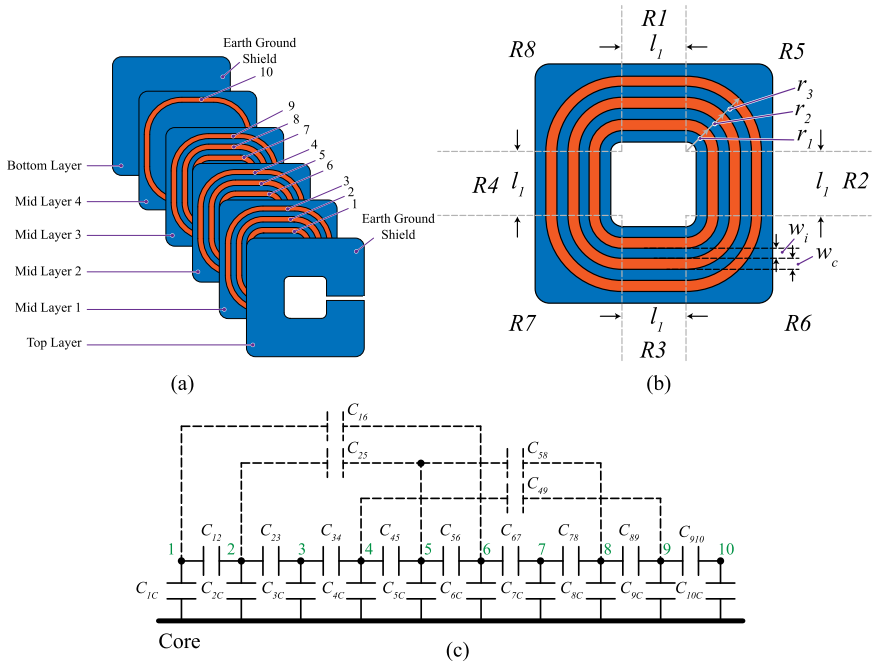

Fig. 4. (a) Internal layers of the PCB used for the high voltage isolation transformer winding. The ten turn winding is shown here for illustration. (b) Cross section of a single layer of the winding structure showing the internal dimensions. The windings are shown in orange and the PCB (insulation) is shown in blue. (c) Parasitic capacitance present in the isolation transformer between the windings, and windings and core (only one winding is shown here for illustration).

TABLE I
PARAMETERS OF THE GATE DRIVE MV ISOLATION TRANSFORMER

Parameter	*Value*
ϵ_0	8.85×10^{-12} F/m
ϵ_r	3.4
t	0.0014224 m
w_i	0.002 m
w_c	0.002 m
r_1	0.005 m
r_2	0.009 m
r_3	0.013 m
l_1	0.005 m

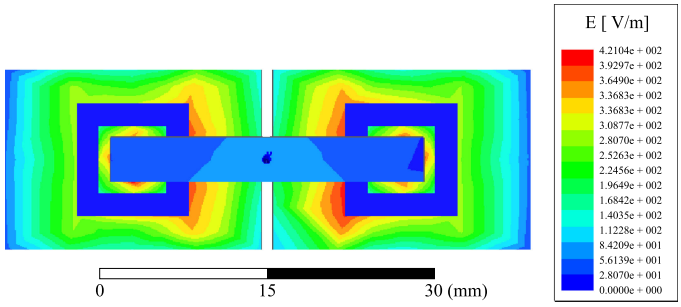

Fig. 5. Finite element modeling of the isolation transformer core showing the electric field distribution. The interwinding capacitance comes out to be 1.6 pF.

The parameters of the transformer is mentioned in Table I.

From the values, the turn-to-shield capacitance comes out to be 24 pF and the interwinding capacitance (which is a series connection of both the turn-to-core capacitance) is found to be 2 pF.

In addition, a finite element modeling of the transformer core using Ansys Maxwell is also carried out (as shown in Fig. 5). The interwinding capacitance and the turn-to-shield capacitance are found to be 1.6 and 22 pF, respectively, and these results are in close agreement with analytical and experimental results.

Also, in order to meet the insulation requirements, each of the primary and the secondary windings are inserted on the middle layers of the PCB, which ensures that the windings have proper insulation both from the top and the bottom sides. The dielectric strength of FR4 is around 800 V/mil which reduces down to 300 V/mil with aging [26] which does not meet the insulation requirements for this application. The designed transformer PCB is manufactured using a polyamide material, Arlon 85S whose dielectric strength is 1.5 times that of FR4 with 1200 V/mil (when new) and around 700 V/mil with aging [27] to maintain the insulation standards. This satisfies the required insulation levels. After aging, insulation between core and winding: (700 kV/mil $\times$ 78.74 mil (thickness of the PCB layer) $=$ 55 kV blocking capability. Fig. 7 shows the sideview of the transformer used for the gate drive circuit.

3) Primary Shield Design: A primary winding shield is provided on the transformer primary winding. This shield is directly grounded and it ensures a lower impedance path for the CM current as compared to the path which powers the signal stage, thus, improving the CM performance. Two major factors (wrt CM issues) are taken into consideration while designing the isolation transformer shield. The capacitance between the CM path and ground (C_{shield}) should be higher than the parasitic capacitance across the isolation transformer of the dc power supply (C_{PS}). This ensures that the CM current has a

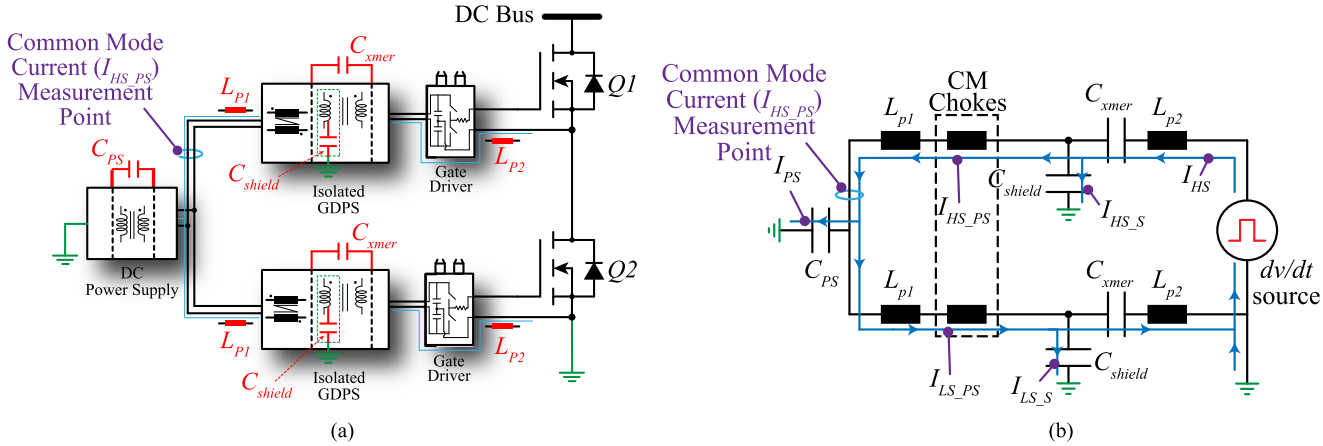

Fig. 6. Architecture of the system showing (a) driver circuit with power supplies and (b) equivalent high frequency circuit showing the common mode current path and grounding considerations.

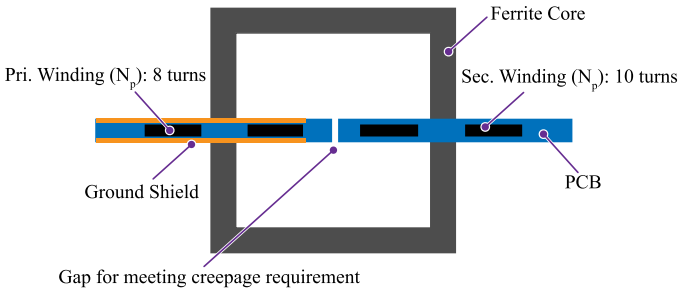

Fig. 7. Representation of the designed transformer. The outer dimensions of the ferrite core is 28 mm × 28 mm × 4 mm. The area of cross section (A_s) is 16 mm^2. The distance between the open terminals is kept at 52 mm.

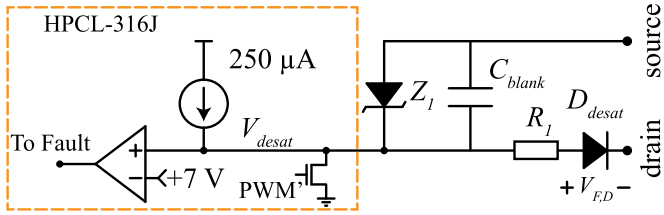

Fig. 8. Short-circuit protection feature of the designed gate driver.

lower impedance path through the shield capacitance. To reinforce this, CM chokes are added in the input supply path in order to increase the impedance for the CM current path (high frequency impedance) flowing into the power supply. This ensures that the CM current flow is impeded through the dc-power supply, but allowed to flow through the ground connection. The equivalent circuit for CM current is depicted in Fig. 6. The ratio between $I_{\mathrm{HS\_}S}$ and I_{PS} can be determined by the following:

$$\frac{I_{\mathrm{HS\_}S}}{I_{\mathrm{PS}}} = \frac{C_{\mathrm{shield}}}{C_{PS}}\left[s(L_{p1}+L_{\mathrm{cm}})\left(sC_{\mathrm{PS}} + \frac{s(L_{p2}C_{\mathrm{shield}}C_{\mathrm{xmer}}s^2 + C_{\mathrm{shield}} + C_{\mathrm{xmer}})}{(L_{p2}+L_{\mathrm{cm}})C_{\mathrm{shield}}C_{\mathrm{xmer}}s^3 + C_{\mathrm{xmer}}L_{p2}s^2 + 1}\right) + 1\right]. \quad (6)$$

The capacitance between the primary transformer winding and the shield C_{shield} is deliberately designed to be greater than C_{PS} by maximizing the overlapping area between the primary winding and the shield which gives $C_{\mathrm{shield}} > C_{\mathrm{PS}}$. Therefore, from (6), it can be shown that the expression on the right-hand side is greater than 1. This establishes the fact that CM current flowing to the earth through the shield capacitance C_{shield} is greater than the CM current flowing through C_{PS}, thus, enabling a reduction in the CM current (through the power supply).

B. Signal Transfer Stage

The input control gate signal to the gate driver is transmitted over fiber-optic cable. This method of signal transfer is extremely reliable with no limits of isolation voltage or dv/dt. The optical transmitter and receiver typically need a voltage of $+5$ V. The transmitter is relatively more immune to dv/dt since it operates at the signal ground. The receiver (which is present on the secondary side of the SAB) derives its power from the dc–dc stage. Proper isolation of the dc–dc stage transformer ensures a reliable operation of the signal transfer.

C. Gate Driving Stage

The gate driver used in this design is a HPCL-316J from Broadcom [28]. This gate driver is chosen due to its inbuilt desat (short-circuit) protection function. The opto-isolation provided by the gate driver is not used since the signal isolation is provided by the optical fiber. The fault and the reset signals from/to the gate driver is transferred to the controller (DSP/FPGA) using optical fibers to ensure smooth and safe operation. A current buffer (IXYS IXDN614YI) stage is provided to increase the current driving capability of the gate drive circuit. While the HPCL-316J has a peak output current capability of 2.5 A; the IXYS IXDN614YI has a 14 A peak current capability allowing the devices to be switched using a much lower gate resistance which might be required to drive SiC devices with multiple parallel dies. Unlike lower voltage (1200 V) SiC MOSFETs, the gate-source capacitance, and consequently the gate charge of 10 kV SiC MOSFETs, is around five times

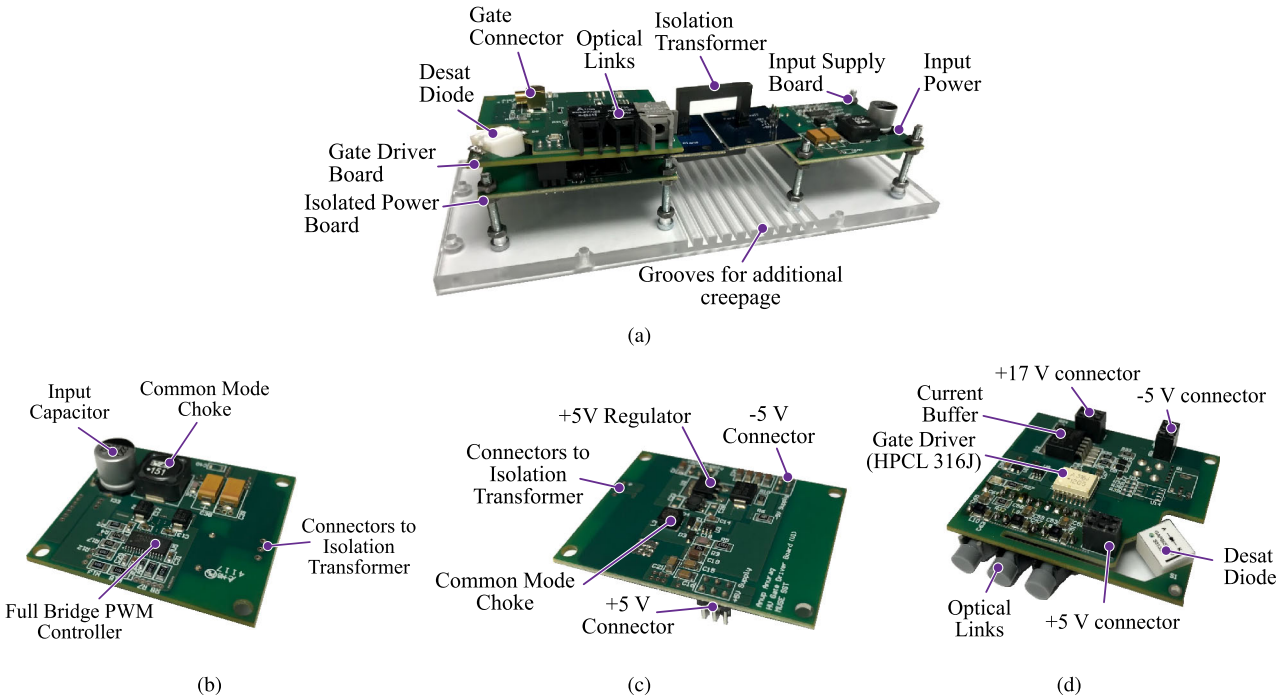

Fig. 9. (a) Designed gate driver for driving 10 kV SiC MOSFETs which includes inherent short-circuit protection and provides low capacitive isolation. The dimensions of the circuit is given by 6 in $\times$ 2 in $\times$ 1.5 in. Photograph of the (b) input power board, (c) isolated power board, and (d) gate driver board. The input power board takes the input to generate a 100 kHz square wave for the isolation transformer. At the isolated power board, this square wave is rectified and the power supplies are generated. The gate driver board includes all the functions for driving the 10 kV SiC MOSFETs.

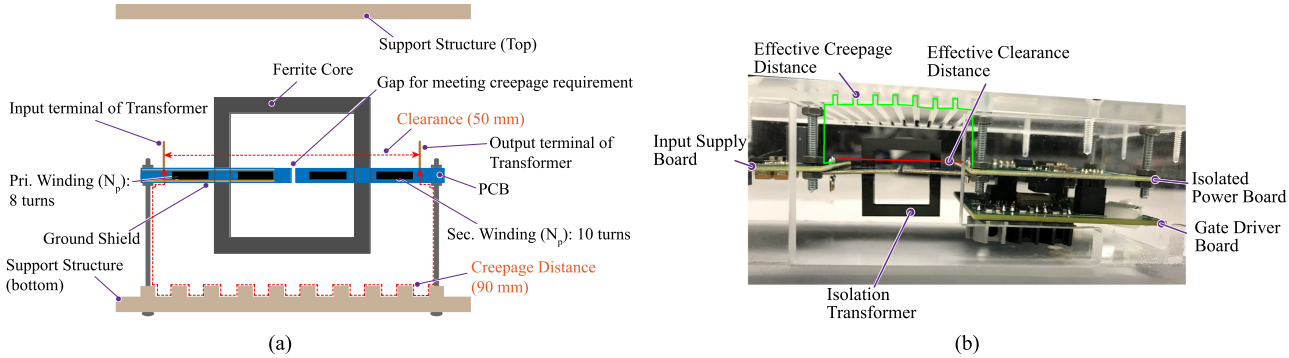

Fig. 10. (a) Schematic diagram of the isolation transformer showing the clearance and creepage distances maintained across the isolation transformer for the MV gate driver circuit. (b) Picture of the actual gate driver showing the clearance and creepage distances maintained across the isolation transformer for the MV gate driver circuit.

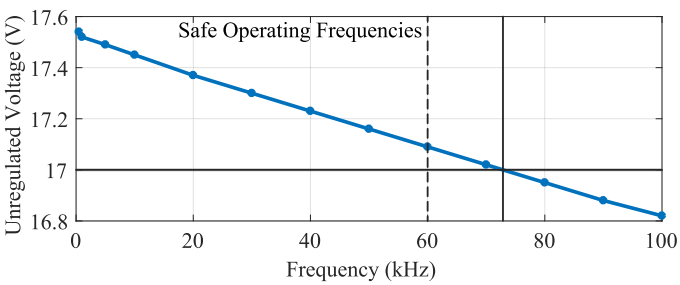

Fig. 11. Loading profile of the designed gate driver. The voltage drops below 17 V beyond a switching frequency of around 60 kHz. For obtaining higher switching frequency, the input power supply needs to be increased. However, an overvoltage protection of +20 V is provided at the input for safety.

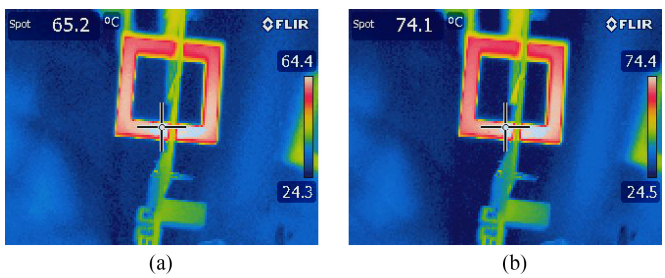

Fig. 12. Temperature of the gate driver isolation transformer. (a) In an unloaded conditions. (b) In a loaded condition. The gate driver transformer operates at a frequency of 100 kHz and a maximum flux saturation density of 0.15 T. The measurements are carried out using Flir E6 infrared camera.

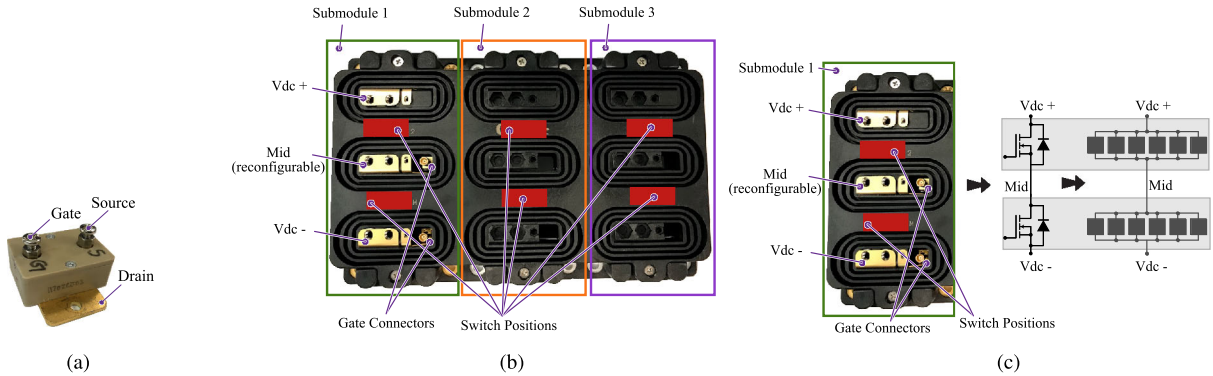

Fig. 13. (a) Single die 10 kV SiC MOSFET packaged in a goldenpack module. The goldenpack module is an experimental package just for testing the dies. (b) Schematic of a XHV-6 module. (c) Six 10 kV SiC MOSFET dies in parallel packaged in the form of a half-bridge in a XHV-6 module. Submodule 2 and submodule 3 are not populated in the XHV-6 module.

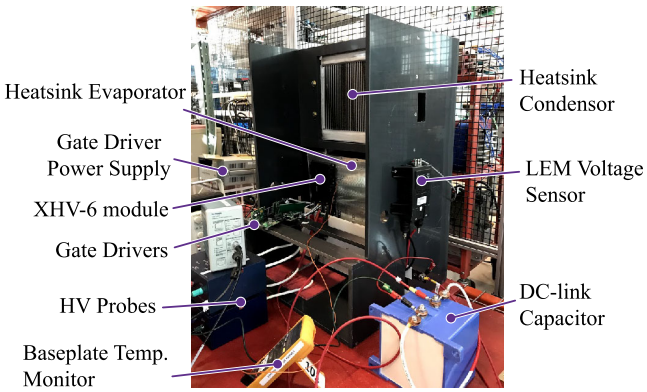

Fig. 14. Experimental setup for testing the gate driver for double pulse tests, and continuous tests.

higher for similar current rated devices (5.6 nC for 1200 V MOSFETs (C2M0280120D) and 24 nC for a single 10 kV SiC die (measured using curve tracer)) [29]–[31]. The difference is gate charge calls for a higher current rating of the gate driver for achieving similar switching speeds (due to the fact that the gate resistance needs to be lower for a higher gate charge). Considering the gate driver circuit with gate resistance of R_g, driving MOSFET with gate-source and gate-drain capacitance of C_{gs} and C_{gd}, respectively, when a step voltage of V_{gg} is applied across the gate-source terminal, the gate current i_g can be represented as [32]

$$i_g = \frac{V_{\text{gg}}}{R_g} e^{-\frac{t}{R_g (C_{\text{gs}} + C_{\text{gd}})}} \tag{7}$$

The gate current equals V_{gg}/R_g at time $t = 0$. Therefore, lower values of gate resistance R_g causes an increase in peak gate current during each switching transient. This peak gate current needs to be supplied from the gate driver IC (or the current buffer IC). This serves as a design criteria for the current buffer stage after the gate driving stage. In this design, a 14 A current buffer is used to enable the gate driver to drive SiC MOSFETs with low gate resistances.

D. Short-Circuit Protection Stage

In order to protect the devices from short-circuit conditions, a short-circuit protection scheme is implemented in the gate driver circuitry. It is necessary to design this short-circuit circuitry to make sure that the device is turned OFF when the current exceeds a particular value. Fig. 8 shows the short-circuit protection block used in this design. A zener diode (Z_1) is placed across the blanking capacitor to avoid any unexpected voltage overshoot. The desat diode ($V_{f,D}$) is the most important part for the short-circuit protection circuit. During the OFF state of the device, this diode is required to block the voltage across the MOSFET. In addition, the diode should be sufficiently fast to respond to the fault. Due to these reasons, a Schottky diode (GAP05SLT80-220) is used for this design [33]. With an 8 kV blocking voltage capability and extremely fast switching speed, this diode fulfills the required criteria. The capacitor C_{blank} determines the blanking time and is chosen at the design stage. The blanking time t_{blank} is given by

$$t_{\text{blank}} = \frac{C_{\text{blank}} \times V_{\text{desat}}}{I_{\text{chg}}} \tag{8}$$

where I_{chg} is the charging current and V_{desat} is the fault threshold voltage. The values depends on the IC used. For HPCL-316J, the charging current is 250 μA and the fault threshold voltage is set at 7 V. The blanking capacitor is set at a recommended value of 100 pF which sets the blanking time at 2.8 μs. The blanking time represents the minimum time it takes for the gate driver IC to respond to the fault condition. In this case, the shut down sequence begins after 2.8 μs, if the device goes to saturation region while the input gate signal in high. The blanking time is provided to avoid any spurious trip during turn-ON transients.

This design is chosen from the fact that the 10 kV SiC MOSFET is driven at 17 V, which allows better short-circuit protection due to its $i - v$ characteristic curve, and is recommended by the manufacturer. Also, the ON-state resistance of the device ($R_{\text{ds,on}}$) has a negligible variation with respect to a change in an ON-state gate voltage from +20 V to +17 V.

For MV SiC MOSFETs, conventionally, a series of diodes with balancing resistors are used. The series connection of the these sensing diodes causes a higher equivalent diode forward

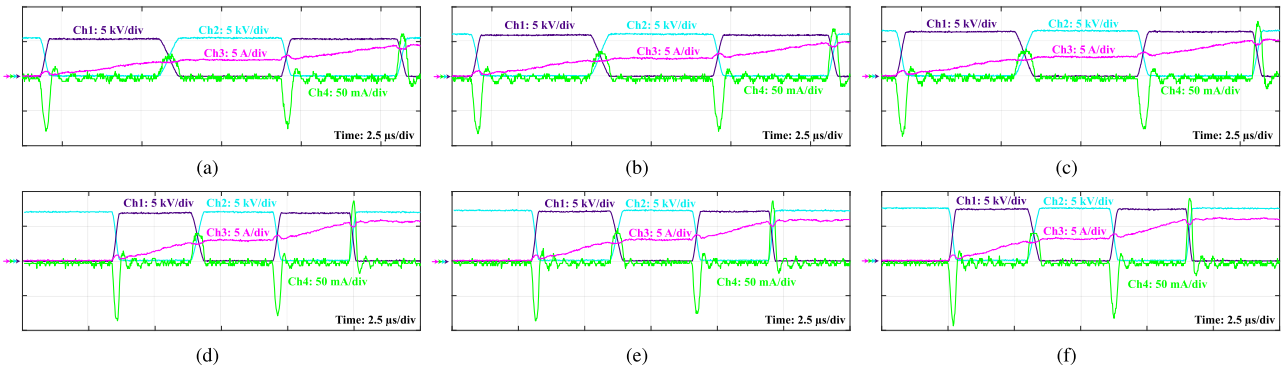

Fig. 15. Experimental results showing the variation in the common mode current with increasing voltage for a dc-link voltage of (a) 5.5 kV (b) 6 kV (c) 6.5 kV (d) 7 kV (e) 7.2 kV, and (f) 7.5 kV. The maximum common mode current occurs at a dv/dt of 36 kV/μs. (Ch1: Voltage across bottom device; Ch2: Voltage across top device; Ch3: Current through the inductor; Ch4: Common mode currents through the gate driver circuit).

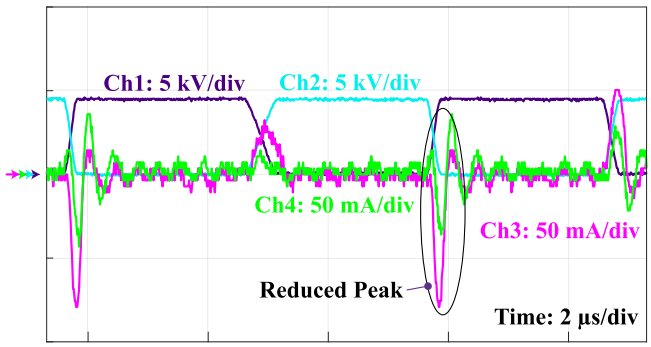

Fig. 16. Comparison between the common mode currents flowing through the gate driver circuit for the two cases (Ch1: Voltage across bottom device; Ch2: Voltage across top device; Ch3: Common mode currents when the shield is not grounded to earth; and Ch4: Common mode currents after shielding the primary side of the gate driver).

voltage, which results in a large offset in the sensed voltage [11], [12]. This complicates the circuit and increases the gate driver footprint. In addition, the additional forward voltage drop of the diode requires a voltage divider circuit in order to bring the sensed voltage down within the fault threshold voltage of commercially available gate drivers [18], and also for better resolution of the sensed voltage. In this design, a single diode is used (with a forward voltage drop of just 2 V) which allows the elimination of the additional diodes and other accompanying circuitry. The trip settings required for the 10 kV SiC MOSFET, to not exceed its rated current at any point of time, is taken as the major design criteria.

For the 10 kV SiC MOSFET, the rated current is around 10 A in continuous operation (at room temperature). Assuming the same power loss at a temperature of 150 °C, the maximum current capability reduces to 5.5 A. The ON-state resistance of the MOSFET increases from around 330 mΩ to around 1 Ω over a temperature range from 25 to 150 °C [34]. If the designed turn-OFF threshold current limit be kept at nearly 15 A for room temperature, and 5 A at an elevated temperature, the voltage drop comes out to be around 5 V (for the given ON-state resistances). This, when added with the ON-state resistance of the diode (around 2 V) gives the fault threshold voltage of 7 V. The short-circuit protection is based on the fact that the sensed voltage V_{desat} should be smaller than the reference voltage of +7 V during normal operation. The gate driver IC is chosen based on its fault threshold voltage of +7 V. The value of v_{ds} for which the protection triggers is given by

$$v_{\text{ds}} = 7 - V_{F,D}\,. \tag{9}$$

The short-circuit protection scheme implemented here serves as a simple scheme with minimal components to achieve short-circuit protection for 10 kV SiC MOSFETs. It should be noted that paralleling the 10 kV SiC MOSFET dies (as in a XHV-6 module) does not change the trip setting due to the fact that the current carrying capability of the MOSFET increases inversely with the ON-state resistance making $v_{\text{ds}} = I_{\text{fault}} \times R_{\text{on}}$ constant for any number of dies in parallel.

III. Experimental Results

Fig. 9 shows the designed gate driver. The dimensions of the gate driver is given by 6 in $\times$ 2 in $\times$ 1.5 in. The gate driver consists of three boards namely input supply board, isolated power board, and gate driver board, as shown in Fig. 9(b)–(d), and an isolation transformer. The clearance and the creepage requirements are satisfied via proper designing of the MV isolation transformer terminals, and by providing the required creepage through the support structure. A clearance of 50 mm is These maintained between the open terminals of the isolation transformer, and the creepage distance is maximized to around 90 mm by providing grooves as shown in Fig. 10(a). satisfy the IEC 61800-5-1 standards (Minimum clearance: 25 mm and creepage distance of 32.5 mm for a working voltage of 7.2–7.6 kV) [24]. The creepage distance is maintained through the support structure as shown in Fig. 10(b). The gate driver is tested with double pulse and continuous tests along with short-circuit tests. In addition, individual tests on the gate driver including thermal tests and loading tests have also been performed.

A. Electrical Loading

The gate driver is directly connected with a 10 kV SiC MOSFET having six dies in parallel [XHV-6 module as shown

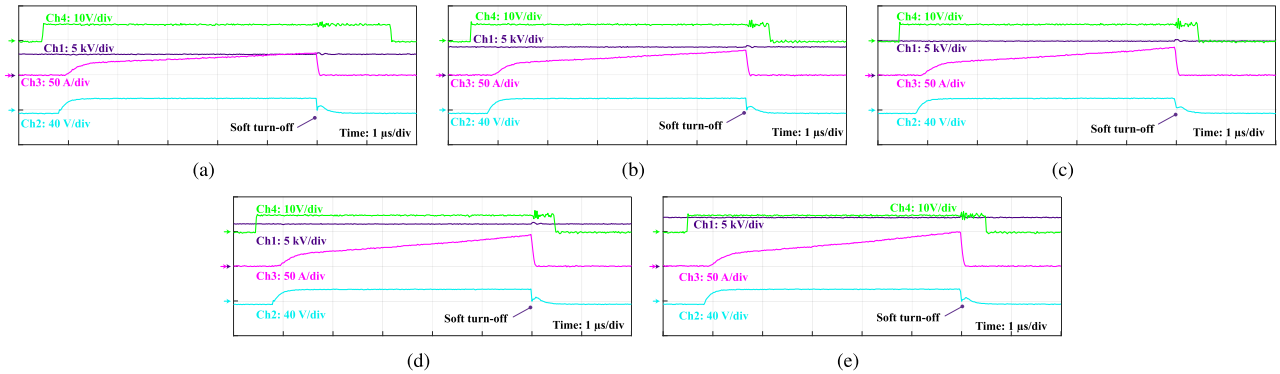

Fig. 17. Experimental results showing the short-circuit protection capability of the designed gate driver for dc-link voltages of (a) 3 kV (b) 4 kV (c) 5 kV (d) 6 kV, and (e) 7 kV. The gate driver turns OFF the device within 5 μs of the fault. (Ch1: Voltage across the device; Ch2: Gate-source voltage at the device; Ch3: Current through the device; and Ch4: Input pulse from the DSP/FPGA).

in Fig. 13(c)] with no-dc link voltage. The switching frequency is varied and the voltage output of the transformer after the diode rectifier is observed. Fig. 11 gives the relation between the power supply loading of the gate driver transformer with the maximum switching frequency the gate driver can support. It is seen that the output voltage drops below 17 V beyond the switching frequency of around 60 kHz.

B. DC-Isolation Test

A dc-isolation test is conducted on the gate driver by connecting the gate driver inputs and outputs across a dc-source through a resistor. The resistor is provided as a protection for the input dc source. Testing is done up to 20 kV for a period of 20 min and no significant leakage current is observed. This ensures the high isolation capability of the designed gate driver. This is possible due to the fact that the windings of the transformer are not exposed and sufficient clearance is maintained between the primary and the secondary side.

C. Thermal Loading

The validation of the operating capability of the gate driver is verified through loading the gate driver and measuring the temperature of the components. All the components are designed to be within their power ratings. The isolation transformer handles the required power to drive the SiC-MOSFET gate and due to its design, it becomes the hottest spot on the gate driver. The transformer is designed to be within a temperature of 100 °C at all operating conditions. Fig. 12 shows the temperature of the isolation transformer at an unloaded condition and a conditions where it is loaded with a XHV-6 module.

D. Experimental Test Setup

Testing is done on two kinds of devices depending on the suitability of operation: a single die 10 kV SiC MOSFET (in a goldenpack) and in a XHV-6 module with six dies in parallel as shown in Fig. 13. The goldenpack device is basically a single 10 kV SiC die mounted on a copper baseplate with gate, source, and drain terminal connections provided [30]. The goldenpack is an experimental device with no baseplate isolation and hence continuous tests are not conducted on those. The XHV-6 module is capable of housing six switch positions per module and each switch positions can have maximum of six dies in parallel in each switch position as shown in Fig. 13(b). However, for initial testing purposes, this particular experimental module is populated with two switches connected in half-bridge configuration. Each of the switch has six parallel dies as shown in Fig. 13(c). The experimental setup featuring the 10 kV SiC MOSFETs in the XHV-6 module is shown in Fig. 14.

E. Common Mode Performance

The most important challenge in designing a gate driver for MV devices is designing a transformer with very low isolation capacitance in order to have low CM currents through the gate driver input. The gate driver is tested with double pulse test setup and the golden-pack device package. The gate resistance is maintained at 20 Ω for all the test conditions. Initially, the testing is done without connecting the primary side shield to the earth ground. The CM currents through the gate driver from 4 to 7.5 kV dc-link voltage is shown in Fig. 15. The CM current is measured using a Pearson current monitor (Pearson 6600) which has a bandwidth of 120 MHz [35]. The current is measured on the connecting wire between the dc power supply and the gate driver as shown in Fig. 6. A maximum peak CM current of around 90 mA is observed for the dc-link voltage of 7.5 kV, where the dv/dt comes out to be at maximum of 36 kV/μs. This results in a coupling capacitance of 2.5 pF.

The primary side shield is connected to the earth ground and the CM currents are observed. The electrical shield provides a low impedance path for the CM current and hence this current does not flow through the gate driver supplies. The CM performance of the gate driver with shield is compared with the CM performance of the gate driver without shield for a dc-link voltage of 5 kV, as shown in Fig. 16. While the gate driver without shield shows a peak CM current of 79 mA at a dv/dt of 30.5 kV/μ s; the shielding effect reduces the CM current to

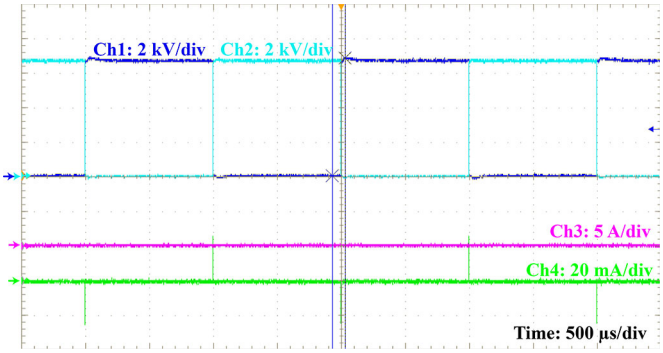

Fig. 18. Operation of a XHV-6 module using the designed gate driver in a no-load, no-current circuit. The switching frequency is 500 Hz and the dc-link voltage is kept at 6.5 kV.

36 mA (which is less than two times the CM current value) rendering it at an effective parasitic capacitance of 1.2 pF.

F. Short-Circuit Performance

The short-circuit protection performance of the gate driver is tested. The dc link is shorted through the device and the functionality is tested at the MOSFET's saturation region. Since, the device is driven at +17 V, it can be seen that the saturation current is not very high (in ranges of 50 A). The gate driver is able to detect the short-circuit fault and cutoff the gate pulse within 5 μs (as shown in Fig. 17) which is within the device's safe operating zone. The avalanche tests of the 10 kV SiC MOSFET (in the golden-pack package) shows that it can withstand a short circuit of up to 13 μs at a dc-link voltage of 6 kV [34].

G. Continuous Tests

The gate driver is tested in a continuous mode of operation using boost converter, and a synchronous buck converter with and without loading. Testing is also done on a half bridge with an unconnected midpoint to validate the operation of the gate driver. Fig. 18 shows the device operation at an unconnected midpoint at a dc-link voltage of 6.5 kV.

The initial validation of the gate driver is carried out by the no load, no current testing. Thereafter, the testing is carried out in a synchronous buck configuration (with and without load) in order to test for both hard and soft switching conditions. Testing is done at a lower value of dc-link voltage (at 2800 and 2000 V, respectively) due to limitations in the laboratory power supply. Fig. 19(a) and (b) shows the operation of the XHV-6 module with the designed gate driver in both hard switching and soft switching operation. In order to test the isolation voltages in a continuous mode of operation, the gate driver is tested in a boost converter up to 5.5 kV as shown in Fig. 19(c). It should be noted that a protection is set at 6 kV output voltage for continuous mode of operation in order to avoid damaging the device in any unforeseen circumstances. A duty cycle of 0.65 is applied to an input of 2 kV in order to generate an output voltage of 6 kV. The test conditions for all the different tests are summarized in Table II.

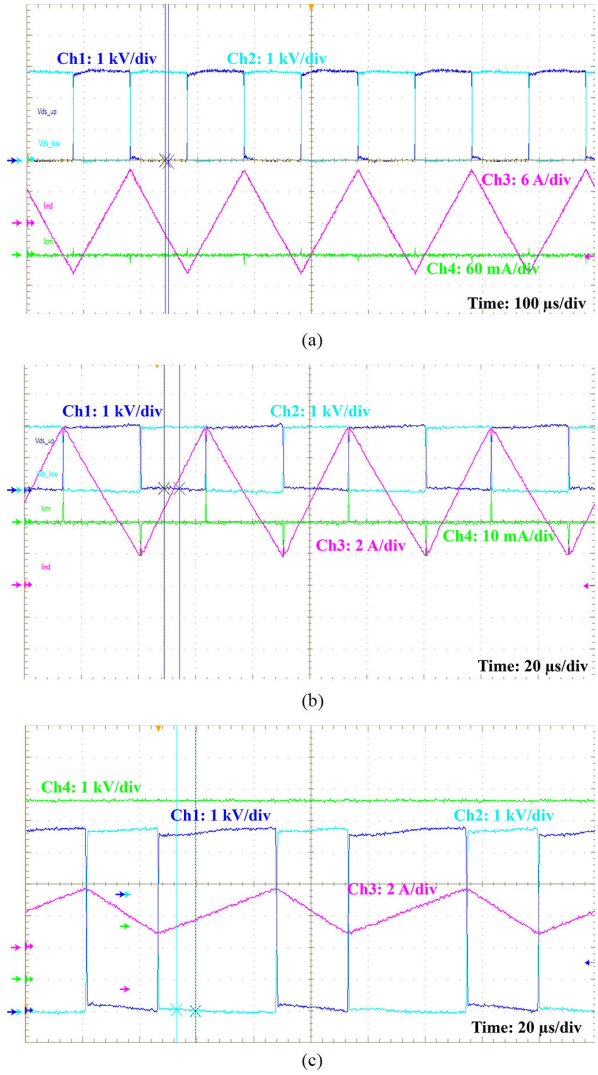

Fig. 19. Operation of the XHV-6 module. (a) Synchronous buck rectifier configuration at no load. (b) Synchronous buck rectifier configuration with load. (c) Boost converter operation. Two cases for the synchronous buck operation are shown for demonstrating the operation at both soft switching and hard switching conditions.

TABLE II
OPERATING CONDITIONS FOR TESTING THE GATE DRIVER IN DIFFERENT MODES OF OPERATION

	CM Tests	*SC Tests*	*Buck*	*Boost*
Package Used	Golden-pack	Golden-pack	XHV-6	XHV-6
Input Voltage Range	5.5 kV to 7.5 kV	3 kV to 6 kV	2 kV - 2.8 kV	0 kV - 2 kV
Output Voltage Range	-	-	1 kV - 1.4 kV	0 kV - 5.5 kV
Switching Frequency	-	-	5 kHz - 15 kHz	15 kHz
Gate Resistance	20 Ω			

IV. CONCLUSION

This paper proposes a gate driver for driving MV SiC devices. The key feature of the gate driver is the design of the isolation stage, which is realized using a ferrite core and windings embedded in a polyamide material, in form of a printed circuit board.

This helps in reducing the overlap area between the winding and the core, which consequently reduces the coupling capacitance. The CM currents are then measured for the gate driver design. A coupling capacitance of approximately 2 pF is observed in such a design. A ground shield is added to the primary winding in order to further reduce the effective capacitance to around 1.2 pF. A short-circuit protection circuit is also implemented and validated for voltages up to 6 kV. Continuous tests are done on the gate driver to further validate the operation and design of the designed gate driver. Since, the gate driver design is one of the challenging parts for a MV system, this gate driver design is aimed at providing a reliable building block for MV converter systems.

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