DAVIC: A New Distributed Adaptive Virtual Impedance Control for Parallel-Connected Voltage Source Inverters in Modular UPS System

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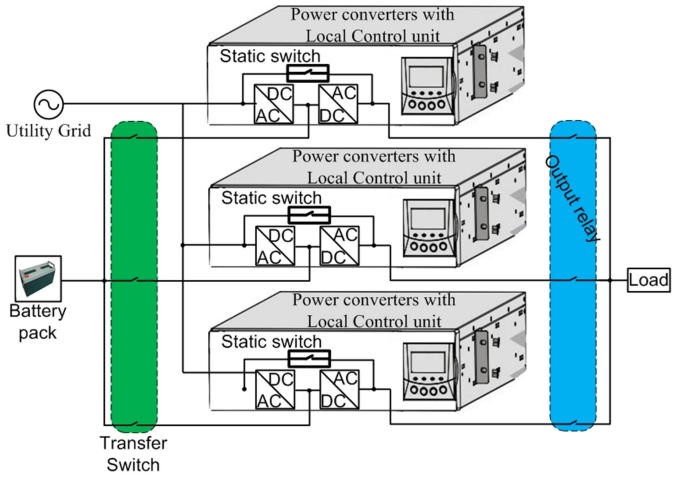
***Abstract*—In this paper, an average active power sharing control strategy based on the distributed concept for the parallel operation of voltage source inverters is proposed to be applied to the modular uninterruptible power supply (UPS) systems. The presented method is named distributed adaptive virtual impedance control (DAVIC), which is coordinated with the droop control method. Low bandwidth CAN-based communication is used for the requirement of data sharing of the proposed method in the real modular UPS system. Unlike the conventional virtual impedance control techniques, the virtual impedance of a converter module is adjusted automatically by using global information when DAVIC is applied, further to tune the output impedance of the power modules. The adaptive virtual impedance is calculated by using the difference between the active power of a local module and the average active power of all the modules in a modular UPS. The DAVIC overcomes the drawback of the conventional virtual impedance control since an accurate value of the real output impedances of different converter modules is not required. Simulations using PLECS and experiments on a real commercial modular UPS are developed to verify the effectiveness of the proposed control methodology. These results shown a superior power sharing performance is obtained when using the proposed method.**

***Index Terms*—Adaptive virtual impedance, circulating current, droop control, modular uninterruptible power supply (UPS) system, power sharing.**



I. Introduction

THE microgrid concept has been proposed several years ago to meet the requirement of the increasing penetration of renewable energy resources into the grid [1]. In the past few years, the study of microgrids has attracted more attention for its reliability and flexibility due to the use of cooperative control of different distributed generators (DGs), energy storage

Manuscript received May 1, 2018; revised July 24, 2018; accepted August 25, 2018. Date of publication September 12, 2018; date of current version April 20, 2019. This work was supported by the Microgrid Research Program at Aalborg University and the company Salicru S.A., Barcelona under the cooperation project "TROY" (www.troy.et.aau.dk). Recommended for publication by Associate Editor F. W. Fuchs. *(Corresponding author: Baoze Wei.)*

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The control method applied to the control of DGs in the microgrid can be transferred to the modular UPS system [12]–[15]. In the recent years, the most common method that used for the control of parallel-connected converters within a microgrid is based on decentralized droop characteristics, which have been identified as effective approaches [16]–[18]. The droop control is widespread due to its attractive features, such as expandability, modularity, redundancy, and flexibility [19], [20]. It performs the wireless control of multiparallel inverters and is more convenient to implement the decentralized control of DGs in a power plant. However, the performance of the droop control is greatly influenced by the unbalanced output impedances of the converters [2], [9]. Then, the virtual impedance is proposed to adjust the output impedance to decouple the active and reactive powers [2], [12], [17], [20], [21]. However, it is difficult to design a proper virtual impedance in a practical paralleled inverters system since the control parameters and the working conditions will influence the output impedance [2], [22]. With poorly designed virtual impedance, the overall performance cannot be guaranteed, especially the average power sharing requirement for the modular UPS.

For the purpose of improving the performance of the conventional droop plus virtual impedance loop framework, the adaptive virtual impedance control has been proposed in several research works [22]–[26]. The output impedance is commonly adjusted to be inductive in accordance with the conventional droop function, in which the active power can be controlled by the inverter frequency while the reactive power can be regulated by the output-voltage amplitude. In [23] and [26], reactive power sharing methods based on adaptive virtual impedance were presented; the adaptive virtual impedance was obtained by the difference of the reactive power between the parallel DGs. For example in [22], the adaptive inductance was calculated by detecting the circulating current between the parallel inverters, while at the same time, it should monitor the change trend according to the differential of the circulating current to time.

Different from the applications proposed in the existing literatures, the control strategy introduced in this paper is to be applied into a commercial modular UPS based on parallel inverters terminated with *LC* filters. Unlike the grid-connected applications, an *LC* filter is applied instead of *LCL* filter, which can lower the cost and increase the power density with a smaller volume. In addition, the second target is to maximize system flexibility, so that it should work as a three-phase system, but it should be able to operate as a single-phase or two phases system as well. Thanks to this flexibility, maintenance becomes easier and single-phase tests are feasible, which are important features of such a product. The control under three-phase stationary coordinates is implemented for this purpose, which can reduce the overall resource consumption of the digital signal processor (DSP) since the coordinate transform is not required.

For the modular UPS project, particular control strategies should be developed. The basic control diagram is based on the decentralized droop and the virtual impedance control. Considering the *LC* filter and the purpose of simplifying the control scheme as mentioned above, the reverse droop (*P-V* and *Q-f* scheme) function is adopted instead of the conventional droop method (*P-f* and *Q-V* scheme) [12]. For the requirement of resistive output impedance, a virtual resistance loop is adopted. However, with the virtual impedance only, it is not enough to reach another important target, which is the average active power sharing between the power modules. Note that a poor power sharing performance will lead to serious circulating current problem and may cause different current stress on the switching devices, then significantly decrease the system efficiency and lifetime of modules whose output power are higher. Further, direct currents flowing from one module to another may cause active power absorption in some modules, which may contribute to dc-link voltage raises in UPS' with unidirectional rectifiers [33]. Hence, average active power sharing is necessary when considering modular UPS'.

In real applications, like the modular UPS, even though using the same models, there is an unavoidable mismatch between output impedances of the converter modules that may produce differences between them. In addition, offsets and gain errors may occur in the analog acquisition of the currents and voltages, while DSP clocks also present frequency drifts due to imperfection, which result in active and reactive power inaccuracies. Further, these differences will cause problems in some cases, such as the preset value of the virtual impedance and voltage references, which are considered in this paper, and will influence active and reactive power sharing between the parallel modules.

In order to solve the above-mentioned issues, this paper presents a new distributed adaptive virtual impedance control (DAVIC) strategy. The adaptive virtual impedance is calculated by the difference between the local active power of the module and the average active power of all the modules, then it is added to a preset virtual impedance to tune the output impedances of the power modules. With the proposed DAVIC, the total virtual impedance is not a constant value; it will be adjusted automatically by the difference of local active power and average active power of all the modules. It can be sure, at any time, the total active power can be average shared between the parallel converters, so there will be no current flowing from one module to another to keep the safety of the dc links. The active power information is being shared through the low bandwidth CAN bus on the real UPS system for the realization of the distributed control, which can improve the reliability of droop control and solve the single point failure of the centralized control fashion [27].

Compared with the conventional virtual impedance control and the existing adaptive virtual impedance control, the contribution of this paper is to propose an adaptive virtual impedance control for a modular UPS product. With the proposed method, it can reduce both the cost of the power plant and the control unit by choosing a cheaper digital controller. Simulations using PLECS and experiments on a real modular UPS platform have been developed. In both the simulation and experiments, unbalanced set of virtual impedances are intentionally programmed in order to simulate different output impedance values of different power modules and to imitate the inner offset of the DSPs.

The rest of this paper is organized as follows. In Section II, the concept of the traditional droop method and the virtual impedance loops are briefly introduced. In Section III, the idea

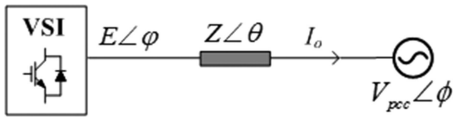

Fig. 2. Equivalent circuit of a VSI connected to an ac bus.

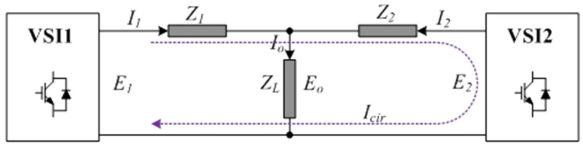

Fig. 3. Equivalent circuit of two parallel inverters.

of the proposed DAVIC is introduced, the design guideline of the adaptive virtual impedance control parameters and the stability analysis are also provided. In Section IV, simulation results are presented, which verify the effectiveness of the proposed approach. Experimental verification in an industrial modular UPS platform is presented in Section V. The conclusions are given in Section VI.

II. Review of the Conventional Droop Method and the Virtual Impedance Control

In this section, the basic concept of the droop and virtual impedance framework is reviewed. This is one of the most popular ways of control the paralleling UPS inverters [3], [9], [12], [13], [18]–[22]. Each of the inverters operate as a voltage source. In order to analyze the conventional approach, a VSI connected to an ac bus can be simply drawn as in Fig. 2. Thus, the power injected into the ac bus from the VSI is given by [28], [29]

$$P = \frac{EV_{\rm pcc}}{Z}\cos(\theta-\varphi) - \frac{{V_{\rm pcc}}^2}{Z}\cos\theta \tag{1}$$

$$Q = \frac{EV_{\rm pcc}}{Z}\sin(\theta-\varphi) - \frac{{V_{\rm pcc}}^2}{Z}\sin\theta \tag{2}$$

where E and $V_{\rm pcc}$ are the amplitude of the inverter output voltage and the ac bus voltage, φ is the power angle of the inverter, and Z and θ represent the amplitude and the phase of the output impedance. Conventionally, the output impedance is considered highly inductive, which is often obtained with a large filter inductor connected to the ac bus [30]. In this case and assuming that the output impedance is purely inductive ($\theta = 90^\circ$), the active and reactive power expressions can be simplified as

$$P = \frac{EV_{\rm pcc}}{Z}\sin\varphi \tag{3}$$

$$Q = \frac{EV_{\rm pcc}}{Z}\cos\varphi - \frac{{V_{\rm pcc}}^2}{Z}. \tag{4}$$

The output impedance of the closed-loop inverter determines the droop control strategy [12]. Normally, the power angle φ is very small, ($\sin\varphi \approx \varphi$, $\cos\varphi \approx 1$), then the active power P is mainly related with φ, and the reactive power Q is mainly influenced by the voltage error $(E - V_{\rm pcc})$ [12], [23]. Thus, the conventional droop scheme $P-\omega$ and $Q-V$ is often used, so that the voltage and frequency droop functions are given as [2], [12]

$$E = E^* - m_q Q \tag{5}$$

$$\omega = \omega^* - m_p P \tag{6}$$

in which ω^* and E^* represent the frequency and voltage amplitude references, respectively, m_p and m_q are the droop coefficients [2], [8], [12]. Similarly, for a highly resistive output impedance ($\theta = 0^\circ$), the active and reactive power can be calculated as

$$P = \frac{EV_{\rm pcc}}{Z}\cos\varphi - \frac{{V_{\rm pcc}}^2}{Z} \tag{7}$$

$$Q = -\frac{E{V_{\rm pcc}}^2}{Z}\sin\varphi. \tag{8}$$

Different from the conventional droop, the droop function should be modified as [12], [31], and [32]

$$E = E^* - m_p P \tag{9}$$

$$\omega = \omega^* + m_q Q. \tag{10}$$

Thus, the active power can be controlled by the inverter output-voltage amplitude while the reactive power can be regulated by the inverter frequency, which is the opposite strategy of the conventional droop, it is also named as reverse droop [31], [32]. More details about the choice of droop function and the analysis of output impedance can be found in [12], [28], [33], [35], and [36].

As the output impedance plays an important role for the choice of the droop function, and for the conventional droop control scheme, a highly inductive output impedance is required to decouple the influence of P and Q to the frequency and voltage amplitude [12], [28]. Typically, an *LCL* filter will be connected the inverter to the common ac bus. As discussed in the introduction, virtual impedance can be added to adjust the output impedance. The parallel three-phase inverters considering the output impedances can be simplified as Fig. 3 because of the similar principle of three-phase and single-phase inverters.

In Fig. 3, Z_1 and Z_2 are the output impedances of the two parallel inverters, respectively, Z_L is the load impedance, E_1 and E_2 are the output voltages of the two inverters, I_1 and I_2 are the output currents, E_o is the common as bus voltage, and I_o is the load current. In a practical system, Z_1 and Z_2 will be unbalanced because of the different values of filters and line impedances or stray parameters. According to the literature [34], the circulating current can be defined as

$$I_{\rm cir} = \frac{I_1 - I_2}{2}. \tag{11}$$

As shown in Fig. 3, the following equations can be written:

$$I_1 = \frac{E_1 - E_o}{Z_1} \tag{12}$$

$$I_2 = \frac{E_2 - E_o}{Z_2}. \tag{13}$$

Assuming that the output impedances of the parallel inverters are equal to each other, $Z_1 = Z_2 = Z$, then substituting (12),

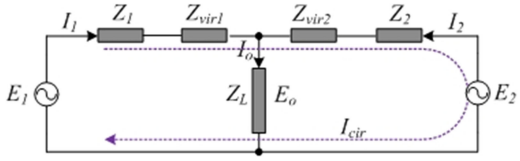

Fig. 4. Equivalent circuit of two parallel inverters with virtual impedances.

(13) into (11) gives us

$$I_{\rm cir} = \frac{E_1 - E_2}{2Z}. \tag{14}$$

Based on the former analysis, if the output voltages and the output impedances of the parallel inverters are equal to each other, respectively, the circulating current can be eliminated to obtain the target of average power sharing. The equivalent circuit of two parallel-connected inverters with virtual impedances is shown in Fig. 4, $Z_{\rm vir1}$ and $Z_{\rm vir2}$ are the virtual impedances

$$Z_{\rm virk} = jX_{\rm virk} + R_{\rm virk} \tag{15}$$

Equation (15) depicts the virtual impedance for the kth inverter in a system. The virtual impedance can be purely resistive, inductive or a combination with two of them based on the output impedance differences between parallel inverters.

III. Distributed Adaptive Virtual Impedance Control (DAVIC)

A. Proposed DAVIC Method

In the UPS project that discussed in this paper, the *LC* filter is applied instead of an *LCL* filter, then the line impedance is mainly resistive in the low-voltage line [35], [36]. Thus, in coherence with the line impedance, a virtual resistive impedance is selected, consequently the reverse droop (9), (10) is implemented. For the purpose of improving the active power sharing accuracy between parallel converter modules, an adaptive virtual impedance control is proposed, which is realized by using a distributed control concept as shown in Fig. 5. The adaptive virtual impedance is calculated by the difference between the active powers between the power modules in the UPS. In that figure, $R_{\rm vir\_pre}$ is the preset virtual impedance; $R_{\rm vir\_adp}$ is the adaptive virtual impedance, so that the final virtual impedance per power module will be $R_{\rm vir\_pre} + R_{\rm vir\_adp}$.

Assuming that there are a number of *n* power modules that operate in parallel in a modular UPS, the control scheme considering the adaptive virtual impedance control is shown in Fig. 5. The calculation of the adaptive virtual impedance can be expressed as

$$R_{\rm vir\_adp} = (P_i - P_{\rm av})\left(K_{P\rm adp} + \frac{K_{I\rm adp}}{s}\right), P_{\rm av} = \frac{1}{n}\sum_{i=1}^{n} P_i. \tag{16}$$

The local active power P_i (i = 1 to n) will be compared with the average active power $P_{\rm av}$ of the paralleled modules in the UPS. Then, through the PI controller, the adaptive virtual impedance $R_{\rm vir\_adp}i$ (i = 1 to n) is obtained. The reason of P_i in the position of minuend is that, suppose that P_i is higher than the average active power of the parallel-connected modules, it means the virtual impedance of the ith module should increase to reduce the output power of P_i. In Fig. 5, $R_{\rm vir\_adp}i$ will be positive through the calculation using (16), so the final total virtual impedance of ith module will increase, which demonstrates the correct compensation direction. The whole control diagram of a modular UPS with the proposed adaptive virtual impedance control is shown in Fig. 6.

B. Design of the Control Parameters of the Adaptive Virtual Impedance Loop

In order to give a design guideline of the parameters of the adaptive virtual impedance control, a simple model considering two parallel-connected inverters is built, which is shown in Fig. 7. R_{D1} and R_{D2} represent the virtual impedance, which consist the adaptive virtual impedance. $R_{\rm line1}$ and $R_{\rm line2}$ represent the line impedances, only resistive line impedance is considered since it is mainly resistive in low-voltage line [35], [36].

Based on Fig. 7, when considering both of the adaptive virtual impedance and the line impedance, (12) and (13) will be changed as

$$I_1 = \frac{E_1 - E_o}{R_{D1} + R_{\rm line1}} \tag{17}$$

$$I_2 = \frac{E_2 - E_o}{R_{D2} + R_{\rm line2}}. \tag{18}$$

If $I_1 = I_2$, the following is obtained:

$$\frac{E_1 - E_o}{R_{D1} + R_{\rm line1}} = \frac{E_2 - E_o}{R_{D2} + R_{\rm line2}} \tag{19}$$

$$\frac{E_1 - E_o}{E_2 - E_o} = \frac{R_{D1} + R_{\rm line1}}{R_{D2} + R_{\rm line2}} = \frac{(P_1 - P_{\rm av})(K_{P\rm adp} + K_{I\rm adp}/s) + R_{\rm pre1} + R_{\rm line1}}{(P_2 - P_{\rm av})(K_{P\rm adp} + K_{I\rm adp}/s) + R_{\rm pre2} + R_{\rm line2}}. \tag{20}$$

We consider $R_{\rm pre1}$ and $R_{\rm line1}$ as one parameter R_{l1}, $R_{\rm pre2}$, and $R_{\rm line2}$ as R_{l2}; $(E_1 - E_o)$ and $(E_2 - E_o)$ are represented by δ_{E1}, δ_{E2}, respectively; δ_{P1} and δ_{P2} are used to substitute $(P_1 - P_{\rm av})$ and $(P_2 - P_{\rm av})$. Then, (20) will be rewritten as

$$\frac{\delta_{E1}}{\delta_{E2}} = \frac{R_{D1} + R_{\rm line1}}{R_{D2} + R_{\rm line2}} = \frac{\delta_{P1}(K_{P\rm adp} + K_{I\rm adp}/s) + R_{l1}}{\delta_{P2}(K_{P\rm adp} + K_{I\rm adp}/s) + R_{l2}}. \tag{21}$$

From (21), the following relationship will be obtained:

$$\delta_{E1} = \delta_{P1}(K_{P\rm adp} + K_{I\rm adp}/s) + R_{l1} \tag{22}$$

$$\delta_{E2} = \delta_{P2}(K_{P\rm adp} + K_{I\rm adp}/s) + R_{l2}. \tag{23}$$

In order to simplify the design, we consider only proportional control first, and $R_{l1} = R_{l2} = 0$ in ideal condition. Thus, (22) will be rewritten as

$$\delta_{E1} = \delta_{P1} K_{P\rm adp}. \tag{24}$$

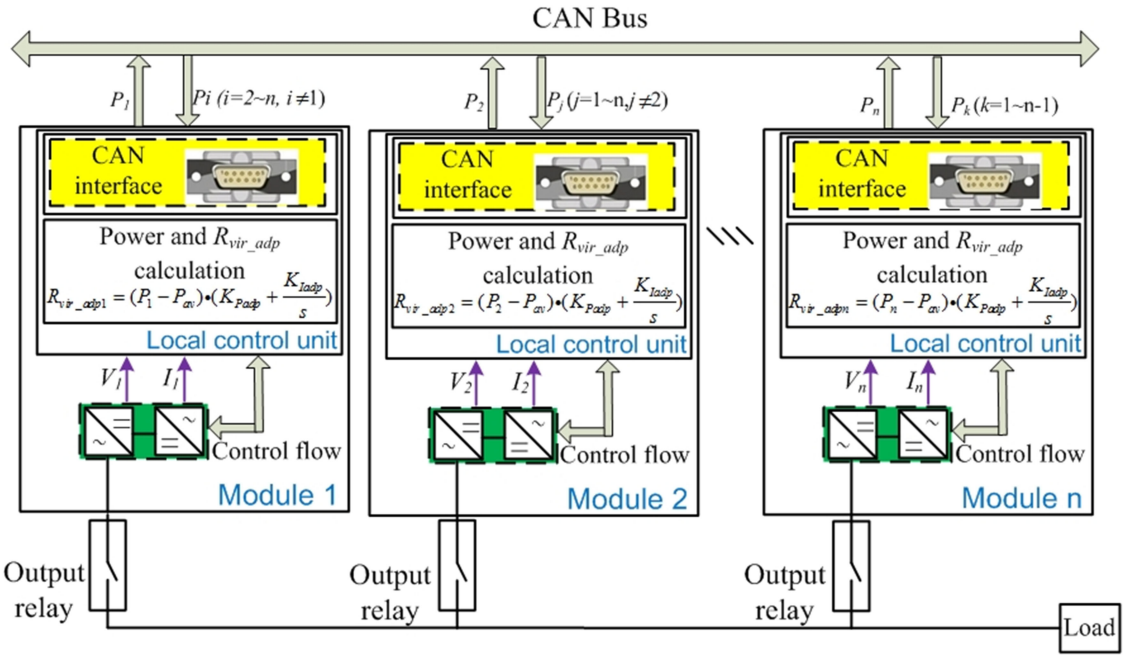

Fig. 5. Control scheme for a number *n* modules in a modular UPS system.

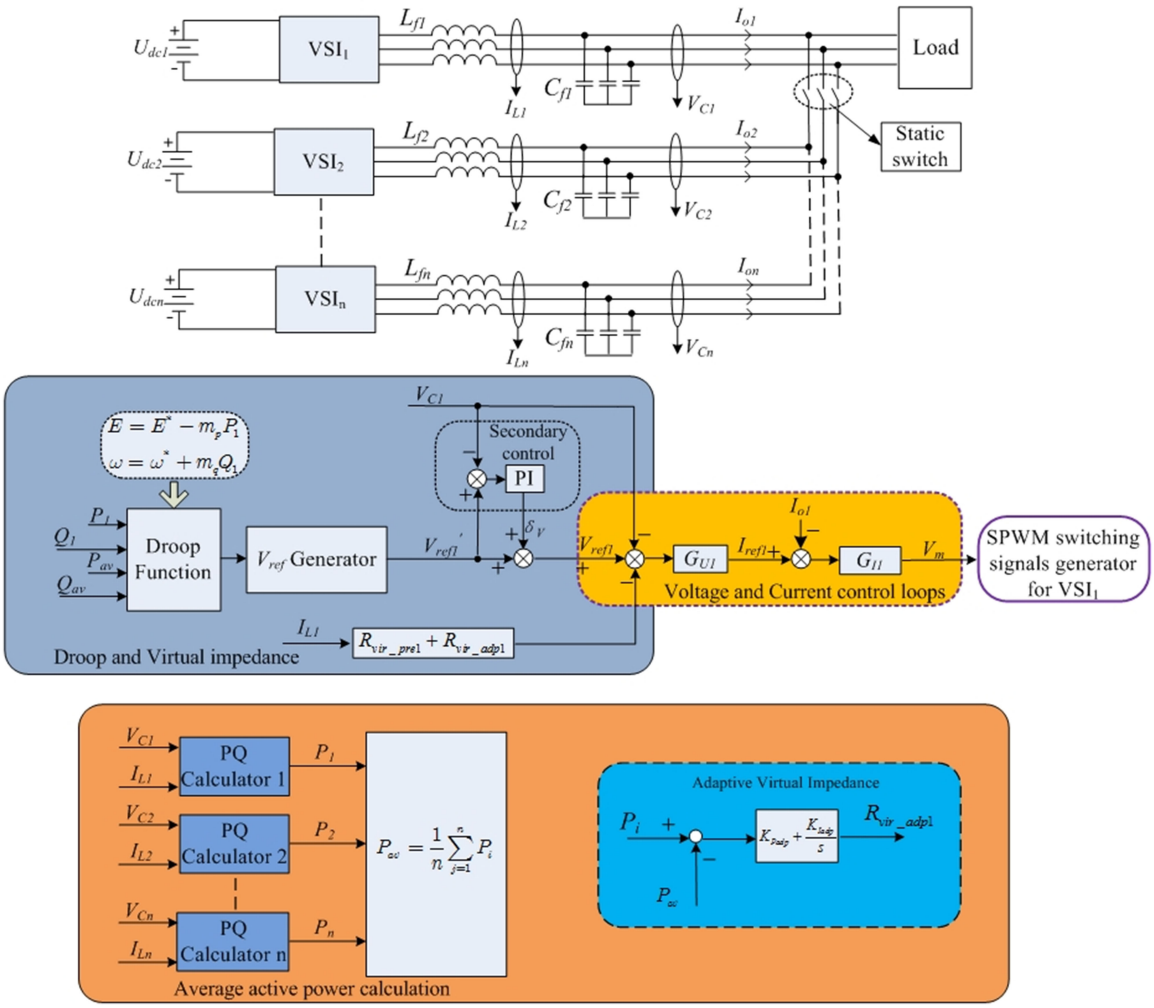

Fig. 6. Block diagram of the control structure with the adaptive virtual impedance control.

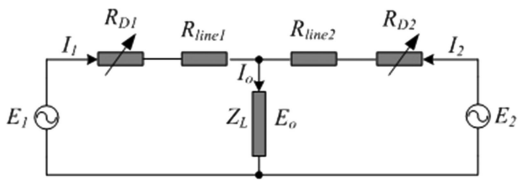

Fig. 7. Equivalent circuit when two inverters connected in parallel.

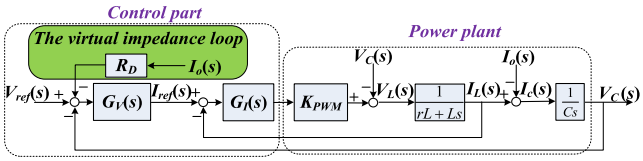

Fig. 8. Linear model of voltage and current control loops with virtual impedance.

Thus, with (25), we can calculate $K_{P\text{adp}}$, in which V_{ref} represents the reference voltage, η is a number of percentage, which represents the maximum difference between the real output voltage and the reference voltage that allowed for safety running of the system; and $P_{\max}$ is the maximum power of each power module

$$K_{P\text{adp}} = \frac{\delta_{E1}}{\delta_{P1}} = \frac{V_{\text{ref}}\eta}{P_{\max}/3}. \tag{25}$$

In the modular UPS project that discussed in this paper, the allowed maximum of η is 2%. The maximum active power $P_{\max}$ for each module in the simulation is 10 kW. Thus, in the extreme condition, for each phase, $K_{P\text{adp}}$ can be calculated as 0.00138. Normally a low-pass filter $\frac{\omega_f}{s+\omega_f}$ is implemented with the power calculation, in which ω_f is the cutoff frequency that normally smaller than a decade of the fundamental frequency [20], [33]. Based on the experience relationship between proportional and integral parameter, $K_{I\text{adp}}$ equals to $\frac{K_{P\text{adp}}}{\tau}$, τ is a time constant, here it mainly comes from the low-pass filter. In this paper, the cutoff frequency is selected as 2 Hz, then $K_{I\text{adp}}$ will be obtained as

$$K_{I\text{adp}} = \frac{K_{P\text{adp}}}{\tau} = \frac{0.00138}{1/2} = 0.00276. \tag{26}$$

Thus, with (25) and (26), we can calculate the approximate control parameters for the proposed DAVIC. It should be noticed that optimized parameters will be obtained further based on the simulation and experiments. The control parameters that used in the paper are shown in Table I, it can be seen that the optimized parameters for the DAVIC are close to the calculated values.

C. Selection of Virtual Impedance and the Stability Analysis

Since the output impedance will influence the performance of the droop characteristic, it is necessary to analyze the selection of virtual impedance by using the proposed DAVIC method. A limit of the total virtual impedance will be set in the controller to guarantee the stability of the system. The linear model of voltage and current control loops without virtual impedance is shown in Fig. 8, in which, $G_V(s)$ and $G_I(s)$ represent the voltage and current controller, respectively.

TABLE I
ELECTRICAL AND CONTROL PARAMETERS IN SIMULATIONS AND EXPERIMENTS

Coefficient	Parameter	Value
Voltage reference (RMS)	V_{ref}	230 V/50Hz
Filter inductor	L	200 μH
Filter capacitor	C	60 μF
Equivalent resistor of filter inductor at 50Hz	rL	0.0628 Ω
Voltage proportional controller	K_{PV}	0.8 A/V
Voltage resonant controller	K_{RV}	1000 As/V
Current proportional controller	K_{PI}	1.25 V/A
Current resonant controller	K_{RI}	600 Vs/A
Preset virtual impedance	R_D	0.5 Ω
Active power droop coefficient	m_P	0.00005 V/W
Reactive power droop coefficient	m_Q	0.00001 Hz/Var
Proportional controller of the adaptive virtual impedance control	K_{Padp}	0.002 V/W
Integral controller of the adaptive virtual impedance control	K_{Iadp}	0.004 V/Ws
Proportional controller of the secondary control	K_{Psec}	0.01
Integral controller of the secondary control	K_{Isec}	3.2
Total load power in the simulation	--	20 kW
Total load power in the experiment	--	24.75 kW
Digital controller	--	TMS320F28377D
Normal communication cycle for data exchange between power modules	T_c	20 ms

Defining the voltage and current controllers as

$$G_V(s) = K_{PV} + \frac{K_{RV}s}{s^2+\omega^2} \tag{27}$$

$$G_I(s) = K_{PI} + \frac{K_{RI}s}{s^2+\omega^2}. \tag{28}$$

From Fig. 8, the close-loop transfer function of the conventional voltage and current control without the virtual impedance loop can be derived as

$$V_C(s) = G(s)\cdot V_{\text{ref}}(s) - Z_0(s)\cdot I_o(s) \tag{29}$$

in which, $Z_0(s)$ represents the output impedance

$$Z_0(s) = \frac{As^5 + Bs^4 + Ds^3 + Es^2 + Fs + G}{as^6 + bs^5 + cs^4 + ds^3 + es^2 + fs + g} \quad (30)$$

being

$$\begin{aligned}
A &= L \\
B &= rL + K_{PI}K_{\mathrm{PWM}} \\
D &= 2\omega^2 L + K_{RI}K_{\mathrm{PWM}} \\
E &= 2\omega^2 rL + 2\omega^2 K_{PI}K_{\mathrm{PWM}} \\
F &= \omega^4 L + \omega^2 K_{RI}K_{\mathrm{PWM}} \\
G &= \omega^4 rL + \omega^4 K_{PI}K_{\mathrm{PWM}} \quad (31) \\
a &= LC \\
b &= (rL + K_{PI}K_{\mathrm{PWM}})C \\
c &= 2\omega^2 LC + K_{RI}K_{\mathrm{PWM}}C + K_{PV}K_{PI}K_{\mathrm{PWM}} + 1 \\
d &= 2\omega^2 rLC + 2\omega^2 CK_{PI}K_{\mathrm{PWM}} + K_{PV}K_{RI}K_{\mathrm{PWM}} \\
&\quad + K_{RV}K_{PI}K_{\mathrm{PWM}} \\
e &= \omega^4 LC + \omega^2 K_{RI}K_{\mathrm{PWM}} + 2\omega^2 K_{PV}K_{PI}K_{\mathrm{PWM}} \\
&\quad + K_{RV}K_{RI}K_{\mathrm{PWM}} + 2\omega^2 \\
f &= \omega^4 CrL + \omega^4 CK_{PI}K_{\mathrm{PWM}} + \omega^2 K_{PV}K_{RI}K_{\mathrm{PWM}} \\
g &= \omega^4 K_{PV}K_{PI}K_{\mathrm{PWM}} + \omega^2 K_{PI}K_{RV}K_{\mathrm{PWM}} + \omega^4. \quad (32)
\end{aligned}$$

When considering the virtual impedance in the control loops in Fig. 8, where R_D is the total virtual impedance that consists the preset virtual impedance and the adaptive virtual impedance, the close-loop transfer function will be

$$V_C(s) = G(s) \cdot V_{\mathrm{ref}}(s) - (Z_0(s) + G(s) \cdot R_D) \cdot I_o(s) \quad (33)$$

where

$$\begin{aligned}
Z_0{}^*(s) &= Z_0(s) + G(s) \cdot R_D \\
&= \frac{A^*s^5 + B^*s^4 + D^*s^3 + E^*s^2 + F^*s + G^*}{as^6 + bs^5 + cs^4 + ds^3 + es^2 + fs + g} \quad (34)
\end{aligned}$$

being

$$\begin{aligned}
A^* &= A \\
B^* &= B + K_{PI}K_{PV}K_{\mathrm{PWM}}R_D \\
D^* &= D + K_{PI}K_{RV}K_{\mathrm{PWM}}R_D + K_{RI}K_{PV}R_D \\
E^* &= E + 2\omega^2 K_{PI}K_{PV}K_{\mathrm{PWM}}R_D + K_{RI}K_{RI}R_D \\
F^* &= F + \omega^2 K_{PI}K_{RV}K_{\mathrm{PWM}}R_D + \omega^2 K_{RI}K_{PV}R_D \\
G^* &= G + \omega^4 K_{PI}K_{PV}K_{\mathrm{PWM}}R_D. \quad (35)
\end{aligned}$$

In order to have a better performance of the parallel operation, the output impedance of the closed-loop control for the inverter should be examined. Fig. 9 shows the frequency-domain behavior of the output impedance through the Bode diagram [12]. As it can be seen, the impedance is highly resistive around the frequency range of interest that encloses the line frequency [12].

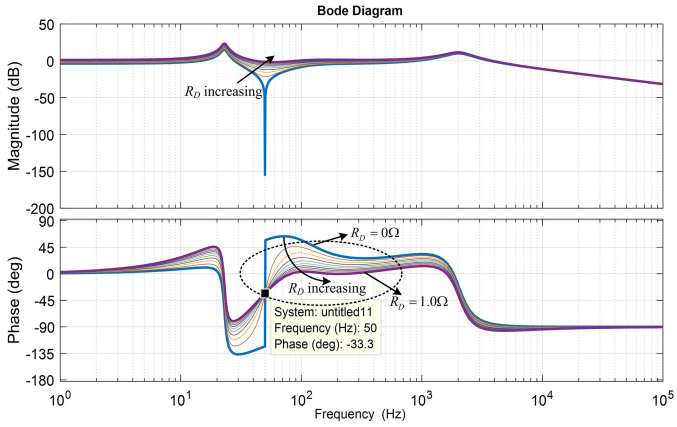

Fig. 9. Bode diagram of the output impedance $R_D = 0 \sim 1\,\Omega$ with increment of 0.1 Ω.

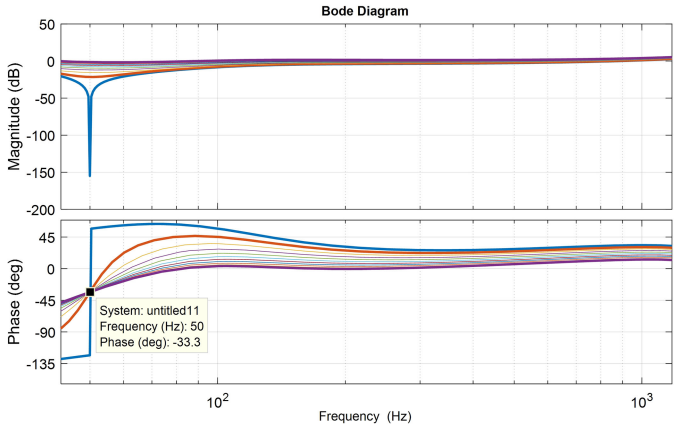

Fig. 10. Zoomed-in Bode diagram of the output impedance around 50 Hz.

The zoomed-in Bode diagram around this range is shown in Fig. 10.

It can be noticed that with the range of virtual impedance (from 0.1 to 1.0 Ω), the frequency-domain behavior of the output impedance through the Bode diagram is nearly resistive, which is suitable to adopt the reverse droop function for the proposed adaptive virtual impedance control. An interesting phenomenon is that at 50 Hz the phase degree will always cross a point around –33° for any virtual impedance value. Fig. 11 shows the Bode diagram of the output impedance with the range of virtual impedance values from 1.0 to 10.0 Ω. It can be noticed that when the virtual impedance is bigger than 1.0 Ω, the trend of the degree of the virtual impedance will be lower than 0°. Based on the analysis of the output impedance of the close loop, the total virtual impedance can be selected around 1.0 Ω. A highly resistive output impedance will be obtained, which is suitable for the reverse droop function adopted in this paper. The limit range of the total virtual impedance used in this paper was chosen between 0.3 and 1.1 Ω, which shows a good performance of the average power sharing. Notice that for $R_D = 0\,\Omega$, phase is sharped changed due to the PR controller effect, while increasing R_D, phase changes became flatter.

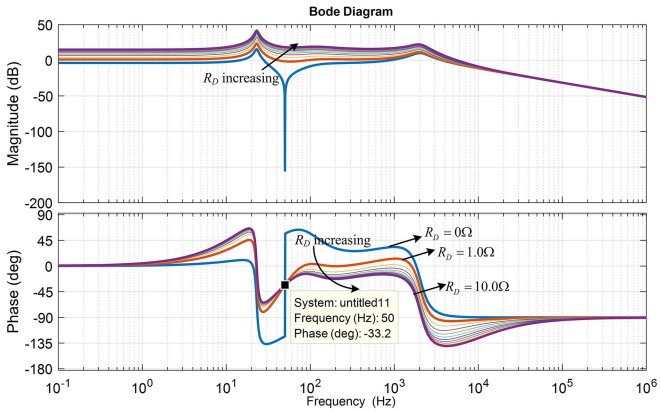

Fig. 11. Bode diagram of the output impedance $R_D = 0 \sim 10\,\Omega$ with increment of 1.

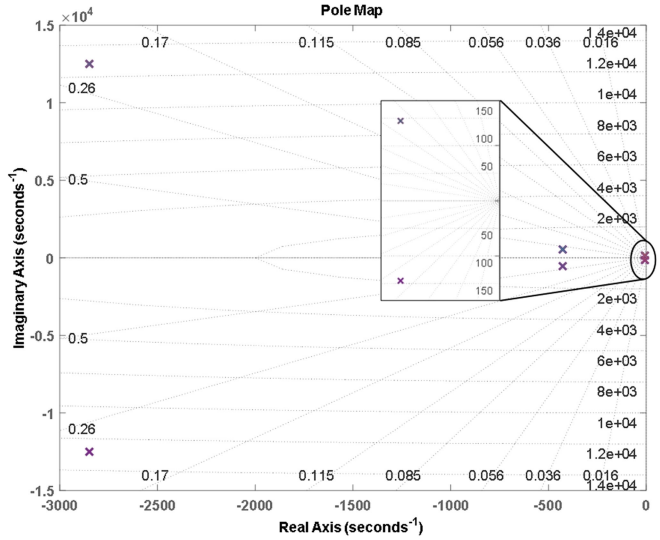

Fig. 12. Pole map of the characteristic function.

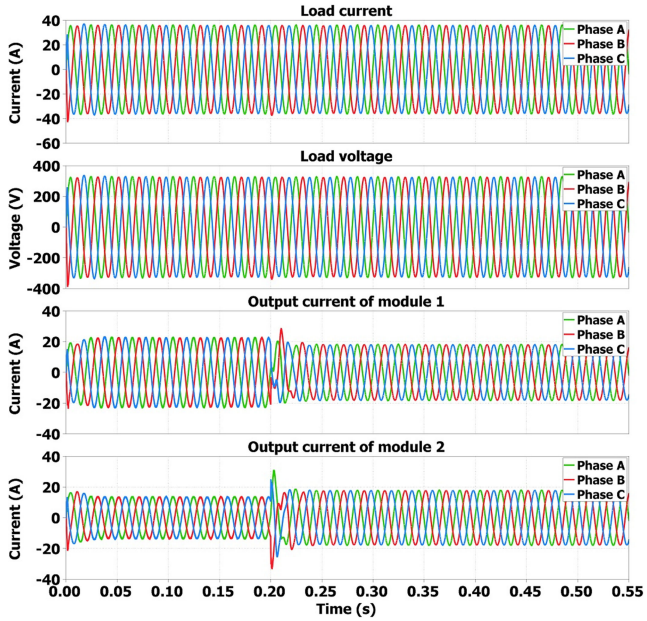

Fig. 13. Simulation results when the adaptive virtual impedance control was enabled at $t = 0.2$ s.

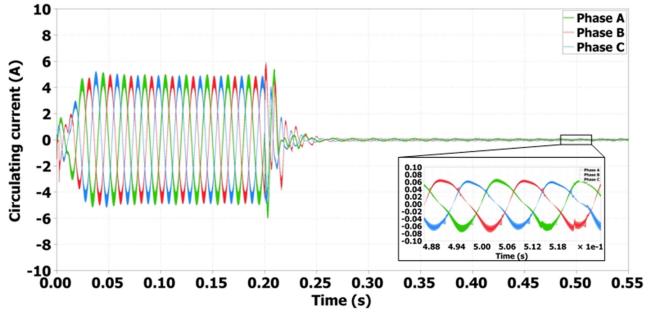

Fig. 14. Circulating current between the two modules.

For the system stability analysis, the characteristic function of the system can be obtained from (34)

$$H(s) = as^6 + bs^5 + cs^4 + ds^3 + es^2 + fs + g. \qquad (36)$$

As shown in (32) and (36), the virtual impedance and the adaptive virtual impedance controller are not shown in the characteristic function, thus, it will not influence the stability of the system. From the pole map of the characteristic function that shown in Fig. 12, the system will remain stable.

IV. Simulation Results

In order to verify the effectiveness of the proposed adaptive virtual impedance control, a UPS model consists of two inverter modules was built in PLECS. Different preset virtual impedance was used in the simulation to analyze system dynamics when considering unbalanced output impedances.

A. Performance Verification of the Proposed Adaptive Virtual Impedance Control

1) Different Preset Virtual Impedance to Mimic Unbalanced Output Impedances: In this simulation, the preset virtual impedance values were 0.3 Ω for module 1 and 0.5 Ω for module 2, which imitated unbalanced output impedances. The adaptive virtual impedance control was enabled at $t = 0.2$ s to see the effect of the proposed approach. From Figs. 13 to 16, we can notice that by using the proposed control, a better average active and reactive power sharing performances are obtained under unbalanced output impedances. From Fig. 16, it can be seen that the total virtual impedances of the parallel modules are close to each other once the adaptive virtual impedance control is enabled, and the peak value of the circulating current between the two modules is around 60 mA. In Fig. 15, we can see that the power can be approximately average shared between the parallel modules.

2) Different Preset Voltage References to Mimic the Offset in Different Digital Controllers: Different preset voltage refer-

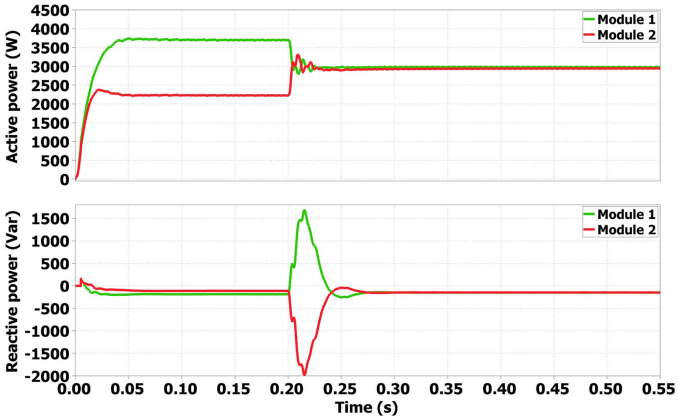

Fig. 15. Active and reactive power on Phase A of the two modules.

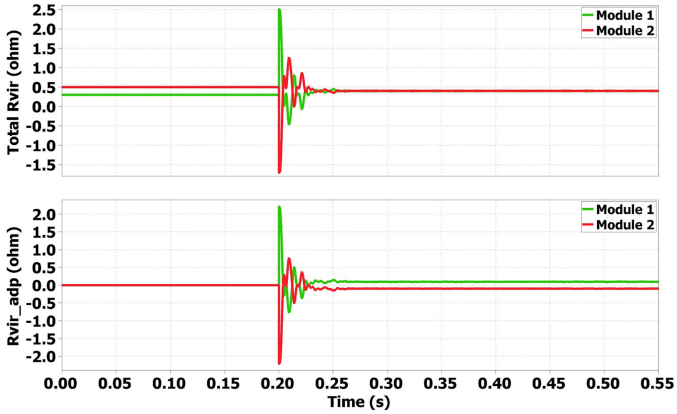

Fig. 16. Total value of virtual impedance and the value of the adaptive virtual impedance for the two modules.

TABLE II
PARAMETERS SETTING OF DIFFERENT CASES

	Voltage Reference
Module 1	230*1.01V(RMS)
Module 2	230V(RMS)

ences are applied for the parallel-connected modules to simulate the offset of different digital controllers. Details are shown in Table II. Although the condition of different set of voltage references will not happen in the real application, however, voltage offset and gains of different hardware platforms will exist.

In this case-study, the adaptive virtual impedance was enabled at $t = 0.1$ s, Module 2 was disconnected at $t = 0.2$ s, and then reconnected at $t = 0.4$ s. From the results in Figs. 17 to 19, it can be seen that the average power sharing performance is obtained by using the proposed adaptive virtual impedance. From the result of the dynamic test, though there is distortion in the output current of the two power modules during the transient time at 0.4 s, the current and voltage at the load side are quite stable.

B. Dynamic Performance Test Under Different Output Impedances

To further verify the effectiveness of the presented DAVIC, more dynamic test is performed in this section. The preset virtual

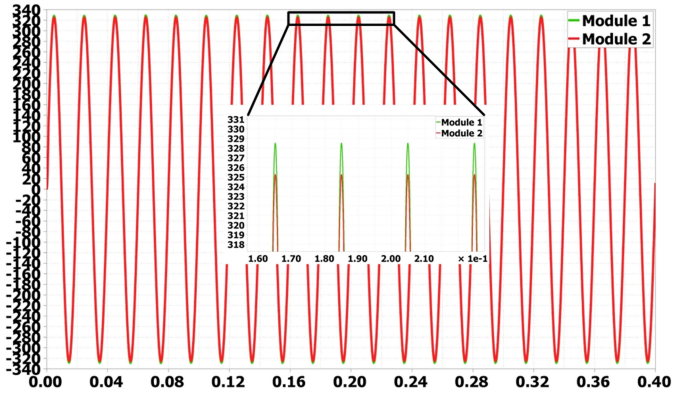

Fig. 17. Voltage references of the two modules.

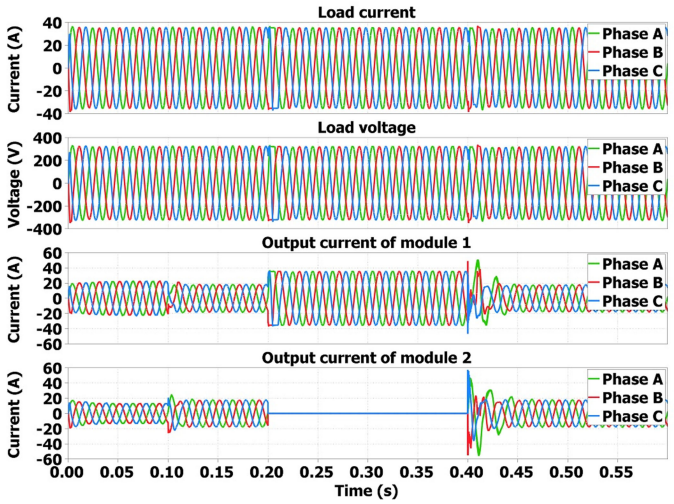

Fig. 18. Simulation results with different preset voltage references.

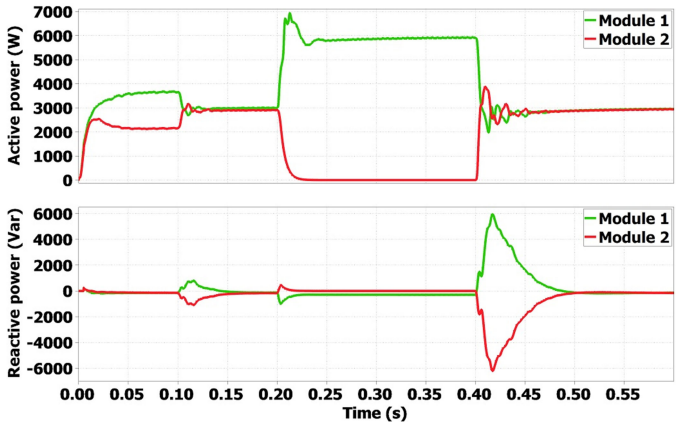

Fig. 19. Active and reactive power of the two modules.

impedances for both modules were 0.3 and 0.5 Ω, respectively, to emulate the condition of unbalanced output impedances of the parallel modules.

1) Conventional Virtual Impedance Control Method: In the dynamic test, module 2 was disconnected at $t = 0.15$ s, and then it was suddenly reconnected at $t = 0.25$ s. From the results

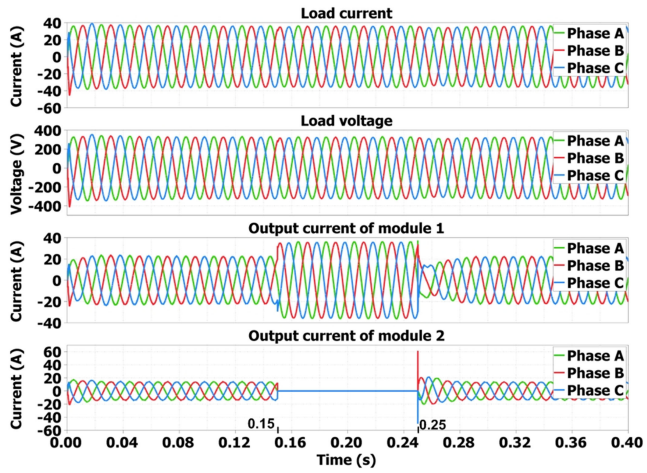

Fig. 20. Simulation results suing the conventional virtual impedance control.

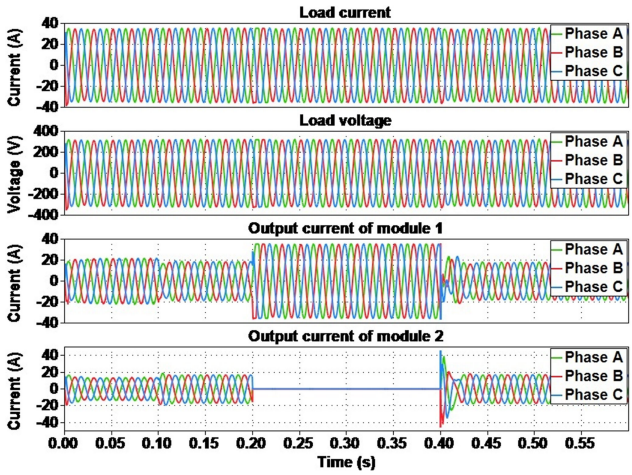

Fig. 22. Voltage and current waveforms of the dynamic test.

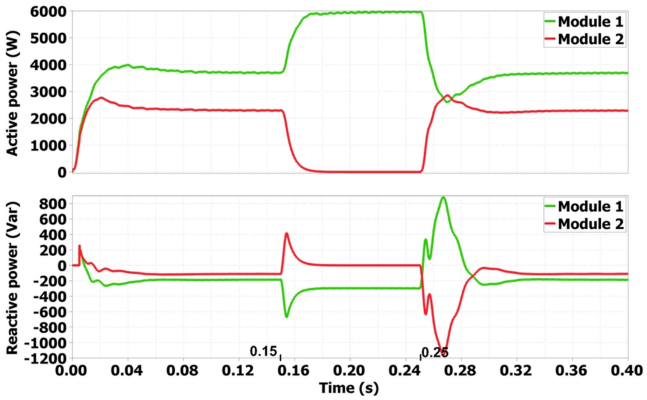

Fig. 21. Active and reactive power using the conventional virtual impedance control.

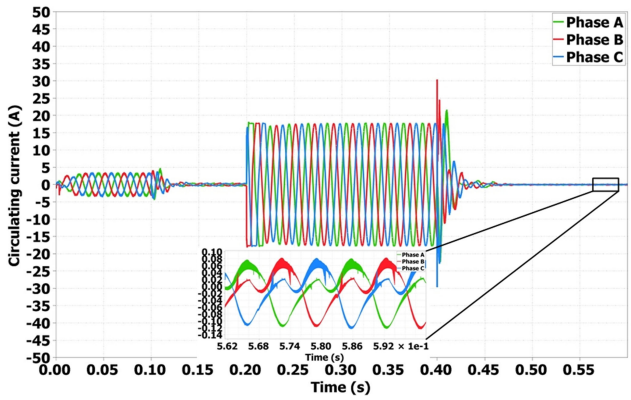

Fig. 23. Circulating current between the two modules of the dynamic test.

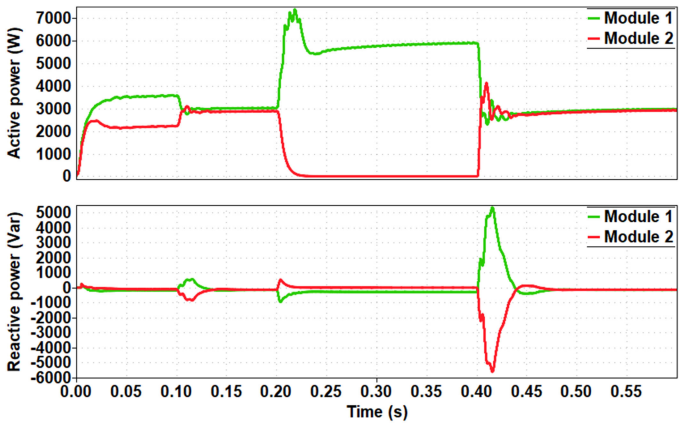

Fig. 24. Active and reactive power on Phase A of the two modules during the dynamic test.

shown in Figs. 20 and 21, it can be seen that, once the output impedances of the parallel modules are unbalanced, the power cannot be properly shared by using the conventional virtual impedance control.

2) Proposed DAVIC: In the simulation, the DAVIC is enabled at $t = 0.1$ s, Module 2 was disconnected at $t = 0.2$ s, and reconnected at $t = 0.4$ s. From results in Figs. 22 to 24, we can notice that compared to Figs. 20 and 21, average power sharing performance is obtained during the dynamic test by using the proposed DAVIC. In Fig. 25, we can see that the total virtual impedance of the parallel modules will be close to each other once the DAVIC is enabled, which will lead to balanced output impedances. Thus, the power sharing performance will be enhanced. During the transient time within two fundamental cycles, distortion appeared in the output currents of the parallel modules. Nevertheless, the load current remained almost with no perturbation. The phenomenon of the distortion and overcurrent issue will be better in the real UPS platform because of the inherent impedance of the hardware, which can be noticed in Section V.

3) Verification of the Proposed Adaptive Virtual Impedance Control With Communication Delay: In real application, communication delay sometimes happens between the agents that need data exchange. Thus, in this section, simulation results are presented when there is communication delay between the parallel-connected power modules. Different preset virtual impedances are applied in the two modules, 0.3 Ω for Module 1 and 0.5 Ω for Module 2. Normally, the data communication cycle T_c between the modules is 20 ms. In order to verify the effectiveness of the proposed method, a communication delay

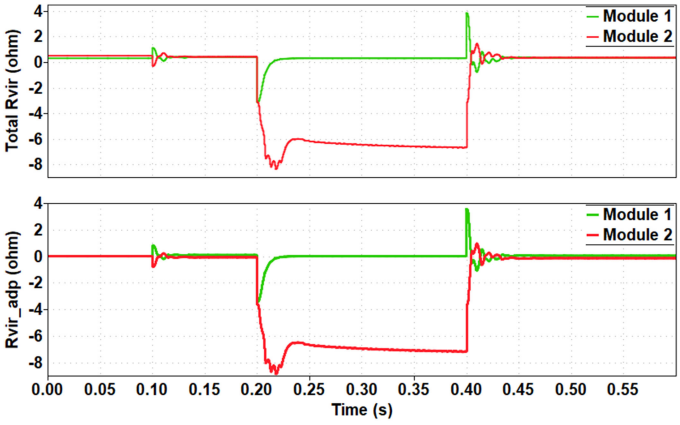

Fig. 25. Adaptive virtual impedance and the total virtual impedance of the two modules in one phase.

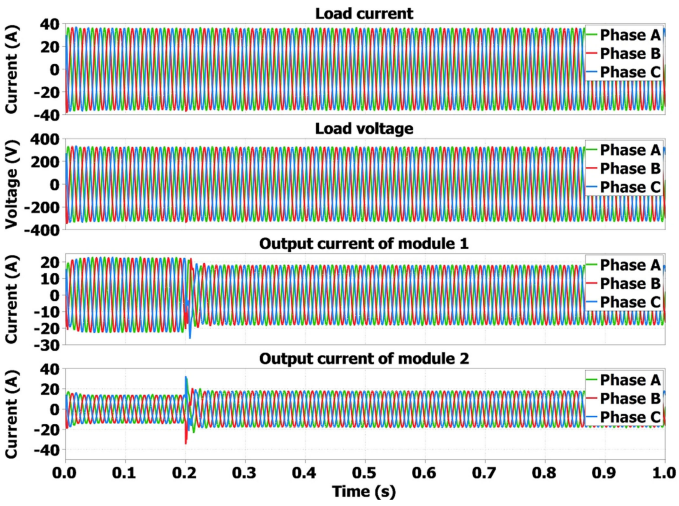

Fig. 26. Voltage and current when there is communication delay between the two modules.

is set in the Module 1 at $t = 0.6$ s, the communication cycle is changed from 20 to 40 ms, which is shown in Fig. 28. The DAVIC is enabled at $t = 0.2$ s, from the results in Figs. 26 and 27. The power sharing performance of the proposed DAVIC will not be influenced by the communication delay, since that the DAVIC control loop only need low bandwidth communication, and the data that received from the communication link will be stored in a register until it receives a new data. Thus, even there is communication delay for one module, it will only change the data update cycle in the register, the controller can still use the data that received in the previous cycle until a new data arrives.

V. Experimental Results

The preset virtual impedances for the experiments with a modular UPS platform are shown in Table III. Two different presets of unbalanced virtual impedances are applied in the experiments to verify the proposed control. The modular UPS platform is shown in Fig. 29. The Delfino 32-bit DSP from TI,

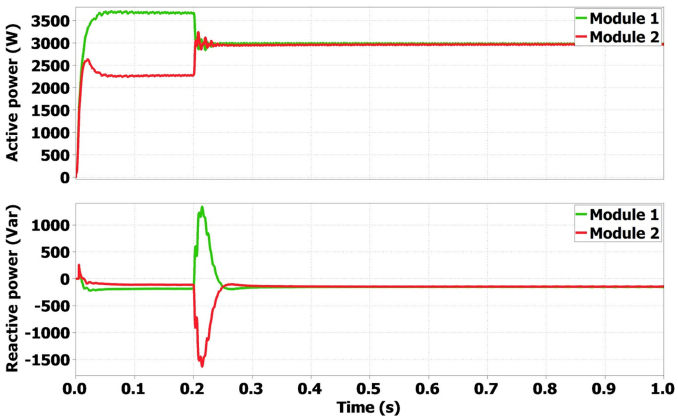

Fig. 27. Active and reactive power of Phase A when there is communication delay between the two modules.

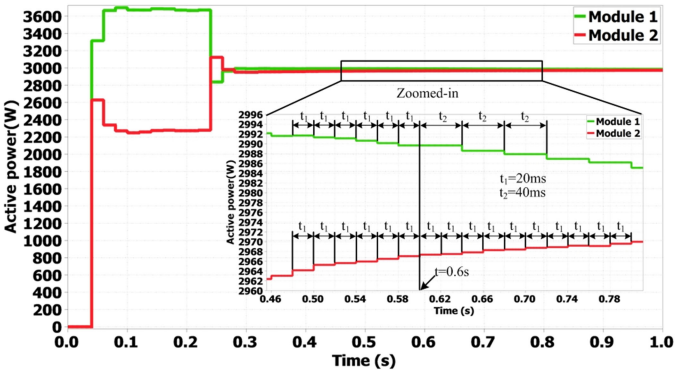

Fig. 28. Data communication delay happens between the two modules.

TABLE III
Preset Value of Virtual Impedances

	Balanced	Unbalanced preset 1	Unbalanced preset 2
Module 1	0.5Ω	0.3Ω	0.5Ω
Module 2	0.5Ω	0.5Ω	0.8Ω

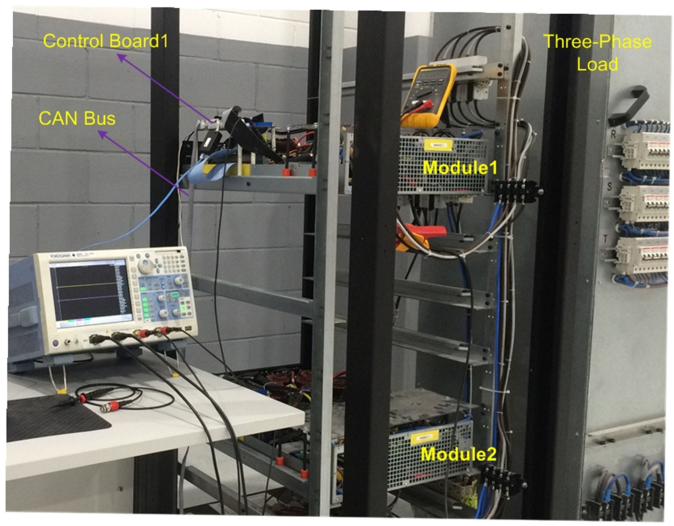

Fig. 29. Modular UPS platform (Courtesy Salicru S.A.).

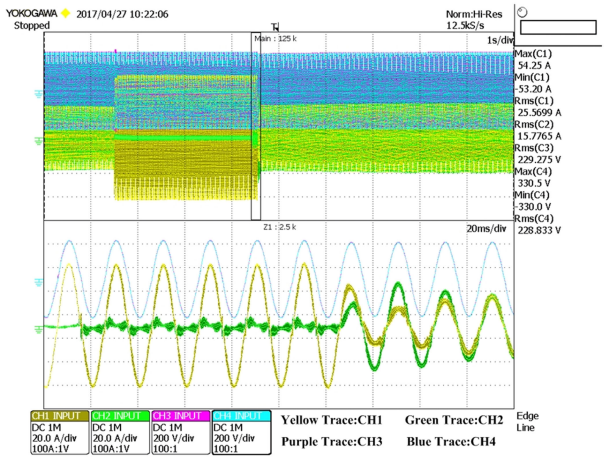

Fig. 30. Experimental results during the transient time under dynamic test, CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

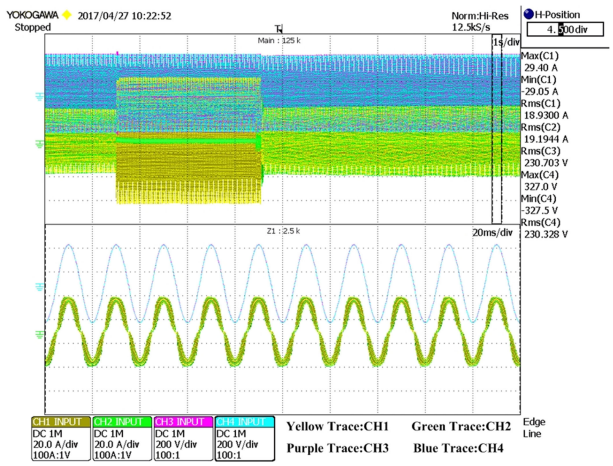

Fig. 31. Steady-state waveforms, CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

TMS320F28377D, is applied as the digital controller on the control boards.

Four case-studies were considered in the experiments:

1) Balanced preset virtual impedances using the conventional virtual impedance control,
2) Unbalanced preset virtual impedances using the conventional virtual impedance control,
3) Balanced preset virtual impedances using the proposed adaptive virtual impedance control,
4) Two different presets of unbalanced virtual impedances to verify the proposed adaptive virtual impedance control.

It should be mentioned that all the experiments are implemented with plug and play test to verify the effectiveness of the proposed method under dynamic condition, which means that one of the modules will be disconnected and reconnected to the load to see the results.

The experimental results are shown from Figs. 30 to 41. From Figs. 31 and 35, we can notice that the power sharing performance of the conventional control and the proposed DAVIC are

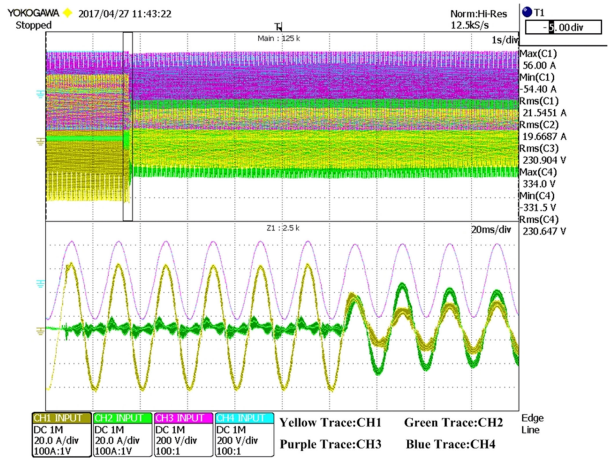

Fig. 32. Experimental results during the transient time under dynamic test using the unbalanced virtual impedance preset 1, CH1: Phase A current of Module1, CH2: Phase A current of Module2, CH3: Phase A voltage of Module 1, CH4: Phase A voltage of Module 2.

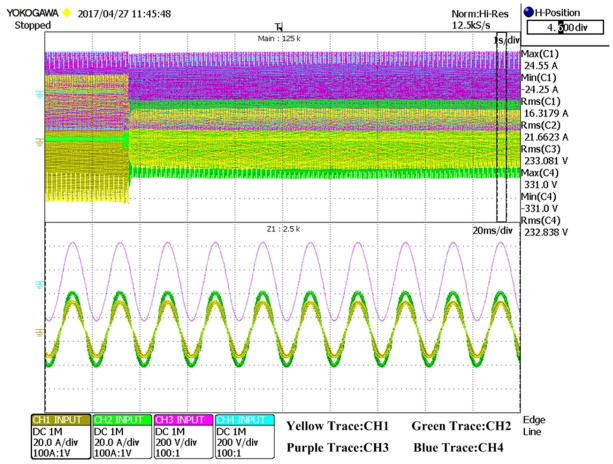

Fig. 33. Steady-state waveforms without adaptive virtual impedance, CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

almost the same under the condition of the same preset virtual impedance. However, under the condition of different preset virtual impedances that indicate different output impedances, the performance of the proposed DAVIC was much better than the conventional virtual impedance control, which are shown in Figs. 33, 38, and 41, respectively. Notice that in this case the average power sharing can still be guaranteed. More details are shown below.

A. Experimental Results With the Same Preset Virtual Impedance in the Parallel Modules Using Conventional Virtual Impedance Control

B. Experimental Results With Different Preset Virtual Impedance in the Parallel Modules Using Conventional Virtual Impedance Control

In Fig. 33, it is clearly shown that the load current cannot be averaged shared between the inverter modules using the

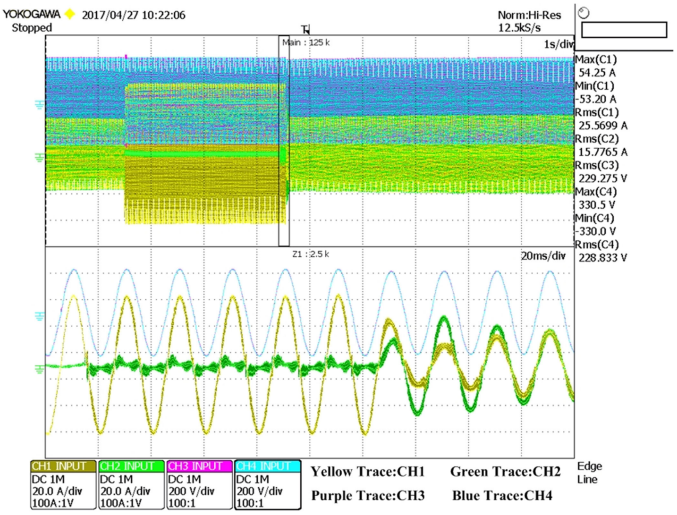

Fig. 34. Waveforms during the transient time using the adaptive virtual impedance control, CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

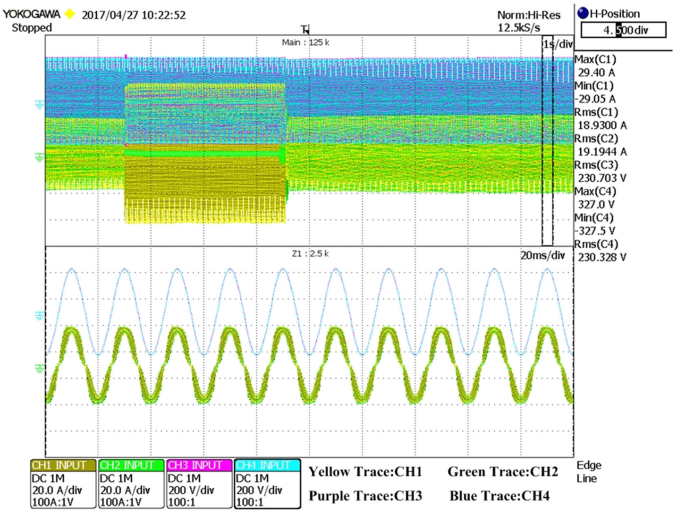

Fig. 35. Steady-state waveforms using the adaptive virtual impedance control, CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

conventional virtual impedance. It can be foreseen that in real applications, when output impedances are unbalanced between the parallel power modules, the conventional virtual impedance control cannot guarantee a good power sharing performance automatically.

C. Experimental Results With the Same Preset Virtual Impedance in the Parallel Modules With Adaptive Virtual Impedance

Figs. 34 and 35 demonstrate an excellent average power sharing performance of the adaptive virtual impedance control under balanced output impedances.

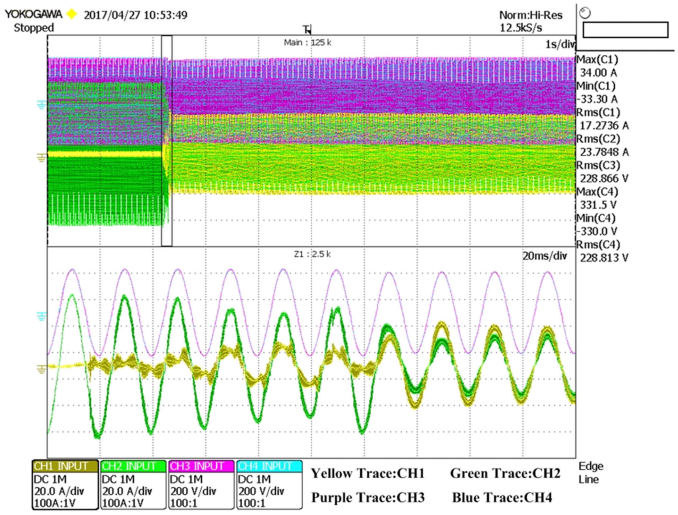

Fig. 36. Waveforms during the transient time using the adaptive virtual impedance control with unbalance output impedances (preset 1), CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

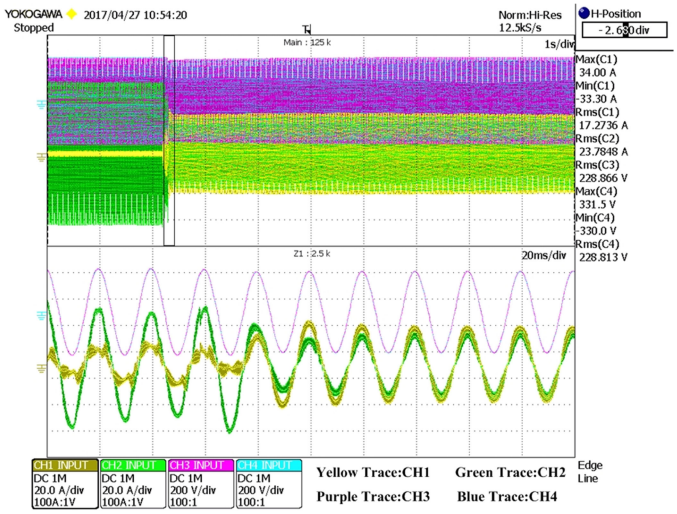

Fig. 37. Waveforms during the transient time using the adaptive virtual impedance control with unbalance output impedances (preset 1), CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

D. Experimental Results With the Two Different Presets of Unbalanced Virtual Impedances in the Parallel Modules Using the Proposed Control

In this section, two different presets of unbalanced virtual impedances are applied in the experiments to verify the proposed control method.

From the experimental results shown in Figs. 38 and 41, we can notice that, with unbalanced preset virtual impedance, the transient time is a little bit longer than the results in Fig. 34 with balanced virtual impedances, but finally the current will be average shared between the parallel modules when using the proposed DAVIC. When compares Figs. 37 and 40, we can see the phenomenon that it will take a little bit long time,

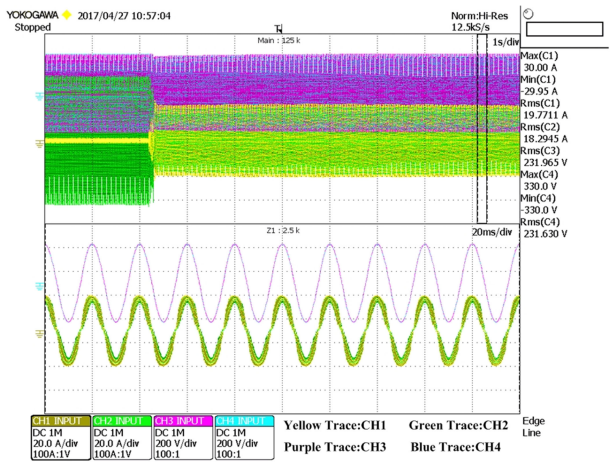

Fig. 38. Experimental results under steady state with unbalance output impedances (preset 1), CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

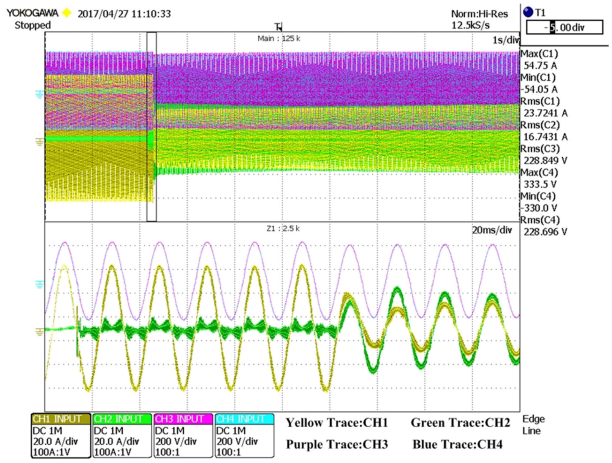

Fig. 39. Waveforms during the transient time using the adaptive virtual impedance control with unbalance output impedances (preset 2), CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

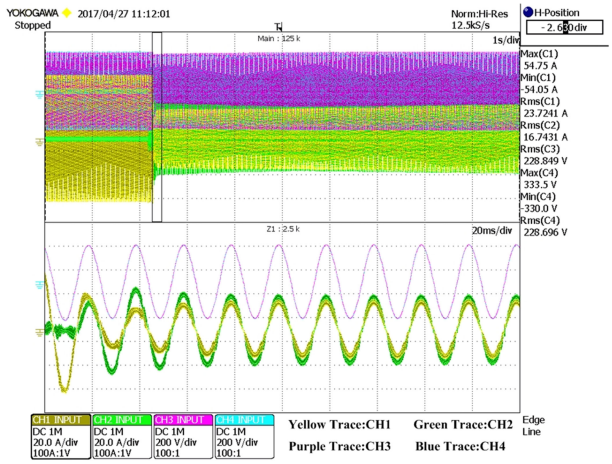

Fig. 40. Waveforms during the transient time using the adaptive virtual impedance control with unbalance output impedances (preset 2), CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

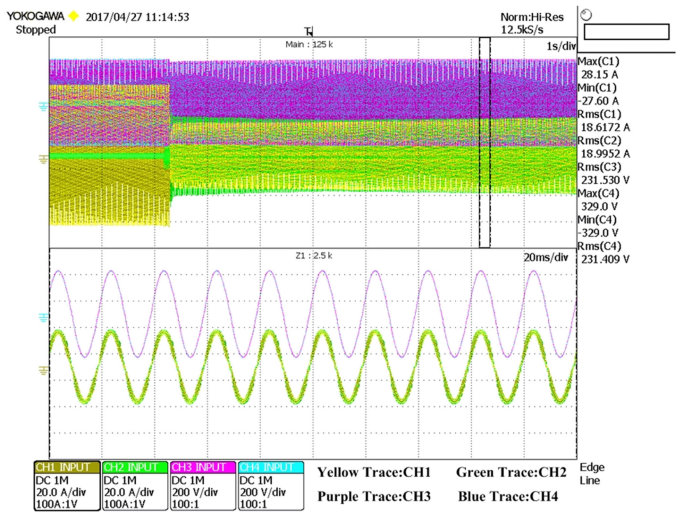

Fig. 41. Experimental results under steady state with unbalance output impedances (preset 2), CH1: Phase A current of Module1; CH2: Phase A current of Module2; CH3: Phase A voltage of Module 1; CH4: Phase A voltage of Module 2.

a few fundamental cycles, to reach the stable state when the output impedances are more unbalanced between the parallel power modules. The results show the ability of tuning the output impedances of the inverter modules automatically to guarantee the performance of average power sharing using the proposed adaptive virtual impedance control, which can strengthen the availability and reliability of the modular UPS system.

VI. Conclusion

Modular UPS systems are becoming more and more attractive in industrial applications with high levels of reliability and, in this case, the average power sharing performance is very important. An adaptive virtual impedance control method was proposed in this paper for the control of the modular UPS systems, and the control parameter design procedure for the adaptive virtual impedance loop is provided as well. In addition, the selection criteria of the virtual impedance are presented as well. Simulation results including two inverter modules were obtained by using the software PLECS to verify the availability and reliability of the proposed control. Experiments based on an industrial modular UPS platform have been implemented. Through the dynamic test, when compares to the conventional virtual impedance control, the circulating current between the parallel modules can be effectively suppressed under the condition of different output impedances, thus presenting a better average power sharing performance than using conventional approaches.

Acknowledgment

The authors would like to thank the colleagues J. Montero, R. Pinyol, R. Ciurans, D. Revilla, and A. Sabe, from Salicru for their active support during this project.

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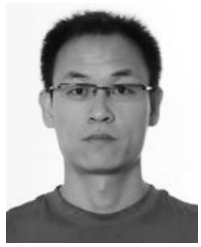

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