Asymmetrical Reactive Power Capability of Modular Multilevel Cascade Converter Based STATCOMs for Offshore Wind Farm

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***Abstract*—Modular multilevel cascade converters (MMCCs) are becoming attractive solutions as high-voltage Static Synchronous Compensators (STATCOMs) for power plants in renewable energy generation, in order to satisfy the strict grid codes under both normal and grid fault conditions. This paper investigates the performances of four potentially used configurations of the MMCC family for the STATCOM in large-scale offshore wind power plants, with special focus on asymmetrical low-voltage ride through capability under grid faults. The specifications and the sizing of components of each type of practical 80-MVar/33-kV-scaled MMCC-STATCOM are carefully designed and compared. The total cost and volume are compared based on the total power semiconductor chip area and the total energy stored in the passive components. Asymmetrical reactive power delivering operation of the MMCC family considering the dc-link capacitor voltage-balancing method is solved mathematically in order to quantitatively understand the performance limitations and behaviors. The electrothermal stress of the power modules used in each type of the MMCC for a practical 80-MVar/33-kV-scaled STATCOM is analyzed. The asymmetrical reactive power capability of the MMCC solutions is compared under different scenarios of grid faults, while considering the device temperature limits as well as voltage saturation. It is found that the MMCC configuration with double-star bridge cells becomes the most attractive circuit configuration for the STATCOM application based on the obtained results.**

***Index Terms*—Asymmetrical grid faults, modular multilevel cascade converter (MMCC), reactive power, static VAR compensators, Static Synchronous Compensator (STATCOM), wind power generation.**

I. Introduction

THE capacity of renewable energy generation has continued to grow in the last decade, and it will reach 2.5 TW in 2020 [1]. In accordance with the construction of large-scale

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in back-to-back converters such as medium-voltage motor drive and high-voltage direct current (HVDC) transmission applications typically, but they can also be used for a STATCOM application. They can keep operating under asymmetrical grid faults by activating the voltage-balancing control using circulating dc current having two degrees of freedom [13]–[15]. This voltage-balancing method also results in increased current stress of the converters. However, this method may have higher reactive power delivering capability compared with an SSBC and SDBC because of more flexibility in the circulating dc current.

Numerous authors have proposed many useful control schemes and design methods for each type of MMCC solution until now. However, the optimum MMCC solution for the STATCOM application is still an open question because a comprehensive comparison between the four types of MMCC solutions has not been done yet [16], [17], [28], [29]. In addition to the total cost and volume of the MMCC solutions, the asymmetrical reactive power delivering capability under grid faults becomes much important for the STATCOM application.

This paper clarifies the performances of potentially used four configurations of the MMCC family with SSBC, SDBC, DSCC, and DSBC for the STATCOM in large-scale offshore wind power plants, with a special focus on asymmetrical low-voltage ride through (LVRT) capability under grid faults. In Section II, the system configuration of typical offshore wind power plant and system grid fault scenarios are summarized. In Section III, specifications and the component sizing of each type of practical 80-MVar/33-kV-scaled MMCC-STATCOM are carefully designed and compared. The total cost and volume are compared based on the total power semiconductor chip area and the total energy stored in the passive components. In Section IV, the mathematical formulation for the STATCOM based on the MMCC solutions under asymmetrical compensation operation is developed, which contributes to quantitative understanding of the performance limitations and circuit behaviors under the asymmetrical compensation. In Section V, the electrothermal stresses of actual power modules used in each type of the MMCC with practical controls are analyzed in detail. The asymmetrical reactive power capacity focusing on the MMCC solutions is compared under different scenarios of grid faults, with the consideration of device temperature limits and voltage saturations. Finally, in Section VI, most attractive MMCC solution for the STATCOM application is suggested based on the results we obtained.

II. Typical Offshore Wind Plant and System Fault Scenarios

A. System Configuration for Analysis

Fig. 1 shows the system configuration of a typical offshore wind power plant and an MMCC-based STATCOM. The generated active power from the offshore wind farm needs to be provided to the PCC as *Bus* A (400 kV in this case) by an HVAC transmission system (220 kV in this case) with long-distance submarine cables. Reactive power induced by the submarine cable is compensated by the full-scale converters of wind turbines, the shunt reactor, and the STATCOM connected to *Bus* B via a delta–star transformer. Other power generators and loads beside the wind power plant may also be connected to *Bus* A.

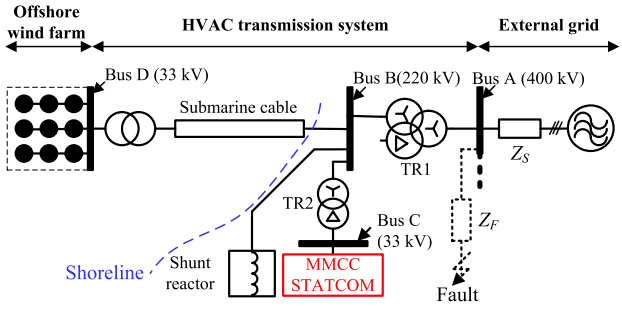


Fig. 1. Typical offshore wind power plant with an MMCC-STATCOM.

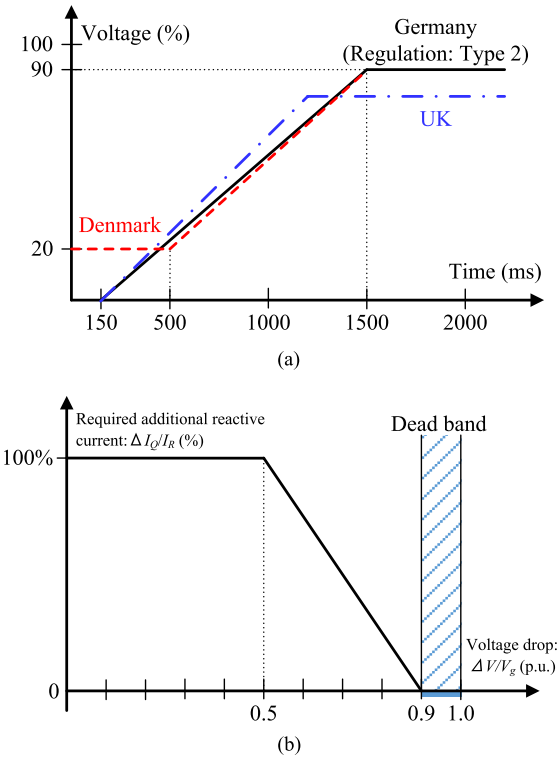
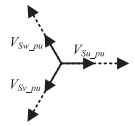
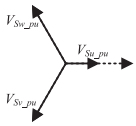
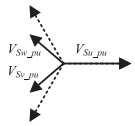
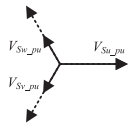


Fig. 2. Reactive power requirements of large-scale generating plants under grid fault. (a) LVRT requirement by different countries. (b) Additional reactive current requirement during LVRT.

B. Reactive Power Requirement Under Grid Fault

Besides the normal operation, TSOs in different countries have issued strict grid supporting requirement for the growing large-scale renewable power plant such as the offshore wind power plant under grid fault, which is specified in Fig. 2 [18], [19]. According to the grid codes, the offshore wind power plant has to keep the operation regarding the voltage sag under grid fault, as shown in Fig. 2(a), and in the case of German and Danish codes it should be able to inject additional reactive current to support the recovery of grid voltage sag, which is also shown in Fig. 2(b). The reactive current reference is only defined as positive-sequence component because recent grid codes do not require negative-sequence current to compensate

TABLE I
PHASOR DIAGRAM AND VECTOR DEFINITIONS OF DIFFERENT FAULT SCENARIOS ON PCC (*Bus* A)

Fault types	Phasor diagram diffinitions	Vecter deffinitions
(a) Three-phase-to-ground fault		$V_{Su\_pu} = D$ $V_{Sv\_pu} = -\frac{1}{2}D - j\frac{\sqrt{3}}{2}D$ $V_{Sw\_pu} = -\frac{1}{2}D + j\frac{\sqrt{3}}{2}D$
(b) Single-phase-to-ground fault		$V_{Su\_pu} = D$ $V_{Sv\_pu} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$ $V_{Sw\_pu} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$
(c) Phase-to-phase short-circuit fault		$V_{Su\_pu} = 1$ $V_{Sv\_pu} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}D$ $V_{Sw\_pu} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}D$
(d) Two-phase-to-ground fault		$V_{Su\_pu} = 1$ $V_{Sv\_pu} = -\frac{1}{2}D - j\frac{\sqrt{3}}{2}D$ $V_{Sw\_pu} = -\frac{1}{2}D + j\frac{\sqrt{3}}{2}D$

the asymmetrical grid fault voltage recovering. However, this feature may become a future requirement [20]. In this paper, the positive sequence reactive current injection capabilities of each type of MMCC solution under grid faults are analyzed.

C. Grid Fault Scenarios

Table I shows the representative grid fault voltage phasors and vectors corresponded to three-phase-to-ground fault, single-phase-to-ground fault, phase-to-phase short-circuit fault and two-phase-to-ground fault [21], [22]. It is assumed that the short-circuit faults happen somewhere on a feeder with the line impedance Z_F to *Bus* A (PCC) in Fig. 1. The line impedance from the PCC to the grid with a higher voltage level is Z_s. A voltage dip severity D is determined by the ratio of Z_s and Z_F with positive-, negative-, and zero-sequence impedance. In order to simplify the grid fault scenarios, D is considered as a real part only, and more details are explained and classified in [23] and [24].

In this paper, three asymmetrical grid fault scenarios are chosen, as shown in Table I (b), (c), and (d), respectively. It is noted that where the asymmetrical grid fault voltage on *Bus* A is propagated to *Bus* B, the *Bus* A and *Bus* B voltages do not appear significantly different due to the used neutral point grounded wye–wye–delta transformer TR1. However, the voltage on *Bus* B shows different characteristics, when it is propagated to *Bus* C, which is seen by the STATCOM due to the used delta–wye transformer TR2. Table II shows the asymmetrical grid fault scenarios on *Bus* C corresponding to each grid fault. $\dot{V}_{dq}^{+}$, $\dot{V}_{dq}^{-}$, and $\dot{V}^{0}$ are positive-, negative, and zero-sequence components of the voltage, respectively, which are defined as scenarios used in this paper.

TABLE II
SEQUENCE VOLTAGE AMPLITUDE DEFINITION OF DIFFERENT GRID FAULTS SCENARIOS ON *Bus* C (V_s IS THE RATED VOLTAGE ON *Bus* C)

Fault types	Each sequence voltage vector
(b) Single-phase-to-ground fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{D}{3} + \frac{2}{3} \\ \frac{D}{6} - \frac{1}{6} + j\left(\frac{D}{2\sqrt{3}} - \frac{1}{2\sqrt{3}}\right) \\ 0 \end{bmatrix}$
(c) Phase-to-phase short-circuit fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{D}{2} + \frac{1}{2} \\ -\frac{D}{4} + \frac{1}{4} + j\left(-\frac{\sqrt{3}D}{4} - \frac{\sqrt{3}}{4}\right) \\ 0 \end{bmatrix}$
(d) Two-phase-to-ground fault	$\begin{bmatrix} V_{dq}^{+} \\ V_{dq}^{-} \\ V^{0} \end{bmatrix} = V_S \begin{bmatrix} \frac{2}{3}D + \frac{1}{3} \\ -\frac{D}{6} + \frac{1}{6} + j\left(-\frac{D}{2\sqrt{3}} + \frac{1}{2\sqrt{3}}\right) \\ 0 \end{bmatrix}$

III. SPECIFICATIONS OF THE MMCC-STATCOMS FOR STUDY

An 80-MVar/33-kV case study for a practical STATCOM application is selected in this paper. Fig. 3 shows circuit configurations of the STATCOM based on MMCC with SSBC, SDBC, DSCC, and DSBC. Table III shows the specifications, the cell numbers, and key components. The design procedure is given in the following subsections.

A. Basic Structure and Power Semiconductor Device

The rated dc-link voltage $V_{C,\mathrm{dc}}$ of each converter cell in the four types of the MMCC solutions is designed to be the same at 2600 Vdc where widely used 4.5-kV insulated gate bipolar transistor (IGBT) modules are selected for each converter cell in this case study. The nominal output ac voltage of each converter cell in the SSBC, SDBC, and DSBC is designed to be 1450 Vrms with the nominal modulation factor $\alpha_n = 0.8$. The margin of the modulation factor (0.2) is determined by the voltage drop of the output impedance, current control dynamics, pulsewidth limitation due to dead time, and modular redundancy. However, the circuit configuration of the converter cell for the DSCC is a chopper converter, which cannot output negative voltage. Because $+/-$ output voltage is also required for the DSCC-based STATCOM, the output voltage in each chopper converter cell is superimposed with the half-value of the rated dc-voltage (i.e., 1300 Vdc). When the above-mentioned design guideline is followed, the nominal output ac voltage each converter cell in the DSCC becomes ac 725 Vrms with the nominal modulation factor for ac component being $\alpha_n = 0.8$.

The cell converter counts N_{cell} of the MMCC solutions with SSBC, SDBC, DSCC, and DSBC are expressed by the equations in Table IV. The total number of switching devices N_{sw} for each MMCC topology is derived by each cell circuit type and N_{cell}.

Rated output currents I_r in each cell among the MMCC solutions are also expressed by the equations in Table IV. The current ratings of the IGBT modules in each of the cell converter among the MMCC solutions are selected depending on I_r. It is worth

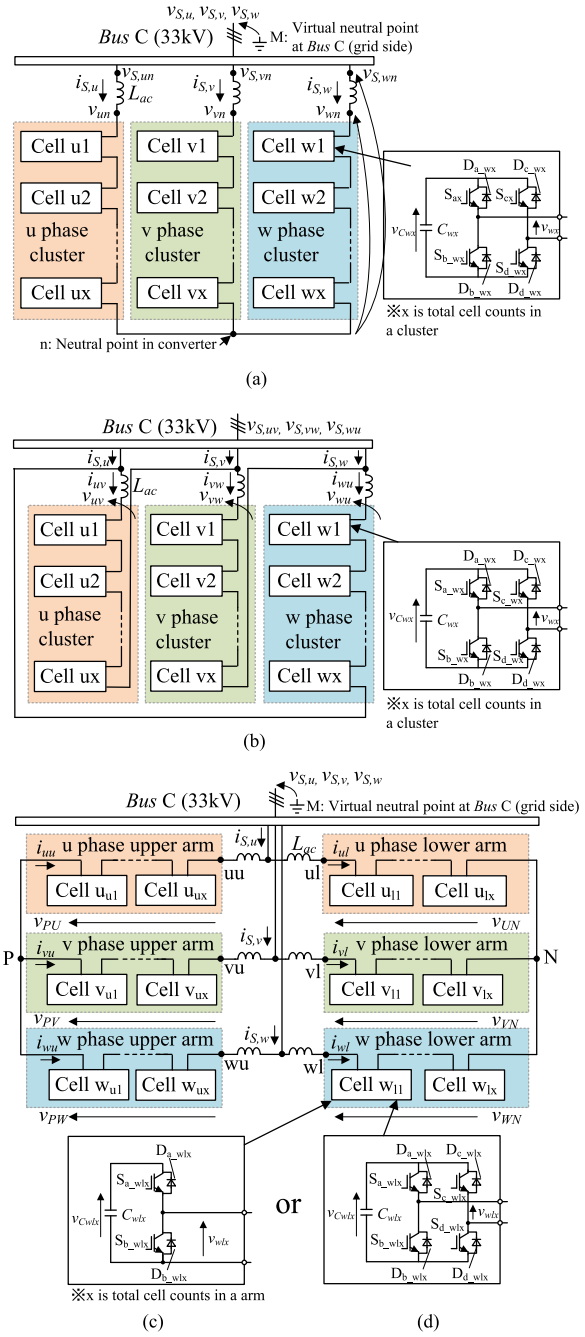


Fig. 3. Circuit configurations of the MMCC family for a STATCOM application. (a) SSBC. (b) SDBC. (c) DSCC. (d) DSBC.

noting that $N_{\rm sw}$ and $N_{\rm cell}$ are different among the MMCC solutions. However, the equivalent total power semiconductor chip area calculated by the total IGBT module counts, the current capacity of each IGBT module, and the rated voltage of each IGBT module, which strongly influences the total cost of the STATCOM, have approximately same values.

B. Modulation Type and Frequencies for Pulsewidth Modulation (PWM)

Phase-shift PWM is chosen because of the advantage that the electrothermal stresses of the IGBT modules and capacitors are equally distributed among the cells in the same cluster (or arm). The equivalent switching frequency of the MMCC $f_{\rm eq\_sw}$ is designed to be the same at 10 kHz. In this result, the carrier frequencies f_c of the MMCC solutions with SSBC and SDBC are 380 and 215 Hz, respectively. The carrier frequencies f_c of the MMCC solutions with DSCC and DSBC are the same at 190 Hz. It is noted that f_c of each MMCC solution should not be an integer multiple of the fundamental frequency in order to avoid diverging the capacitor voltages among the cells when f_c is below several hundred hertz [25], [26].

C. Interconnection Inductance

In this case study, $L_{\rm ac}$ is designed as 6% of the normalized impedance $Z_{\rm pu}$ based on 33-kV and 80-MVar operating condition of the converter. In this design rule, $L_{\rm ac}$ of the MMCC solutions with SSBC, SDBC, DSCC, and DSBC is calculated by equations given in Table IV. The total energy stored in the whole interconnection inductor E_L has the same value among the MMCC solutions in this designed case, which will strongly influence the total volume of the STATCOM.

D. DC-Link Capacitance

The dc-link capacitance of each cell C_x is designed as capacitor voltage ripple scaled by the rated dc-link voltage $V_{c,\rm dc}$ (2600 V). The voltage ripple $\Delta V_{c,\rm pu}$ is designed to be 10% below nominal rated operation. The relationship between the voltage ripple and the capacitance C_x of the MMCC solutions with SSBC, SDBC, DSCC, and DSBC is also expressed by equations given in Table IV based on an averaging model [12], [32]. Here, α is a modulation factor of a cell, which is set to be 1, assuming the largest voltage ripple in this case study. The total energy stored in all dc-link capacitors E_C among the MMCC solutions can be expressed as

$$E_C = \frac{N_{\rm cell}}{2} C_x V_{C,\rm dc}^2. \tag{1}$$

After $N_{\rm cell}$, C_x, and I_r, as shown in Table IV, are substituted in (1), the E_C among the MMCC solutions is updated to the formulation shown in Table IV. It is noted that E_C for SSBC, SDBC, and DSBC is the same. However, E_c of the DSCC is four times larger than those of the others because of the used chopper cells. As an example, when E_C of the DSCC is compared with the DSBC, both $N_{\rm cell}$ and C_x of the DSCC become twice higher than those of DSBC because of the used chopper cells with the output voltage being superimposed with the half-value of the rated dc-voltage $V_{C,\rm dc}$. It should be noted that E_C depends greatly on the total volume of the STATCOM.

IV. Theoretical Operation of the MMCC Family Under Asymmetrical Reactive Power Compensation

In this section, the theoretical operation of each MMCC solution is solved by a mathematical formula, focusing on the asymmetrical reactive power compensation. This analysis contributes to understanding the limitation of the asymmetrical compensation capability of the MMCC solutions. The asymmetrical three-phase systems are solved by using vector representation, where the method seems the simplest way to do it according to previous works [27]–[29].

TABLE III
MMCC SPECIFICATIONS FOR THE CASE STUDY

Circuit type of MMCC	SSBC	SDBC	DSCC	DSBC
Rated power Q_r	±80 MVA			
Rated line-to-line voltage V_s	33 kVrms (Source angular frequency ω_s : 2π×50 rad/s)			
Rated DC-link voltage each cell $V_{C,dc}$	2600 Vdc			
Nominal output voltage each cell	AC 1450 Vrms DC 0 Vdc		AC 725 Vrms DC 1300 Vdc	AC 1450 Vrms DC 0 Vdc
Equivalent switching frequency f_{eq_sw}	10 kHz (with Phase Shift PWM)			
Number of total cells N_{cell}	39 (13 cells/cluster)	69 (23 cells/cluster)	156 (26 series/arm)	78 (13 series/arm)
Number of total switching devices N_{sw}	156	276	312	312
Rated output current of each cell I_r	1400 Arms	808 Arms	700 Arms	700 Arms
Carrier frequency f_c	380 Hz	215 Hz	190 Hz	190 Hz
Total energy stored in interconnection inductor E_L	15 kJ (L_{ac} = 2.6 mH)	15 kJ (L_{ac} = 7.8 mH)	15 kJ (L_{ac} = 5.2 mH)	15 kJ (L_{ac} = 5.2 mH)
Total energy stored in dc-link capacitor E_C	1.6 MJ (C_x = 12 mF)	1.6 MJ (C_x = 7.0 mF)	6.3 MJ (C_x = 12 mF)	1.6 MJ (C_x = 6.0 mF)
IGBT module	MBN1500FH45F (4500V/1500A)	MBN900D45A (4500V/900A)	MBN800H45E2 (4500V/800A)	MBN800H45E2 (4500V/800A)

TABLE IV
KEY EQUATIONS FOR THE DESIGN OF THE MMCC SOLUTIONS

	SSBC	SDBC	DSCC	DSBC
The cell converter counts N_{cell}	$\frac{\sqrt{6}V_s}{\alpha_n V_{C,dc}}$	$\frac{3\sqrt{2}V_s}{\alpha_n V_{C,dc}}$	$\frac{4\sqrt{6}V_s}{\alpha_n V_{C,dc}}$	$\frac{2\sqrt{6}V_s}{\alpha_n V_{C,dc}}$
Rated output current of each cell I_r	$\frac{Q_r}{\sqrt{3}V_s}$	$\frac{Q_r}{3V_s}$	$\frac{Q_r}{2\sqrt{3}V_s}$	
The interconnection inductance L_{ac}	$\frac{Z_{pu}V_s^2}{\omega_S Q_r}$	$\frac{3Z_{pu}V_s^2}{\omega_S Q_r}$	$\frac{2Z_{pu}V_s^2}{\omega_S Q_r}$	
The DC-link capacitance of each cell C_x	$\frac{\sqrt{2}\alpha Q_r}{2\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}\alpha Q_r}{6\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}Q_r}{2\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$	$\frac{\sqrt{2}\alpha Q_r}{4\sqrt{3}\omega_S \Delta V_{C,pu} V_{C,dc} V_s}$
Total energy stored in dc-link capacitor E_C	$\frac{\alpha Q_r}{2\alpha_n \Delta V_{C,pu} \omega_S}$		$\frac{2Q_r}{\alpha_n \Delta V_{C,pu} \omega_S}$	$\frac{\alpha Q_r}{2\alpha_n \Delta V_{C,pu} \omega_S}$

A. *Definition of the Grid Fault Voltage and Current on Bus C*

The grid voltages and currents on *Bus* C are defined as

$$\begin{cases} v_{S,u} = V_S^+ \sin(\omega_S t) + V_S^- \sin(\omega_S t + \phi_{\rm vn}) \\ v_{S,v} = V_S^+ \sin\left(\omega_S t - \frac{2\pi}{3}\right) + V_S^- \sin\left(\omega_S t + \phi_{\rm vn} + \frac{2\pi}{3}\right) \\ v_{S,w} = V_S^+ \sin\left(\omega_S t + \frac{2\pi}{3}\right) + V_S^- \sin\left(\omega_S t + \phi_{\rm vn} - \frac{2\pi}{3}\right) \end{cases} \tag{2}$$

$$\begin{cases} i_{S,u} = I_S^+ \sin(\omega_S t + \phi_{ip}) + I_S^- \sin(\omega_S t + \phi_{\rm in}) \\ i_{S,v} = I_S^+ \sin\left(\omega_S t + \phi_{\rm ip} - \frac{2\pi}{3}\right) + I_S^- \sin\left(\omega_S t + \phi_{\rm in} + \frac{2\pi}{3}\right) \\ i_{S,w} = I_S^+ \sin\left(\omega_S t + \phi_{\rm ip} + \frac{2\pi}{3}\right) + I_S^- \sin\left(\omega_S t + \phi_{\rm in} - \frac{2\pi}{3}\right) \end{cases} \tag{3}$$

where V_S^+ is the amplitude of positive-sequence voltage, V_S^- and $\phi_{\rm vn}$ are the amplitude and phase angle of negative-sequence voltage, I_S^+ and $\phi_{\rm ip}$ are the amplitude and phase angle of positive-sequence current, and I_S^- and $\phi_{\rm in}$ are the amplitude and phase angle of negative-sequence current, respectively. After a *dq* transformation of (2) and (3), the grid voltage $\dot{V}_{S,dq}^+$, $\dot{V}_{S,dq}^-$ can be expressed as

$$\begin{cases} \dot{V}_{S,dq}^+ = V_{S,d}^+ + jV_{S,q}^+ \\ \dot{V}_{S,dq}^- = V_{S,d}^- + jV_{S,q}^-. \end{cases} \tag{4}$$

$V_{S,d}^+$, $V_{S,q}^+$, $V_{S,d}^-$, and $V_{S,q}^-$ are detected by a dual-frame *dq* transformation scheme in an actual current controller [30].

It is noted that $V_{S,q}^{+}$ has a zero value because the standard phase is set at the *d*-axis of the positive-sequence grid voltage by the phase-locked loop (PLL).

Similarly, the grid current $\dot{I}_{S,dq}^{+},\ \dot{I}_{S,dq}^{-}$ on *Bus* C can be expressed as

$$\begin{cases} \dot{I}_{S,dq}^{+} = I_{S,d}^{+} + jI_{S,q}^{+} \\ \dot{I}_{S,dq}^{-} = I_{S,d}^{-} + jI_{S,q}^{-}. \end{cases} \tag{5}$$

$I_{S,d}^{+},\ I_{S,q}^{+},\ I_{S,d}^{-}$, and $I_{S,q}^{-}$ are supplied by the STATCOM, which values are considered to be the same as these reference values $I_{S,d,\mathrm{ref}}^{+},\ I_{S,q,\mathrm{ref}}^{+},\ I_{S,d,\mathrm{ref}}^{-}$, and $I_{S,q,\mathrm{ref}}^{-}$ as

$$\begin{cases} I_{S,d}^{+} = I_{S,d,\mathrm{ref}}^{+} \\ I_{S,q}^{+} = I_{S,q,\mathrm{ref}}^{+} \\ I_{S,d}^{-} = I_{S,d,\mathrm{ref}}^{-} \\ I_{S,q}^{-} = I_{S,q,\mathrm{ref}}^{-} \end{cases} \tag{6}$$

Here, $I_{S,d,\mathrm{ref}}^{+}$ is set to have a zero value because of reactive power compensation operation. $I_{S,q,\mathrm{ref}}^{+}$ is given from the central control of the wind power plant under normal operation. In this result, the STATCOM has two operating modes, namely, inductive operation in the case of $I_{S,q,\mathrm{ref}}^{+} < 0$ and capacitive operation in the case of $I_{S,q,\mathrm{ref}}^{+} > 0$. When a grid fault happens, the additional amount of $I_{S,q,\mathrm{ref}}^{+}$ may be required due to a recent published grid code of TSOs. $I_{S,d,\mathrm{ref}}^{-}$ and $I_{S,q,\mathrm{ref}}^{-}$ are set to have a zero value according to the mentioned recent grid codes.

B. MMCC-SSBC With Zero-Sequence AC Voltage

When the zero-sequence ac voltage with the same frequency as the phase-cluster current is injected, the zero-sequence voltage and the cluster current formulate the different active power between the clusters in the MMCC-SSBC. This phenomenon is used for the dc-link capacitor voltage balancing control between the phase-clusters under asymmetrical grid fault conditions, whose value is solved as follows.

Each phase-cluster voltage of the MMCC-SSBC including the back electromotive forces (EMFs) of the interconnection inductor L_{ac} can be expressed as

$$\begin{bmatrix} \dot{V}_{S,un} \\ \dot{V}_{S,vn} \\ \dot{V}_{S,wn} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} + \dot{V}^{0} \tag{7}$$

where $\dot{V}_{S,u},\ \dot{V}_{S,v}$, and $\dot{V}_{S,w}$ are the grid voltage on *Bus* C, and $\dot{V}^{0}$ is the zero-sequence voltage of the MMCC-SSBC, which is the voltage difference between the point *n* and *M,* as shown in Fig. 3(a). $\dot{V}^{0}$ is defined as

$$\dot{V}^{0} = x_{\mathrm{SSBC}} + jy_{\mathrm{SSBC}} \tag{8}$$

where x_{SSBC} is the real part of $\dot{V}^{0}$, y_{SSBC} is the imaginary part of $\dot{V}^{0}$. $\dot{V}_{S,u},\ \dot{V}_{S,v}$, and $\dot{V}_{S,w}$ can be expressed as (9) shown at the bottom of this page.

The grid currents $\dot{I}_{S,u},\ \dot{I}_{S,v},$ and $\dot{I}_{S,w}$ at *Bus* C can be expressed as (10) shown at the bottom of this page.

The instantaneous active powers $p_u, p_v,$ and p_w of each phase-cluster of the MMCC-SSBC including the L_{ac} can be expressed as

$$\begin{bmatrix} p_u \\ p_v \\ p_w \end{bmatrix} = \begin{bmatrix} \frac{1}{2}\Re\left[\dot{V}_{S,un}^{*} \cdot \dot{I}_{S,u}\right] \\ \frac{1}{2}\Re\left[\dot{V}_{S,vn}^{*} \cdot \dot{I}_{S,v}\right] \\ \frac{1}{2}\Re\left[\dot{V}_{S,wn}^{*} \cdot \dot{I}_{S,w}\right] \end{bmatrix} \tag{11}$$

$$\begin{bmatrix} \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,dq}^{+} + \dot{V}_{S,dq}^{-} \\ \dot{V}_{S,dq}^{+}e^{-j2\pi/3} + \dot{V}_{S,dq}^{-}e^{j2\pi/3} \\ \dot{V}_{S,dq}^{+}e^{j2\pi/3} + \dot{V}_{S,dq}^{-}e^{-j2\pi/3} \end{bmatrix} = \begin{bmatrix} \left(V_{S,d}^{+} + V_{S,d}^{-}\right) + j\left(V_{S,q}^{-}\right) \\ \left(-\frac{1}{2}V_{S,d}^{+} - \frac{1}{2}V_{S,d}^{-} - \frac{\sqrt{3}}{2}V_{S,q}^{-}\right) + j\left(-\frac{\sqrt{3}}{2}V_{S,d}^{+} + \frac{\sqrt{3}}{2}V_{S,d}^{-} - \frac{1}{2}V_{S,q}^{-}\right) \\ \left(-\frac{1}{2}V_{S,d}^{+} - \frac{1}{2}V_{S,d}^{-} - \frac{\sqrt{3}}{2}V_{S,q}^{-}\right) + j\left(\frac{\sqrt{3}}{2}V_{S,d}^{+} - \frac{\sqrt{3}}{2}V_{S,d}^{-} - \frac{1}{2}V_{S,q}^{-}\right) \end{bmatrix} \tag{9}$$

$$\begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix} = \begin{bmatrix} \dot{I}_{S,dq}^{+} + \dot{I}_{S,dq}^{-} \\ \dot{I}_{S,dq}^{+}e^{-j2\pi/3} + \dot{I}_{S,dq}^{-}e^{j2\pi/3} \\ \dot{I}_{S,dq}^{+}e^{j2\pi/3} + \dot{I}_{S,dq}^{-}e^{-j2\pi/3} \end{bmatrix} = \begin{bmatrix} \left(I_{S,d}^{-}\right) + j\left(I_{S,q}^{+} + I_{S,q}^{-}\right) \\ \left(\frac{\sqrt{3}}{2}I_{S,q}^{+} - \frac{1}{2}I_{S,d}^{-} - \frac{\sqrt{3}}{2}I_{S,q}^{-}\right) + j\left(-\frac{1}{2}I_{S,q}^{+} + \frac{\sqrt{3}}{2}I_{S,d}^{-} - \frac{1}{2}I_{S,q}^{-}\right) \\ \left(-\frac{\sqrt{3}}{2}I_{S,q}^{+} - \frac{1}{2}I_{S,d}^{-} + \frac{\sqrt{3}}{2}I_{S,q}^{-}\right) + j\left(-\frac{1}{2}I_{S,q}^{+} - \frac{\sqrt{3}}{2}I_{S,d}^{-} - \frac{1}{2}I_{S,q}^{-}\right) \end{bmatrix} \tag{10}$$

$$\begin{aligned} \dot{V}^{0} = {} & \frac{V_{S,d}^{+}\left(I_{S,d}^{-}I_{S,d}^{-} - I_{S,q}^{-}I_{S,q}^{-} - I_{S,q}^{+}I_{S,q}^{-}\right) + V_{S,d}^{-}I_{S,q}^{+}\left(I_{S,q}^{+} + I_{S,q}^{-}\right) + V_{S,q}^{-}I_{S,q}^{+}I_{S,d}^{-}}{\left(I_{S,q}^{+}I_{S,q}^{+} - I_{S,d}^{-}I_{S,d}^{-} - I_{S,q}^{-}I_{S,q}^{-}\right)} \\ & + j\frac{V_{S,d}^{+}\left(I_{S,d}^{-}I_{S,q}^{-} + I_{S,d}^{-}I_{S,q}^{-} - I_{S,q}^{+}I_{S,q}^{-}\right) + V_{S,q}^{-}I_{S,q}^{+}\left(I_{S,q}^{-} - I_{S,q}^{+}\right) + V_{S,d}^{-}I_{S,q}^{+}I_{S,d}^{-}}{\left(I_{S,q}^{+}I_{S,q}^{+} - I_{S,d}^{-}I_{S,d}^{-} - I_{S,q}^{-}I_{S,q}^{-}\right)} \end{aligned} \tag{12}$$

where $\dot{V}^*_{S,un}$ is the complex conjugate of the $\dot{V}_{S,un}$. By using (11), $\dot{V}^0$ in order to make $p_u = p_v = p_w$ can be solved by (12) shown at the bottom of the previous page.

Each phase-cluster converter output voltage $\dot{V}_{un}$, $\dot{V}_{vn}$, and $\dot{V}_{wn}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{un} \\ \dot{V}_{vn} \\ \dot{V}_{wn} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,un} \\ \dot{V}_{S,vn} \\ \dot{V}_{S,wn} \end{bmatrix} - \begin{bmatrix} \dot{V}_{L,u} \\ \dot{V}_{L,v} \\ \dot{V}_{L,w} \end{bmatrix} \tag{13}$$

where $\dot{V}_{L,u}$, $\dot{V}_{L,v}$, and $\dot{V}_{L,w}$ are the back EMFs of L_{ac}. $\dot{V}_{L,u}$, $\dot{V}_{L,v}$, and $\dot{V}_{L,w}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{L,u} \\ \dot{V}_{L,v} \\ \dot{V}_{L,w} \end{bmatrix} = j\omega_S L_{\text{ac}} \begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix} \tag{14}$$

where the resistance of L_{ac} is neglected because the resistance is much smaller than the total impedance given by the inductance. Then, maximum phase-cluster peak voltage $V_{\text{max\_pu}}$ between the three-phases standardized by peak-rated phase-grid voltage $\sqrt{2/3}\,V_S$ can be expressed as

$$V_{\text{max\_pu}} = \frac{\max\left(\left|\dot{V}_{un}\right|, \left|\dot{V}_{vn}\right|, \left|\dot{V}_{wn}\right|\right)}{\sqrt{\frac{2}{3}}V_s}. \tag{15}$$

The maximum phase-cluster rms current $I_{\text{max\_pu}}$ between the three phases normalized by the rated phase current $\sqrt{2}I_r$ of the STATCOM can be expressed as

$$I_{\text{max\_pu}} = \frac{\max\left(\left|\dot{I}_u\right|, \left|\dot{I}_v\right|, \left|\dot{I}_w\right|\right)}{\sqrt{2}I_r}. \tag{16}$$

The line graphs in Fig. 4 show the calculated result of the normalized maximum phase-cluster peak voltage and rms current of the MMCC-SSBC under the different types of the grid fault scenarios as a function of the voltage dip severity D using (15) and (16). I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given in Table II. The normalized inductance of L_{ac} is set to be 6% with reference to the model mentioned in Table III. In the case of a single-phase fault, the maximum phase-cluster peak voltage reaches the voltage saturated level of the designed STATCOM when $D = 0.45$. On the other hand, the maximum phase-cluster rms current does not increase as a function of grid fault conditions. The marks in Fig. 4 indicate simulation results using PLECS software, whose conditions are shown in the next section. The calculated values correspond reasonably well with the PLECS simulations based on the given STATCOM configurations.

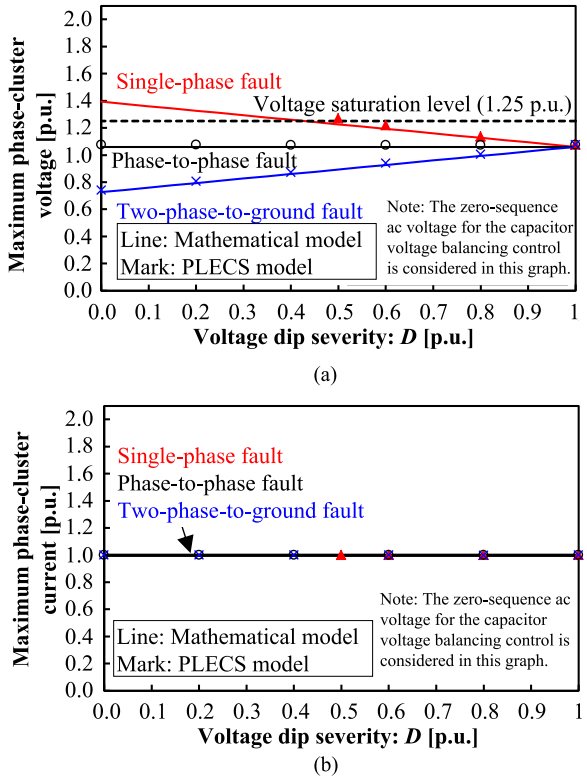


Fig. 4. Maximum phase-cluster output of the MMCC-SSBC corresponding to various grid fault scenarios. (a) Maximum phase-cluster peak voltage. (b) Maximum phase-cluster rms current.

C. MMCC-SDBC With Zero-Sequence AC Current

When the zero-sequence ac current with the same frequency as the cluster output voltage is injected, the zero-sequence current and the cluster output voltage formulate the different active power between the clusters in the MMCC-SDBC. This phenomenon is used for the dc-link capacitor voltage-balancing control among the phase-clusters under asymmetrical grid fault conditions, whose values are solved as follows.

For the configuration of MMCC-SDBC, the phase-cluster current $\dot{I}_{uv}$, $\dot{I}_{vw}$, $\dot{I}_{wu}$can be expressed as (17) shown at the bottom of the previous page. Where $\dot{I}^0$ is the zero-sequence current circulated in the MMCC-SDBC. $\dot{I}^0$ can be expressed as

$$\dot{I}^0 = x_{\text{SDBC}} + jy_{\text{SDBC}} \tag{18}$$

$$\begin{bmatrix} \dot{I}_{uv} \\ \dot{I}_{vw} \\ \dot{I}_{wu} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} \dot{I}^+_{S,dq} e^{j\pi/6} + \dot{I}^-_{S,dq} e^{-j\pi/6} \\ \dot{I}^+_{S,dq} e^{-j\pi/2} + \dot{I}^-_{S,dq} e^{j\pi/2} \\ \dot{I}^+_{S,dq} e^{j5\pi/6} + \dot{I}^-_{S,dq} e^{-j5\pi/6} \end{bmatrix} + \dot{I}^0 = \begin{bmatrix} \left(x_{\text{SDBC}} - \frac{I^+_{S,q}}{2\sqrt{3}} + \frac{I^-_{S,q}}{2\sqrt{3}} + \frac{I^-_{S,d}}{2}\right) + j\left(y_{\text{SDBC}} + \frac{I^+_{S,q}}{2} + \frac{I^-_{S,q}}{2} - \frac{I^+_{S,d}}{2\sqrt{3}}\right) \\ \left(x_{\text{SDBC}} + \frac{\sqrt{3}I^+_{S,q}}{3} - \frac{I^-_{S,q}}{3}\right) + j\left(y_{\text{SDBC}} + \frac{\sqrt{3}I^-_{S,q}}{3}\right) \\ \left(x_{\text{SDBC}} - \frac{I^+_{S,q}}{2\sqrt{3}} + \frac{I^-_{S,q}}{2\sqrt{3}} - \frac{I^-_{S,d}}{2}\right) + j\left(y_{\text{SDBC}} - \frac{I^+_{S,q}}{2} - \frac{I^-_{S,q}}{2} - \frac{I^-_{S,d}}{2\sqrt{3}}\right) \end{bmatrix} \tag{17}$$

where x_{SDBC} is the real part of $\dot{I}^0$, and y_{SDBC} is the imaginary part of $\dot{I}^0$. Each line-to-line voltage $\dot{V}_{S,uv}$, $\dot{V}_{S,vw}$, $\dot{V}_{S,wu}$ of the MMCC-SDBC including the back EMFs of L_{ac} can be expressed as (19) shown at the bottom of this page.

$\dot{I}^0$ in order to make the instantaneous active powers between the phase-clusters to have the same value can be expressed as follows [24]: (20) shown at the bottom of this page.

Each phase-cluster converter output voltage $\dot{V}_{uv}$, $\dot{V}_{vw}$, $\dot{V}_{wu}$ of the MMCC-SDBC can be expressed as

$$\begin{bmatrix} \dot{V}_{uv} \\ \dot{V}_{vw} \\ \dot{V}_{wu} \end{bmatrix} = \begin{bmatrix} \dot{V}_{S,uv} \\ \dot{V}_{S,vw} \\ \dot{V}_{S,wu} \end{bmatrix} - \begin{bmatrix} \dot{V}_{L,uv} \\ \dot{V}_{L,vw} \\ \dot{V}_{L,wu} \end{bmatrix} \tag{21}$$

where $\dot{V}_{L,uv}$, $\dot{V}_{L,vw}$, and $\dot{V}_{L,wu}$ are the back EMFs of L_{ac}. $\dot{V}_{L,uv}$, $\dot{V}_{L,vw}$, and $\dot{V}_{L,wu}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{L,uv} \\ \dot{V}_{L,vw} \\ \dot{V}_{L,wu} \end{bmatrix} = j\omega_S L_{\mathrm{ac}} \begin{bmatrix} \dot{I}_{uv} \\ \dot{I}_{vw} \\ \dot{I}_{wu} \end{bmatrix} \tag{22}$$

where the resistance of L_{ac} is neglected. The maximum phase-cluster peak voltage and rms current of the MMCC-SDBC can be calculated in the same way as the MMCC-SSBC.

The line graphs in Fig. 5 show the normalized maximum phase-cluster peak voltage and rms current of the MMCC-SDBC under different types of the grid fault scenarios with respect to the voltage dip severity D. I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given in Table II. The normalized inductance of L_{ac} is set to be 6% with reference to the model mentioned in Table III. It is noted that the maximum phase-cluster peak voltage does not increase with regard to grid fault conditions. The maximum phase-cluster rms current increases rapidly when $D < 0.5$ under the phase-to-phase short-circuit fault and two-phase-to-ground fault, and reaches the over current level (1.25) decided by over junction temperature of the IGBT model, which will be discussed in the next section. When D approaches 0 under these faults, the current approaches to an infinite value, while the denominator of (20) is close to zero. When D is zero under these fault voltages, there is no solution of the zero-sequence current, and it is claimed to be the major problem of the MMCC-SDBC for the STATCOM application [9], [29]. The marks in Fig. 5 indicate simulation results using PLECS software, and the condition is shown in the next section. The calculation values correspond reasonably well with the PLECS simulation values based on the practical scaled STATCOM model.

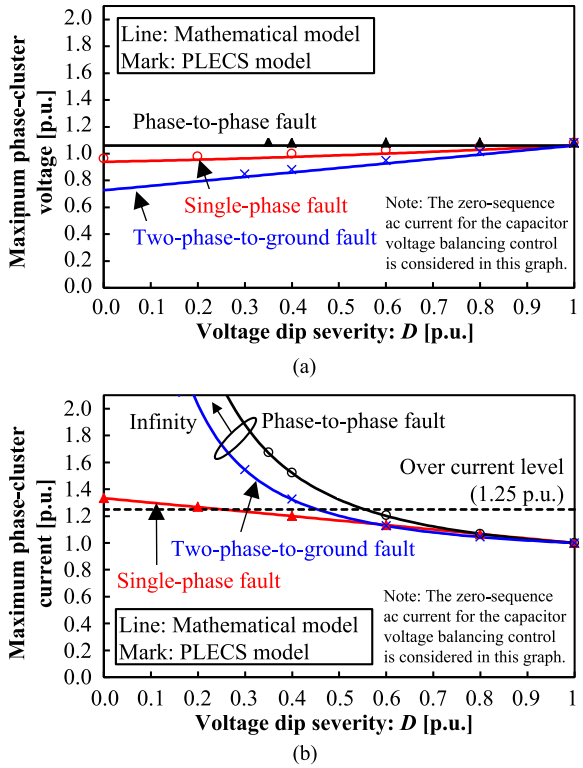


Fig. 5. Maximum phase-cluster output of the MMCC-SDBC corresponding to various grid fault scenarios. (a) Maximum phase-cluster peak voltage. (b) Maximum phase-cluster rms current.

$$\begin{bmatrix} \dot{V}_{S,uv} \\ \dot{V}_{S,vw} \\ \dot{V}_{S,wu} \end{bmatrix} = \sqrt{3} \begin{bmatrix} \dot{V}_{S,dq}^+ e^{j\pi/6} + \dot{V}_{S,dq}^- e^{-j\pi/6} \\ \dot{V}_{S,dq}^+ e^{-j\pi/2} + \dot{V}_{S,dq}^- e^{j\pi/2} \\ \dot{V}_{S,dq}^+ e^{j5\pi/6} + \dot{V}_{S,dq}^- e^{-j5\pi/6} \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{2}\left\{\left(\sqrt{3}V_{S,d}^+ + \sqrt{3}V_{S,d}^- + \sqrt{3}V_{S,q}^-\right) + j\left(V_{S,d}^+ - V_{S,d}^- + \sqrt{3}V_{S,q}^-\right)\right\} \\ \sqrt{3}\left\{-V_{S,q}^- + j\left(-V_{S,d}^+ + V_{S,d}^-\right)\right\} \\ \frac{\sqrt{3}}{2}\left\{\left(V_{S,q}^- - \sqrt{3}V_{S,d}^+ - \sqrt{3}V_{S,d}^-\right) + j\left(V_{S,d}^+ - V_{S,d}^- - \sqrt{3}V_{S,q}^-\right)\right\} \end{bmatrix} \tag{19}$$

$$\begin{aligned} \dot{I}^0 = {} & \frac{I_{S,q}^+\left(V_{S,d}^- V_{S,d}^- - V_{S,d}^- V_{S,d}^+ - V_{S,q}^- V_{S,q}^-\right) + I_{S,q}^- V_{S,d}^+\left(V_{S,d}^+ - V_{S,d}^-\right) - I_{S,d}^- V_{S,d}^+ V_{S,q}^-}{\sqrt{3}\left(V_{S,d}^- V_{S,d}^- - V_{S,d}^+ V_{S,d}^+ + V_{S,q}^- V_{S,q}^-\right)} \\ & + j\frac{I_{S,q}^+\left(V_{S,d}^- V_{S,q}^- + V_{S,d}^- V_{S,q}^- + V_{S,d}^+ V_{S,q}^-\right) + I_{S,d}^- V_{S,d}^+\left(V_{S,d}^+ + V_{S,d}^-\right) - I_{S,q}^- V_{S,d}^+ V_{S,q}^-}{\sqrt{3}\left(V_{S,d}^- V_{S,d}^- - V_{S,d}^+ V_{S,d}^+ + V_{S,q}^- V_{S,q}^-\right)} \end{aligned} \tag{20}$$

D. MMCC-DSCC With Circulating DC Current and DC Voltage Between P and N Terminals

The DSCC has two neutral points P and N in each single star connection. The differential voltage $V_{\rm PN}$ between P and N is normally 50% of the rated dc-link voltage in each converter cell in the DSCC in order to output ac voltage using the chopper converter cells. When the circulating dc current is injected in each leg of the DSCC, the circulating current and the $V_{\rm PN}$ formulate the independent active power between the legs in the MMCC-DSCC. This phenomenon is used for the dc-link capacitor voltage-balancing control among the legs under asymmetrical grid fault conditions, whose value is solved as follows.

The instantaneous active power on $\alpha\beta 0$ frame $p_{S,\alpha}$, $p_{S,\beta}$, $p_{S,0}$ of the MMCC-DSCC arising from asymmetrical reactive power supply can be expressed as

$$\begin{bmatrix} p_{S,\alpha} \\ p_{S,\beta} \\ p_{S,0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} \frac{1}{2}\Re\left[\dot{V}^*_{S,u} \cdot \dot{I}_{S,u}\right] \\ \frac{1}{2}\Re\left[\dot{V}^*_{S,v} \cdot \dot{I}_{S,v}\right] \\ \frac{1}{2}\Re\left[\dot{V}^*_{S,w} \cdot \dot{I}_{S,w}\right] \end{bmatrix} \tag{23}$$

where $\dot{V}_{S,u}$, $\dot{V}_{S,v}$, and $\dot{V}_{S,w}$ are the same as in (9), and $\dot{I}_{S,u}$, $\dot{I}_{S,v}$, and $\dot{I}_{S,w}$ are the same as in (10). It is noted that $p_{S,\alpha}$ and $p_{S,\beta}$ are the instantaneous active power imbalances among the phases. $p_{S,0}$ denotes the instantaneous active power of the three-phase MMCC-DSCC. Normally, each converter cell of the MMCC-DSCC has injected dc-bias voltage with 50% of modulation factor in order to output ac (+/−) voltage using chopper cells in which the dc-bias voltage appears to be the differential voltage $V_{\rm PN}$ between P and N terminals. $V_{\rm PN}$ can be expressed as

$$V_{\rm PN} = 2\sqrt{\frac{2}{3}} V_s \alpha_{\rm mgn} \tag{24}$$

where $\alpha_{\rm mgn}$ is the ratio between maximum converter output voltage and rated grid voltage and is used as a design margin. The circulating currents of each of leg $i_{z,u}$, $i_{z,v}$, and $i_{z,w}$ can be expressed as

$$\begin{bmatrix} i_{z,u} \\ i_{z,v} \\ i_{z,w} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} i_{uu} + i_{ul} \\ i_{vu} + i_{vl} \\ i_{wu} + i_{wl} \end{bmatrix}. \tag{25}$$

Based on (23) and (24), the circulating currents to cancel out the instantaneous active power imbalance among the phases arising by the asymmetrical reactive power output operation can be expressed as

$$\begin{bmatrix} i_{z,u} \\ i_{z,v} \\ i_{z,w} \end{bmatrix} = \frac{1}{V_{\rm PN}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} P_{S,\alpha} \\ P_{S,\beta} \end{bmatrix}. \tag{26}$$

The ac component of each arm output voltage $\dot{V}_{\rm PU,ac}$, $\dot{V}_{\rm PV,ac}$, $\dot{V}_{\rm PW,ac}$, $\dot{V}_{\rm NU,ac}$, $\dot{V}_{\rm NV,ac}$, and $\dot{V}_{\rm NW,ac}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{\rm PU,ac} \\ \dot{V}_{\rm PV,ac} \\ \dot{V}_{\rm PW,ac} \\ \dot{V}_{\rm UN,ac} \\ \dot{V}_{\rm VN,ac} \\ \dot{V}_{\rm WN,ac} \end{bmatrix} = \begin{bmatrix} -\dot{V}_{S,u} \\ -\dot{V}_{S,v} \\ -\dot{V}_{S,w} \\ \dot{V}_{S,u} \\ \dot{V}_{S,v} \\ \dot{V}_{S,w} \end{bmatrix} - \begin{bmatrix} \dot{V}_{L,uu} \\ \dot{V}_{L,vu} \\ \dot{V}_{L,wu} \\ \dot{V}_{L,wu} \\ \dot{V}_{L,vl} \\ \dot{V}_{L,wl} \end{bmatrix} \tag{27}$$

where $\dot{V}_{L,uu}$, $\dot{V}_{L,vu}$, $\dot{V}_{L,wu}$, $\dot{V}_{L,ul}$, $\dot{V}_{L,vl}$, and $\dot{V}_{L,wl}$ are the back EMFs of $L_{\rm ac}$. $\dot{V}_{L,uu}$, $\dot{V}_{L,vu}$, $\dot{V}_{L,wu}$, $\dot{V}_{L,ul}$, $\dot{V}_{L,vl}$, and $\dot{V}_{L,wl}$ can be expressed as

$$\begin{bmatrix} \dot{V}_{L,ul} \\ \dot{V}_{L,vl} \\ \dot{V}_{L,wl} \end{bmatrix} = -\begin{bmatrix} \dot{V}_{L,uu} \\ \dot{V}_{L,vu} \\ \dot{V}_{L,wu} \end{bmatrix} = j\frac{\omega_S L_{\rm ac}}{2} \begin{bmatrix} \dot{I}_{S,u} \\ \dot{I}_{S,v} \\ \dot{I}_{S,w} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} \dot{V}_{L,u} \\ \dot{V}_{L,v} \\ \dot{V}_{L,w} \end{bmatrix} \tag{28}$$

where the resistance of $L_{\rm ac}$ is neglected. $\dot{V}_{L,u}$, $\dot{V}_{L,v}$, and $\dot{V}_{L,w}$ are given in (14). The maximum arm output peak voltage $V_{\rm max\_pu}$ between the arm converters normalized by rated grid voltage $\sqrt{2/3}V_S$ can be expressed as (29) shown at the bottom of this page.

Each arm output rms current $i_{uu,\rm rms}$, $i_{vu,\rm rms}$, $i_{wu,\rm rms}$, $i_{ul,\rm rms}$, $i_{vl,\rm rms}$, and $i_{wl,\rm rms}$ can be expressed as

$$\begin{bmatrix} i_{uu,\rm rms} \\ i_{vu,\rm rms} \\ i_{wu,\rm rms} \end{bmatrix} = \begin{bmatrix} i_{ul,\rm rms} \\ i_{vl,\rm rms} \\ i_{wl,\rm rms} \end{bmatrix} = \begin{bmatrix} \sqrt{\left(\frac{|\dot{I}_{S,u}|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,u}}{2}\right)^2} \\ \sqrt{\left(\frac{|\dot{I}_{S,v}|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,v}}{2}\right)^2} \\ \sqrt{\left(\frac{|\dot{I}_{S,w}|}{\sqrt{2}}\right)^2 + \left(\frac{i_{z,w}}{2}\right)^2} \end{bmatrix}. \tag{30}$$

The maximum arm output rms current $I_{\rm max\_pu}$ normalized by the rated arm current of STATCOM $1/2I_r$ can be expressed as

$$I_{\rm max\_pu} = \frac{\max\left(i_{uu,\rm rms}, i_{vu,\rm rms}, i_{wu,\rm rms}\right)}{I_r/2}. \tag{31}$$

The line graphs in Fig. 6 show the calculated result of the normalized maximum arm output peak voltage and rms current of the MMCC-DSCC under different types of grid fault scenarios with regard to the voltage dip severity D by using (29) and (31). I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given in Table II. The normalized inductance of

$$V_{\rm max\_pu} = \frac{V_{\rm PN} + \max\left(\left|\dot{V}_{\rm PU,ac}\right|, \left|\dot{V}_{\rm PV,ac}\right|, \left|\dot{V}_{\rm PW,ac}\right|, \left|\dot{V}_{\rm UN,ac}\right|, \left|\dot{V}_{\rm VN,ac}\right|, \left|\dot{V}_{\rm WN,ac}\right|\right)}{\sqrt{\frac{2}{3}}V_s} \tag{29}$$

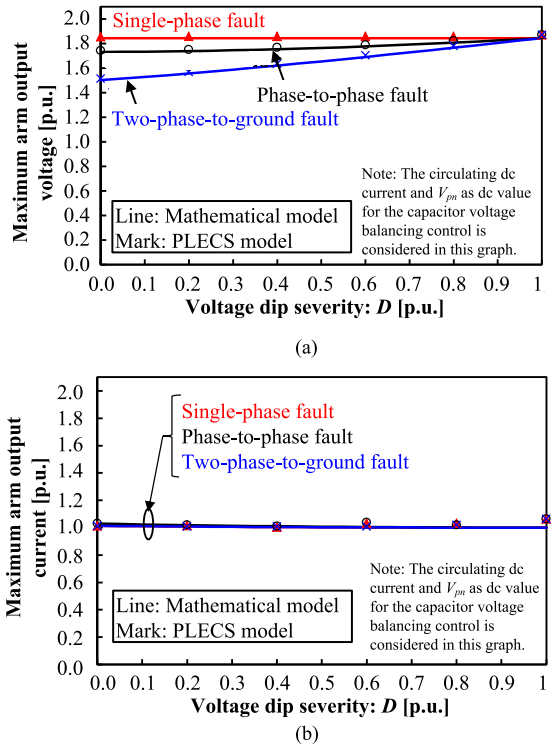


Fig. 6. Maximum arm output of the MMCC-DSCC corresponding to various grid fault scenarios. (a) Maximum arm output peak voltage. (b) Maximum arm output rms current.

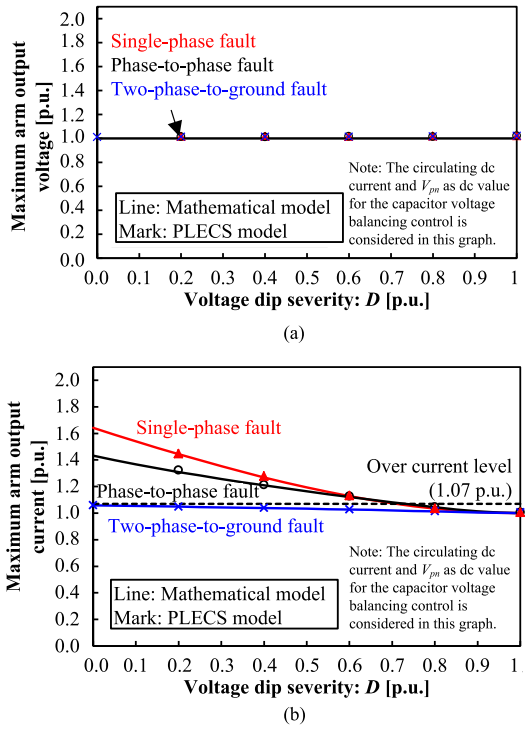


Fig. 7. Maximum arm output of the MMCC-DSBC corresponding to various grid fault scenarios. (a) Maximum arm output peak voltage. (b) Maximum arm output rms current.

$L_{\rm ac}$ is set to be 6%; $\alpha_{\rm mgn}$ is set to be 1.127 with reference to the practical scaled model mentioned in Table III. It is noted that the maximum arm output peak voltage and rms current do not increase significantly under different grid fault conditions. The marks in Fig. 6 plot the simulation result using the PLECS software, whose simulation conditions are shown in the next section. The calculated values correspond reasonably well to the PLECS simulation values based on the practical scaled STATCOM model.

E. MMCC-DSBC With Circulating DC Current and DC Voltage Between P and N Terminals

The operation principle of the MMCC-DSBC is almost the same as that of the MMCC-DSCC. The only difference is the amplitude of $V_{\rm PN}$. In the case of the MMCC-DSBC, each of the arms is able to supply ac (+/−) voltage without $V_{\rm PN}$ because of the used H-bridge converter cells. However, due to the voltage-balancing control, $V'_{\rm PN}$ is required, which can be expressed as

$$V'_{\rm PN} = \alpha_{\rm DSBC} V_{\rm PN} \tag{32}$$

where $\alpha_{\rm DSBC}$ is the amplitude ratio of the differential voltage between P and N terminals of the DSCC to the DSBC. The injectable $\alpha_{\rm DSBC}$ is normally less than 20% in order to avoid the voltage saturation when the DSBC is designed practically. The maximum value of $\alpha_{\rm DSBC}$ considering the grid fault condition can be expressed as (33) shown at the bottom of this page, where $\dot{V}_{\rm PU,ac}$, $\dot{V}_{\rm PV,ac}$, $\dot{V}_{\rm PW,ac}$, $\dot{V}_{\rm UN,ac}$, $\dot{V}_{\rm VN,ac}$, and $\dot{V}_{\rm WN,ac}$ are mentioned in (27). It is noted that the circulating dc current of the DSBC becomes larger than that of the DSCC because $V'_{\rm PN}$ for the DSBC becomes smaller than that for the DSCC. The maximum arm output voltage and current can be solved in the same way as that of the MMCC-DSCC.

The line graphs in Fig. 7 show the calculated result of the normalized maximum arm output peak voltage and rms current of the MMCC-DSBC under different types of grid fault scenarios with respect to the voltage dip severity D. I_q^+ is set to be the rated phase current value as $\sqrt{2}I_r$. The grid voltage is given in Table II. The normalized inductance of $L_{\rm ac}$ is set to be 6%; $\alpha_{\rm mgn}$ is set to be 1.127 with reference to the practical scaled model given in Table III. The marks are the practical scaled simulation results, whose test conditions will be shown in the next section. It is noted that the maximum arm peak voltage tracks 1 p.u. by the injected $V'_{\rm PN}$ as the designed maximum value. The maximum arm rms current increases moderately with respect to D but reaches the over current level (1.07), which is decided

$$\alpha_{\rm DSBC} = \frac{\sqrt{\frac{2}{3}} V_s \alpha_{\rm mgn} - \max\left(\left|\dot{V}_{\rm PU,ac}\right|, \left|\dot{V}_{\rm PV,ac}\right|, \left|\dot{V}_{\rm PW,ac}\right|, \left|\dot{V}_{\rm UN,ac}\right|, \left|\dot{V}_{\rm VN,ac}\right|, \left|\dot{V}_{\rm WN,ac}\right|\right)}{\sqrt{\frac{2}{3}} V_s \alpha_{\rm mgn}} \tag{33}$$

by the over junction temperature of the IGBT module, which is shown in the next section. The arm current becomes larger than the DSCC because of the lower V'_{PN}. The over current level becomes lower than that of the SDBC because the current distribution between the IGBT modules in a converter cell increases by injected dc voltage and current for the capacitor voltage-balancing method. The marks in Fig. 7 show the simulation result using PLECS software, whose conditions are given in the next section. The calculated values correspond reasonably well to the PLECS simulation values based on the practical scaled STATCOM model.

V. Performance Benchmark of MMCC Solutions

A. Electrical and Thermal Simulation Modeling

In this paper, the LVRT capability of a STATCOM that is based on the MMCC with SSBC, SDBC, DSCC, and DSBC is simulated by using the PLECS software. The three types of grid fault voltage are given by the voltage vector mentioned in Table II. The voltage is applied at the *Bus* B side of TR2, as shown in Fig. 2 and as discussed in Section II. In order to fix the standard voltage vectors applied to the MMCC, the impedance of TR2 is neglected. The specifications of the MMCC with SSBC, SDBC, and DSCC are assembled based on the parameters given in Table III. The reactive current reference is set to rated 1 p.u. of the positive-sequence only, as recent grid codes do not require negative sequence current to compensate for the asymmetrical grid voltage.

The modulation schemes for the MMCC with SSBC, SDBC, DSCC, and DSBC are selected on the basis of widely used phase-shift PWM, as mentioned in Section III.B. The output current is controlled by a dual-frame control scheme with sequence decoupling using a notch filter [30]. The capacitor voltage control method for SSBC is selected [11] using a zero-sequence ac voltage injection method. The capacitor voltage control method for SDBC is selected [12] using a zero-sequence ac current injection method. The capacitor voltage control method for DSCC is selected [13] using a circulating ac current injection method. The capacitor voltage control method for DSBC is selected [15] using a circulating dc current injection method.

The electrical losses and junction temperatures on each power semiconductor module are simulated by thermal simulation function on the PLECS. The electrical losses of the power semiconductor modules consist of the conduction loss of the IGBTs, turn ON/OFF loss of the IGBTs, conduction loss of the diodes, and recovery loss of the diodes in the power modules. The electrical loss parameters depending on the flowing currents, applied voltages, and junction temperatures are selected from the datasheets for the power modules mentioned in Table III [31]. The thermal network between the power semiconductor chip and heatsink for power module is constructed by a Foster *RC* network, as shown in Fig. 8. Here, p_S is the power loss of the IGBT chip; p_D is the power loss of the diode chip; T_{S_j} is the junction temperature of IGBT; T_{D_j} is the junction temperature of the diode; T_c is the case temperature in the power semiconductor module; T_h is the heat sink temperature; $R_S(j-cn)$, $\tau_D(j-cn)$, $R_S(j-cn)$, and $\tau_D(j-cn)$ are the thermal parameters for the

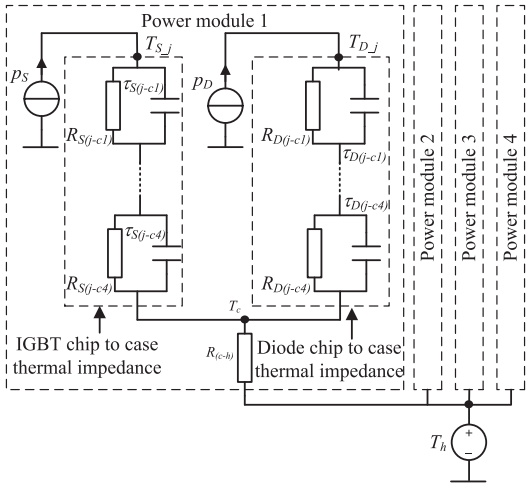


Fig. 8. Thermal network between power semiconductor chip and heat sink on each cell converter.

Foster RC network of the power semiconductor module (n = 1–4). The thermal impedances of the power modules are also selected from the datasheets. The heat sink temperature based on the liquid cooling system is considered as a constant value at 60 °C in this simulation model because the temperature of the heatsink is normally much lower and more stable compared with the junction temperature in a properly designed converter system.

B. Electrical and Thermal Simulations of the MMCC-SSBC

Fig. 9 shows the key waveforms of the MMCC-SSBC under the single-phase-to-ground fault with the dip severity *D* of 0.5 p.u. It can be seen that the peak value of the reference voltage increases by 22% maximum on *w* phase cluster under the single-phase-to-ground fault in order to inject zero-sequence voltage v_{zero} to balance the dc-link capacitor voltages of the converter cells. Here, the injected zero-sequence voltage is expressed by the following equation when all capacitor voltages are balanced:

$$v^*_{\mathrm{zero}} = \frac{v^*_{u1} + v^*_{v1} + v^*_{w1}}{3}. \tag{34}$$

Fig. 10 shows the junction temperatures of four IGBTs and diodes in cells *u*1, *v*1, and *w*1 under the same simulation conditions. The peak junction temperatures of the IGBT and diode are the same, 115 and 109 °C, respectively, among the different cluster cells. The temperatures are below the limit of 128 °C by considering a 15% margin for the IGBT modules with the absolute maximum rating of the junction temperature defined by the manufacturers.

Fig. 11 shows the maximum peak voltage command and the peak junction temperature of the IGBT and diode among the cells with respect to the dip severity *D* under various grid fault scenarios. It can be noted that the peak voltage command saturates with the single-phase-to-ground fault at $D = 0.5$ p.u. The maximum peak junction temperatures of the IGBT and diode are approximately 115 and 109 °C, respectively, regardless of the grid conditions.

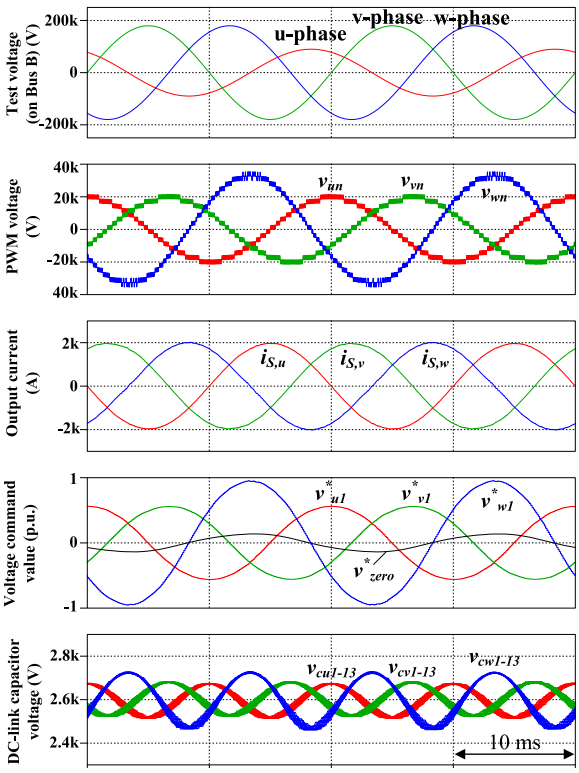


Fig. 9. Key waveforms of the MMCC-SSBC under single-phase fault with a dip severity D of 0.5 p.u.

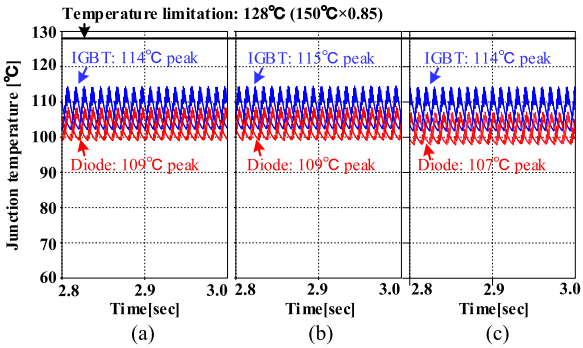


Fig. 10. Thermal distribution of the MMCC-SSBC under single-phase fault with dip severity D of 0.5 p.u. (a) $u1$ cell. (b) $v1$ cell. (c) $w1$ cell.

C. Electrical and Thermal Simulations of the MMCC-SDBC

Fig. 12 shows the simulated key waveforms of the MMCC-SDBC under the phase-to-phase fault with the dip severity D of 0.4 p.u. It can be noted that the peak value of the cluster current increases by maximum 52% at v and w clusters under the phase-to-phase fault in order to inject zero-sequence current i_{zero} to balance the dc-link capacitor voltages of the converter cells. Here, the injected zero-sequence current is expressed as

$$i_{\text{zero}} = \frac{i_{uv} + i_{vw} + i_{wu}}{3}. \tag{35}$$

Fig. 13 shows the junction temperatures of four IGBTs and diodes in $u1$, $v1$, and $w1$ cells under the same conditions.

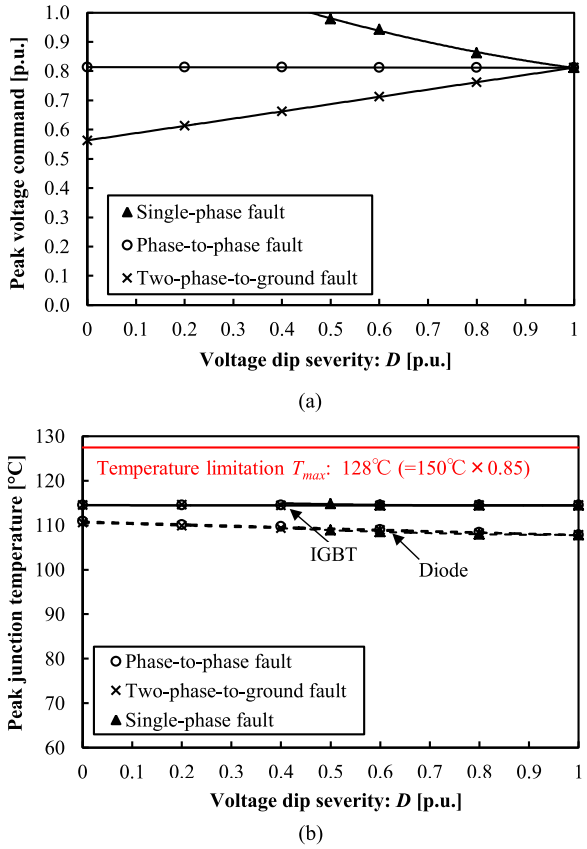


Fig. 11. Electrical–thermal simulations of the MMCC-SSBC at different dip severities. (a) Peak voltage command. (b) Peak junction temperature.

The peak junction temperatures increase to maximum 121 and 114 °C at the diodes and IGBTs of $v1$ and $w1$ cells. These temperatures are over the limit of 106 °C by considering a 15% margin for the IGBT modules with the absolute maximum rating of junction temperature defined by the manufacturers.

Fig. 14 shows the maximum peak voltage command and peak junction temperature among the cells for different dip severities D under various grid fault scenarios. It can be noted that the peak voltage command does not saturate under various grid fault scenarios. The peak junction temperatures increase quickly under phase-to-phase fault and two-phase-to-ground fault conditions and reach an upper limit temperature of 106 °C when the voltage dips are 0.55 and 0.45 p.u., respectively.

D. Electrical and Thermal Simulations of the MMCC-DSCC

Fig. 15 shows the simulated key waveforms of the MMCC-DSCC under the phase-to-phase fault with the dip severity D of 0 p.u. It can be noted that the arm currents (i.e., i_{uu}, i_{ul}, i_{vu}, i_{vl}, i_{wu}, and i_{wl}) contain both half-value of the output phase current and the circulating dc current i_{zu}, i_{zv}, and i_{zw} for the dc-link capacitor voltage balancing under asymmetrical grid fault conditions. Here, the circulating current is defined as

$$i_{Zu} = \frac{i_{uu} + i_{ul}}{2},\ i_{Zv} = \frac{i_{vu} + i_{vl}}{2},\ i_{Zw} = \frac{i_{wu} + i_{wl}}{2}. \tag{36}$$

It is noted that the rms value of the arm current increases by only a few percentages under the phase-to-phase fault.

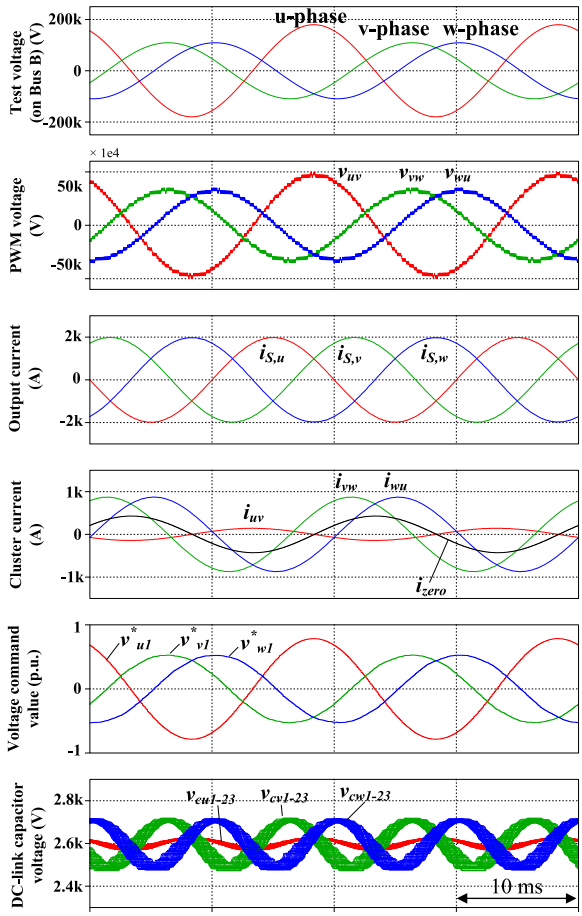


Fig. 12. Key waveforms of the MMCC-SDBC under phase-to-phase fault with a dip severity D of 0.4 p.u.

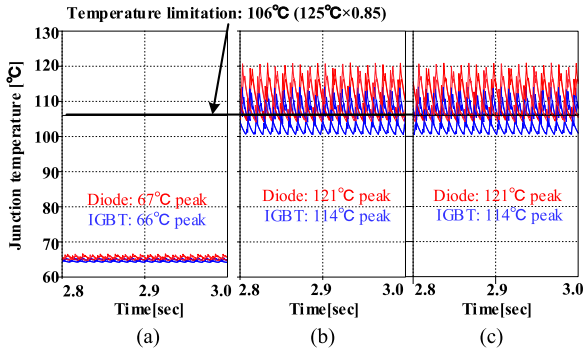


Fig. 13. Thermal distribution of the MMCC-SDBC under phase-to-phase fault with the dip severity D of 0.4 p.u. (a) $u1$ cell. (b) $v1$ cell. (c) $w1$ cell.

Fig. 16 shows the junction temperatures of IGBTs and diodes in chopper converter cells $uu1$, $vu1$, $wu1$, $ul1$, $vl1$, and $wl1$ under the same conditions. The junction temperatures are widely distributed among the arms compared with the other MMCC types because the chopper converter cells are used with different modulation factors among the arms. The peak junction temperature increases to maximum 104 °C at the diodes of $u1$ cells. This temperature is below the limit of 106 °C by considering a 15% margin for the IGBT modules with the absolute maximum rating of junction temperature defined by the manufacturers.

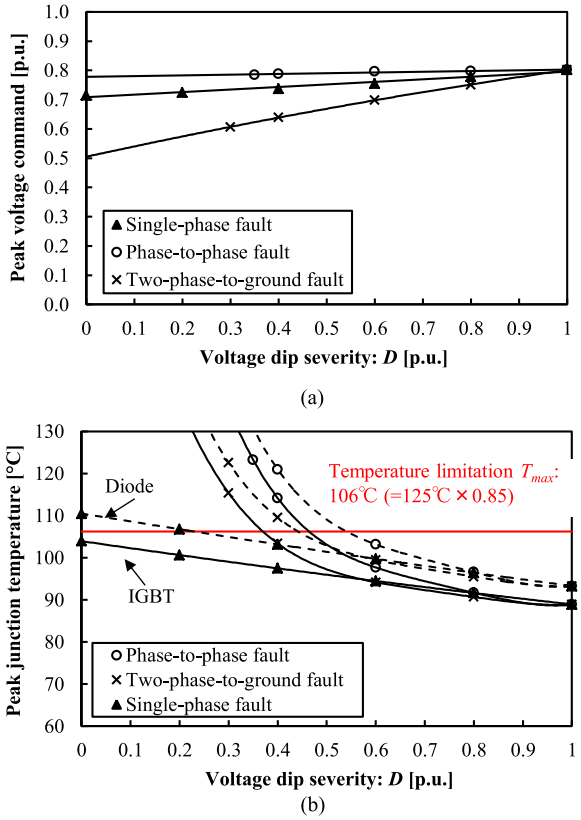


Fig. 14. Electrical–thermal simulations of the MMCC-SDBC at different dip severities. (a) Peak voltage command. (b) Peak junction temperature.

Fig. 17 shows the maximum peak voltage command value and peak junction temperature among the arms with regard to the voltage dip severity D under various grid fault scenarios. It can be noted that the peak voltage command does not saturate under various grid fault scenarios. The peak junction temperature does not reach the temperature limitation under various grid fault scenarios.

E. Electrical and Thermal Simulations of the MMCC-DSBC

Fig. 18 shows the simulated key waveforms of the MMCC-DSBC under the single-phase-to-ground fault with dip severity D of 0.4 p.u. It can be noted that the arm currents and PWM output voltage of each arm contain the dc component as well as the DSCC. However, the amplitude of the PWM output voltage with the dc component is smaller than the DSCC because it avoids the voltage saturation of each cell output voltage command. In this result, the circulating dc current increases for the capacitor voltage-balancing control.

Fig. 19 shows the junction temperatures of IGBTs and diodes in chopper converter cells $uu1$, $vu1$, $wu1$, $ul1$, $vl1$, and $wl1$ under the same conditions. The junction temperatures are widely distributed among the arms compared with the MMCC-SDBC because of the injected dc component with different modulation factors among the arms. The peak junction temperature increases to maximum 104 °C at the diodes of $uu1$ cells. This

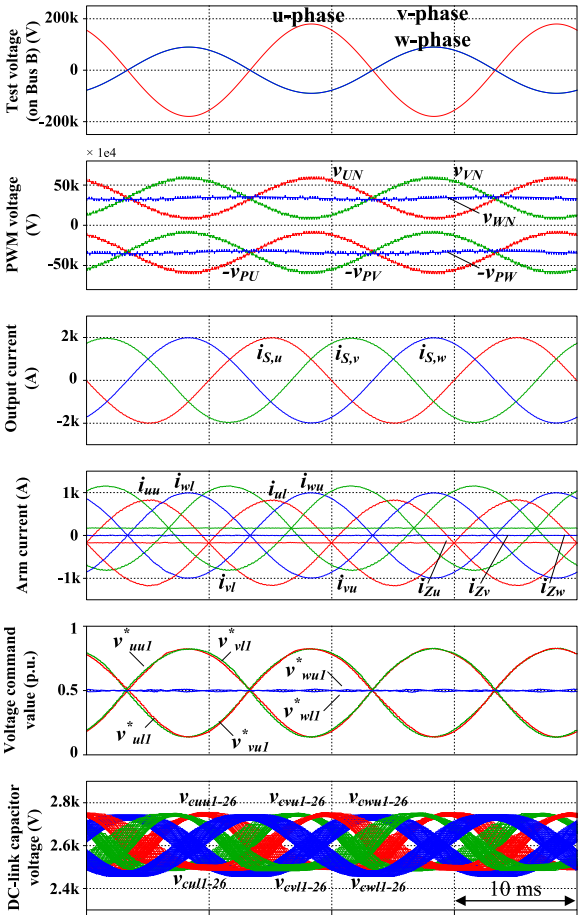


Fig. 15. Key waveforms of the MMCC-DSCC under phase-to-phase fault with a dip severity D of 0 p.u.

temperature is below the limit of 106 °C by considering a 15% margin for the IGBT modules with the absolute maximum rating of junction temperature defined by the manufacturers.

Fig. 20 shows the maximum peak voltage command value and peak junction temperature among the arms with regard to dip severity D under various grid fault scenarios. It can be noted that the peak voltage command keeps the same value under various grid fault conditions with different voltage dip severities because V_{PN} is injected to a maximum value to minimize the amplitude of the circulating dc current. The peak junction temperatures exceed the limitation value when D is lower than 0.6. However, the slope is moderate compared with that of the SDBC.

F. Performance Comparison Between the MMCC Family

Fig. 21(a) shows the reactive current compensation capability for the MMCC solutions with SSBC, SDBC, DSCC, and DSBC to enable a proper voltage balancing under different dip severities D with various grid faults. The compensation capability limits of MMCC family are determined by the modulation saturation point and maximum junction temperature. Fig. 21(b) and (c) plots the peak voltage command and peak junction temperature of the IGBT modules in the whole converter cells corresponding to the operating conditions in panel (a). The peak

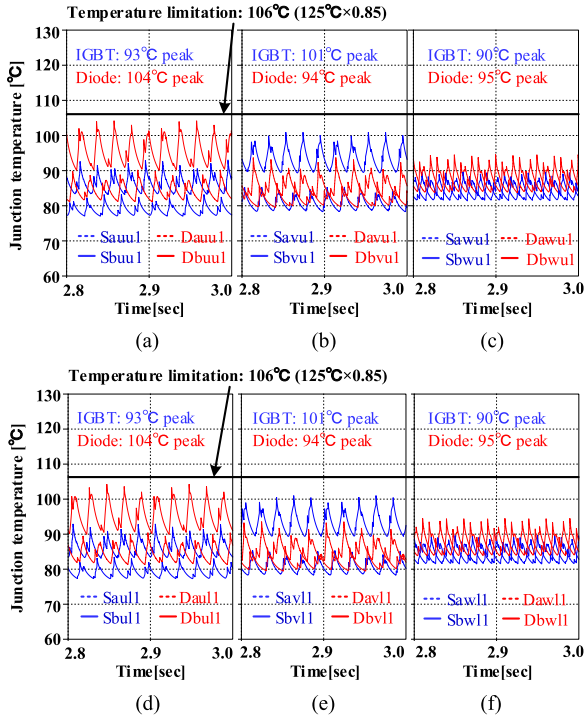


Fig. 16. Thermal distribution of the MMCC-DSCC under phase-to-phase fault with a dip severity D of 0 p.u. (a) $uu1$ cell. (b) $vu1$ cell. (c) $wu1$ cell. (d) $ul1$ cell. (e) $vl1$ cell. (f) $wl1$ cell.

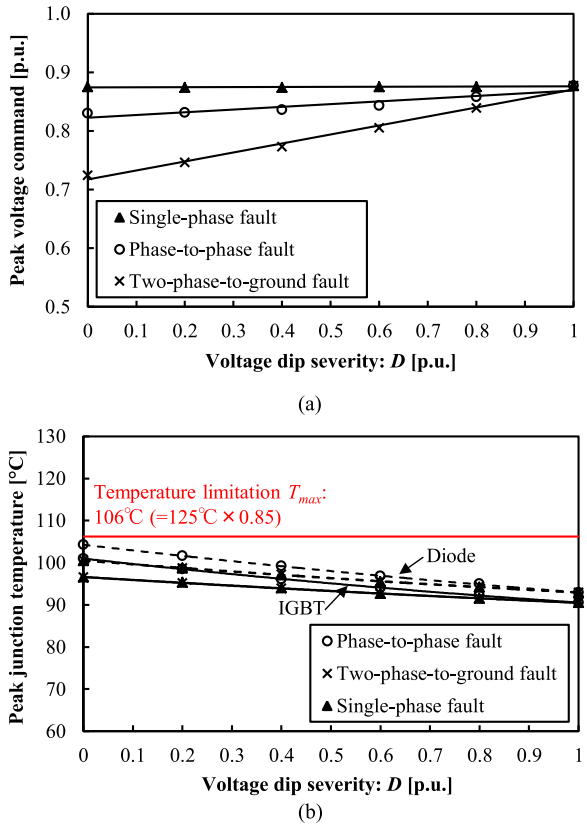


Fig. 17. Electrical–thermal simulations of the MMCC-DSCC at different dip severities. (a) Peak voltage command. (b) Peak junction temperature.

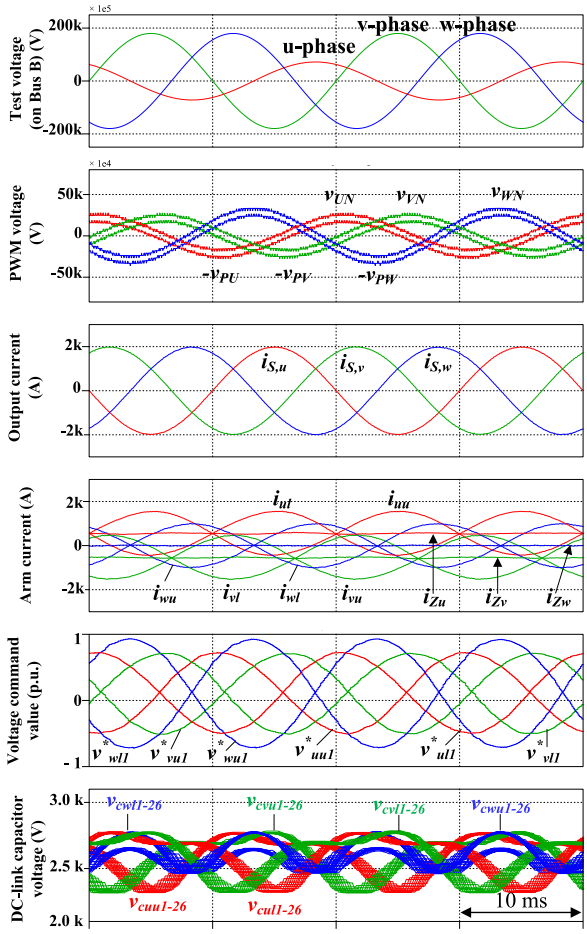


Fig. 18. Key waveforms of the MMCC-DSBC under single-phase-to-ground fault with a dip severity D of 0.4 p.u.

voltage command and junction temperature are normalized by instantaneous dc-link voltage of each cell converter and the temperature limitation value decided by the manufacturers, as mentioned in Section V.B–D. The MMCC family can continue to supply the rated reactive current when the dip severity of the grid voltage is higher than 0.7 p.u., but the reactive current compensation capability shows different characteristics for the dip severity lower than 0.7 p.u. as discussed in the following.

1) *MMCC-SSBC:* It reveals that the SSBC can supply the rated reactive current under phase-to-phase fault and two-phase-to-ground fault conditions regardless of the dip severity. However, the reactive current capability decreases sharply at a voltage dip severity of 0.4 p.u. under single-phase-to-ground fault, and it cannot operate anymore even if the current derates because of the saturation of peak voltage command by the zero-sequence ac voltage injection. It seems that this characteristic is problematic in practical use.
2) *MMCC-SDBC:* The SDBC can supply the reactive current by a few percentages of reactive current derating under single-phase-to-ground fault to avoid over junction temperature by slightly increased zero-sequence ac current. The SDBC can also keep the operation under phase-to-phase short fault and two-phase-to-ground fault

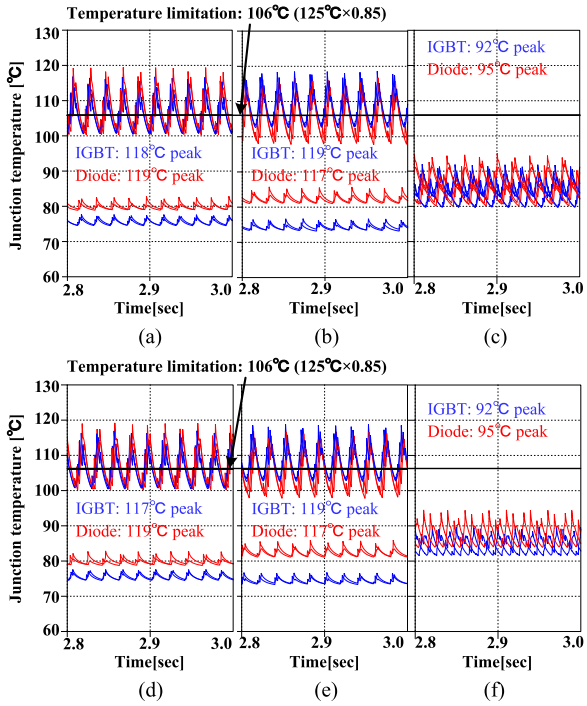


Fig. 19. Thermal distribution of the MMCC-DSBC under single-phase-to-ground fault with a dip severity D of 0.4 p.u. (a) *uu*1 cell. (b) *vu*1 cell. (c) *wu*1 cell. (d) *ul*1 cell. (e) *vl*1 cell. (f) *wl*1 cell.

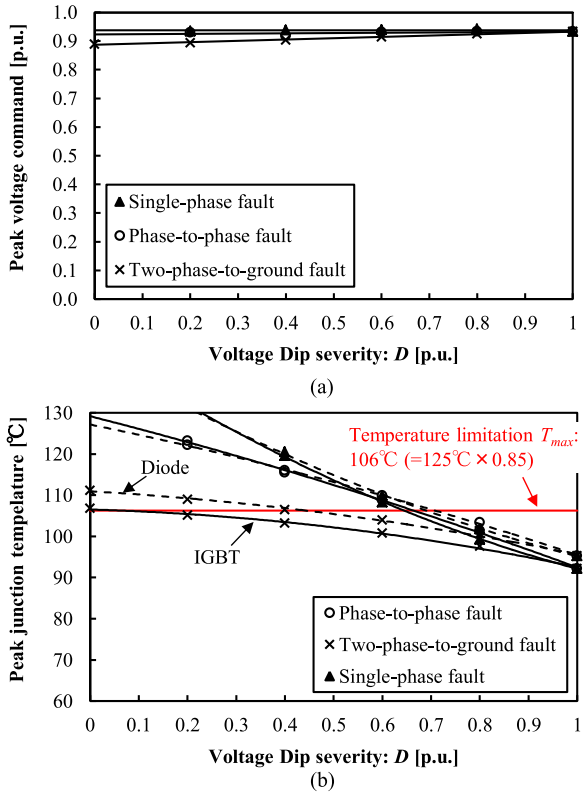


Fig. 20. Electrical–thermal simulations of the MMCC-DSBC at different dip severities. (a) Peak voltage command. (b) Peak junction temperature.

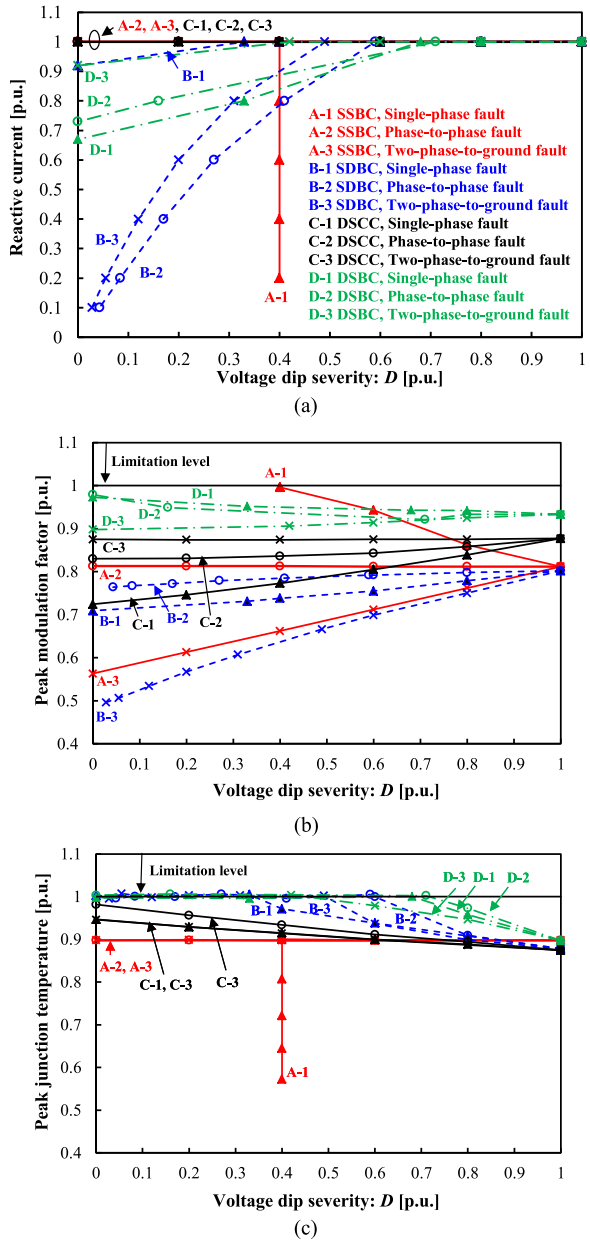


Fig. 21. Reactive current compensation capability of the MMCCs for different dip severities. (a) Reactive current capability. (b) Voltage command according to the reactive current. (c) Junction temperature according to the reactive current.

due to a larger reactive current derating, which seems to be a better characteristic than the SSBC. However, the required zero-sequence current is dramatically increased toward an infinite value when the voltage dip severity approaches zero under the phase-to-phase short-circuit fault and two-phase-to-ground fault, as explained theoretically in Section III.

3) *MMCC-DSCC:* The DSCC could be injected with circulating dc current having two degrees of freedom to balance the dc-link capacitor voltages under asymmetrical grid fault conditions. The amplitude of the circulating dc current becomes smaller than the zero-sequence ac current for the SDBC, which has only one degree of freedom. In this outcome, the DSCC can supply the reactive current under all grid fault scenarios without reactive current derating in this STATCOM case.

4) *MMCC-DSBC:* The dc-link capacitor voltage-balancing method for the DSBC is similar to that for the DSCC. However, the amplitude of the circulating dc current on the DSBC attains a larger value compared with that of the DSCC in compensation for a lower injectable dc voltage capability between P and N terminals. The DSBC can keep the operation under all grid fault scenarios with a maximum of 35% current derating to avoid the over junction temperature, whose characteristics are worse than those of the DSCC but much better than those of the SSBC and SDBC.

VI. Conclusion

This paper investigates the performances of four configurations of the MMCC family with SSBC, SDBC, DSCC, and DSBC for the STATCOM in large-scale offshore wind power plants, with a special focus on asymmetrical LVRT capability under various grid faults. The sizing of the key components, the number of cells, electrothermal analysis, mathematical analysis under asymmetrical reactive power output condition by considering the dc-link capacitor voltage balancing control and the reactive current capability of a practical 80-MVar/33-kV-scaled MMCC-based STATCOM are presented.

The practically designed SSBC and SDBC have unavailable LVRT operating conditions under some of the grid fault conditions because of the dc-link capacitor voltage control. The DSCC can keep the operation in all grid fault scenarios for the whole voltage dip severity without any current derating. However, the total volume of the MMCC-DSCC seems larger than those of other MMCC solutions because the total energy stored in the capacitors becomes larger by using chopper converter cells. The DSBC can keep the operation in all grid fault scenarios for the whole dip severity with a maximum of 35% current derating in this case study. The total cost and volume of the DSBC seem similar to those of SSBC and SDBC because of the similar total power semiconductor chip area and the total energy stored in the passive components. The present result suggests that the DSBC becomes the most attractive solution for the STATCOM application on the MMCC family.

As a future work, the asymmetrical faulty grid voltage recovering performance of the DSBC-based STATCOM by using a negative-sequence reactive current injection method will be studied, which becomes a most advanced requirement emerging in a European country as an optional code.

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