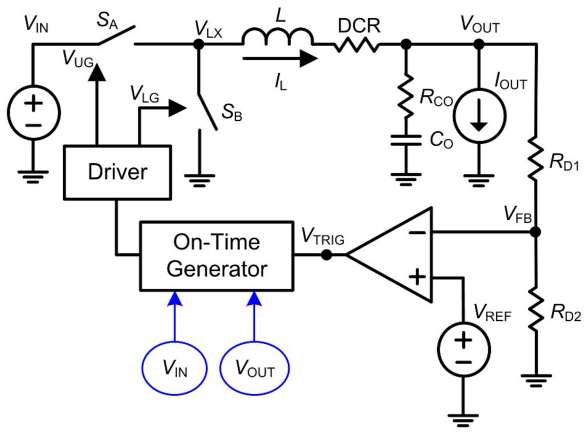
A Novel Dynamic Ramp Valley Control in a Current-Mode Adaptive On-Time Controller for the On-Chip Buck Converter

Wen-Wei Chen, *Member, IEEE*, and Jih-Sheng Lai, *Fellow, IEEE*

***Abstract*—This paper proposes a novel dynamic ramp valley control in a current-mode adaptive on-time controller for the on-chip buck converter. It improves the system stability and reduces the output voltage under the load-dump. The proposed novel dynamic ramp valley control uses a sample and hold circuit, a comparator, and a ramp valley control to avoid the generation of an erroneous pulse signal while regulating the output voltage under the load-dump. Finally, a buck converter with 12 to 19 V input voltage range and 1.05 V output voltage with the novel dynamic ramp valley control is implemented in an integrated circuit. Based on the hardware experimental results, the output voltage under the load-dump with and without the proposed dynamic ramp valley control is 156 and 224 mV, respectively. Thus, the output voltage with the proposed dynamic ramp valley control is lower by 68 mV than that without the proposed dynamic ramp valley control, avoiding the potential damage of the output load, moreover, this performance has been verified with the SIMPLIS simulation and hardware experimental results.**

***Index Terms*—Adaptive on-time (AOT) controller, current-mode, dynamic ramp valley control, erroneous pulse, load-dump.**



I. Introduction

THE conventional fixed-frequency pulsewidth-modulated (PWM) control scheme for power converters [1]–[13] normally employs the current-mode control instead of the voltage-mode control to improve the transient response with a fast current feedback loop.

The adaptive on-time (AOT) controller for the buck converter is extensively used to improve efficiency because they can minimize switching frequency and reduce switching-related losses [14]–[22]. It also has a faster transient response than the traditional voltage-mode and current-mode control [14]–[22], because, the current-mode AOT control circuit can generate multiple pulses with a minimum off-time mechanism to prevent $V_{\rm OUT}$ from decreasing significantly. The current-mode AOT control circuit is useful for the reduction of $V_{\rm OUT}$ peak-to-peak voltage

Manuscript received April 7, 2018; revised June 28, 2018; accepted August 7, 2018. Date of publication August 21, 2018; date of current version April 20, 2019. This work was supported by the Ministry of Science and Technology of Taiwan under Award MOST 106-2917-I-564-010. Recommended for publication by Associate Editor P. S. Shenoy. *(Corresponding author: Wen-Wei Chen.)*

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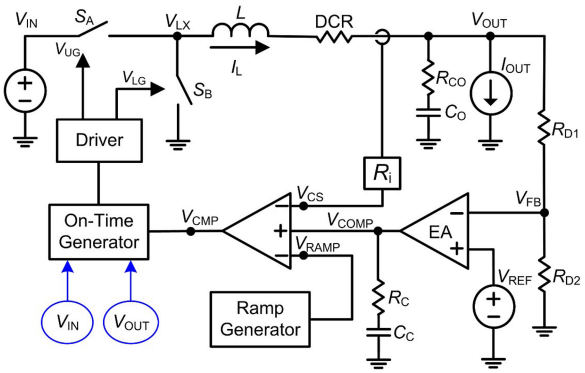

Fig. 2. Current-mode AOT controller for buck converter.

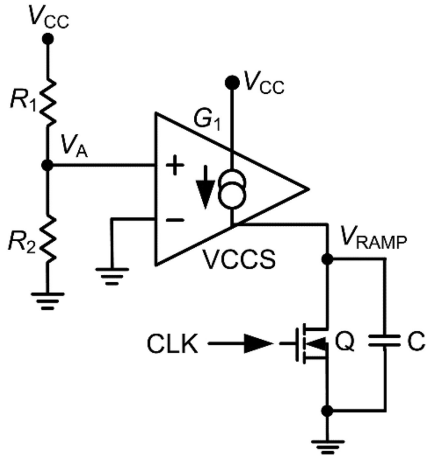

Fig. 3. Circuit diagram of ramp generator for the current-mode AOT controller.

Fig. 2 shows the circuit diagram of a current-mode AOT controller for buck converter [5]. In the diagram, S_A and S_B are the switches, L is the output inductor, DCR is the dc resistor of the inductor, R_i is a current sense ratio that is used to transfer an inductor-current signal to a voltage signal $V_{\rm CS}$, and $R_{\rm CO}$ is the ESR of output capacitor C_O. The driver circuit uses the output of on-time generator to produce two gate drive signals $V_{\rm UG}$ and $V_{\rm LG}$ for upper and lower switches S_A and S_B, respectively. These two signals should not be turned ON at the same time to avoid shoot-through problems. The diagram shows that the output voltage ripple, which includes inductor-current information, can be directly used as the ramp for modulation. Current source $I_{\rm OUT}$ is the output load, and R_{D1} and R_{D2} are the feedback resistors that determine the output voltage. The compensation of R_C and C_C should have an optimal design to increase the transient response, if the system simply connects R_C, and it makes the system operate at load line status. Only the feedback signal $V_{\rm FB}$ and reference voltage $V_{\rm REF}$ are built internal of the IC. The output signal $V_{\rm CMP}$ of the comparator depends on the results on the input signals $V_{\rm COMP}$, $V_{\rm CS}$, and $V_{\rm RAMP}$.

In addition, the current-mode AOT controller also has faster transient response than the conventional voltage-mode and current-mode controllers. The on-time generator circuit samples the $V_{\rm IN}$ and $V_{\rm OUT}$ signals to adjust the on-time width to control the driver circuit and to regulate the voltage.

There are two types of on-time control circuits for the current-mode AOT controller: constant frequency on-time control circuit and constant current ripple on-time control circuit [20]–[22]. The constant frequency on-time control circuit for the current-mode AOT controller samples $V_{\rm IN}$ and $V_{\rm OUT}$ controlling $T_{\rm ON}$ using the following equation:

$$T_{\rm ON} = \frac{V_{\rm OUT}}{V_{\rm IN}} \times \frac{R_1 \times C_1}{G_1}. \tag{1}$$

In this circuit, $V_{\rm OUT}$ needs to be monitored to limit the voltage of capacitor C_1 using (1). $V_{\rm OUT}$ divided by $V_{\rm IN}$ is the duty cycle, and R_1, C_1, and G_1 are constant values, similar to the switching period T_S, as shown in (1). G_1 is the gain of the voltage-controlled current source. Even if the input voltage $V_{\rm IN}$ and output voltage $V_{\rm OUT}$ are changed, the system still maintains the same switching frequency [20]–[22].

The constant current ripple on-time control circuit for the current-mode AOT controller also samples $V_{\rm IN}$ and $V_{\rm OUT}$ controlling $T_{\rm ON}$ using (2). The voltage drop between $V_{\rm IN}$ and $V_{\rm OUT}$ depends on the inductor current ripple, as shown in (3)

$$T_{\rm ON} = \frac{R_1}{V_{\rm IN} - V_{\rm OUT}} \times \frac{C_1 \times V_{\rm BIAS}}{G_1} \tag{2}$$

$$T_{\rm ON} = \frac{L}{V_{\rm IN} - V_{\rm OUT}} \times \Delta I_L \tag{3}$$

where G_1 is the gain of the voltage-controlled current source. $V_{\rm BIAS}$ is a voltage bias for on-time generation circuit. Therefore, even if the voltage drop between $V_{\rm IN}$ and $V_{\rm OUT}$ is changed, the inductor current ripple maintains a constant value, because the R_1, C_1, $V_{\rm BIAS}$, and G_1 are constant values. The constant current ripple on-time control circuit is suitable for applications with a large difference between input and output voltages and those require the same output voltage ripple [20]–[22] like voltage regulator for CPU application.

Fig. 3 shows the circuit diagram of the ramp generator for the current-mode AOT controller. The ramp compensation is designed according to the inductor current ripple, which is determined by the input voltage, output voltage, and inductance. A general control IC often imbeds a fixed ramp into the control loop, and this ramp can directly increase the noise immunity and prevent the system from suffering from a subharmonic issue [23]–[29]. The voltage V_A depends on $V_{\rm CC}$, which is also an input signal for voltage control current source (VCCS). The output signal of VCCS charges the capacitor C to generate the dynamic ramp $V_{\rm RAMP}$, which can be calculated using the following equation:

$$V_{\rm RAMP} = \frac{G_1 \times \left(V_{\rm CC} \times \frac{R_2}{R_1 + R_2}\right)}{C * T_S}. \tag{4}$$

The current-mode AOT controller for buck converter is similar to the current-mode controller for buck converter, but the on-time generator of the current-mode AOT controller is significantly different. Fig. 4 shows the simulation results, which

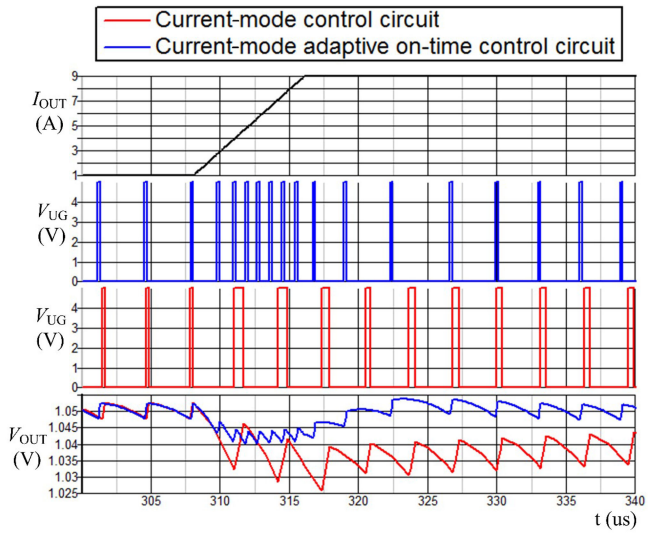

Fig. 4. Comparison between the current-mode AOT controller and the current-mode controller at the droop.

TABLE I
OPERATION CONDITIONS FOR THE CURRENT-MODE AOT CONTROLLER AND THE CURRENT-MODE CONTROLLER FOR BUCK CONVERTER

V_{IN}	19 V	F_S	320 kHz	L	2.2 µH
V_{OUT}	1.05 V	R_{D1}	8 kΩ	C_{OUT}	330 µF*2
I_{OUT}	1~9 A (8µs)	R_{D2}	20 kΩ	R_{CO}	5 mΩ
V_{REF}	0.75 V	R_C	1.5 MΩ	C_C	40 pF

can be used to compare the current-mode AOT controller with the current-mode controller at the droop. These simulation results use the same operation conditions to compare between the current-mode AOT controller and the current-mode controller, as shown in Table I. The current-mode AOT controller can generate multiple pulses with minimum off-time mechanism to prevent V_{OUT} from dropping significantly. The current-mode AOT controller is useful for the reduction of V_{OUT} peak-to-peak voltage at the droop. However, the current-mode controller can simply increase its PWM pulsewidth with the same switching frequency at the droop. The comparison between the current-mode AOT controller and the current-mode controller at the droop shows that the former can generate more PWM pulses than the latter. Therefore, the current-mode AOT controller can achieve a faster transient response than the current-mode controller.

II. NOVEL DYNAMIC RAMP VALLEY CONTROL IN CURRENT-MODE AOT CONTROLLER FOR BUCK CONVERTER

The current-mode AOT controller for buck converter can solve problems related to the AOT controller for buck converter, such as improving the noise immunity, and can use the low ESR of ceramic capacitors without leading to instability. For low duty cycle buck applications, as shown in Table I, the peak-to-peak of the output voltage at the load-dump tends to be much larger than the peak-to-peak of the output voltage at the droop for load current transients, as shown in Fig. 5.

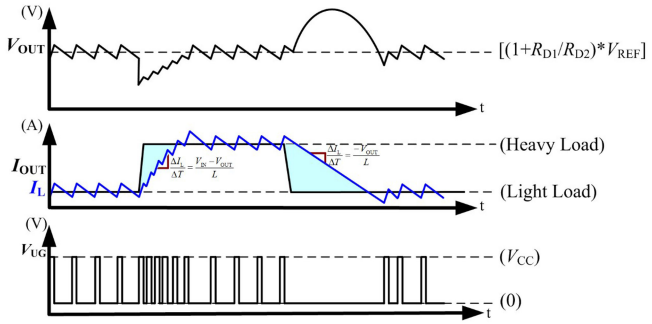

Fig. 5. Peak-to-peak of the output voltage at the load-dump tends to be much larger than the peak-to-peak of the output voltage at the droop for load current transients.

In a typical regulator application of the high input voltage 19 V to low output voltage 1.05 V, it should be recognized that the load-dump transient represents the worst case. In that case, the steady-state duty cycle is close to 5.5% and the inductor current falling slew rate when the duty cycle collapses to zero can be calculated using the following equation:

$$\frac{\Delta I_L}{\Delta T} = -\frac{V_{\mathrm{OUT}}}{L}. \tag{5}$$

Compared to the droop, the inductor current takes much faster to transition to the required level with the minimum on-time. However, at the load-dump, the surplus of charge in the output capacitor causes the output voltage to significantly overshoot, so the output load does not need more power from input power to output terminal and the control signal V_{UG} does not generate on-time pulse. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp down its nominal level following the load step at PWM mode. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and rein in the voltage overshoot, so the user must design for the larger overshoot criteria when choosing output capacitors.

However, the consumer's products are usually designed for a wide range of the input voltage, the output voltage, and the output load operation conditions, so it is very difficult to design an optimal compensator to avoid an erroneous pulse under the load-dump, so based on a worse condition, the current-mode AOT controller for buck converter may have easily in generating an erroneous pulse under the load-dump, as shown in Fig. 6, because the V_{COMP} signal should be regulated by the system loop. Thus, the V_{COMP} cannot decrease quickly under the load-dump, resulting in an erroneous pulse V_{UG} signal to turn ON the S_A switch. Such an erroneous pulse pushes the input source to deliver extra energy to the output load, and the output voltage is higher than its normal condition. In other words, a voltage higher than the normal output voltage can occur and damage the output load equipment. Based on this problem of a higher output voltage with an erroneous pulse at the load-dump, it has three major methods to solve this problem. The first method directly uses the charge balance controller to improve the peak-to-peak value of the output voltage ΔV_{OUT} at the droop and load-dump [30], [31] or implements an auxiliary circuit to reduce the higher

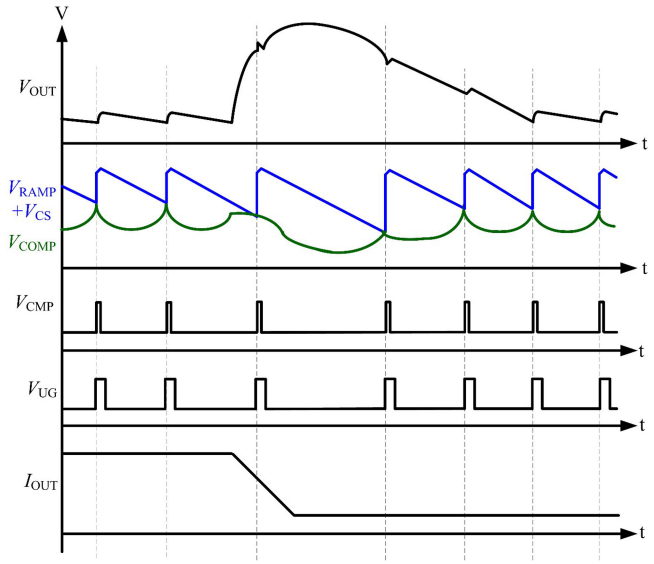

Fig. 6. Control signals for without the novel dynamic ramp valley control with an erroneous pulse under the load-dump.

output voltage with an erroneous pulse at the load-dump [32], [33]. These papers proposed the use of extra auxiliary circuits and more complicated control to control and drive the auxiliary switch directly [32], [33]. The auxiliary circuit uses an inductor, switch, and diode. However, the auxiliary circuit can also reduce the efficiency for extra switch and diode at the load-dump.

The second method is to use a Schottky diode to parallel the low-side switch S_B to increase the voltage drop of the inductor L at the load-dump using the following equation, so the voltage drop is equal to the output voltage and the forward voltage V_F of the Schottky diode [34], [35]:

$$\frac{\Delta I_L}{\Delta T} = -\frac{(V_{\rm OUT} + V_F)}{L}. \tag{6}$$

This method can make the inductor current ripple to become a sharp falling slew rate, resulting in a lower output voltage. However, this control method also reduces the efficiency at the load-dump, because the power consumption is needed to consider this Schottky diode loss.

For consumer's products, it is the most important to reduce the bill of materials (BOM) cost and increase power density, so the auxiliary circuit is not a good way to design these products. The third method to solve this problem of a higher output voltage at the load-dump is to avoid an erroneous pulse, so a novel dynamic ramp valley control in the current-mode AOT controller for the on-chip buck converter is proposed to avoid an erroneous pulse under the load-dump without the auxiliary circuit and a Schottky diode. This proposed circuit can achieve a better efficiency and a lower output voltage without an erroneous pulse under the load-dump. Comparison of the three major methods to solve a higher output voltage with an erroneous pulse at the load-dump is shown in Table II.

To prevent the system loop under wide input voltage, output voltage, and output load operation conditions from generating an erroneous pulse $V_{\rm UG}$ signal to drive switch S_A that pushes

TABLE II
COMPARISON OF THREE MAJOR METHODS TO SOLVE A HIGHER OUTPUT VOLTAGE WITH AN ERRONEOUS PULSE AT THE LOAD-DUMP

	[30]-[31]	[32]-[33]	[34]-[35]	This Proposed
Implementation Complexity	Medium	Complicated	Simple	Simple
An Erroneous Pulse	Unavoidable	Unavoidable	Unavoidable	Avoidable
Extra Diode	Unrequired	Required	Required	Unrequired
Extra Inductor	Unrequired	Required	Unrequired	Unrequired
Extra Switch	Unrequired	Required	Unrequired	Unrequired
Reduced Output Voltage	Good	Great	Good	Good
Power Loss	Good	Worse	Bad	Good

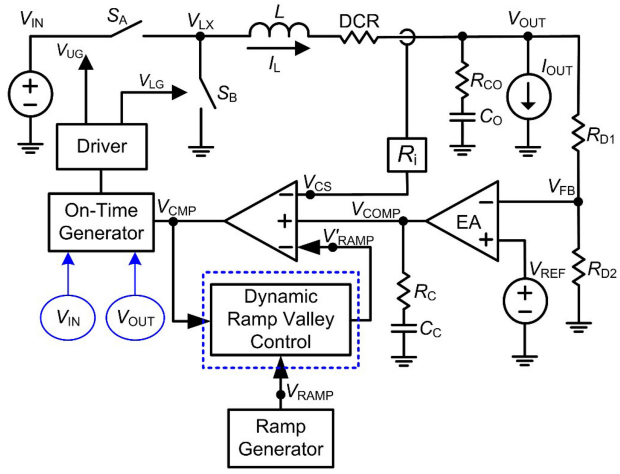

Fig. 7. Novel dynamic ramp valley control in the current-mode AOT controller for buck converter.

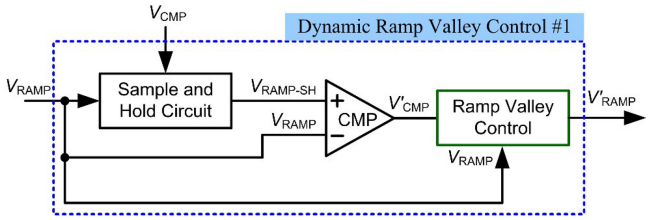

Fig. 8. Block diagram of the novel dynamic ramp valley control sensing $V_{\rm RAMP}$ signal.

the input source to deliver extra energy to the output terminal and causes the output voltage high than the specification that may damage the output load equipment, a novel dynamic ramp valley control is proposed in this paper. Fig. 7 shows the circuit diagram of the proposed novel dynamic ramp valley control in the current-mode AOT controller for buck converter. In the diagram, S_A and S_B are the switches, L is the output inductor, DCR is the dc resistor of the inductor, R_i is a current sense ratio that is used to transfer an inductor-current signal to a voltage signal $V_{\rm CS}$, and $R_{\rm CO}$ is the ESR of output capacitor C_O. The diagram shows that the output voltage ripple, which includes inductor-current information, can be directly used as the ramp for modulation. Current source $I_{\rm OUT}$ is the output load, and R_{D1} and R_{D2} are the feedback resistors that determine the output voltage. The compensation of R_C and C_C should have an optimal design to increase the transient response. Only the feedback signal $V_{\rm FB}$ and reference voltage $V_{\rm REF}$ are built internal

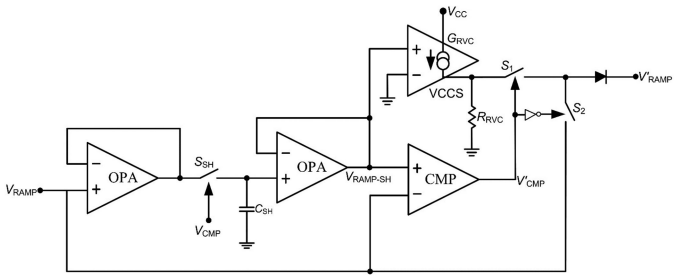

Fig. 9. Implemented circuit of the novel dynamic ramp valley control sensing V_{RAMP} signal.

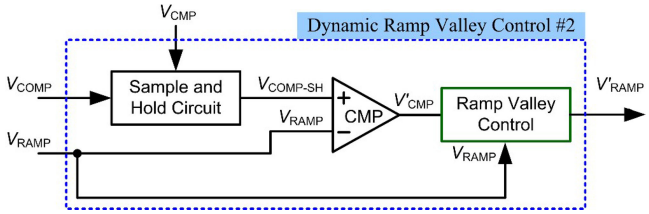

Fig. 10. Block diagram of the novel dynamic ramp valley control sensing V_{COMP} signal.

of the IC. The output signal V_{CMP} of the comparator depends on the results on the input signals V_{COMP}, V_{CS}, and V_{RAMP}. This circuit structure simply adds one block diagram for the novel dynamic ramp valley control. The controller can be used to control the valley of the ramp signal V'_{RAMP} to avoid an error in regulating the output signal V_{CMP} of the comparator during load-dump or sudden release condition.

Fig. 8 shows the block diagram of the novel dynamic ramp valley control sensing V_{RAMP} signal. The novel dynamic ramp control is used to change the valley limitation of V_{RAMP} and to generate a new ramp signal V'_{RAMP} to increase the level of the output signal V'_{CMP} of the comparator. The concept of the novel dynamic ramp valley control uses a sample and hold circuit, a comparator, and a ramp valley control circuit. The sample and hold circuit is used to sample the valley of the V_{RAMP} signal and hold the dc signal $V_{\mathrm{RAMP\text{-}SH}}$ when the output signal V_{CMP} of the comparator reaches a high level. Hence, the signal of $V_{\mathrm{RAMP\text{-}SH}}$ is a constant voltage, and it is useful in determining the output load that has changed. The comparator can detect from heavy load to light load, when the V_{RAMP} signal is lower than the $V_{\mathrm{RAMP\text{-}SH}}$ signal and the output signal V'_{CMP} of the comparator can reach a high level. The ramp valley control uses the V'_{CMP} signal to control the final ramp signal V_{RAMP} equal to $V_{\mathrm{RAMP\text{-}SH}}$.

During the load-dump or sudden release condition, the signal $V_{\mathrm{RAMP\text{-}SH}}$ is larger than the signal V_{RAMP}, the V'_{CMP} signal reaches a high level, the V'_{CMP} signal is used to turn ON switch S_1 and turn OFF S_2, and the signal V'_{RAMP} is controlled by $V_{\mathrm{RAMP\text{-}SH}}$ at this status to clamp a dc value to avoid V'_{RAMP}, similar to the problem in which the V_{RAMP} dropped and had an erroneous pulse. At steady-state operation, the signal $V_{\mathrm{RAMP\text{-}SH}}$ is smaller than the signal V_{RAMP}, the V'_{CMP} signal is at a low level, the V'_{CMP} signal is used to turn ON S_2 and turn OFF S_1, and the signal V'_{RAMP} is connected by V_{RAMP} without an erroneous pulse like the implemented circuit, as shown in Fig. 9.

On the other hand, the sample and hold circuit can also sample the peak of V_{COMP} signal and hold the dc signal $V_{\mathrm{COMP\text{-}SH}}$. The block diagram and implemented circuit of the novel dynamic ramp valley control sensing V_{COMP} signal are shown in Figs. 10 and 11. Thus, the signal of $V_{\mathrm{COMP\text{-}SH}}$ is a constant voltage that can be used to determine the output load that has changed, because the peak of V_{COMP} signal is the same as the valley of V_{RAMP} signal when the output signal V_{CMP} of the comparator is at a high level; therefore, the novel dynamic ramp valley control can achieve the same function of avoiding an erroneous pulse generated during load-dump or sudden release condition. During load-dump or sudden release condition, the signal $V_{\mathrm{COMP\text{-}SH}}$ is larger than the signal V_{RAMP}, the V'_{CMP} signal is at a high level, the V'_{CMP} signal is used to turn ON S_1 and turn OFF S_2, and the signal V'_{RAMP} is controlled by $V_{\mathrm{RAMP\text{-}SH}}$ at this status to clamp a dc value to avoid V'_{RAMP}, similar to the issue in which the V_{RAMP} dropped and had an erroneous pulse.

The two implemented circuits as shown in Figs. 9 and 11 can achieve the novel dynamic ramp valley control that avoids an erroneous pulse generated during load-dump or sudden release condition. However, the implemented circuit illustrated in Fig. 11 needs to sense the signal V_{COMP}, and it is an output terminal of an error amplifier, thus making it a sensitive signal. On the other hand, the noise immunity is also needed for sensing the signal V_{COMP}.

The proposed circuit can avoid an error in regulating the output signal V_{CMP} of the comparator during load-dump or sudden release condition. It has two ways to avoid an error in regulating the output signal V_{CMP} of the comparator. These two ways are to control the V_{RAMP} signal and to control the V_{COMP} signal. The V_{RAMP} is an input signal, whereas the V_{COMP} signal is an output signal; therefore, the V_{COMP} signal is not a good approach for changing and controlling its waveform. Thus, the proposed circuit is intended to control the V_{RAMP} signal to avoid the extra pulse generated during load-dump or sudden release condition. Fig. 12 shows these control signals for the novel dynamic ramp valley control, which can be used to control and clamp the V'_{RAMP} with a dc value without an erroneous pulse being generated during load-dump or sudden release condition.

III. Experimental Verification

SIMPLIS simulation and experimental verifications were conducted to test the feasibility and performance of the proposed circuit with the proposed dynamic ramp valley control in the current-mode AOT controller for the on-chip buck converter. The operation conditions are as follows:

1) Input dc voltage (V_{IN}): 19 V;
2) Output dc voltage (V_{OUT}): 1.05 V;
3) Output load current (I_{OUT}): 9 A;
4) Switching frequency (F_S): 300 kHz;
5) Feedback resistors (R_{D1}, R_{D2}): 8 and 20 kΩ;
6) Main inductor (L): 2.2 μH;
7) Output capacitors (C_O): 330 μF/6.3 V∗2 (R_{CO}: 6 mΩ);
8) Reference voltage (V_{REF}): 0.75 V;

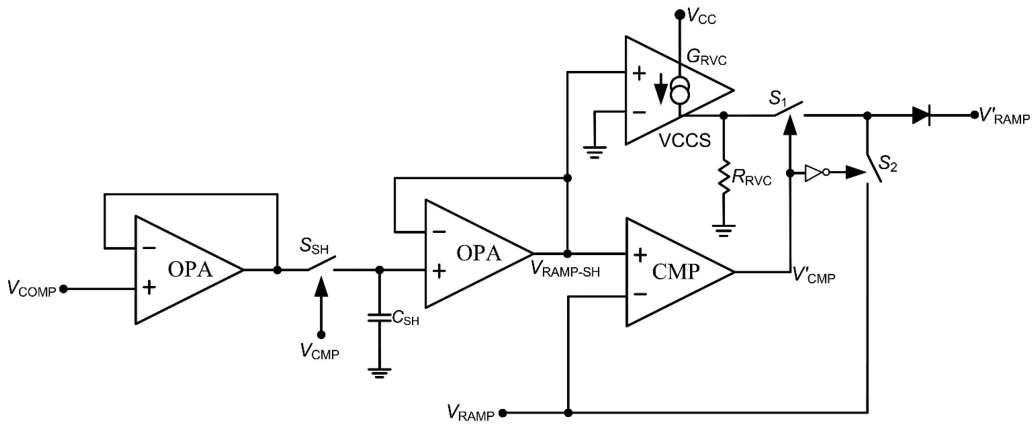

Fig. 11. Implemented circuit of the novel dynamic ramp valley control sensing V_{COMP} signal.

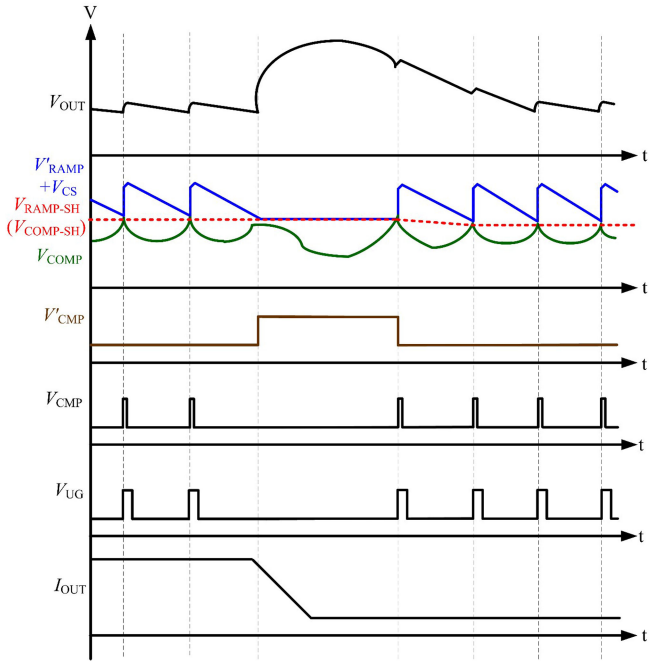

Fig. 12. Control signals for with the novel dynamic ramp valley control without an erroneous pulse under the load-dump.

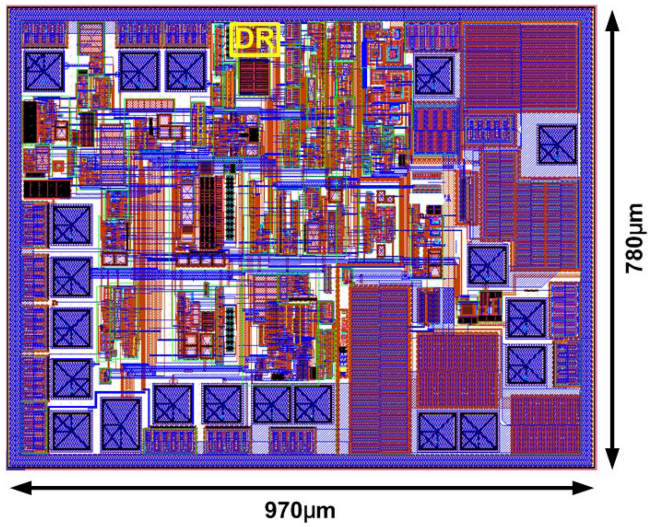

Fig. 13. Chip layout of the control IC.

9) Compensator: $G_M = 260\ \mu$A/V; $R_D = 142$ MΩ; $R_C = 1.5$ MΩ; $C_C = 40$ pF;
10) On-time generator: $R_1 = 185$ kΩ; $C_1 = 3$ pF; $G_1 = 0.166$ A/V.

Fig. 13 shows the chip layout of the control IC, in which the proposed dynamic ramp valley control of the current-mode AOT controller occupies the area marked by the DR with a die size of 780 μm × 970 μm.

Fig. 14 compares SIMPLIS simulation results for the open-loop control-to-output Bode plot using with the dynamic ramp valley control and without the dynamic ramp valley control for buck converter. SIMPLIS is used to simulate results with the dynamic ramp valley control and without the dynamic ramp valley control circuit, as shown in Figs. 9 and 3, respectively. The blue-colored line waveform represents the open-loop control-to-output Bode plot with the dynamic ramp valley control for buck converter. The red-colored dot waveform represents the open-loop control-to-output Bode plot without the dynamic ramp valley control for buck converter. These SIMPLIS simulation results can compare and prove that the open-loop control-to-output with the dynamic ramp valley control for buck converter is very approached to without the dynamic ramp valley control for buck converter, because the dynamic ramp valley control circuit is just designed to control and clamp the valley of ramp to avoid the generation of an erroneous pulse signal while regulating the output voltage under the load-dump, so this dynamic ramp valley control circuit is not to obtain a pole or zero for this system control loop.

Fig. 15 compares SIMPLIS simulation results and experimental results for the closed-loop loop gain Bode plot using with the dynamic ramp valley control for buck converter. SIMPLIS simulation results and experimental results are performed with the dynamic ramp valley control for buck converter, as shown in Fig. 9. The blue-colored line waveform represents the closed-loop loop gain Bode plot for experimental results with

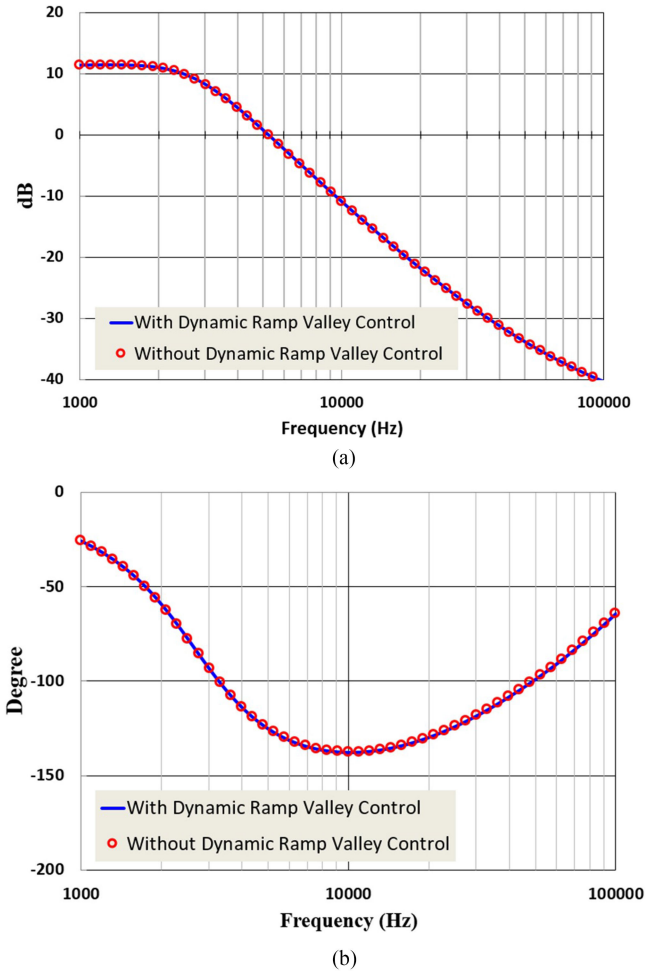

Fig. 14. Comparison of SIMPLIS simulation results for the open-loop control-to-output Bode plot using with the dynamic ramp valley control and without the dynamic ramp valley control for buck converter. (a) Gain. (b) Phase.

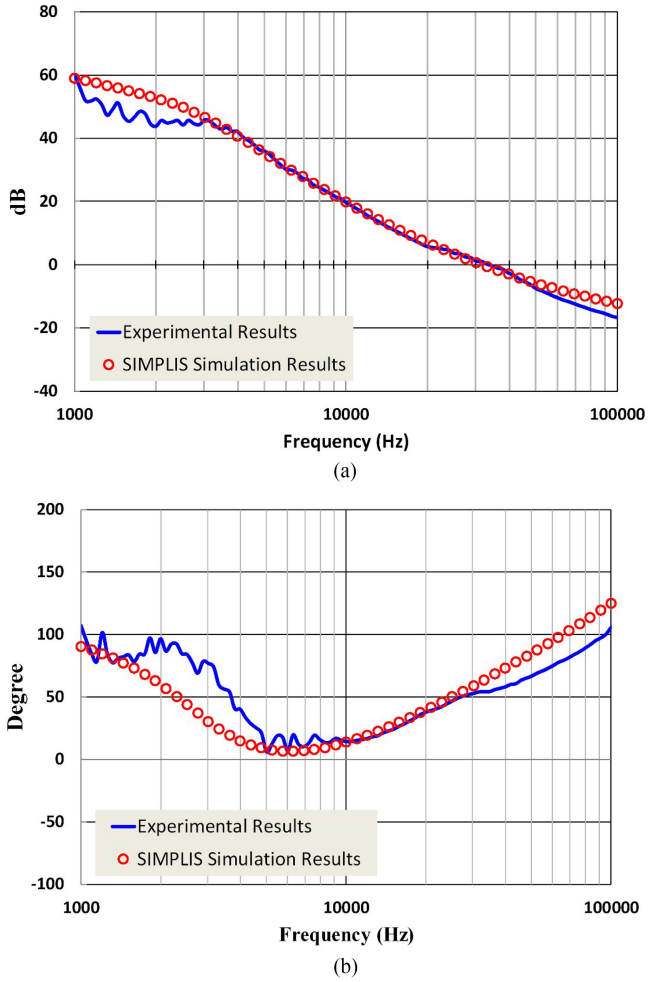

Fig. 15. Comparison of SIMPLIS simulation results and experimental results for the closed-loop loop gain Bode plot using with the dynamic ramp valley control for buck converter. (a) Gain. (b) Phase.

the dynamic ramp valley control for buck converter. The red-colored dot waveform represents the closed-loop loop gain Bode plot for SIMPLIS simulation results with the dynamic ramp valley control for buck converter. These results can be confirmed and verified between SIMPLIS simulation results and experimental results with the dynamic ramp valley control for buck converter.

The dynamic ramp valley control for buck converter uses the same compensation parameters to obtain SIMPLIS simulation results and experimental results. The bandwidth of the dynamic ramp valley control for buck converter for the SIMPLIS simulation results and experimental results are very approached to 36 kHz; whereas the bandwidth of the dynamic ramp valley control for buck converter for the SIMPLIS simulation results and experimental results are very close to each other. The phase margin of the experimental results is 58° very close to SIMPLIS simulation results of 65°.

Fig. 16 shows experimental results for load regulation using with the dynamic ramp valley control for buck converter. The experimental results for load regulation are without a steady-status error at an output voltage of 1.05 V under different input voltages of 5, 12, and 17 V. The blue-colored line waveform represents the input voltage 5 V for experimental results at a widely output load current during 0 to 20 A. The red-colored line waveform represents the input voltage 12 V for experimental results at a widely output load current during 0 to 20 A. The black-colored line waveform represents the input voltage 17 V for experimental results at a widely output load current during 0 to 20 A. The load regulation is a key performance for an integrated circuit and it is also a key specification. The specification of load regulation is generally defined as $+1\%/-1\%$ of the output voltage 1.05 V. Based on this operation condition, the output voltage should range from 1.0395 to 1.0605 V. In Fig. 16, the lower input voltage 5 V is a worst case to obtain a wide output voltage during 1.0428 to 1.0448 V, but these results of input voltage 5 V are still to meet the load regulation specification. The experimental results meet this specification of load regulation and can prove that the output load current does not affect the output voltage regulation. For these reasons, the dynamic ramp valley control for buck converter is suitable for applications with a fixed output voltage under different output load currents.

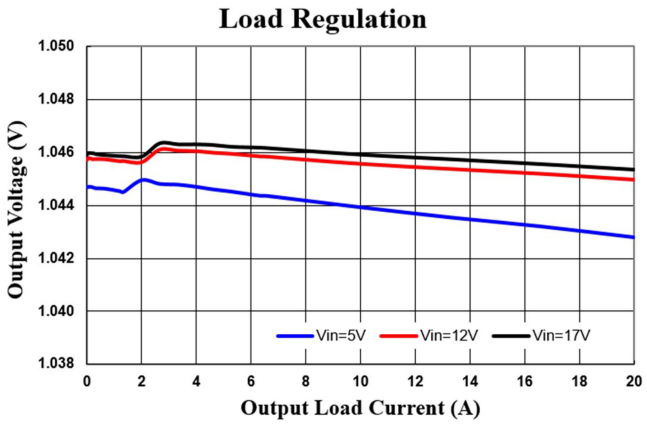

Fig. 16. Experimental results for load regulation using with the dynamic ramp valley control for buck converter.

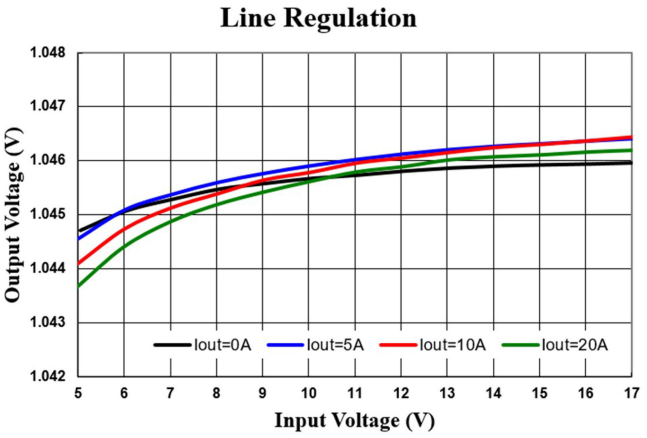

Fig. 17. Experimental results for line regulation using with the dynamic ramp valley control for buck converter.

If the system control loop response is fast, the output voltage may suffer from a low voltage drop. If the system control loop response is too fast, then the power converter may suffer from noise jitter, subharmonic, or even result in an unstable system. If the system control loop response is slow, the output voltage may suffer from a large voltage drop. A large voltage drop causes consumer electronic products to suffer from damage or failure; hence, the design of the system control loop response is a tradeoff. The system control loop response is an optimal design based on its operation conditions and must cover the worst operation conditions.

Fig. 17 shows experimental results for line regulation using with the dynamic ramp valley control for buck converter. The experimental results for line regulation are an output voltage of 1.0 V under different output load currents of 0, 5, 10, and 20 A. The black-colored line waveform represents the output load current 0 A for experimental results at a widely input voltage during 5 to 17 V. The blue-colored line waveform represents the output load current 5 A for experimental results at a widely input voltage during 5 to 17 V. The red-colored line waveform represents the output load current 10 A for experimental results at a widely input voltage during 5 to 17 V. The green-colored line waveform represents the output load current 20 A for experimental results at a widely input voltage during 5 to 17 V.

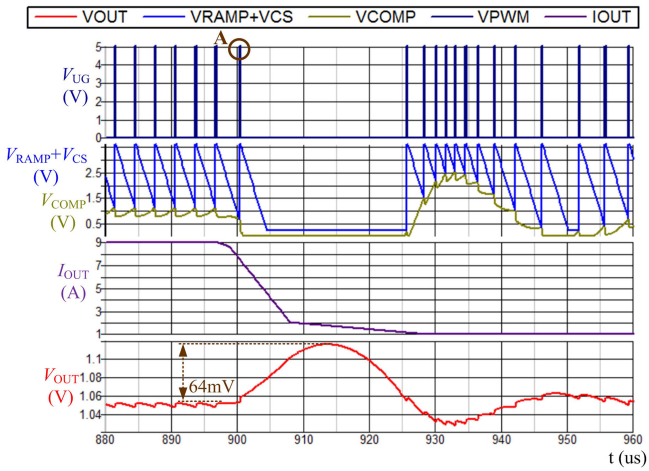

Fig. 18. Simulation results without the proposed dynamic ramp valley control under the load-dump.

The line regulation is also a key performance for an integrated circuit, especially for portable devices or products, because the portable devices or products are usually used as a battery to serve as an input power, so the input voltage of battery is dependent on its capacity, based on this reason, the control-integrated circuit is needed to achieve a great line regulation in order to avoid a damage or an error operation for this portable device or product. The specification of line regulation is generally defined as $+1\%/-1\%$ of the output voltage 1.05 V like the load regulation. Based on this operation condition, the output voltage should range from 1.0395 to 1.0605 V. In Fig. 17, the larger output load current 20 A is a worst case to obtain a wide output voltage during 1.0436 to 1.0462 V, but these results of output load current 20 A are still to meet the line regulation specification. The experimental results meet this specification of line regulation and can prove that the input voltage does not affect the output voltage regulation. For these reasons, this dynamic ramp valley control for buck converter is also suitable for applications with a fixed output voltage under different input voltages.

Fig. 18 shows the results of the SIMPLIS simulation without the proposed dynamic ramp valley control under the load-dump. The red-colored waveform represents the simulated output voltage without the proposed dynamic ramp valley control under the load-dump, and the purple-colored waveform represents the simulated output load current. This output voltage is simulated by the same slew rate like the electronic load. $V_{\rm OUT}$ under the load-dump without the proposed dynamic ramp valley control is 64 mV, and it is simulated by the peak-to-peak value. The sum signal of $V_{\rm RAMP}$ and $V_{\rm CS}$ does not have the proposed dynamic ramp valley control; hence, this signal is down to zero voltage, and an erroneous pulse is easily generated, as shown at point "A" in Fig. 18. Thus, the output voltage becomes out of specification or damages the output load equipment.

Fig. 19 shows the results of the SIMPLIS simulation with the proposed dynamic ramp valley control under the load-dump. The red-colored waveform represents the simulated output

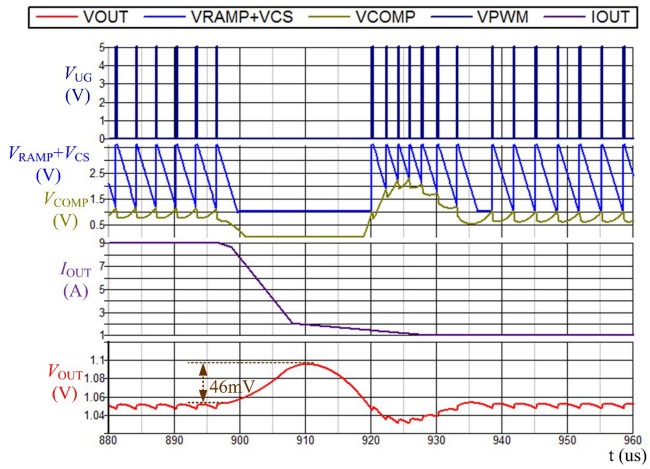

Fig. 19. Simulation results with the proposed dynamic ramp valley control under the load-dump.

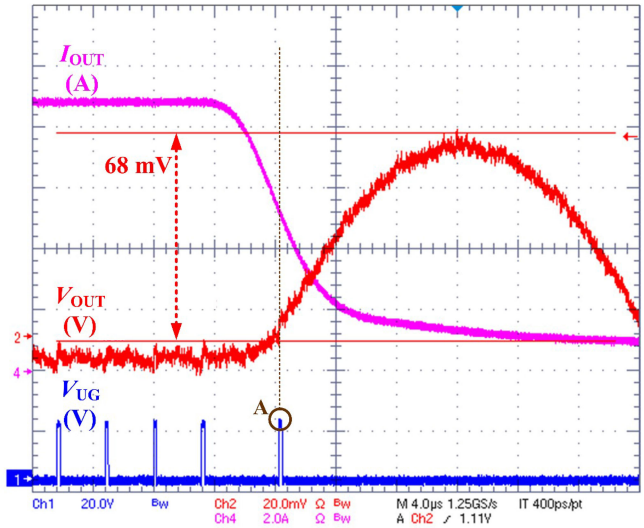

Fig. 20. Experimental results without the proposed dynamic ramp valley control under the load-dump.

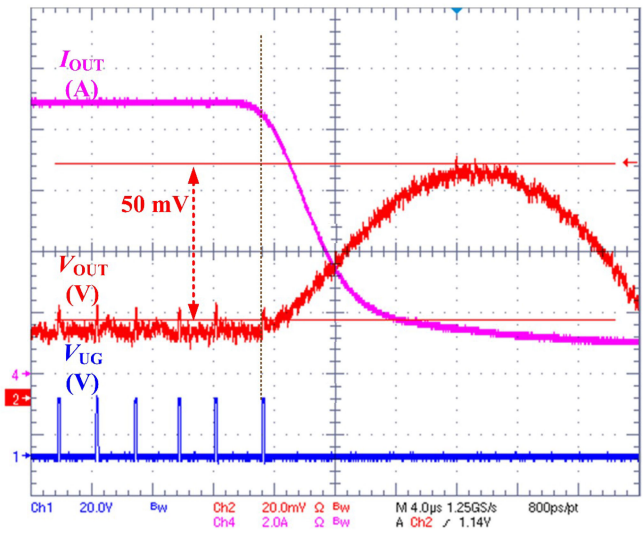

Fig. 21. Experimental results with the proposed dynamic ramp valley control under the load-dump.

voltage with the proposed dynamic ramp valley control under the load-dump, and the purple-colored waveform represents simulated output load current. This output voltage is simulated by the same slew rate like the electronic load. $V_{\rm OUT}$ under the load-dump with the proposed dynamic ramp valley control is 46 mV, and it is simulated by the peak-to-peak value. The sum signal of $V_{\rm RAMP}$ and $V_{\rm CS}$ does have the proposed dynamic ramp valley control; hence, the valley of the sum signal is controlled by the output signal $V'_{\rm CMP}$ of the comparator. When the $V_{\rm RAMP}$ signal is lower than the $V_{\rm RAMP\text{-}SH}$ signal, the output signal $V'_{\rm CMP}$ of the comparator reaches a high level. The ramp valley control uses the $V'_{\rm CMP}$ signal to control the final ramp signal $V_{\rm RAMP}$ equal to $V_{\rm RAMP\text{-}SH}$. The sample and hold voltage $V_{\rm RAMP\text{-}SH}$ is the same as the previous value at the $V_{\rm RAMP}$ and is equal to $V_{\rm COMP}$.

The output voltage with and without the proposed dynamic ramp valley control are based on the same output current load. The resulting $V_{\rm OUT}$ under the load-dump with and without the proposed dynamic ramp valley control is 46 and 64 mV, respectively. Thus, $V_{\rm OUT}$ with the proposed dynamic ramp valley control is lower by 18 mV than without the proposed dynamic ramp valley control. The erroneous pulse is also eliminated. In addition, the settling time of $V_{\rm OUT}$ with the proposed dynamic ramp valley control is faster than that without the proposed dynamic ramp valley control. The settling time of simulation results with the proposed dynamic ramp valley control reaches a steady state is at 940 μs, whereas the settling time of simulation results without the proposed dynamic ramp valley control is at 960 μs.

Fig. 20 shows the results of the experiment without the proposed dynamic ramp valley control under the load-dump. The red-colored waveform represents the experimental output voltage without the proposed dynamic ramp valley control, the blue-waveform represents the $V_{\rm UG}$ signal, and the pink-colored waveform represents the output current load. The resulting $V_{\rm OUT}$ under the load-dump without the proposed dynamic ramp valley control is 68 mV, and it is measured by the peak-to-peak value. The $V_{\rm RAMP}$, $V_{\rm CS}$, and $V_{\rm COMP}$ signals are built inside the IC; therefore, they cannot be measured by external components and evaluation board. However, an erroneous pulse can be easily generated, as shown at point "A" in Fig. 20. Thus, the output voltage becomes out of specification or damages the output load equipment.

Fig. 21 shows the results of the experiment with the proposed dynamic ramp valley control under the load-dump. The red-colored waveform represents the experimental output voltage with the proposed dynamic ramp valley control, the blue-colored waveform represents the $V_{\rm UG}$ signal, and the pink-colored waveform represents the output current load. The resulting $V_{\rm OUT}$ under the load-dump with the proposed dynamic ramp valley control is 50 mV, and it is measured by the peak-to-peak value.

The output voltage with and without the proposed dynamic ramp valley control are based on the same output current load. The resulting $V_{\rm OUT}$ under the load-dump with and without the

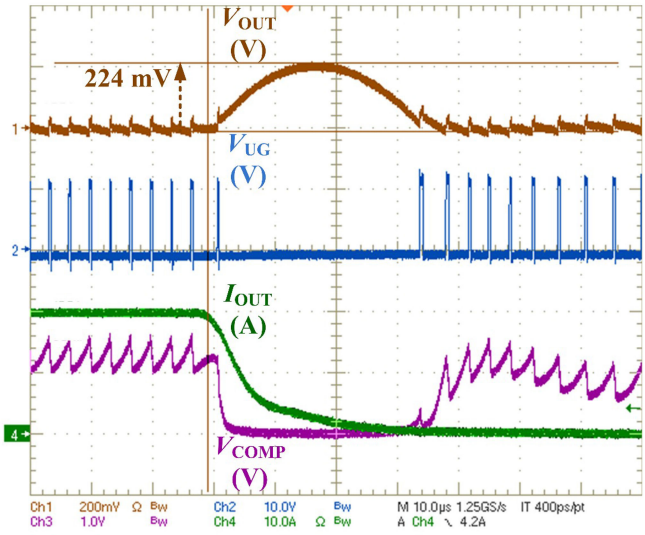

Fig. 22. Experimental results to measure V_{COMP} signal without the proposed dynamic ramp valley control under the load-dump.

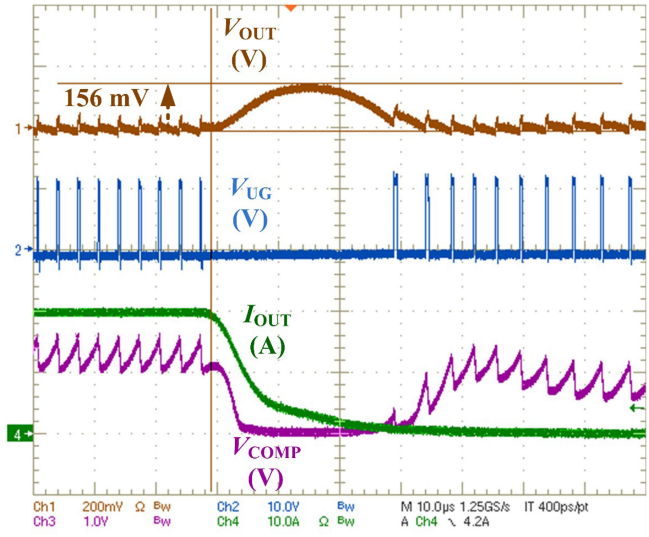

Fig. 23. Experimental results to measure V_{COMP} signal with the proposed dynamic ramp valley control under the load-dump.

proposed dynamic ramp valley control is 50 and 68 mV, respectively. Thus, V_{OUT} with the proposed dynamic ramp valley control is lower by 18 mV than that without the proposed dynamic ramp valley control. It also eliminates the issue of an erroneous pulse.

To further test the feasibility and performance of the proposed dynamic ramp valley control, the same IC with a COMP pin is added to measure V_{COMP}. The V_{COMP} signal is almost the same with and without the proposed dynamic ramp valley control, but the proposed dynamic ramp valley control avoids the generation of an erroneous pulse. The experiment of the two ICs is conducted with the operation conditions as follows:

1) Input dc voltage (V_{IN}): 12 V;
2) Output dc voltage (V_{OUT}): 1.05 V;
3) Output load current (I_{OUT}): 20 A;
4) Switching frequency (F_S): 330 kHz;
5) Feedback resistors (R_{D1}, R_{D2}): 6.3 and 20 kΩ;
6) Main inductor (L): 1 μH;
7) Output capacitors (C_O): 330 μF/ 6.3 V∗1 (R_{CO}: 6 mΩ);
8) Reference voltage (V_{REF}): 0.8 V;
9) Compensator: $G_M = 220$ μA/V; $R_D = 168$ MΩ; $R_C =$ 20 kΩ; $C_C = 10$ nF;
10) On-time generator: $R_1 = 185$ kΩ; $C_1 = 3$ pF; $G_1 = 0.166$ A/V.

Fig. 22 shows results of the experiment to measure V_{COMP} signal without the proposed dynamic ramp valley control under the load-dump. The brown-colored waveform represents the experimental output voltage without the proposed dynamic ramp valley control under the load-dump, the light blue-colored waveform represents the V_{UG} signal, the green-colored waveform represents the output current load, and the purple-colored waveform represents the V_{COMP} signal. The resulting V_{OUT} under the load-dump without the proposed dynamic ramp valley control is 224 mV, and it is measured by the peak-to-peak value. The V_{RAMP} signal and the V_{CS} signal are built inside the IC; therefore, they cannot be measured by external components and evaluation board.

TABLE III
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART BUCK CONVERTERS

	[30]	[31]	[32]	[33]	This Proposed
V_{IN} (V)	12 V	12 V	12 V	12 V	12 V
V_{OUT} (V)	1.5 V	1.5 V	1.5 V	1.5 V	1.05 V
I_{OUT} (A)	10 A to 0 A	11.5 A to 0 A	11.5 A to 0 A	20 A to 0 A	20 A to 0 A
F_S (kHz)	400 kHz	400 kHz	400 kHz	400 kHz	330 kHz
F_{AUX} (kHz)	--	--	2000 kHz	2000 kHz	--
L (µH)	1 µH	1 µH	1 µH	1 µH	1 µH
C_O (µF)	180 µF	180 µF	180 µF	190 µF	330 µF, 6.3 V
R_{CO} (mΩ)	0.5 mΩ	0.5 mΩ	0.5 mΩ	0.5 mΩ	6 mΩ
ΔV_{OUT} (mV)	169 mV	160 mV	70 mV	220 mV	156 mV

Fig. 23 shows the results of the experiment to measure V_{COMP} signal with the proposed dynamic ramp valley control under the load-dump. The brown-colored waveform represents the experimental output voltage with the proposed dynamic ramp valley control under the load-dump, the light blue-colored waveform represents the V_{UG} signal, the green-colored waveform represents the output current load, and the purple-colored waveform represents the V_{COMP} signal. The resulting V_{OUT} under the load-dump with the proposed dynamic ramp valley control is 156 mV, and it is measured by the peak-to-peak value.

The output voltage with and without the proposed dynamic ramp valley control are based on the same output current load. V_{OUT} under the load-dump with and without the proposed dynamic ramp valley control is 156 and 224 mV, respectively. Thus, V_{OUT} with the proposed dynamic ramp valley control is lower by 68 mV than that without the proposed dynamic ramp valley control, avoiding the potential damage of the output load.

Table III presents the performance comparison with other state-of-the-art buck converters. In [30]–[33], these experimental results were measured under very similar operation conditions such as the input voltage, output voltage, and switching frequency to compare this proposed circuit of the

novel dynamic ramp valley control in the current-mode AOT controller for the on-chip buck converter. In [32] and [33], these papers use extra auxiliary circuits and more complicated control to control and drive the auxiliary switch directly, so the auxiliary frequency should be addressed to drive this auxiliary switch as shown in Table III.

IV. Conclusion

The SIMPLIS simulation results and experimental results confirm that the proposed circuit with the novel dynamic ramp valley control in the current-mode AOT controller for the on-chip buck converter can significantly reduce the output voltage ripple without generating an erroneous pulse during load-dump or sudden release condition. The two ICs confirmed and verified that the proposed circuit is useful in avoiding the input source to deliver extra energy to the output load under the load-dump. Moreover, the proposed novel dynamic ramp valley control has a simple structure and design in the current-mode AOT controller for the on-chip buck converter.

Acknowledgment

The authors would like to thank the Ministry of Science and Technology of Taiwan for sharing their facilities under Award MOST 106-2917-I-564-010.

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