






# A New Standby Structure Integrated With Boost PFC Converter for Server Power Supply

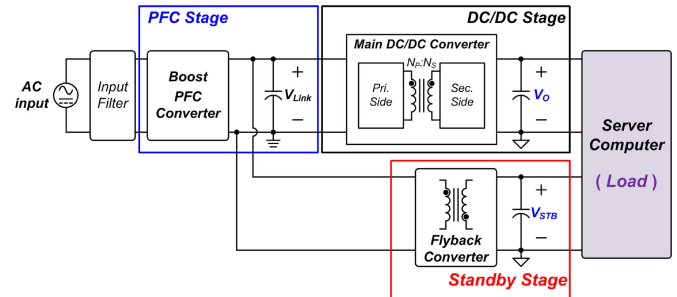
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**Abstract**—In the standby stage of a server power supply, the flyback converter has been widely used due to its simple structure and low cost. However, since the flyback converter suffers from high-voltage stress and a large transformer, it degrades the efficiency and power density of the server power supply. To relieve these drawbacks, this paper proposes a new standby structure where a flyback converter is integrated with a boost power-factor-correction (PFC) converter. The proposed standby structure can relieve the high-voltage stress and eliminate the large transformer of the conventional flyback converter because the primary side of the flyback converter is merged with the boost PFC converter. Thus, the proposed structure can achieve high efficiency and high power density in the standby stage. Furthermore, it can help the boost PFC converter achieve a soft switching operation, which results in a high-efficiency PFC stage. As a result, the proposed structure improves the overall efficiency and power density of the server power supply. The validity of the proposed structure is confirmed by a prototype with 100–240 V<sub>rms</sub> ac input, 750-W PFC output, and 12-V/2-A standby output.

**Index Terms**—Boost power factor correction (PFC) converter, flyback converter, PFC stage, server power supply, soft switching, standby stage.

## I. INTRODUCTION

RECENTLY, as the internet traffic has increased all over the world, the data center market has consistently grown. Accordingly, the server power supply for the data center has also been developed actively. In general, the server power supply requires high efficiency under heavy load conditions because it operates under heavy loads during the day. Moreover, since the server power supply runs under light-load conditions at night and dawn, the light-load efficiency has also become important in the server power supply market [1]. This tendency is confirmed



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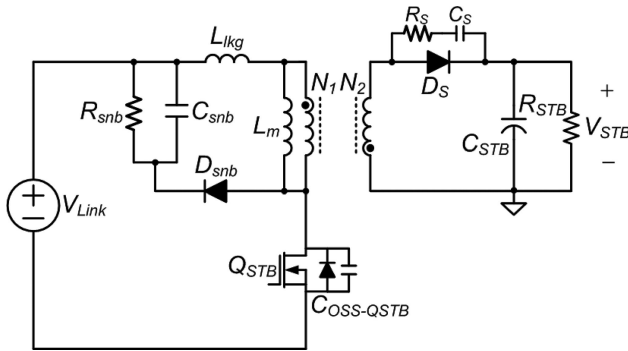


Fig. 2. Circuit diagram of the conventional flyback converter.

power loss in the primary side [9]–[12], which degrades the efficiency of the server power supply over all the load conditions [9]–[11]. First, since the switch ( $Q_{STB}$ ) in the flyback converter suffers from high-voltage stress and hard switching operation,  $Q_{STB}$  causes a large switching loss. Second, the primary  $RCD$  snubber results in a large power loss due to high-voltage stress and additional voltage spike caused by the resonance between the leakage inductor of the transformer ( $L_{lkg}$ ) and the output capacitor of  $Q_{STB}$  ( $C_{OSS-Q_{STB}}$ ). Furthermore, it has a large transformer because of the dc-offset magnetizing current in the transformer [13]. Therefore, the flyback converter also degrades the power density of the server power supply.

For those reasons, many approaches have been proposed to improve the efficiency and power density of the flyback converter [9]–[12]. In [9], the secondary side of the flyback converter was integrated into that of a multi-output phase-shifted full-bridge (PSFB) converter with one additional switch. This method regulated  $V_{STB}$  through the operations of the PSFB converter and the additional switch instead of the primary side of the flyback converter. Thus, it eliminated the power loss caused by the primary side of the flyback converter. However, the method proposed in [9] caused additional conduction loss in the PSFB converter so it has limitations in achieving a high-efficiency server power supply. Moreover, in the standby mode, since  $V_{STB}$  needs to be regulated without the operation of the PSFB converter, this structure still has to utilize the primary circuit and large transformer of the flyback converter. Thus, this approach degrades the power density and increase the cost due to the large transformer and the additional switch. In [10], the primary side of the two-switch flyback converter was combined with that of the PSFB converter by sharing the lagging leg switches of the PSFB converter. In the normal mode, the structure proposed in [10] achieved high efficiency by removing the  $RCD$  snubber loss and obtaining the zero voltage switching (ZVS) operation of primary switches without additional components. However, this structure also increases the conduction loss of the PSFB converter and still has a large transformer of the two-switch flyback converter, which results in a low power density. Next, in [11], the output of the flyback converter was merged with that of the PSFB converter using an ORing diode. In the normal mode, since the PSFB converter that is highly efficient is only used to regulate  $V_O$  and  $V_{STB}$ ,

the power loss of the primary side in the flyback converter can be eliminated. However, this structure cannot eliminate any component of the flyback converter to provide  $V_{STB}$  in the standby mode. Furthermore, two additional diodes are required to integrate outputs of the flyback converter and PSFB converter. Above all, this structure can only be applied to applications requiring the same  $V_O$  and  $V_{STB}$ . Meanwhile, another study focused on the flyback converter itself. In [12], the resonant operation was applied to the flyback converter to achieve the soft switching operation of the primary switch. That approach increased the switching frequency with a small switching loss, which enabled the flyback converter to reduce its transformer size. However, the structure proposed in [12] also requires an additional diode and has the  $RCD$  snubber loss and switching loss.

Meanwhile, to achieve high efficiency and high power density, integrating the boost PFC converter and flyback converter can also be a good approach [14]–[16]. In [14], the boost PFC and flyback converters were integrated to eliminate the flyback switch. Moreover, the converter proposed in [14] reduced the  $RCD$  snubber loss by adopting lossless snubber. However, it suffers from the hard switching operation and requires two magnetic cores and additional diode, which results in a low efficiency and low power density. The converter proposed in [15] achieved high power density by eliminating one magnetic core. In addition, it obtained the soft switching operation of all switches without additional components. Nevertheless, this converter has limitation in obtaining high efficiency because it requires small boost inductance to achieve the soft switching operation. Above all, the converters proposed in [14] and [15] cannot be applied to the server power supply because they are not able to regulate  $V_O$  and  $V_{STB}$ , simultaneously. Meanwhile, the converter proposed in [16] can regulate  $V_O$  and  $V_{STB}$  despite of the integration. Besides, by combining the active snubber inductor and flyback transformer, it minimized the switching loss of the boost PFC stage and losses of the active snubber cell, which leads to high efficiency. However, this approach still has to use two magnetic core and  $RCD$  snubber. Moreover, it requires active snubber cell composed of a diode and switch to obtain the soft switching operation. Therefore, the converter proposed in [16] also has a limitation in achieving a high power density.

In this paper, a new standby structure is proposed to achieve a high-efficiency and high-power-density server power supply. The proposed standby structure can be effectively derived by integrating the primary side of the flyback converter with the boost PFC converter. The proposed standby structure has three desirable features that make it superior to the conventional standby structure, which is composed of the boost PFC converter and flyback converter. First, since the boost PFC converter is used as the primary side of the flyback converter, the proposed structure relieves high-voltage stress and eliminates the  $RCD$  snubber. Second, the transformer of the flyback converter is able to be removed by integrating it with the boost inductor. Finally, the proposed structure achieves the soft switching operation of the boost PFC converter through the interaction of the integrated

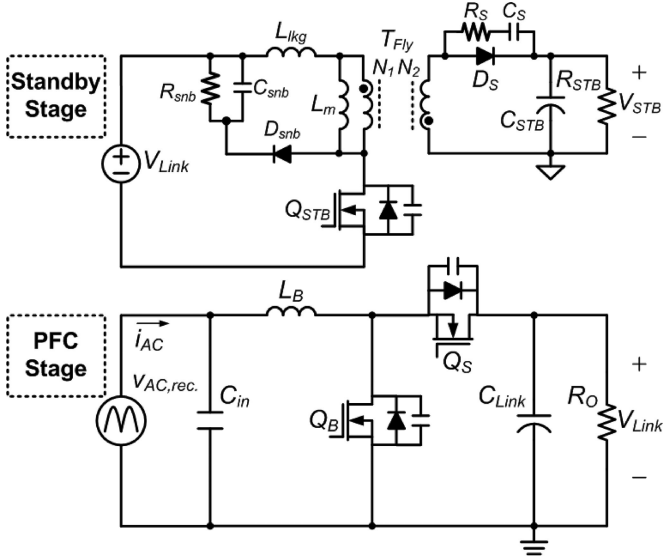


Fig. 3. Circuit diagram of the conventional standby structure.

structure of the boost PFC and flyback converters. As a result, the proposed structure achieves high efficiency and high power density for the server power supply without any additional components. The analysis, design consideration, and experimental results of the proposed structure are discussed in the following sections.

## II. ANALYSIS OF THE PROPOSED STANDBY STRUCTURE

### A. Circuit Configuration

Fig. 3 shows the circuit diagram of the conventional standby structure. This figure shows that the boost PFC converter is used for the PFC stage, and it is composed of an input filter capacitor ( $C_{in}$ ) for electromagnetic interference (EMI) noise, a boost inductor ( $L_B$ ), a boost switch ( $Q_B$ ), and a link capacitor ( $C_{Link}$ ). Moreover, the synchronous rectifier switch ( $Q_S$ ) can be used in place of the SiC diode due to the advancement of wide-band gap devices, such as SiC MOSFET and GaN FET, which results in higher efficiency by reducing the conduction loss [17], [18]. Next, in the standby stage, the flyback converter is used and it consists of the primary switch ( $Q_{STB}$ ), the  $RCD$  snubber for clamping the voltage stress of  $Q_{STB}$ , the transformer ( $T_{Fly}$ ), which has a magnetizing inductor ( $L_m$ ) and a leakage inductor ( $L_{lkg}$ ), a single-ended rectifier, and an  $RC$  snubber to limit the voltage stress of  $D_S$  [13].

Fig. 4 shows the circuit diagram of the proposed standby structure. In the proposed structure, since the primary side of the flyback converter is combined with the boost PFC converter, the proposed structure has three desirable features compared to the conventional one. First, in the PFC stage, the conventional boost inductor ( $L_B$ ) is replaced with a boost transformer ( $T_{Pro}$ ) to integrate  $L_B$  and  $T_{Fly}$ . Thus, the proposed structure effectively eliminates  $T_{Fly}$  only by adding a secondary winding ( $N_2$ ) to  $L_B$ . Second, in the standby stage,  $Q_{STB}$  of the conventional flyback converter is moved into the secondary side. Thus, the

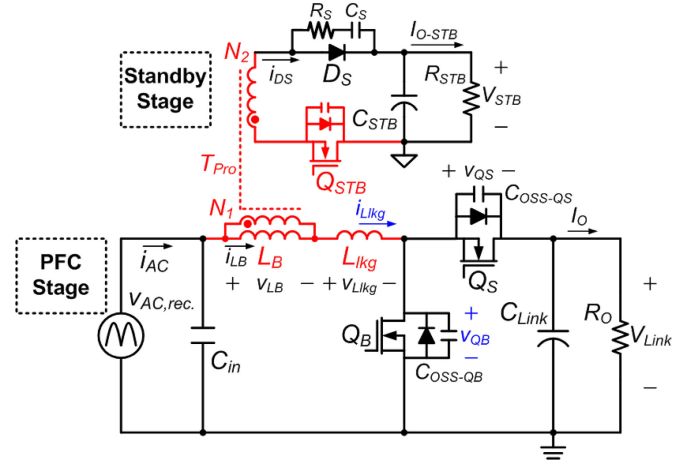


Fig. 4. Circuit diagram of the proposed standby structure.

proposed structure can considerably reduce the voltage stress on  $Q_{STB}$  compared to the conventional one because  $V_{STB}$  is much smaller than  $V_{Link}$ . Moreover, since the voltage stress on  $Q_{STB}$  can be damped by the  $RC$  snubber of  $D_S$ , the proposed structure is able to remove the conventional  $RCD$  snubber. Finally, the proposed standby structure can achieve the soft switching operation of the PFC stage through the energy transfer between the PFC and standby stages. As a result, the proposed structure can improve the efficiency and power density without any additional components.

### B. Operational Principles

Figs. 4 and 5 show the circuit diagram and key waveforms of the proposed standby structure, respectively. As shown in Fig. 5,  $Q_B$  and  $Q_S$  are complementarily controlled to regulate the input current ( $i_{AC}$ ) and  $V_{Link}$  like the conventional boost PFC converter.  $Q_{STB}$  is controlled to regulate  $V_{STB}$  like the conventional flyback converter. Moreover,  $Q_{STB}$  is turned ON near the end of the ON state of  $Q_S$  to achieve the ZVS operation of  $Q_B$ , and simultaneously, turned OFF with  $Q_B$  not only to obtain the ZCS turn-OFF operation of  $Q_{STB}$  but also to simplify the control of  $Q_{STB}$ .

*Mode 1* [ $t_0-t_1$ ]: At time  $t_0$ , the voltage across  $C_{OSS-QS}$  ( $v_{QS}$ ) becomes zero so the current of  $L_B$  ( $i_{LB}$ ) flows through the body diode of  $Q_S$ . Thus, the ZVS operation of  $Q_S$  is achieved. Then,  $i_{LB}$  starts to decrease because the voltage across  $L_B$  ( $v_{LB}$ ) is  $V_{AC}-V_{Link}$ .  $i_{LB}$  can be given by

$$i_{LB}(t) = i_{Llkg}(t) = i_{LB}(t_0) - \frac{V_{Link} - V_{AC}}{L_B}(t - t_0) \quad (1)$$

where  $i_{Llkg}$  is the current of  $L_{lkg}$ .

During this mode, although  $v_{LB}$  has a negative value, the power cannot be transferred from the PFC stage to  $V_{STB}$  because  $Q_{STB}$  is turned OFF. Therefore, the proposed structure operates like a conventional boost PFC converter in this mode.

*Mode 2* [ $t_1-t_2$ ]: When  $Q_{STB}$  is turned ON at  $t_1$ , the secondary diode ( $D_S$ ) is put into operation. Thus, the voltage reflected from the secondary side is inversely applied to  $L_B$ . The

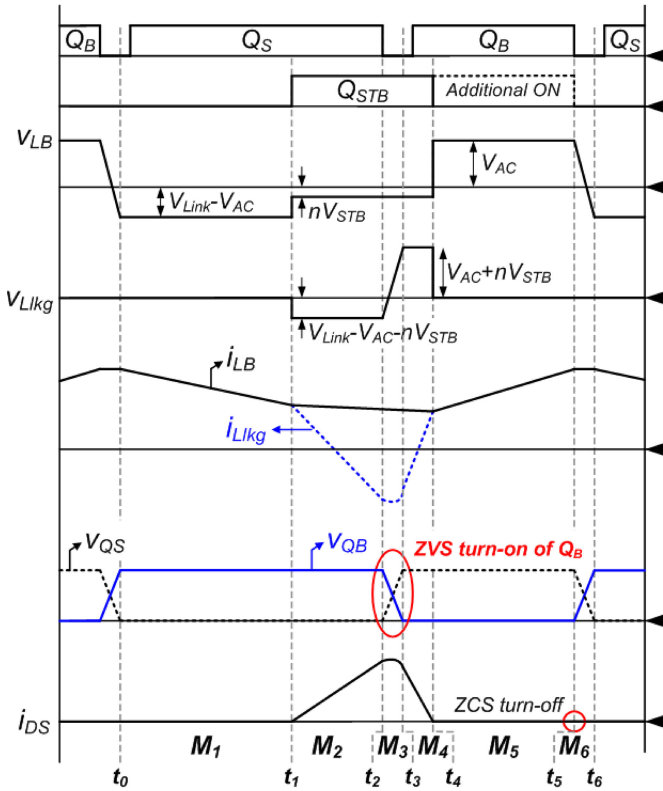


Fig. 5. Operational key waveforms of the proposed standby structure.

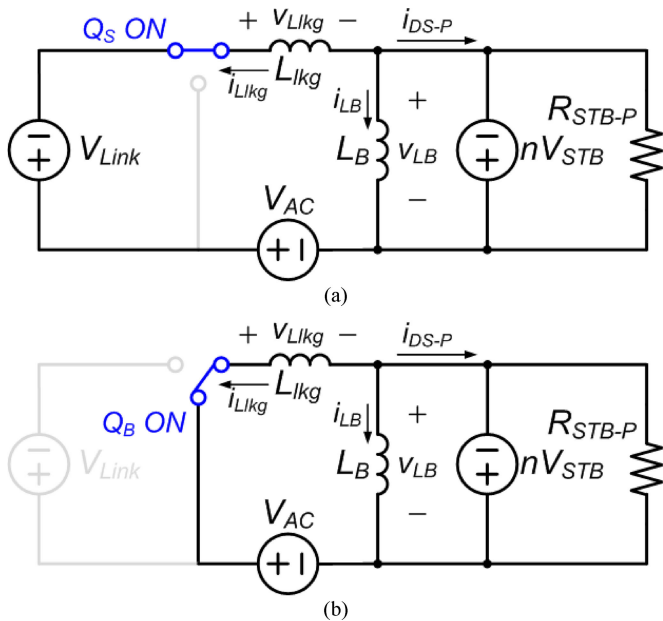


Fig. 6. Equivalent circuit reflected to the primary side. (a) In mode 2. (b) In mode 4.

equivalent circuit reflected to the primary side of this mode is as depicted in Fig. 6(a). In this figure, the voltage across  $L_{lk}$  ( $v_{Llk}$ ) becomes  $V_{AC} + nV_{STB} - V_{Link}$  and  $v_{LB}$  is  $-nV_{STB}$ . Therefore,  $i_{Llk}$  and  $i_{LB}$  can be separated, and the difference between them is transferred into  $i_{DS}$ .  $i_{Llk}$ ,  $i_{LB}$ , and  $i_{DS}$  can be expressed

as follows:

$$i_{LB}(t) = i_{LB}(t_1) - \frac{nV_{STB}}{L_B}(t - t_1) \quad (2)$$

$$i_{Llk}(t) = i_{LB}(t_1) - \frac{(V_{Link} - V_{AC} - nV_{STB})}{L_{lk}}(t - t_1) \quad (3)$$

$$i_{DS}(t) = -ni_{DS-P} = n(i_{LB}(t) - i_{Llk}(t)) \quad (4)$$

where  $n$  is the turns ratio of the transformer ( $T_{Pro}$ ), i.e.,  $N_1/N_2$ , and  $i_{DS-P}$  is the reflected  $i_{DS}$  to the primary side.

In (3), as  $i_{Llk}$  decreases, it is able to have a negative direction at the turn-OFF state of  $Q_S$ , i.e.,  $t_2$ . In addition, when  $Q_{STB}$  is turned ON at  $t_1$ , since the initial current of  $Q_{STB}$  is zero, the ZCS turn-ON of  $Q_{STB}$  can be achieved like the conventional flyback converter that operates with the discontinuous conduction mode (DCM).

**Mode 3 [ $t_2-t_3$ ]:** At time  $t_2$ ,  $Q_S$  is turned OFF. However, unlike the conventional boost PFC converter, since the current direction of  $i_{Llk}$  is negative, the body diode of  $Q_S$  is not conducted. Thus, the reverse recovery problems caused by the body diode of  $Q_S$  are eliminated in the proposed structure. Moreover, because a negative  $i_{Llk}$  is flow through  $C_{oss-QB}$  and  $C_{oss-QS}$ ,  $v_{QB}$  and  $v_{QS}$  can be discharged and charged by the energy stored in  $L_{lk}$ , respectively.

**Mode 4 [ $t_3-t_4$ ]:** At time  $t_3$ ,  $v_{QB}$  becomes zero, and then,  $i_{Llk}$  flows through the body diode of  $Q_B$ . Thus, the ZVS operation of  $Q_B$  can be achieved unlike with the conventional boost PFC converter. Moreover, in Fig. 6(b), since  $v_{Llk}$  is  $(V_{AC} + nV_{STB})$ ,  $i_{Llk}$  increases as follows:

$$i_{Llk}(t) = i_{Llk}(t_3) + \frac{(V_{AC} + nV_{STB})}{L_{lk}}(t - t_3). \quad (5)$$

Meanwhile,  $i_{LB}$  decreases continuously like (2), and the power is still transferred from the PFC stage to  $V_{STB}$  until  $i_{Llk}$  meets  $i_{LB}$ . This mode ends when  $D_S$  is turned OFF and reverse biased.

**Mode 5 [ $t_4-t_5$ ]:** At time  $t_4$ , since  $D_S$  is reverse biased, the additional ON state of  $Q_{STB}$  has no impact on the operation of the PFC stage. Thus,  $i_{LB}$  and  $i_{Llk}$  start to increase like in the conventional boost PFC converter.  $i_{LB}$  and  $i_{Llk}$  can be expressed as follows:

$$i_{LB}(t) = i_{Llk}(t) = i_{LB}(t_4) + \frac{V_{AC}}{L_B}(t - t_4). \quad (6)$$

**Mode 6 [ $t_5-t_6$ ]:** When  $Q_{STB}$  and  $Q_B$  are turned OFF at  $t_5$ , there is no current flow at  $Q_{STB}$  unlike in the conventional flyback converter. Thus,  $Q_{STB}$  can achieve the ZCS turn-OFF operation, which leads to a small turn-OFF switching loss compared to the conventional one. In addition,  $v_{QS}$  and  $v_{QB}$  are discharged and charged by the energy stored in  $L_B$ . This mode ends when  $v_{QS}$  is zero.

### C. Voltage Gain

The voltage gain of the proposed standby structure can be obtained from the operational principles in Section II-B and Fig. 5. Assuming that the duration of *Mode 3* and *Mode 6* are negligibly short, the voltage-second balance across  $L_B$  and  $L_{lk}$

can be expressed as in (7) and (8). Moreover, since the average current of  $i_{DS}$  is equal to  $I_{O-STB}$ , it can be given by (9).

$$(V_{Link} - V_{AC})D_A + nV_{STB}D_{STB} = V_{AC}(D_B - D_X) \quad (7)$$

$$(V_{Link} - V_{AC} - nV_{STB})(D_{STB} - D_X) = (V_{AC} + nV_{STB})D_X \quad (8)$$

$$\frac{1}{2}D_{STB} \times \frac{n(V_{Link} - V_{AC} - nV_{STB})}{L_{lk}}(D_{STB} - D_X)T_S = I_{O-STB} \quad (9)$$

where  $D_{STB}$  is the duty ratio of  $Q_{STB}$  except for the additional ON time,  $D_B$  is the duty ratio of  $Q_B$ ,  $D_A$  is the duty ratio of Mode 1 ( $= 1 - D_B - D_{STB} + D_X$ ),  $D_{STB} - D_X$  is the duty ratio of Mode 2,  $D_X$  is the duty ratio of Mode 4,  $D_B - D_X$  is the duty ratio of Mode 5, and  $T_S$  is the switching period.

Consequently,  $D_X$  and  $D_{STB}$  are derived from (7)–(9) as follows:

$$D_X = \frac{D_{STB}(V_{Link} - V_{AC} - nV_{STB})}{V_{Link}} \quad (10)$$

$$D_{STB} = \sqrt{\frac{2I_{O-STB}L_{lk}V_{STB}}{nT_S(V_{Link} - V_{AC} - nV_{STB})(V_{AC} + nV_{STB})}} \quad (11)$$

By substituting (10) and (11) for (7), the voltage gain of the proposed PFC stage is obtained as follows:

$$V_{Link} = \frac{V_{AC}}{1 - D_B} \quad (12)$$

As can be seen in the aforementioned equation, the voltage gain of the proposed PFC stage is the same as that of the conventional CCM boost PFC converter [19]. Therefore, it is noted that the proposed PFC stage can be designed and controlled like the conventional CCM boost PFC converter.

Meanwhile, the voltage gain of the proposed standby stage can be derived by substituting (10) and (11) for (8) as follows:

$$V_{STB} = \frac{V_{Link}}{n} \left[ \left( \frac{1}{2} - \frac{V_{AC}}{V_{Link}} \right) - \frac{A}{D_{STB}^2} + \sqrt{\frac{1}{4} + \frac{A}{D_{STB}^2} \left( \frac{A}{D_{STB}^2} - 1 + \frac{V_{Link}}{V_{AC}} \right)} \right] \quad (13)$$

where  $A$  is  $L_{lk}/(n^2T_S R_{STB})$  and  $R_{STB}$  is the output resistor of the standby stage.

Using (13),  $V_{STB}$  of the proposed standby stage can be obtained according to  $V_{AC}$ ,  $D_{STB}$ , and  $R_{STB}$ , as shown in Fig. 7. In this figure, it is seen that  $V_{STB}$  decreases as  $D_{STB}$  decreases or  $V_{AC}$  increases because the amount of power delivered to  $V_{STB}$  is determined from Mode 2 to Mode 4 in Fig. 5. Moreover,  $V_{STB}$  decreases as  $R_{STB}$  decreases. As a result, the proposed standby stage should be designed at the highest  $V_{AC}$  and the smallest  $R_{STB}$ , i.e., largest  $I_{O-STB}$ , because converters are generally designed to meet the output voltage requirement at the worst input and output conditions, which will be explained in Section III.

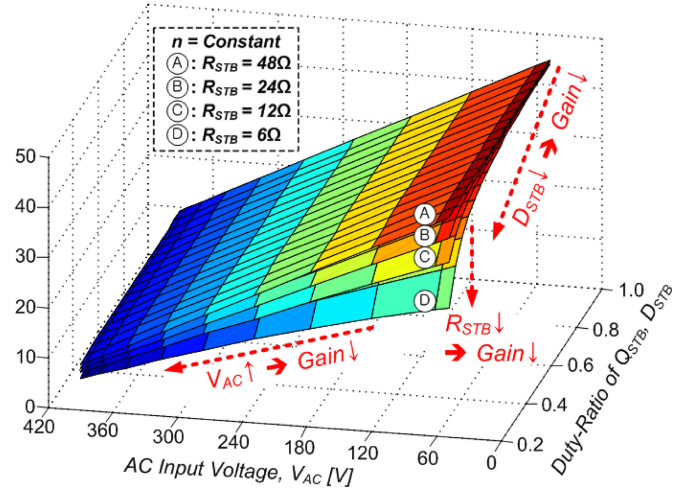


Fig. 7.  $V_{STB}$  of the proposed standby stage according to  $V_{AC}$ ,  $D_{STB}$ , and  $R_{STB}$ .

#### D. Voltage Stress on the Semiconductor Device

In this part, we discuss the voltage stresses on semiconductor devices in the conventional and proposed standby structures. In case of  $Q_B$  and  $Q_S$ , the voltage stresses are clamped to  $V_{Link}$  both in the conventional and proposed standby structures. On the other hand, since  $Q_{STB}$  in the proposed structure is located at the secondary side, the proposed structure has a different voltage stress from the conventional one as follows:

$$V_{Q_{STB-Conv}} = V_{Link} + nV_{STB} \quad (14)$$

$$V_{Q_{STB-Pro}} = (V_{Link} - V_{AC})/n - V_{STB} \quad (15)$$

where  $V_{Q_{STB-Conv}}$  and  $V_{Q_{STB-Pro}}$  are voltage stresses on  $Q_{STB}$  in the conventional and proposed standby structures, respectively.

In (14) and (15),  $V_{Q_{STB-Pro}}$  can be much smaller than  $V_{Q_{STB-Conv}}$  because  $(V_{Link} - V_{AC})$  is divided by  $n$  as well as subtracted by  $V_{STB}$ . Thus, the proposed structure relieves the problems caused by the high-voltage stress of the conventional  $Q_{STB}$ .

Meanwhile, the proposed structure has a similar voltage stress on  $D_S$  as the conventional one as in (16) and (17) because  $D_S$  is located at the secondary side both in the conventional and proposed standby structures

$$V_{DS-Conv} = V_{Link}/n + V_{STB} \quad (16)$$

$$V_{DS-Pro} = V_{AC}/n + V_{STB} \quad (17)$$

where  $V_{DS-Conv}$  and  $V_{DS-Pro}$  are voltage stresses on  $D_S$  in the conventional and proposed standby structures, respectively.

#### E. ZVS Condition of $Q_B$

In the conventional boost PFC converter, the ZVS operation of  $Q_B$  cannot be achieved due to positive turn-ON current of  $Q_B$ . Thus, the conventional boost PFC converter has a large turn-ON switching loss and discharging loss of  $Q_B$ . However, as mentioned in Section II-B,  $i_{Llk}$  of the proposed standby structure decreases considerably while delivering the power from the

TABLE I  
KEY DIFFERENCES BETWEEN THE CONVENTIONAL AND PROPOSED  
STANDBY STRUCTURES

|                | Conventional Structure                     | Proposed Structure                             |
|----------------|--|--|
| Control        | Independent control of $Q_{STB}$ and $Q_B$ | Synchronization control of $Q_{STB}$ and $Q_B$ |
| Magnetic core# | 2  | 1  |
| RCD snubber    | O  | X  |
| $Q_{STB}$      | High voltage stress (ZCS turn ON)          | Low voltage stress (ZCS turn ON/OFF)           |
| $Q_B$ & $Q_S$  | Hard switching operation                   | Soft switching operation                       |

PFC stage to  $V_{STB}$  so it can have a negative direction. Thus, the proposed structure achieves a negative turn-ON current of  $Q_B$ , which can be obtained by using (3), (10), and (11) as follows:

$$i_{QB-ON} = i_{Llk}(t_2)$$

$$= i_{AC-Avg} - 0.5\Delta i_{LB} - \frac{V_{Link} - V_{AC} - nV_{STB}}{L_{lk}}(D_{STB} - D_X)T_S \quad (18)$$

where  $i_{QB-ON}$  is the turn-ON current of  $Q_B$ ,  $i_{AC-Avg}$  is the average input current, and  $\Delta i_{LB}$  is the ripple current of  $i_{LB}$ .

Therefore, provided that  $i_{QB-ON}$  is a negative value, the ZVS operation of  $Q_B$  can be achieved by the energy stored in  $L_{lk}$ . The ZVS condition of  $Q_B$  is expressed as follows:

$$L_{lk}i_{QB-ON}^2 \geq (C_{OSS-QB-ER} + C_{OSS-QS-ER})V_{Link}^2 \quad (19)$$

where  $C_{OSS-ER}$  is the effective energy-related output capacitance of  $C_{OSS-QB}$  and  $C_{OSS-QS}$ .

In summary, based on parts A~E, the key differences between the conventional and proposed standby structures are summarized as shown in Table I. The proposed standby structure can increase the control complexity because it should synchronize the operation of  $Q_{STB}$  and  $Q_B$ . Moreover, it can be effective only in applications where the standby stage provides much lower output power than the PFC stage, such as server power supplies and PC power supplies. This is because higher output power of the standby stage causes much larger negative  $i_{Llk}$ , which leads to larger conduction losses and larger EMI filter size compared to the conventional standby structure. However, in the server power applications, since the standby output power is much smaller than the main output power, the side effect of the negative  $i_{Llk}$  on the conduction loss and EMI filter can be negligible. Moreover, the proposed standby structure can eliminate the conventional flyback transformer ( $T_{Fly}$ ) and RCD snubber, which results in high power density and high efficiency. Furthermore, it can reduce the switching losses on  $Q_{STB}$ ,  $Q_B$ , and  $Q_S$ . Therefore, the proposed standby structure can achieve high efficiency and high power density compared to the conventional standby structure.

### III. DESIGN CONSIDERATION OF THE PROPOSED STANDBY STRUCTURE

The proposed standby structure is composed of the proposed PFC and standby stages as shown in Fig. 4. Thus, we discuss each stage to explain the design consideration of the

TABLE II  
DESIGN PARAMETERS OF PFC STAGES

| Items                   | Conventional  | Proposed   |
|-------------------------|---|--|
| Boost switch, $Q_B$     | IPP60R099C6 ( $C_{OSS-QB-ER}$ : 100pF)  |  |
| Rectifier switch, $Q_S$ | GS66508T<br>( $C_{OSS-QS-ER}$ : 88pF)   | IPP60R099C6<br>( $C_{OSS-QS-ER}$ : 100pF)  |
| Magnetic core           | Boost inductor ( $L_B$ )<br>Core :<br>CH270043*2EA<br>$L_B$ : 610μH<br>$N_j$ : 82T (1.0φ) | Boost transformer ( $T_{pro}$ )<br>Core : CH270043*2EA<br>$L_B$ : 610μH, $L_{lk}$ : 35μH<br>$N_j$ : $N_2$<br>= 82(1.0φ) : 24(0.8φ) |

proposed standby structure in this section. The design specifications are 100–240  $V_{RMS}$  ac input (Nominal input: 115  $V_{RMS}$  and 230  $V_{RMS}$ ), 750-W PFC output, and 24-W/12-V standby output.

#### A. Proposed PFC Stage

In (12), the voltage gain of the proposed PFC stage is the same as that of the conventional CCM boost PFC converter. Thus, the proposed PFC stage can be designed like the conventional CCM boost PFC converter, which is well described in [20]. Table II shows the designed parameters of the conventional and proposed PFC stages. From this table, in the conventional PFC stage, the GaN device is used for  $Q_S$  to relieve the reverse recovery problems. On the other hand, in the proposed PFC stage, the Si-MOSFET can be used for  $Q_S$  because the proposed PFC stage is able to alleviate the reverse recovery problems by obtaining the soft switching operation. The boost inductor ( $L_B$ ) is designed to be about 610 μH using two high-flux CH 270043 cores for 20% ripple current at 115 $V_{RMS}$  condition. Meanwhile, since the proposed PFC stage replaces  $L_B$  with a transformer ( $T_{Pro}$ ), it has a leakage inductor ( $L_{lk}$ ) measured as 35 μH in the experiment due to the secondary winding ( $N_2$ ). Thus, the volume of  $T_{Pro}$  may be slightly larger than that of the conventional  $L_B$  due to  $N_2$ . However, the proposed PFC stage can be designed and controlled like the conventional CCM boost PFC converter because  $L_{lk}$  is much smaller than  $L_B$ .

#### B. Proposed Standby Stage

In the proposed standby structure, since the standby stage shares the structure of the PFC stage, it should be designed not to have influence on the design procedure of the PFC stage. Consequently, almost parameters of the proposed standby stage, such as  $V_{Link}$ ,  $L_B$ , and  $L_{lk}$ , are determined by the design procedure of the PFC stage. As a result, a design parameter of the proposed standby stage is the turns ratio of  $T_{Pro}$  ( $n$ ), which must properly be selected by considering following conditions: 1) voltage gain; 2) voltage stress; and 3) ZVS condition of  $Q_B$ .

First, the voltage gain of the proposed standby stage should be taken into account. As mentioned previously, the worst input and output conditions of the proposed standby stage is the highest  $v_{AC}$  and largest  $I_{O-STB}$ . Moreover, in this example, a 10% voltage margin is considered. Thus,  $n$  should be designed at 264  $V_{RMS}$  input and 2-A output current conditions. Fig. 8 shows  $V_{STB}$  of the proposed standby stage according to  $D_{STB}$  and  $n$  at 264  $V_{RMS}$  and full-load conditions. As can be seen in Fig. 8, the

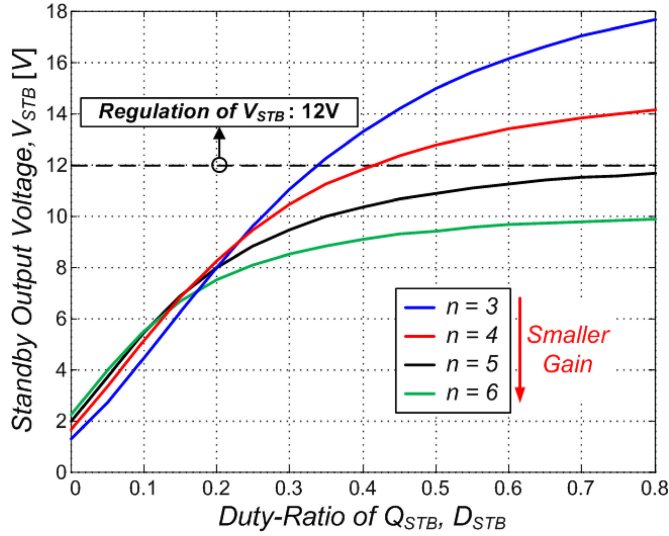


Fig. 8.  $V_{STB}$  of the proposed standby stage according to  $D_{STB}$  and  $n$  at  $264 V_{RMS}$  condition.

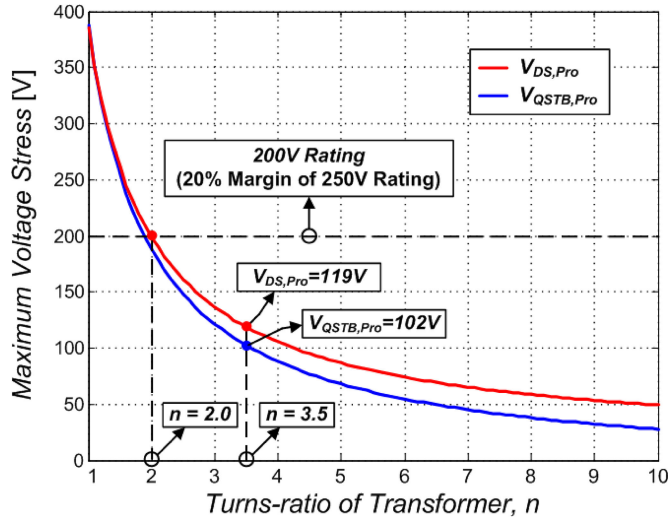


Fig. 9. Maximum voltage stress on  $Q_{STB}$  and  $D_S$  according to  $n$ .

maximum  $V_{STB}$  decreases as  $n$  increases. In particular, when  $n$  is larger than 5, the proposed standby stage cannot regulate  $V_{STB}$  as 12 V regardless of  $D_{STB}$ . Therefore,  $n$  should be smaller than 5 to meet the voltage regulation requirement.

Second, the voltage stresses on  $Q_{STB}$  and  $D_S$  should be considered. In (15) and (17), the maximum  $V_{QSTB-Pro}$  and  $V_{DS-Pro}$  are depicted according to  $n$ , as shown in Fig. 9. From this figure, the maximum  $V_{QSTB-Pro}$  and  $V_{DS-Pro}$  increase when  $n$  decreases. Thus,  $n$  needs to be larger to use lower voltage rated semiconductor devices, which generally have a higher performance, such as a low channel resistance and low forward voltage drop. In particular, considering a 20% voltage margin,  $n$  should be larger than 2 to adopt less than 250-V-rated semiconductor devices in this example.

Finally,  $n$  should be designed taking into account the ZVS condition of  $Q_B$ . As mentioned before, the proposed standby structure can have negative turn-ON current of  $Q_B$  ( $i_{QB-ON}$ )

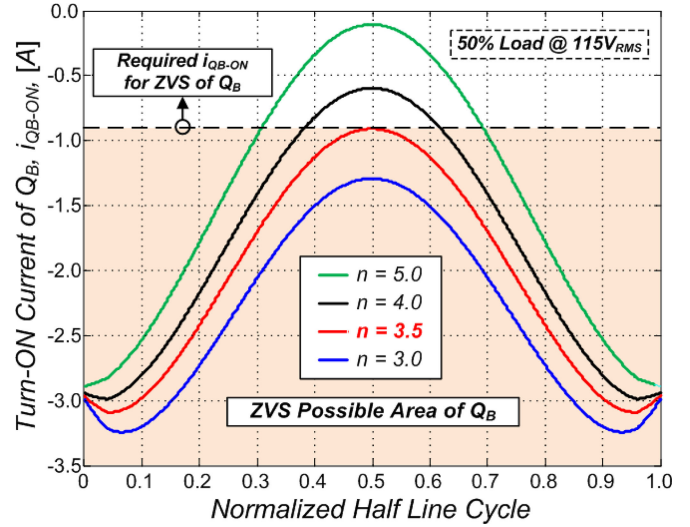


Fig. 10. Turn-ON current of  $Q_B$  according to  $n$  at  $115 V_{RMS}$  and 50% load conditions.

as in (18). Thus, when  $n$  is designed to satisfy (19), the proposed standby structure achieves not only a zero reverse recovery of  $Q_S$  but also the ZVS operation of  $Q_B$ . Meanwhile, among load conditions, the server power supply should achieve the highest efficiency at 50% load conditions [2]. Moreover, between two nominal input voltage conditions, i.e.,  $115 V_{RMS}$  and  $230 V_{RMS}$  conditions, it is difficult to achieve the ZVS operation at  $115 V_{RMS}$  conditions. Thus, the proposed standby structure is designed to achieve the ZVS operation at  $115 V_{RMS}$  and 50% load conditions in this example. Fig. 10 shows  $i_{QB-ON}$  according to  $n$  at  $115 V_{RMS}$  and 50% load conditions. Moreover, based on design specifications and Table II, the required  $i_{QB-ON}$  guaranteeing the ZVS operation of  $Q_B$  is depicted as the dashed line. Thus, the region below the dashed line means the ZVS possible area of  $Q_B$ . For example, when  $n$  is larger than 3.5, the proposed standby structure cannot satisfy the ZVS condition of  $Q_B$  around the peak of  $v_{AC}$ , which results in a turn-ON switching loss and a discharging loss of  $Q_B$ . On the other hand, when  $n$  is smaller than 3.5, too much negative current flows through  $Q_B$  and  $Q_S$ . Thus, it causes a large conduction loss and turn-OFF switching loss of  $Q_B$  and  $Q_S$ .

In summary,  $n$  is selected as 3.5 in this example by considering the three conditions, i.e., voltage gain, voltage stress, and ZVS condition. Thus,  $V_{QSTB-Pro}$  is 102 V,  $V_{DS-Pro}$  is 119 V, and  $N_2$  can be chosen as 24 turns.

#### IV. EXPERIMENTAL RESULTS

To confirm the validity of the proposed standby structure, we built and tested a prototype with the specifications of 100–240  $V_{RMS}$  ac input (Nominal input:  $115 V_{RMS}$  and  $230 V_{RMS}$ ), 750-W PFC output, 24-W/12-V standby output, and 100-kHz switching frequency. In addition, for the comparison, we also implemented a prototype of the conventional standby structure. In two prototypes,  $Q_B$  and  $Q_S$  operate with the CCM duty ratio regardless of load conditions for high power quality by avoiding the input current distortion in the mixed conducted

TABLE III  
DESIGN PARAMETERS OF STANDBY STAGES

| Items         | Conventional  | Proposed   |
|---------------|---|--|
| Switch, $Q_B$ | SPA08N80C3<br>( $V_{DS}=800V$ , $R_{DS}=650m\Omega$ )   | IPI110N20N3G<br>( $V_{DS}=200V$ , $R_{DS}=13m\Omega$ ) |
| Diode, $Q_S$  | STPS20120C<br>( $V_{RRM}=120V$ , $V_F=0.51V$ )  | MBR20200CT<br>( $V_{RRM}=200V$ , $V_F=0.63V$ )         |
| Magnetic core | Core : EED1521<br>$L_m : 1mH$ , $L_{lk} = 30\mu H$<br>$N_1 : N_2$<br>$= 78 (0.25\phi) : 10 (0.6\phi)$ | -  |
| RCD snubber   | $R_{snb} : 40k\Omega$ , $C_{snb} : 47nF$<br>$D_{snb} : SIM(V_{RRM}=1200V)$                            | -  |

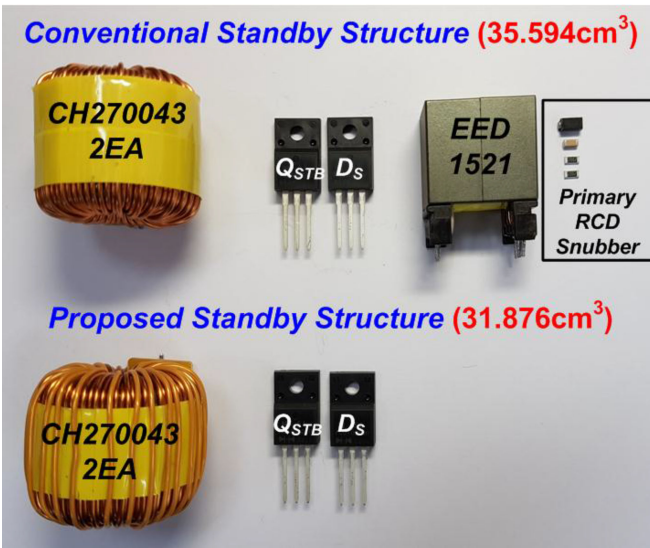


Fig. 11. Size comparison of key components.

mode [4], [21]. Moreover, a digital controller TMS320F28069 was used due to its flexibility, and the designed parameters are presented in Tables II and III. These tables show that the proposed PFC stage has the same parameters as the conventional boost PFC converter except for the secondary winding of  $T_{P_{ro}}$ , which slightly increases the volume of  $T_{P_{ro}}$  compared to the conventional  $L_B$ . On the other hand, in the standby stage, the proposed structure used  $Q_{STB}$  with a 200-V-rated device, which is much smaller than the conventional  $Q_{STB}$  with an 800-V-rated device. Moreover, it eliminates the large transformer and RCD snubber used in the conventional flyback converter. As a result, as shown in Fig. 11, the proposed standby structure reduces the total volume of key components so that it can achieve a higher power density than the conventional standby structure.

Figs. 12 and 13 show the experimental waveforms of the proposed standby structure under 10% and 100% load conditions at  $115V_{RMS}$  and  $230V_{RMS}$ , respectively. These figures show that  $i_{L_{lk}}$  of the proposed structure has a negative current direction, which is unlike the conventional boost PFC converter [3]–[5]. Thus, the proposed structure is able to achieve the soft switching operation of  $Q_B$  and  $Q_S$ . Moreover, despite a negative  $i_{L_{lk}}$ , since the input filter can average the input current ( $i_{AC}$ ), the shape of  $i_{AC}$  is well controlled like  $v_{AC}$ . Therefore,

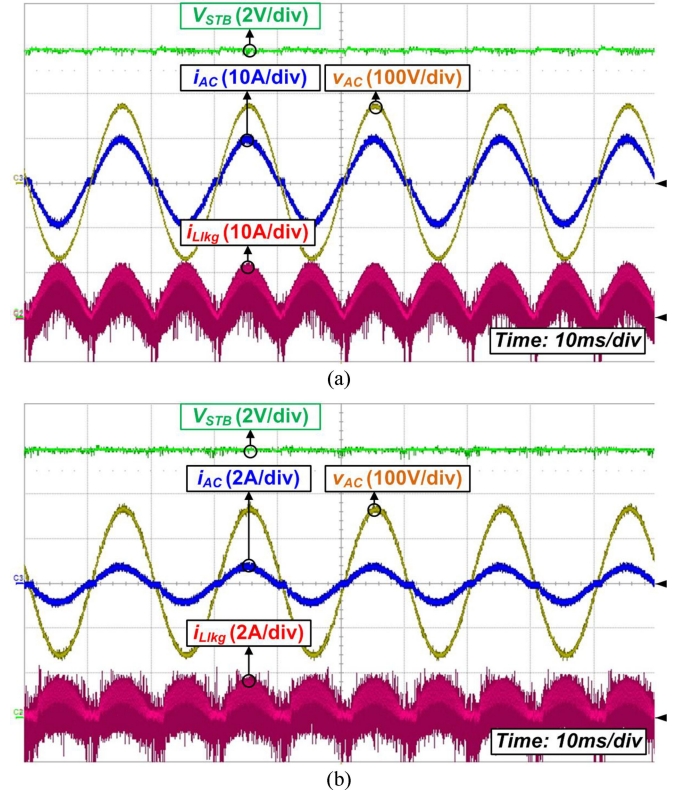


Fig. 12. Experimental key waveforms of the proposed standby structure at  $115V_{RMS}$ . (a) 100% load condition. (b) 10% load condition.

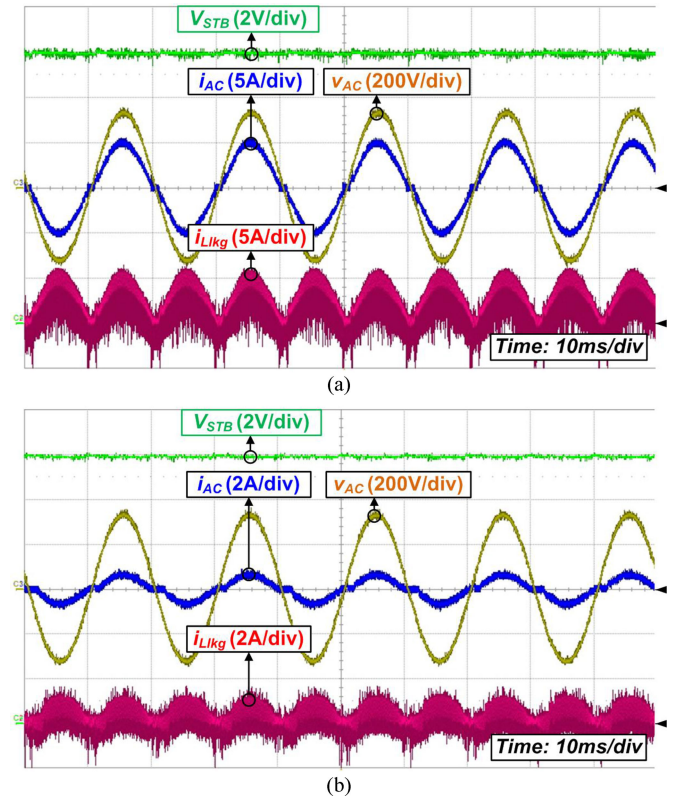


Fig. 13. Experimental key waveforms of the proposed standby structure at  $230V_{RMS}$ . (a) 100% load condition. (b) 10% load condition.

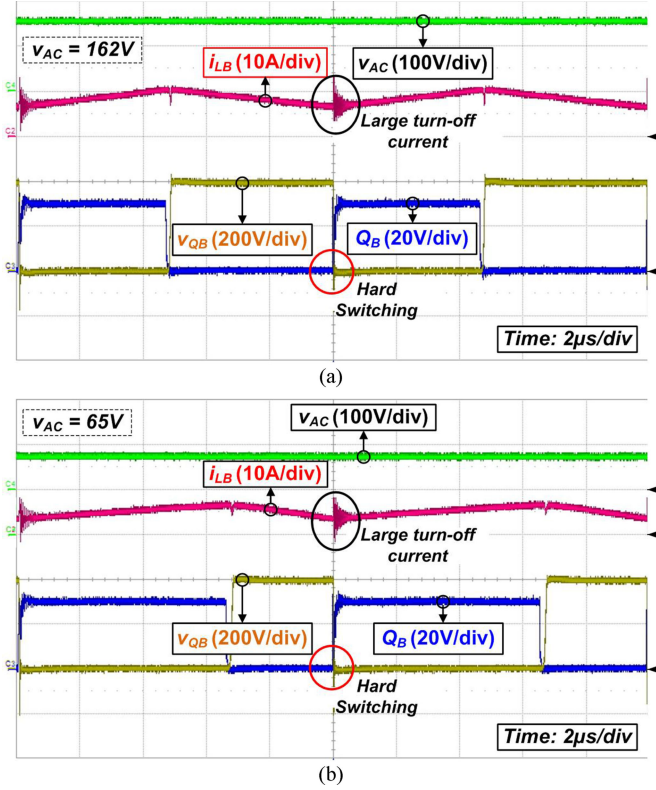


Fig. 14. ZVS waveforms of  $Q_B$  in the conventional standby structure at 115  $V_{RMS}$  and 100% load conditions. (a)  $v_{AC} = 162$  V. (b)  $v_{AC} = 65$  V.

the proposed structure maintains good power quality like the conventional boost PFC converter. Furthermore,  $V_{STB}$  is well regulated in the proposed structure.

Fig. 14 shows the ZVS waveforms of  $Q_B$  in the conventional standby structure at 115 $V_{RMS}$  and 100% load conditions, which is the worst ZVS condition of  $Q_B$  between two nominal input conditions. From these figures, the boost inductor current ( $i_{LB}$ ) has a positive current direction regardless of  $v_{AC}$ . Thus,  $Q_B$  and  $Q_S$  have the hard switching operation, which causes large switching loss and reverse recovery problems at the turn-ON state of  $Q_B$ . On the other hand, Fig. 15 shows the ZVS waveforms of  $Q_B$  in the proposed standby structure. In Fig. 15(a), when  $v_{AC}$  is 162 V,  $i_{Llk}$  does not have a negative current because  $i_{AC}$  is larger than the transferred current into the standby stage. Thus,  $Q_B$  and  $Q_S$  have the hard switching operation like the conventional boost PFC converter. However, since the turn-ON and turn-OFF currents of  $Q_B$  and  $Q_S$  are considerably reduced, the turn-ON switching loss of  $Q_B$  and reverse recovery problems are relieved compared to the conventional ones. On the other hand, in Fig. 15(b), when  $v_{AC}$  is lower than 65 V,  $i_{Llk}$  has enough negative current to achieve the ZVS operation of  $Q_B$  due to a small  $i_{AC}$ . Therefore, unlike the conventional boost PFC converter, the proposed structure achieves the soft switching operation of  $Q_B$  and  $Q_S$ , which results in a small switching loss.

Fig. 16 shows experimental waveforms with the standby load transient at 230 $V_{RMS}$  and 100% PFC output conditions. Since the proposed standby stage has similar characteristics with the

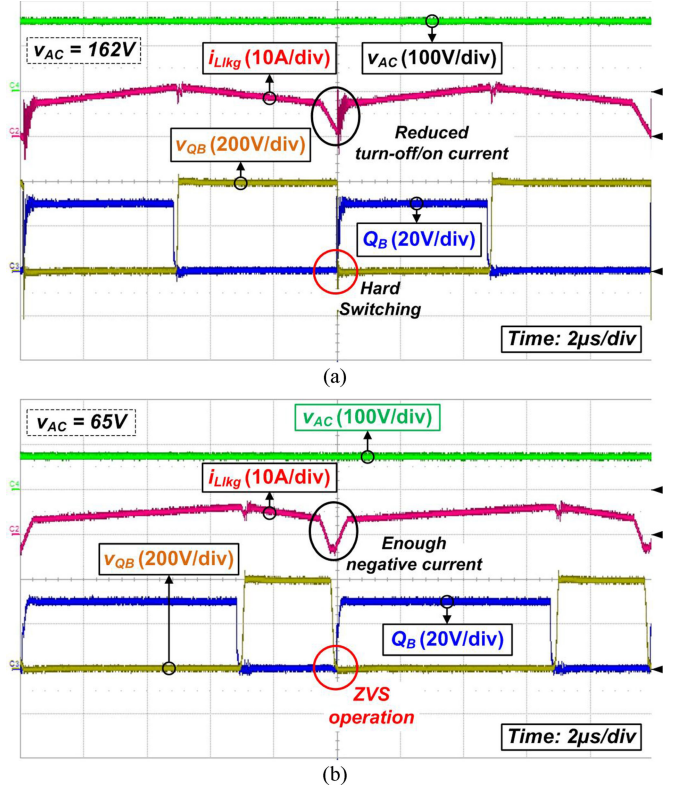


Fig. 15. ZVS waveforms of  $Q_B$  in the proposed standby structure at 115  $V_{RMS}$  and 100% load conditions. (a)  $v_{AC} = 162$  V. (b)  $v_{AC} = 65$  V.

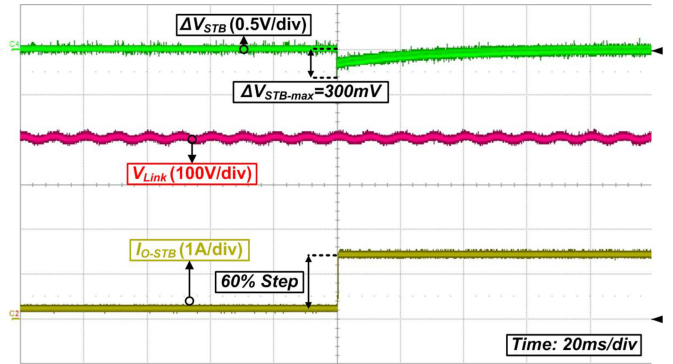


Fig. 16. Experimental waveforms with standby load transient from 10% to 70% at 230  $V_{RMS}$ .

DCM buck converter, it can achieve 10-kHz bandwidth. Thus, despite of the 60% load variation, the standby output voltage is well regulated and varies within 600 mV. Meanwhile, the proposed PFC stage can achieve similar dynamic performance with the conventional one because it is able to be designed like the conventional PFC stage.

Fig. 17 shows the measured system efficiency of the conventional and proposed standby structures at 115  $V_{RMS}$  and 230  $V_{RMS}$  in the normal mode where the server power supply usually operates. Moreover, the efficiency was measured with two power analyzers, WT1600, to measure the input and output power. In this figure, the proposed standby structure has a higher efficiency than the conventional one over the entire

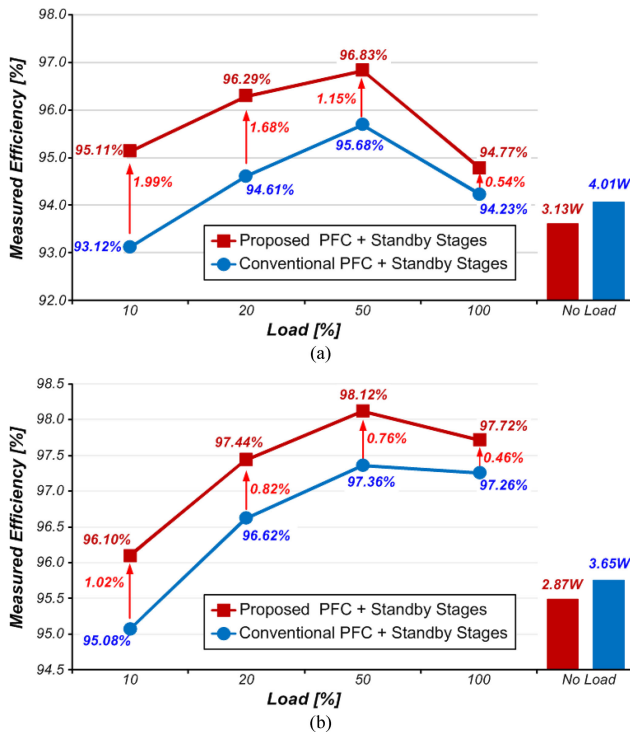


Fig. 17. Measured efficiency. (a) 115  $V_{RMS}$ . (b) 230  $V_{RMS}$ .

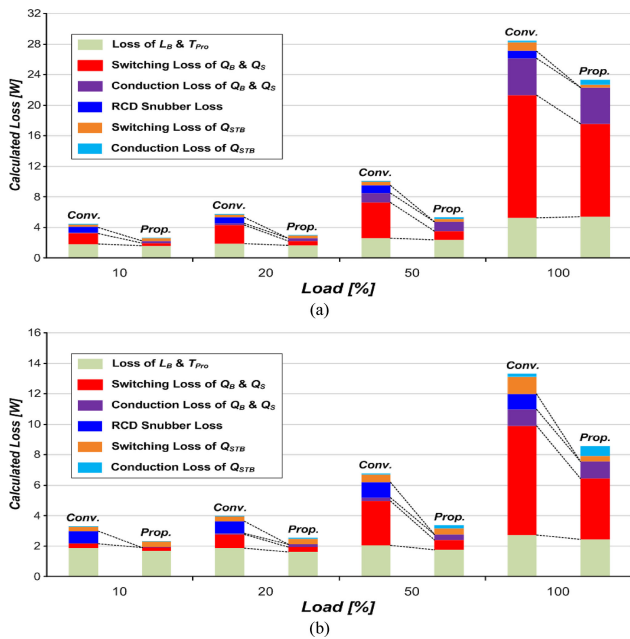


Fig. 18. Loss distribution. (a) 115  $V_{RMS}$ . (b) 230  $V_{RMS}$ .

load and input voltage conditions. This result is achieved by the eliminated *RCD* snubber loss and reduced switching loss of  $Q_B$ ,  $Q_S$ , and  $Q_{STB}$ . In addition, at no-load condition, the proposed standby structure can achieve small no-load power consumption compared to the conventional standby structure because it can reduce the power loss caused by the standby stage. The detailed loss distribution is shown in Fig. 18. In addition, as can be seen in Fig. 19, the proposed structure has a power factor and total harmonic distortion similar to the conventional standby

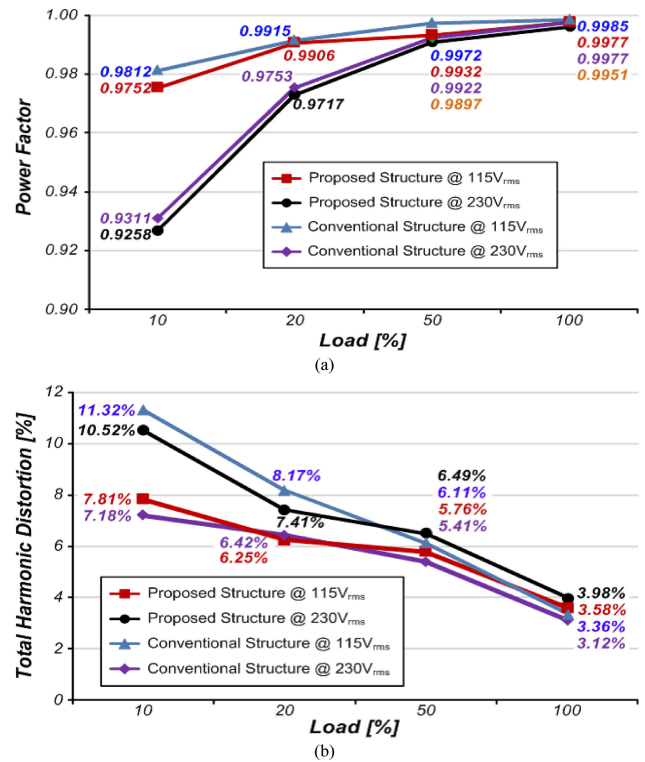


Fig. 19. Measured power quality. (a) 115  $V_{RMS}$ . (b) 230  $V_{RMS}$ .

structure. This is because it can be controlled like the conventional boost PFC converter and its input filter can make the impact of negative  $i_{Llk}$  on the power quality be negligible. As a result, the proposed structure achieves not only higher efficiency but also higher power density than the conventional standby structure while maintaining high power quality.

## V. CONCLUSION

In this paper, we proposed a new standby structure in which the primary side of the flyback converter is integrated with the boost PFC converter to improve the efficiency and power density of the server power supply. Compared to the conventional standby flyback converter, which suffers from high-voltage stress and a large transformer, the proposed standby stage relieves high-voltage stress and eliminates the large transformer. Thus, the proposed standby structure improves the efficiency and power density of the standby stage. Moreover, when the input power is transferred from the proposed PFC stage to the standby stage, the proposed PFC stage can obtain a negative current direction. Thus, the proposed PFC stage can obtain a soft switching operation of  $Q_B$  and  $Q_S$ , which leads to higher efficiency. As a result, the proposed standby structure is expected to be very attractive in a server power supply requiring high efficiency and high power density.

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