A Negative-Output High Quadratic Conversion Ratio DC–DC Converter With Dual Working Modes

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***Abstract*—A negative-output high quadratic conversion ratio dc–dc converter with dual working modes is proposed. One working mode is a step-up mode, and the other is a step-up/step-down mode. Analysis of the circuit principle and different operation modes, steady-state calculation, and small-signal modeling are presented. Comparisons of the proposed converter with other converters demonstrate that the proposed converter has a higher conversion ratio in its two working modes and, under the same voltage gain, the proposed converter in the second working mode has the lowest switching device power rating, a higher efficiency, and small peak-to-peak value of input current. Simulation results based on PSpice and circuit experiments are given to verify the effectiveness of the proposed converter.**

***Index Terms*—DC–DC, dual working modes, negative-output (N-O), quadratic conversion ratio, step up, step up/step down.**

I. Introduction

RENEWABLE and clean energy sources such as photovoltaic (PV) cells and fuel cells are increasing rapidly worldwide, and for these sources' inherent low-voltage characteristic, a prestage high gain dc–dc converter is essential [1], [2]. For example, in a PV system, use of a high-gain dc–dc boost converter is superior to numerical PV modules connected in series to avoid shading problems and decreased reliability [3]. Moreover, dc–dc switched power supplies with high-voltage gain are indispensable in applications to uninterruptible power supplies, X-ray systems, and high-density discharge lamps [4], [5]. However, conventional dc–dc boost converters or buck–boost converters are two common ways to get the required output voltage within a wide range of input voltages, ultrahigh gain cannot be obtained for the requirement of extreme high duty cycle cannot be met because of the constraint of control circuit and semiconductor devices [6].

In the past few decades, numerous new dc–dc converters with high-voltage gain have been devised. Maksimovic and Cuk devised a series of quadratic converters [7], but, in practice, most of them can only work in step-up mode or step-down mode.

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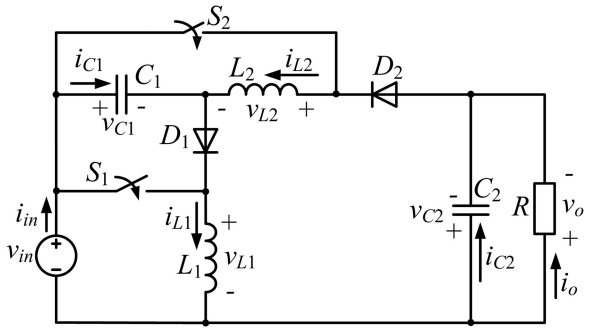

Fig. 1. Proposed high quadratic conversion ratio converter with dual working modes.

ing is presented in Section IV. The design procedure along with the simulation results are given in Section V. Some comparisons with other converters are shown in Section VI. Efficiency analysis and nonideal conversion ratio analysis are given in Section VII. Experimental results are given in Section VIII. Finally, some conclusions are listed in Section IX.

II. Circuit Structure and Operating Principle

Fig. 1 shows the circuit for the proposed high quadratic conversion ratio converter with dual working modes, which contains two power switches (S_1 and S_2), two power diodes (D_1 and D_2), two inductors (L_1 and L_2), two capacitors (C_1 and C_2), and a resistive load R.

A. Mode1 (Step-Up Mode)

Fig. 2 shows the typical time-domain waveforms when power switches S_1 and S_2 are working complementarily in CCM mode.

1) State 1 $(NT \le t < (N+D)T)$*:* As shown in Fig. 3(a), during this time period, power switch S_1 and power diode D_2 are turned ON at the same time, inductor L_1 is magnetized while inductor L_2 is demagnetized, and capacitor C_1 is discharged and output capacitor C_2 is charged. Thus, the following equations can be obtained:

$$V_{L_1} = v_{\text{in}} \tag{1}$$

$$V_{L_2} = -v_{\text{in}} + v_{C1} - v_{C2}. \tag{2}$$

2) State 2 $((N+D)T < t \le (N+1)T)$*:* In state 2, switch S_2 and diode D_1 are conducted, inductor L_1 is demagnetized and inductor L_2 is magnetized, and capacitor C_1 is charged and output capacitor C_2 is discharged. Thus, we obtain the following equations:

$$V_{L_1} = v_{\text{in}} - v_{C1} \tag{3}$$

$$V_{L_2} = v_{C1}. \tag{4}$$

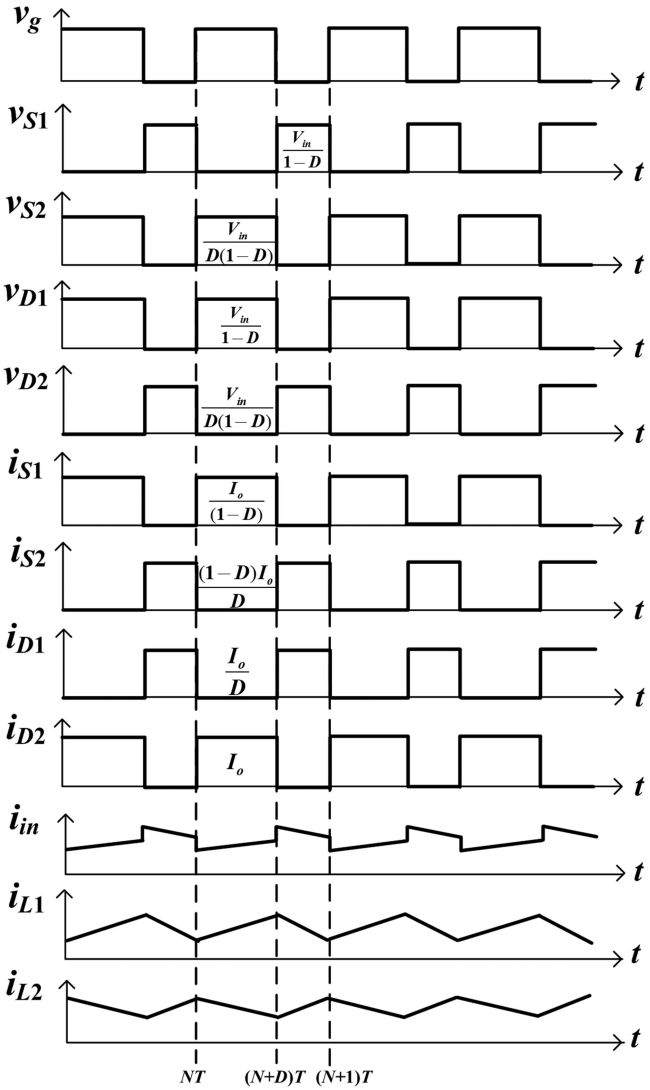

Fig. 2. Typical time-domain waveforms of the proposed converter in mode1 in CCM.

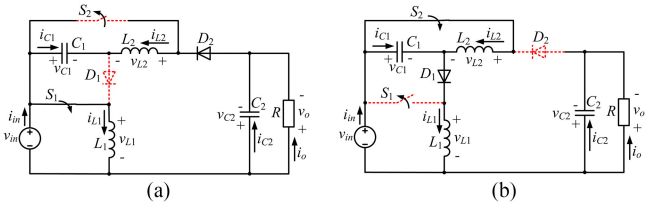

Fig. 3. Equivalent circuits of the proposed converter in mode 1. (a) State 1 ($S = 1$). (b) State 2 ($S = 0$).

B. Mode 2 (Step-Up/Step-Down Mode)

Fig. 4 shows the typical time-domain waveforms when power switches S_1 and S_2 are working simultaneously in CCM mode.

1) State 1 $(NT \le t < (N+D)T)$*:* As shown in Fig. 5(a), during this time period, power switches S_1 and S_2 are turned ON simultaneously, inductor L_1 and L_2 are magnetized, and capacitor C_1 is discharged and output capacitor C_2 is charged.

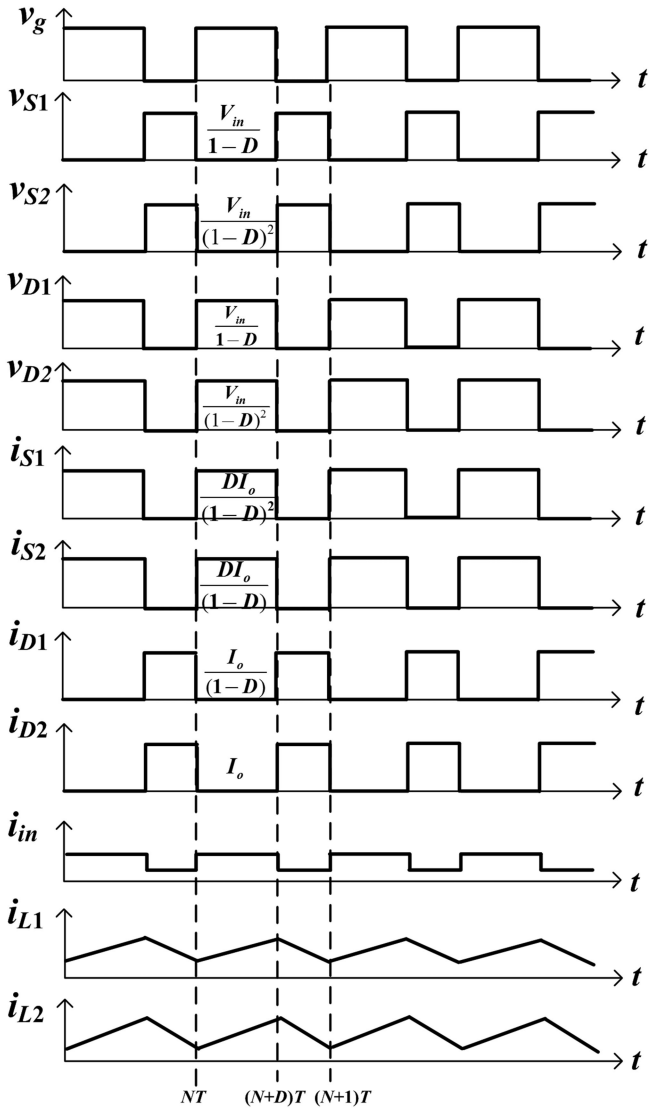

Fig. 4. Typical time-domain waveforms of the proposed converter in mode 2 in CCM.

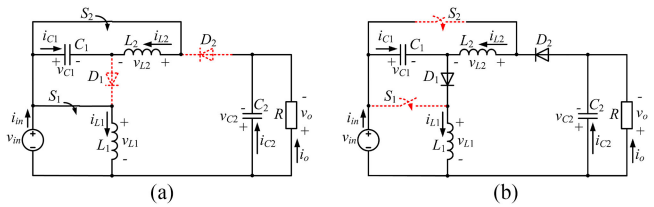

Fig. 5. Equivalent circuits of the proposed converter in mode 2. (a) State 1 ($S = 1$). (b) State 2 ($S = 0$).

Thus, the following equations can be obtained:

$$V_{L_1} = v_{\text{in}} \tag{5}$$

$$V_{L_2} = v_{C1}. \tag{6}$$

2) State 2 ($(N + D)T < t \leq (N + 1)T$): In state 2, the power diodes D_1 and D_2 are conducted, inductors L_1 and L_2 are demagnetized, and capacitor C_1 is charged and output capacitor C_2 is discharged, so we can write the following equations:

$$V_{L_1} = v_{\text{in}} - v_{C1} \tag{7}$$

$$V_{L_2} = -v_{\text{in}} + v_{C1} - v_{C2}. \tag{8}$$

III. Steady-State Analysis

To perform the steady-state analysis, the following assumptions must first be made.

1) The components including resistors, capacitors, and inductors are linear time invariant.
2) Only the CCM is considered.
3) $I_{L1}, I_{L2}, V_{\text{in}}, V_{C1}, V_{C2}$, and D are the steady-state dc values of $i_{L1}, i_{L2}, v_{\text{in}}, v_{C1}, v_{C2}$, and d.

A. Mode1 (Step-Up Mode)

1) Voltage Gain: By applying volt–second balance principle to inductors L_1 and L_2, the voltage across capacitor C_1 in steady state and the voltage gain G can be expressed as

$$V_{C1} = \frac{1}{1-D} V_{\text{in}} \tag{9}$$

$$G = \frac{V_{C2}}{V_{\text{in}}} = \frac{1 - D + D^2}{D(1-D)}. \tag{10}$$

2) Electric Stress Analysis: From a circuit analysis, the voltage stresses of two power switches (S_1 and S_2) and two diodes (D_1 and D_2) are

$$V_{S1} = \frac{1}{1-D} V_{\text{in}} \tag{11}$$

$$V_{S2} = \frac{1}{(1-D)D} V_{\text{in}} \tag{12}$$

$$V_{D1} = \frac{1}{(1-D)} V_{\text{in}} \tag{13}$$

$$V_{D2} = \frac{1}{(1-D)D} V_{\text{in}}. \tag{14}$$

The input current can be expressed by input/output power balance consideration described as $V_{\text{in}} I_{\text{in}} = V_o I_o$

$$I_{\text{in}} = \frac{1 - D + D^2}{D(1-D)} I_o. \tag{15}$$

By applying the ampere–second balance principle to capacitor C_1 and output capacitor C_2, the dc values in steady state of I_{L1} and I_{L2} can be derived as follows:

$$I_{L1} = \frac{1}{(1-D)D} I_o \tag{16}$$

$$I_{L2} = \frac{1}{D} I_o. \tag{17}$$

The current stresses of two power switches (S_1 and S_2) and two diodes (D_1 and D_2) are

$$I_{S1} = DI_{L1} = \frac{1}{(1-D)} I_o \tag{18}$$

$$I_{S2} = (1-D)I_{L2} = \frac{(1-D)}{D} I_o \tag{19}$$

$$I_{D1} = (1-D)I_{L1} = \frac{1}{D} I_o \tag{20}$$

$$I_{D2} = DI_{L2} = I_o. \tag{21}$$

3) Voltage Ripple of Capacitors and Current Ripple of Inductors: The voltage ripples across capacitors C_1 and C_2 and the current ripples through inductors L_1 and L_2 are defined as Δv_{C1} and Δv_{C2} and Δi_{L1} and Δi_{L2} (all of which are peak-to-peak values), respectively. From simulation waveforms, using a geometrical method to calculate the ripples of capacitor voltages $\Delta v_{C1}, \Delta v_{C2}$ and the ripples of inductor currents Δi_{L1} and Δi_{L2}, results in

$$\Delta v_{C1} = \frac{I_{C1}}{C_1} DT = \frac{V_{\text{in}}}{C_1 Rf} \frac{1-D+D^2}{D(1-D)} \tag{22}$$

$$\Delta v_{C2} = \frac{I_{C2}}{C_2} DT = \frac{V_{\text{in}}}{C_2 Rf} \frac{1-D+D^2}{D} \tag{23}$$

$$\Delta i_{L1} = \frac{V_{L1}}{L_1} DT = \frac{V_{\text{in}}}{L_1 f} D \tag{24}$$

$$\Delta i_{L2} = \frac{V_{L2}}{L_2} DT = \frac{V_{\text{in}}}{L_2 f}. \tag{25}$$

4) Boundary Condition Between CCM and Discontinuous-Conduction Mode (DCM): The inductor current is designed to be continuous with respect to EMI and electromagnetic compatibility. In the boundary condition mode, inductor current I_{L1} reaches its zero point at the end of each switching cycle NT and inductor current I_{L2} reaches its zero point at the time point $(N+D)T$ within each switching cycle. For CCM operation, the average value of inductor currents must be greater than half the amount of current ripples

$$I_{L1} > \frac{1}{2} \Delta i_{L1} \tag{26}$$

$$I_{L2} > \frac{1}{2} \Delta i_{L2} \tag{27}$$

where the normalized inductor time constant $\tau_{L1,2}$ is defined as $\tau_{L1,2} = \frac{L_{1,2} f}{R}$. Therefore, the boundary conditions for L_1 and L_2 are

$$\tau_{L1B} = \frac{D^3 (1-D)^2}{2(1-D+D^2)} \tag{28}$$

$$\tau_{L2B} = \frac{D^2 (1-D)}{2(1-D+D^2)}. \tag{29}$$

Based on (28) and (29), the relationship between $\tau_{L1,2}$ and duty cycle D is plotted in Fig. 6. When $\tau_{L1} > \tau_{L1B}$ and $\tau_{L2} > \tau_{L2B}$, the circuit is operating in $L_{1,2}$ − CCM; otherwise, it operates in $L_{1,2}$ − DCM.

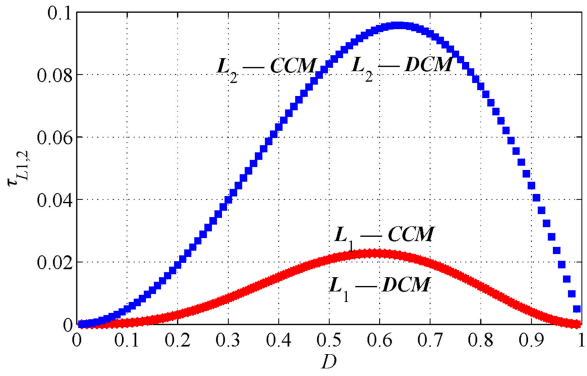

Fig. 6. Boundary conditions for the proposed converter in mode 1.

B. Mode 2 (Step-Up/Step-Down Mode)

1) Voltage Gain: By applying the same principle to inductors L_1 and L_2, the voltage across capacitor C_1 in steady state and the conversion ratio G are determined as

$$V_{C1} = \frac{1}{1-D} V_{\text{in}} \tag{30}$$

$$G = \frac{V_{C2}}{V_{\text{in}}} = \frac{2D - D^2}{(1-D)^2}. \tag{31}$$

2) Electric Stress Analysis: The voltage stresses on power switches (S_1 and S_2) and power diodes (D_1 and D_2) are

$$V_{S1} = \frac{1}{1-D} V_{\text{in}} \tag{32}$$

$$V_{S2} = \frac{1}{(1-D)^2} V_{\text{in}} \tag{33}$$

$$V_{D1} = \frac{1}{(1-D)} V_{\text{in}} \tag{34}$$

$$V_{D2} = \frac{1}{(1-D)^2} V_{\text{in}}. \tag{35}$$

The relationship between input current and output current is

$$I_{\text{in}} = \frac{2D - D^2}{(1-D)^2} I_o. \tag{36}$$

The steady-state dc values of I_{L1} and I_{L2} can be calculated by ampere–second balance principle

$$I_{L1} = \frac{1}{(1-D)^2} I_o \tag{37}$$

$$I_{L2} = \frac{1}{1-D} I_o. \tag{38}$$

The current stress of four semiconductor devices S_1, S_2, D_1, and D_2 is

$$I_{S1} = DI_{L1} = \frac{D}{(1-D)^2} I_o \tag{39}$$

$$I_{S2} = DI_{L2} = \frac{D}{1-D} I_o \tag{40}$$

$$I_{D1} = (1-D)I_{L1} = \frac{1}{(1-D)}I_o \tag{41}$$

$$I_{D2} = (1-D)I_{L2} = I_o. \tag{42}$$

3) Voltage Ripple of Capacitors and Current Ripple of Inductors: The capacitor voltage ripples Δv_{C1} and Δv_{C2} and inductor current ripples Δi_{L1} and Δi_{L2} can be calculated by using the same method

$$\Delta v_{C1} = \frac{I_{C1}}{C_1}DT = \frac{V_{\text{in}}D}{C_1Rf}\frac{2D-D^2}{(1-D)^3} \tag{43}$$

$$\Delta v_{C2} = \frac{I_{C2}}{C_2}DT = \frac{V_{\text{in}}D}{C_2Rf}\frac{2D-D^2}{(1-D)^2} \tag{44}$$

$$\Delta i_{L1} = \frac{V_{L1}}{L_1}DT = \frac{V_{\text{in}}}{L_1 f}D \tag{45}$$

$$\Delta i_{L2} = \frac{V_{L2}}{L_2}DT = \frac{V_{\text{in}}}{L_2 f}\frac{D}{1-D}. \tag{46}$$

4) Boundary Condition Between CCM and DCM: In mode 2, in the boundary condition mode, inductor currents I_{L1} and I_{L2} reach their zero point at the end of each switching cycle. The boundary conditions for L_1 and L_2 are

$$\tau_{L1B} = \frac{(1-D)^4}{2(2-D)} \tag{47}$$

$$\tau_{L2B} = \frac{(1-D)^2}{2(2-D)}. \tag{48}$$

As shown in Fig. 7, when $\tau_{L1} > \tau_{L1B}$ and $\tau_{L2} > \tau_{L2B}$, the circuit is operating in $L_{1,2}-$CCM; otherwise, it operates in $L_{1,2}-$DCM.

IV. Small-Signal Modeling

The state equations in modes 1 and 2 are derived according to Figs. 3 and 5, as shown in (49) and (50) shown at the bottom of this page, respectively, in which Mi and Si stand for mode i and state i, where i equals 1 or 2

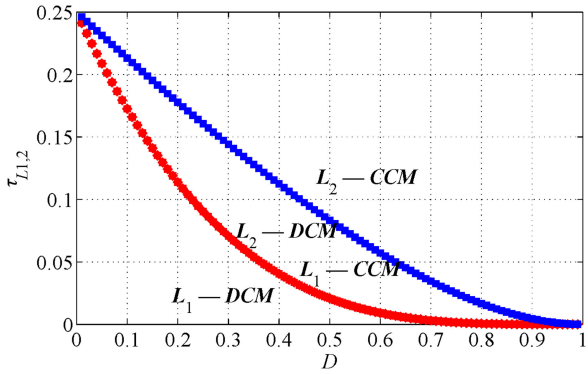

Fig. 7. Boundary conditions for the proposed converter in mode 2.

Using an averaging method to get the average model of the proposed converter in modes 1 and 2 result in

$$\text{Mode 1}\begin{cases} \frac{d\langle i_{L1}\rangle}{dt} = \frac{\langle v_{\text{in}}\rangle}{L_1} - \frac{\langle v_{C1}\rangle}{L_1}(1-d) \\ \frac{d\langle i_{L2}\rangle}{dt} = \frac{\langle v_{C1}\rangle}{L_2} - \frac{\langle v_{\text{in}}\rangle}{L_2}d - \frac{\langle v_{C2}\rangle}{L_2}d \\ \frac{d\langle v_{C1}\rangle}{dt} = -\frac{\langle i_{L2}\rangle}{C_1} + \frac{\langle i_{L1}\rangle}{C_1}(1-d) \\ \frac{d\langle v_{C2}\rangle}{dt} = \frac{\langle i_{L2}\rangle}{C_2}d - \frac{\langle v_{C2}\rangle}{RC_2} \end{cases} \tag{51}$$

$$\text{Mode 2}\begin{cases} \frac{d\langle i_{L1}\rangle}{dt} = \frac{\langle v_{\text{in}}\rangle}{L_1} - \frac{\langle v_{C1}\rangle}{L_1}(1-d) \\ \frac{d\langle i_{L2}\rangle}{dt} = \frac{\langle v_{C1}\rangle}{L_2} - \frac{\langle v_{\text{in}}\rangle}{L_2}(1-d) - \frac{\langle v_{C2}\rangle}{L_2}(1-d) \\ \frac{d\langle v_{C1}\rangle}{dt} = -\frac{\langle i_{L2}\rangle}{C_1} + \frac{\langle i_{L1}\rangle}{C_1}(1-d) \\ \frac{d\langle v_{C2}\rangle}{dt} = -\frac{\langle v_{C2}\rangle}{RC_2} + \frac{\langle i_{L2}\rangle}{C_2}(1-d) \end{cases} \tag{52}$$

in which $\langle i_{L1}\rangle, \langle i_{L2}\rangle, \langle v_{C1}\rangle, \langle v_{C2}\rangle,$ and $\langle v_{\text{in}}\rangle$ are the average values of $i_{L1}, i_{L2}, v_{C1}, v_{C2}$, and v_{in}, respectively.

We can define $\langle x\rangle$, $\hat{x}$, and X as the averaged value, the small ac value, and the dc value of x, respectively, for the circuit variables such as $i_{L1}, i_{L2}, v_{C1}, v_{C2}$, and d. The relationship among $x, \hat{x},$ and X is given in (53) and satisfies the small-signal assumption $\hat{x} \ll X$

$$x = X + \hat{x}. \tag{53}$$

Substituting (53) into (51) and (52), using the small-signal perturbation method, and ignoring high-order ac items, we can

$$M1-S1\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} \\ L_2\frac{di_{L2}}{dt} = v_{C1} - v_{\text{in}} - v_{C2} \\ C_1\frac{dv_{C1}}{dt} = -i_{L2} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} - \frac{v_{C2}}{R} \end{cases} \quad M1-S2\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} - v_{C1} \\ L_2\frac{di_{L2}}{dt} = v_{C1} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} - i_{L2} \\ C_2\frac{dv_{C2}}{dt} = -\frac{v_{C2}}{R} \end{cases} \tag{49}$$

$$M2-S1\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} \\ L_2\frac{di_{L2}}{dt} = v_{C1} \\ C_1\frac{dv_{C1}}{dt} = -i_{L2} \\ C_2\frac{dv_{C2}}{dt} = -\frac{v_{C2}}{R} \end{cases} \quad M2-S2\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} - v_{C1} \\ L_2\frac{di_{L2}}{dt} = v_{C1} - v_{\text{in}} - v_{C2} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} - i_{L2} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} - \frac{v_{C2}}{R} \end{cases} \tag{50}$$

derive the small-signal transfer functions of the proposed converter by using the Laplace transformation. Based on these transfer functions, the small-signal dynamic behaviors of the proposed converter can be analyzed (54) and (55) are shown at the bottom of the next page.

where $\mathbf{A}_1, \mathbf{B}_{11}, \mathbf{B}_{12}, \mathbf{A}_2, \mathbf{B}_{21}$, and $\mathbf{B}_{22}$ are expressed as follows:

$$\mathrm{A}_1 = \begin{bmatrix} 0 & 0 & -\frac{(1-D)}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{D}{L_2} \\ \frac{(1-D)}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{D}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \tag{56}$$

$$\mathrm{A}_2 = \begin{bmatrix} 0 & 0 & -\frac{(1-D)}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{(1-D)}{L_2} \\ \frac{(1-D)}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{(1-D)}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \tag{57}$$

$$\mathrm{B}_{11} = \begin{bmatrix} \frac{V_{C1}}{L_1} \\ -\frac{V_{C2}}{L_2} \\ -\frac{I_{L1}}{C_1} \\ \frac{I_{L2}}{C_2} \end{bmatrix} \mathrm{B}_{12} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{58}$$

$$\mathrm{B}_{21} = \begin{bmatrix} \frac{V_{C1}}{L_1} \\ \frac{V_{C2}}{L_2} \\ -\frac{I_{L1}}{C_1} \\ -\frac{I_{L2}}{C_2} \end{bmatrix} \mathrm{B}_{22} = \begin{bmatrix} \frac{1}{L_1} \\ -\frac{1}{L_2} \\ 0 \\ 0 \end{bmatrix}. \tag{59}$$

V. Design Procedure and Simulations

This proposed converter is designed to operate in the dual working modes. The given specifications are listed in Table I.

From the input voltage and output voltage, the duty cycle in modes 1 and 2 can be calculated as follows:

$$D_1 = \frac{(G+1) \pm \sqrt{(G+1)(G-3)}}{2(G+1)} \tag{60}$$

$$D_2 = 1 - \frac{1}{\sqrt{(G+1)}}. \tag{61}$$

In mode 1, the duty cycle should be chosen as 0.5. In mode 2, the duty cycle should be chosen as 0.1835 in the step-down state and 0.3675 in the step-up state.

TABLE I
Specifications for the Proposed Converter

Given items		Mode 1	Mode 2	
		Step-up state	Step-down state	Step-up state
Input voltage v_{in}		24 V	24 V	24 V
Output voltage v_o		-72 V	-12.0 V	-36.0 V
Output load R		120 Ω	15 Ω	45 Ω
Output power P_o		43.2 W	9.6 W	28.8 W
Switching frequency		50 kHz	50 kHz	50 kHz
Current ripple ratio of	L_1	<40%	<40%	<40%
	L_2	<40%	<40%	<40%
Voltage ripple ratio of	C_1	<10%	<10%	<10%
	C_2	<1%	<1%	<1%

TABLE II
Selected Components for the Proposed Converter

Components	Values or types
Inductor L_1	935 μH with R_{L1}=0.128 Ω
Inductor L_2	1035 μH with R_{L2}=0.131 Ω
Capacitor C_1	4.7 μF with R_{C1}=11.4 mΩ
Capacitor C_2	40 μF with R_{C2}=5.6 mΩ
Power switches S_1 and S_2	IRFP 4668
Diodes D_1 and D_2	MBR 40250

According to the capacitor voltage, inductor current, and ripple calculation shown in (9), (10), (16), (17), and (22)–(25) in mode 1 and in (30), (31), (37), (38), and (43)–(46) in mode 2, the inductors and capacitors should satisfy the following equations:

$$\begin{cases} L_1 > \frac{R}{40\%f} \frac{(1-D_1)^2 {D_1}^3}{1-D_1+{D_1}^2} \\ L_1 > \frac{R}{40\%f} \frac{(1-D_2)^4}{2-D_2} \end{cases} \tag{62}$$

$$\begin{cases} L_2 > \frac{R}{40\%f} \frac{(1-D_1){D_1}^2}{1-D_1+{D_1}^2} \\ L_2 > \frac{R}{40\%f} \frac{(1-D_2)^2}{2-D_2} \end{cases} \tag{63}$$

$$\begin{cases} C_1 > \frac{1}{10\%Rf} \frac{1-D_1+{D_1}^2}{D_1} \\ C_1 > \frac{1}{10\%Rf} \frac{(2-D_2){D_2}^2}{(1-D_2)^2} \end{cases} \tag{64}$$

$$\begin{cases} C_2 > \frac{1}{1\%Rf}(1-D_1) \\ C_2 > \frac{1}{1\%Rf} D_2. \end{cases} \tag{65}$$

Based on the electric stress calculations in modes 1 and 2, the power MOSFET and the power diode are selected for the proposed converter. Table II lists the design parameters.

Fig. 8 shows the PSpice simulations of the proposed converter in modes 1 and 2.

Fig. 9 shows Bode plot comparisons of the proposed converter in two modes between PSIM simulations and numerical calculations.

$$\text{Mode1} \begin{cases} G_{vd1}(s) = \left.\frac{\hat{v}_{C2}(s)}{\hat{d}(s)}\right|_{\hat{v}_{\text{in}}(s)=0} = [0,0,0,1](s\mathrm{I} - \mathrm{A}_1)^{-1}\mathrm{B}_{11} \\ G_{vv1}(s) = \left.\frac{\hat{v}_{C2}(s)}{\hat{v}_{\text{in}}(s)}\right|_{\hat{d}(s)=0} = [0,0,0,1](s\mathrm{I} - \mathrm{A}_1)^{-1}\mathrm{B}_{12} \end{cases} \tag{54}$$

$$\text{Mode2} \begin{cases} G_{vd2}(s) = \left.\frac{\hat{v}_{C2}(s)}{\hat{d}(s)}\right|_{\hat{v}_{\text{in}}(s)=0} = [0,0,0,1](s\mathrm{I} - \mathrm{A}_2)^{-1}\mathrm{B}_{21} \\ G_{vv2}(s) = \left.\frac{\hat{v}_{C2}(s)}{\hat{v}_{\text{in}}(s)}\right|_{\hat{d}(s)=0} = [0,0,0,1](s\mathrm{I} - \mathrm{A}_2)^{-1}\mathrm{B}_{22} \end{cases} \tag{55}$$

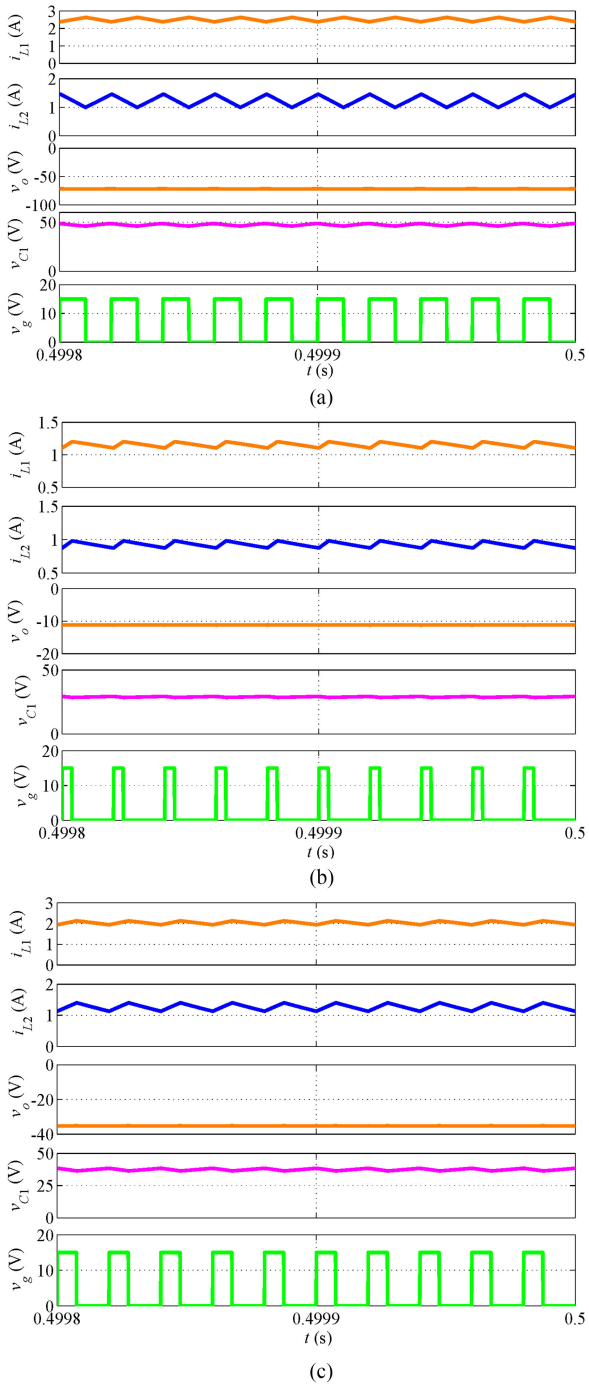

Fig. 8. PSpice simulations of the proposed converter (from top to bottom, i_{L1}, i_{L2}, v_o, v_{C1}, and v_g). (a) Step-up state in mode 1. (b) Step-down state in mode 2. (c) Step-up state in mode 2.

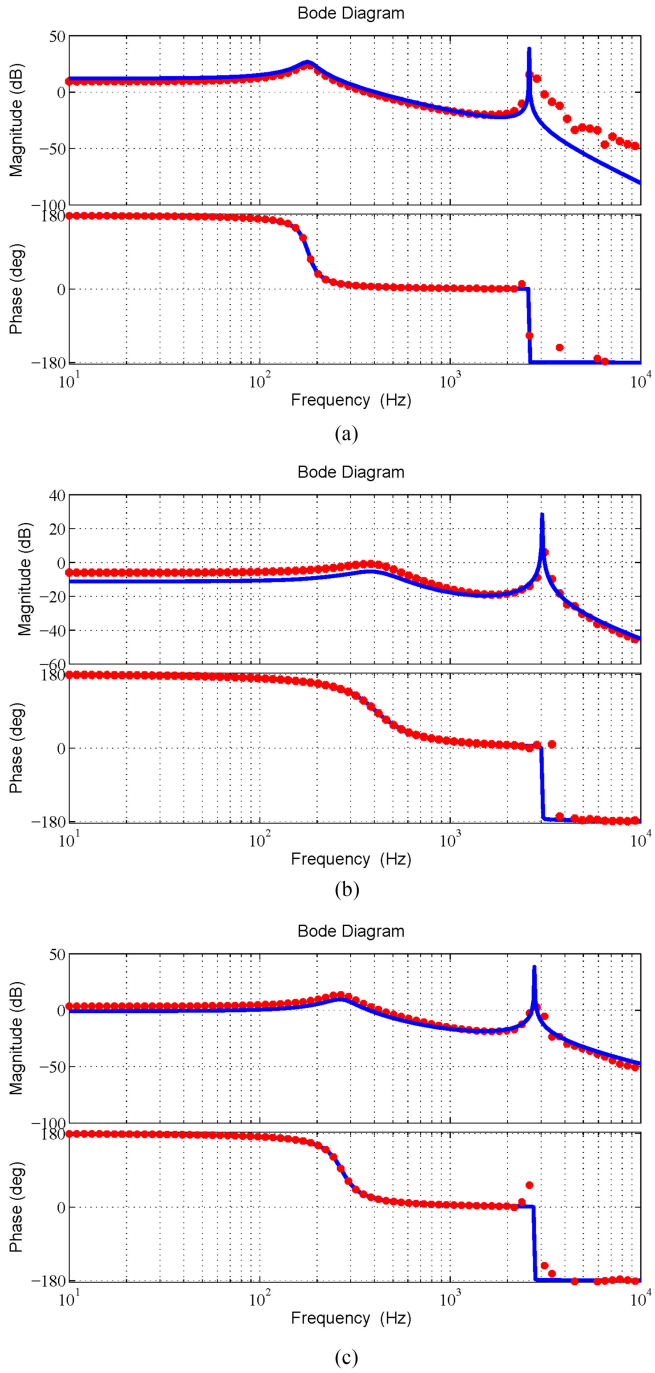

Fig. 9. Bode plot comparisons of the proposed converter (blue solid line: theoretical calculations from derived model; red dashed line: PSIM simulations). (a) Step-up state in mode 1. (b) Step-down state in mode 2. (c) Step-up state in mode 2.

VI. Comparisons With Other Converters

A. Mode1 (Step-Up Mode)

Table III gives comparisons among the traditional boost converter, the N-O self-lift Luo converter [18], the N-O KY boost converter [19], and the proposed N-O converter in mode 1 (step-up mode).

Fig. 10 shows the voltage gains of the traditional boost converter, the N-O self-lift Luo converter, the N-O KY boost converter, and the proposed N-O converter in mode 1 (step-up mode). One can see that the gain of the proposed N-O converter in mode 1 is the largest, and the gain is symmetrical with $D = 0.5$. The lowest voltage gain is 3 when $D = 0.5$.

TABLE III
COMPARISONS AMONG DIFFERENT CONVERTERS (MODE 1: STEP UP)

Topology		Traditional boost converter	N-O self-lift Luo converter	N-O KY boost converter	N-O proposed converter in mode 1
Number of	Switches	1	1	1	2
	Diodes	1	2	2	2
	Inductors	1	2	1	2
	Capacitors	1	3	2	2
Number of elements		4	8	6	8
Voltage gain ($\lvert V_o/V_{in}\rvert$)		$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1-D+D^2}{D(1-D)}$
Duty cycle ($D=f(G)$)		$1-\frac{1}{G}$	$1-\frac{1}{G}$	$1-\frac{1}{G}$	$\frac{(G+1)\pm\sqrt{(G+1)(G-3)}}{2(G+1)}$
Voltage stress of switches (V_S/V_{in})	S_1	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
	S_2	/	/	/	$\frac{1}{D(1-D)}$
Voltage stress of diodes (V_D/V_{in})	D_1	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
	D_2	/	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{D(1-D)}$
Voltage stress of capacitors (V_C/V_{in})	C_1	$\frac{1}{1-D}$	1	$\frac{1}{1-D}$	$\frac{1}{1-D}$
	C_2	/	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1-D+D^2}{D(1-D)}$
	C_3	/	$\frac{1}{1-D}$	/	/
Current stress of switches (I_S/I_o)	S_1	$\frac{D}{1-D}$	Current spike	Current spike	$\frac{1}{1-D}$
	S_2	/	/	/	$\frac{1-D}{D}$
Current stress of diodes (I_D/I_o)	D_1	1	Current spike	1	$\frac{1}{D}$
	D_2	/	1	Current spike	1
Current stress of inductors (I_L/I_o)	L_1	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{D(1-D)}$
	L_2	/	1	/	$\frac{1}{D}$
Order number of small signal models		2	5	3	4

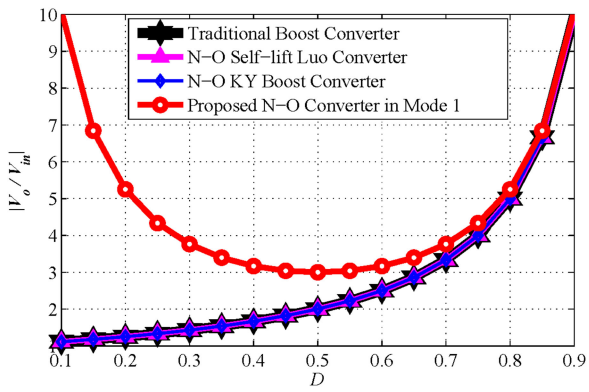

Fig. 10. Voltage gains of different boost converters.

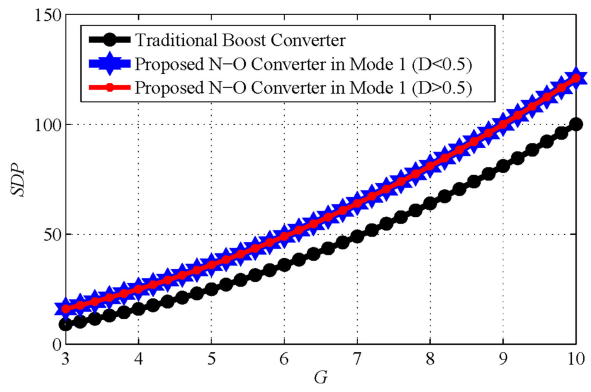

Fig. 11. SDP comparisons of different boost converters.

The switching device power (SDP) rating as the product of the voltage stress V_{si} and the average current stress I_{si} is introduced as a cost indicator for the power device. The total SDP, expressed as $\mathrm{SDP}_{\mathrm{sum}} = \sum_{i=1}^{N} V_{Si} \cdot I_{Si}$, where N is the number of power device used, can be a rough cost estimation of the converter system, and, furthermore, it is also an indicator of the thermal requirements and conversion efficiency [21], [22].

Fig. 11 shows the SDP comparisons of the traditional boost converter and the proposed N-O converter in mode 1. One can see that for the proposed N-O converter in mode 1, the SDP is a little larger than that of the traditional boost converter, and,

TABLE IV
COMPARISONS AMONG DIFFERENT CONVERTERS (MODE 2: STEP UP/STEP DOWN)

Topology		N-O single switch quadratic buck-boost converter [20]	Transformerless quadratic buck–boost converter [10]	N-O hybrid buck-boost converter [6]	Proposed N-O converter in mode 2
Number of	Switches	1	2	1	2
	Diodes	3	2	4	2
	Inductors	2	2	2	2
	Capacitors	2	2	1	2
Number of elements		8	8	8	8
Voltage gain (G=$\lvert V_o/V_{in}\rvert$)		$\frac{D(2-D)}{(1-D)^2}$	$\frac{D^2}{(1-D)^2}$	$\frac{2D}{1-D}$	$\frac{D(2-D)}{(1-D)^2}$
Duty cycle(f(G))		$1-\frac{1}{\sqrt{G+1}}$	$\frac{\sqrt{G}}{1+\sqrt{G}}$	$\frac{G}{2+G}$	$1-\frac{1}{\sqrt{G+1}}$
Voltage stress of switches (V_S/V_{in})	S_1	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$
	S_2	/	$\frac{D}{(1-D)^2}$	/	$\frac{1}{(1-D)^2}$
Voltage stress of diodes (V_D/V_{in})	D_1	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{D}{1-D}$	$\frac{1}{1-D}$
	D_2	$\frac{D}{(1-D)^2}$	$\frac{D}{(1-D)^2}$	$\frac{D}{1-D}$	$\frac{1}{(1-D)^2}$
	D_3	$\frac{1}{(1-D)^2}$	/	1	/
	D_4	/	/	$\frac{1+D}{1-D}$	/
Voltage stress of capacitors (V_C/V_{in})	C_1	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{2D}{1-D}$	$\frac{1}{1-D}$
	C_2	$\frac{D(2-D)}{(1-D)^2}$	$\frac{D^2}{(1-D)^2}$	/	$\frac{D(2-D)}{(1-D)^2}$
Current stress of switches (I_S/I_o)	S_1	$\frac{D(2-D)}{(1-D)^2}$	$\frac{D^2}{(1-D)^2}$	$\frac{2D}{1-D}$	$\frac{D}{(1-D)^2}$
	S_2	/	$\frac{D}{1-D}$	/	$\frac{D}{1-D}$
Current stress of diodes (I_D/I_o)	D_1	$\frac{1}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{1}{1-D}$
	D_2	$\frac{D}{(1-D)^2}$	1	$\frac{D}{1-D}$	1
	D_3	1	/	1	/
	D_4	/	/	1	/
Current stress of inductors (I_L/I_o)	L_1	$\frac{1}{1-D}$	$\frac{2D-1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{(1-D)^2}$
	L_2	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Order number of small-signal model		4	4	3	4

with the same voltage gain, the SDPs are the same under the two corresponding duty cycles.

For the N-O self-lift Luo converter and the N-O KY boost converter, abrupt voltage changes occur for the capacitors, and a very large current spike will flow through the power switch and power diode. Consequently, the SDP cannot be calculated precisely.

B. Mode 2 (Step-Up/Step-Down Mode)

Table IV gives comparisons among the N-O single switch quadratic buck–boost converter in [20], the transformerless quadratic buck–boost converter in [10], the N-O hybrid buck–boost converter in [6], and the proposed N-O converter in mode 2 (step-up/step-down mode).

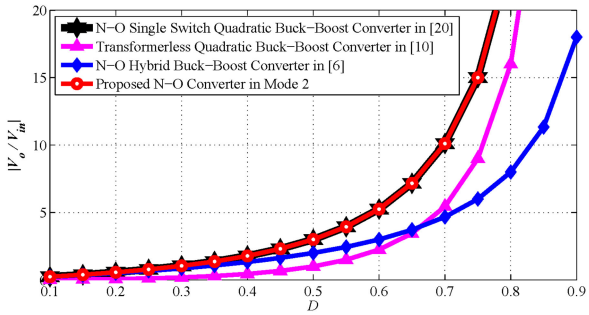

Fig. 12. Voltage gains of different buck–boost converters.

Fig. 12 shows the voltage gains of the N-O single switch quadratic buck–boost converter, the transformerless quadratic

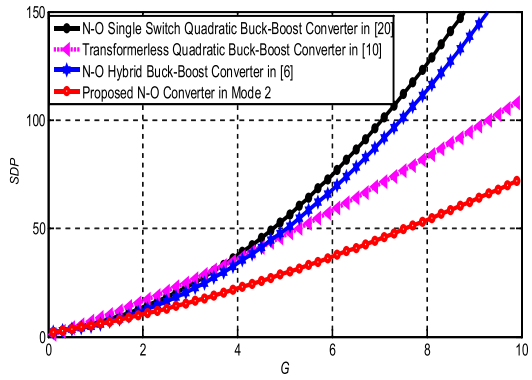

Fig. 13. SDP comparisons of different buck–boost converters.

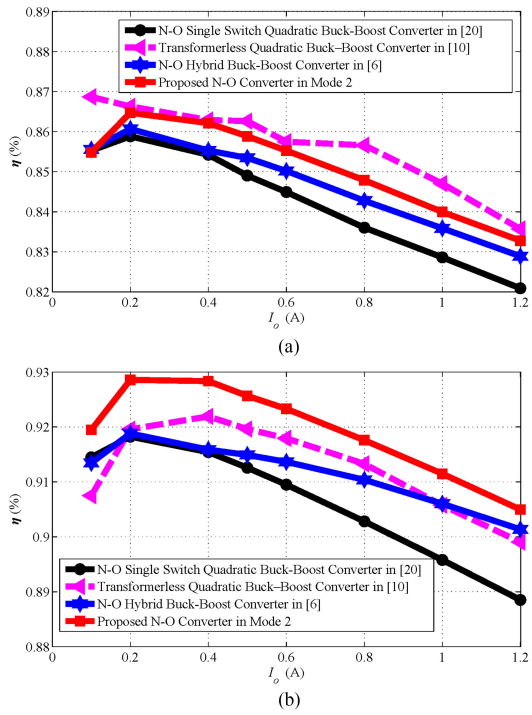

Fig. 14. Efficiency comparisons of different buck–boost converters. (a) Efficiency in step-down state. (b) Efficiency in step-up state.

buck–boost converter, the N-O hybrid buck–boost converter, and the proposed N-O converter in mode 2 (step-up/step-down mode). One can see that the gain of the proposed N-O converter in mode 2 is larger than that of the transformerless quadratic buck–boost converter and the N-O hybrid buck–boost converter and is equal to the gain of the N-O single switch quadratic buck–boost converter.

Fig. 13 shows the SDP comparisons of the N-O single switch quadratic buck–boost converter, the transformerless quadratic buck–boost converter, the N-O hybrid buck–boost converter, and the proposed N-O converter in mode 2. One can see that for the proposed N-O converter in mode 2', the SDP is the smallest one among these four converters under the same voltage gain.

Fig. 14 shows the efficiency comparisons of different buck–boost converters in PSpice simulation based on the same circuit condition, same ripple, and same semiconductor device

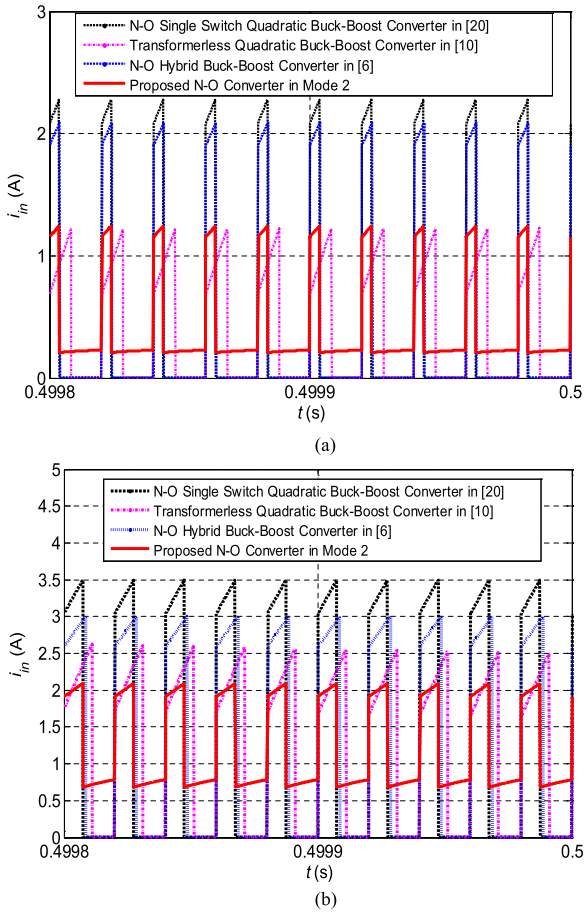

Fig. 15. Input current comparisons of different buck–boost converters. (a) Input current in step-down state. (b) Input current in step-up state.

selection. It is found that in step-down state, the efficiency of the proposed N-O converter in mode 2's is a little lower than that of the transformerless quadratic buck–boost converter, and it is higher than the other two converters'. In step-up state, the efficiency of the proposed N-O converter in mode 2's is always higher than that of the N-O single-switch quadratic buck–boost converter, the transformerless quadratic buck–boost converter, and the N-O hybrid buck–boost converter.

Fig. 15 shows the input current comparisons of different buck–boost converters. It is found that the peak-to-peak value of input current of the proposed N-O converter in mode 2 is lowest.

Fig. 16 gives the FFT analysis of input current among different buck–boost converters. One can see that except the second-order and third-order switching frequency components in step-down state, the switching frequency components of input current of the proposed N-O converter in mode 2 are lowest.

VII. Efficiency Analysis and Nonideal Conversion Ratio Analysis

In general, the power losses of dc–dc converter mainly contain four parts: power switch loss, diode loss, inductor loss, and capacitor loss [23].

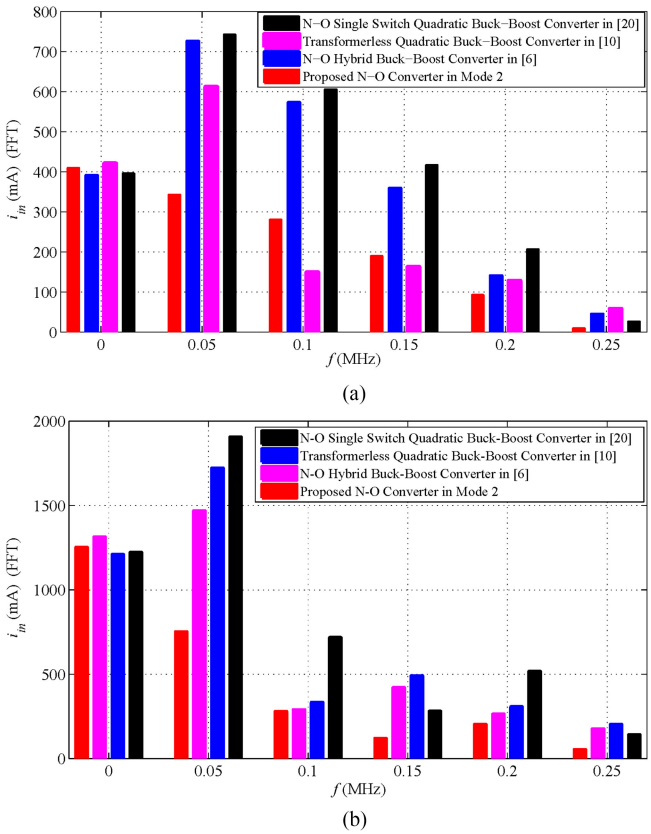

Fig. 16. FFT analysis of input current among different buck–boost converters. (a) Step-down state. (b) Step-up state.

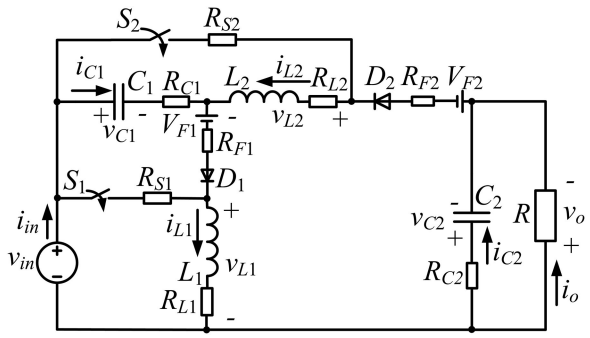

Fig. 17. Equivalent circuit of the proposed converter considering the parasitic elements.

We suppose that R_{S1} and R_{S2} are the power switches S_1 and S_2 (MOSFET) on resistances, V_{F1} and V_{F2} are the power diodes' (D_1 and D_2) threshold voltages, R_{L1}, R_{L2}, R_{C1}, and R_{C2} are the equivalent series resistances (ESRs) of L_1, L_2, C_1, and C_2, respectively, and the voltage and current ripples across the capacitors and the inductors are neglected.

A. Power Loss Analysis of Power Switch

The power losses of power switch (MOSFET) mainly contain switching loss, conduction loss, and driving loss, which are

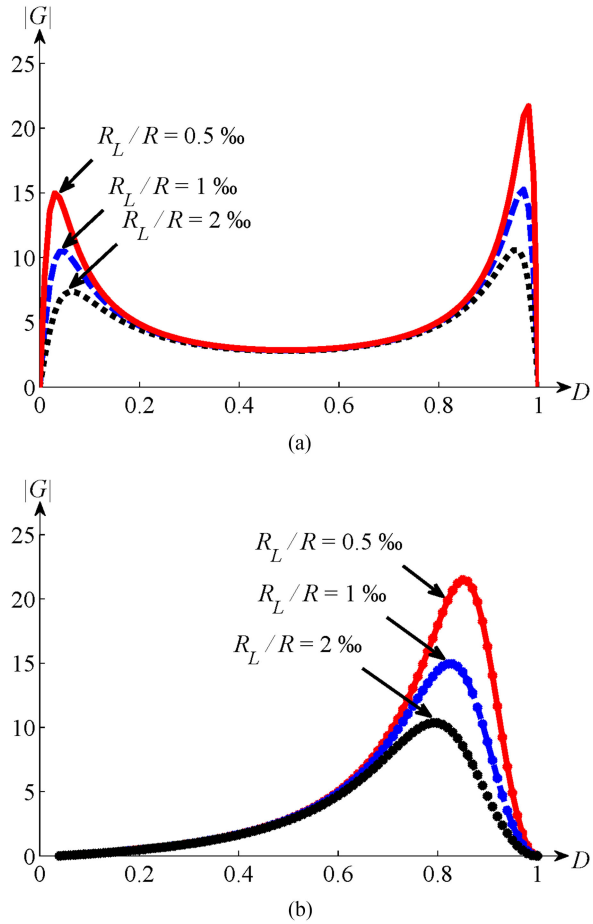

Fig. 18. Absolute value of voltage gain G considering the parasitic elements. (a) Mode 1. (b) Mode 2.

calculated as follows according to [23]:

$$\begin{aligned} P_{S(\text{switching})} &= \sum_{i=1}^{2}(P_{Si\_\text{cross\_turnon}} \\ &\quad + P_{Si\_\text{cross\_turnoff}} + P_{Si\_C_{\text{oss}}}) \\ &= \sum_{i=1}^{2}\left(\frac{1}{2}I_{Si}V_{Si}t_{Si\_\text{cross\_on}}f \right. \\ &\quad \left. + \frac{1}{2}I_{Si}V_{Si}t_{Si\_\text{cross\_off}}f + \frac{1}{2}C_{Si\_\text{oss}}V_{Si}^2 f\right) \end{aligned} \tag{66}$$

$$P_{S(\text{conduction})} = \sum_{i=1}^{2} I_{Si(\text{rms})}^2 R_{Si} \tag{67}$$

$$P_{S(\text{drive})} = \sum_{i=1}^{2} V_{Si\_\text{drive}} Q_{Si\_g} f. \tag{68}$$

Obviously, the switching loss of power switch is related to the turn-ON cross time, turn-OFF cross time, the voltage stress on the power switch, the averaged current through it, switching frequency, and the output capacitor of the switch. The conduction

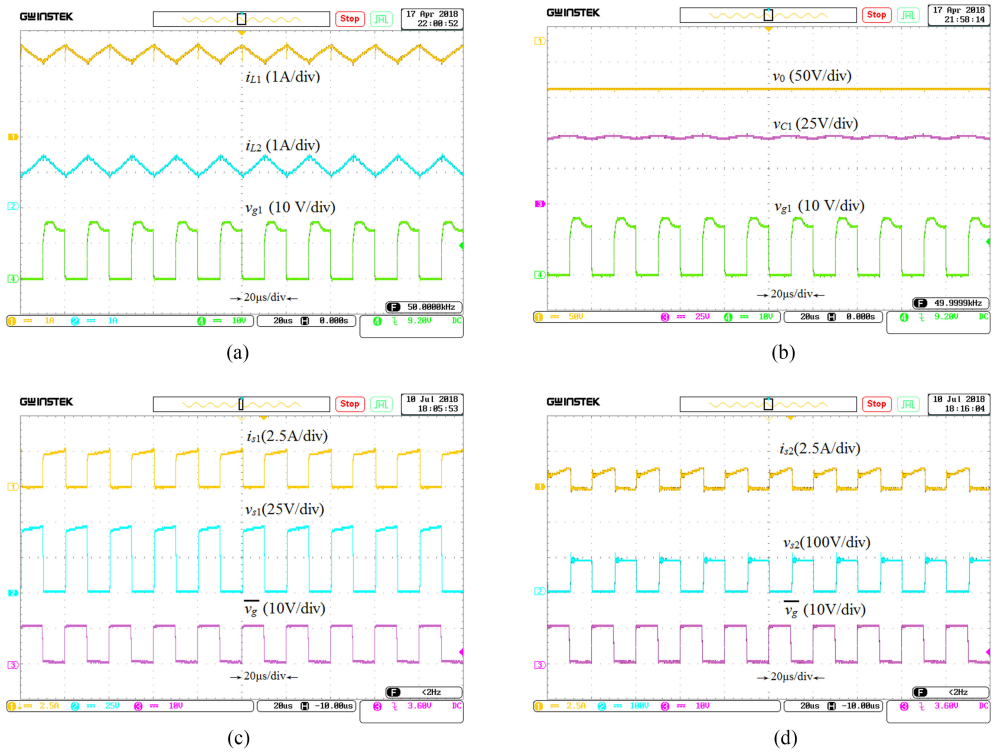

Fig. 19. Experimental waveforms of the proposed converter in step-up state in mode 1 (time: 20 μs/div). (a) i_{L1} (1 A/div), i_{L2} (1 A/div), and v_{g1} (10 V/div). (b) v_o (50 V/div), v_{C1} (25 V/div), and v_{g1} (10 V/div).(c) i_{s1} (2.5 A/div), v_{s1} (25 V/div), and $\overline{v_g}$ (10 V/div). (d) i_{s2} (2.5 A/div), v_{s2} (100 V/div), and $\overline{v_g}$ (10 V/div).

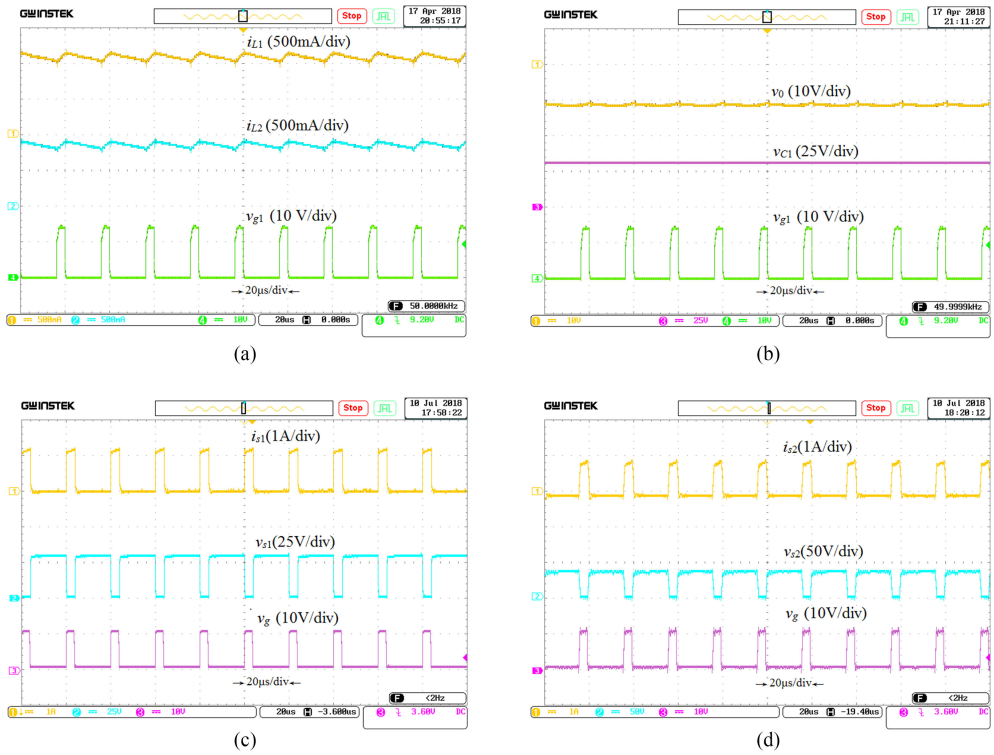

Fig. 20. Experimental waveforms of the proposed converter in step-down state in mode 2 (time: 20 μs/div). (a) i_{L1} (500 mA/div), i_{L2} (500 mA/div), and v_{g1} (10 V/div). (b) v_o (10 V/div), v_{C1} (25 V/div), and v_{g1} (10 V/div). (c) i_{s1} (1 A/div), v_{s1} (25V/div), and v_g (10 V/div). (d) i_{s2} (1 A/div), v_{s2} (50 V/div), and v_g (10 V/div).

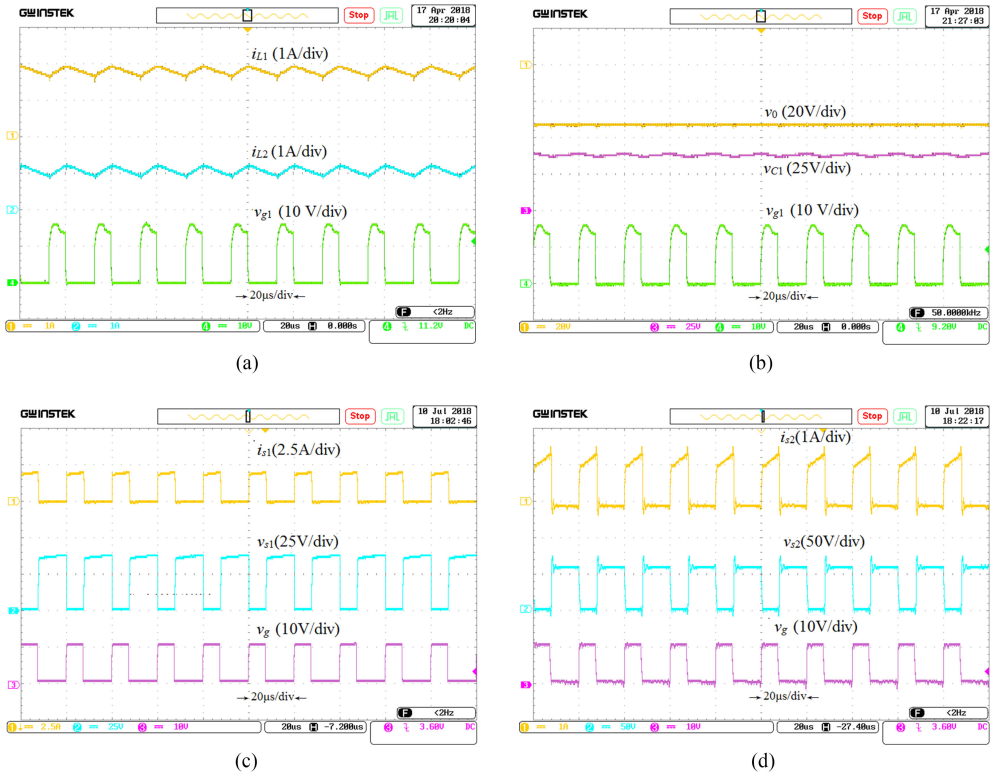

Fig. 21. Experimental waveforms of the proposed converter in step-up state in mode 2 (time: 20 μs/div). (a) i_{L1} (1 A/div), i_{L2} (1 A/div), and v_{g1} (10 V/div). (b) v_o (20 V/div), v_{C1} (25 V/div), and v_{g1} (10 V/div). (c) i_{s1} (2.5 A/div), v_{s1} (25 V/div), and v_g (10 V/div). (d) i_{s2} (1 A/div), v_{s2} (50 V/div), and v_g (10 V/div).

loss of power switch is related to the averaged current through it and the on resistance. The driving loss of power switch is related to drive voltage, gate charge, and the switching frequency.

The total power losses of power switch are the summation of the above three parts

$$P_S = P_{S(\text{switching})} + P_{S(\text{conduction})} + P_{S(\text{drive})}. \tag{69}$$

B. Power Loss Analysis of Diode

The power loss of diode is mainly related to the forward voltage drop and the current through it, and the calculation is

$$P_D = \sum_{i=1}^{2} V_{Fi} I_{Di}. \tag{70}$$

C. Power Loss Analysis of Inductor

The power loss of inductor is mainly the copper loss caused by winding ESR and the core loss caused by eddy current and hysteresis of the magnetic core. The copper losses of inductors are shown as follows

$$P_{L\_\text{copper}} = \sum_{i=1}^{2} I_{Li(\text{rms})}^2 R_{Li}. \tag{71}$$

The core loss calculation is based on the Steinmetz formula in engineering application shown as

$$P_{L\_\text{Core}} = \sum_{i=1}^{2} l_{ei} A_{ei} (C_{mi} f^{\alpha i} B_i^{\beta i}) \tag{72}$$

where C_m, α, and β are experiential parameters derived from fitting curve of the magnetic core date sheet, B is defined as half of the ac-flux swing, l_e is the length of the magnetic path, and A_e is the cross section of the core.

Hence, the total power losses of inductors are as follows

$$P_L = P_{L\_\text{copper}} + P_{L\_\text{Core}}. \tag{73}$$

D. Power Loss Analysis of Capacitor

The capacitors losses are

$$P_C = \sum_{i=1}^{2} I_{Ci(\text{rms})}^2 R_{Ci}. \tag{74}$$

E. Efficiency Calculation

Accordingly, the efficiency can be calculated and its result is

$$\eta = \frac{P_o}{P_o + P_L + P_S + P_D + P_C}. \tag{75}$$

F. Nonideal Conversion Ratio Analysis

Considering the parasitic elements, the equivalent circuit of the proposed converter is shown in Fig. 17.

In two modes, when the power switch S_1 is turned ON, the voltages across the inductors are eq. (76) is shown at the bottom of the next page.

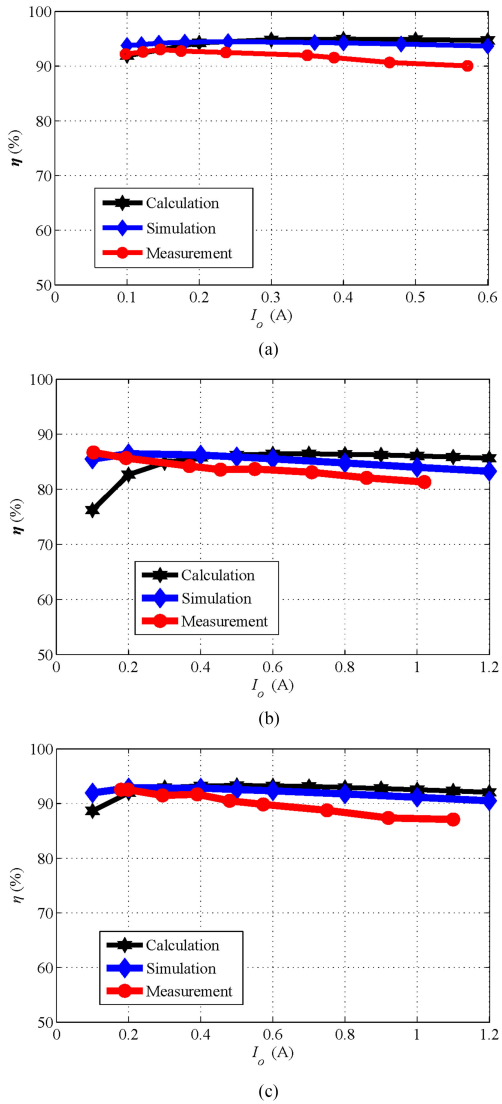

Fig. 22. Efficiency of calculation, PSpice simulation, and experimental measurement of the proposed converter versus output current. (a) Step-up state in mode 1. (b) Step-down state in mode 2. (c) Step-up state in mode 2.

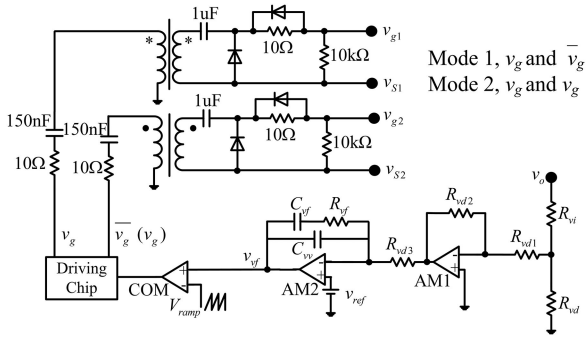

Fig. 23. Control block diagram of the proposed converter with dual working modes.

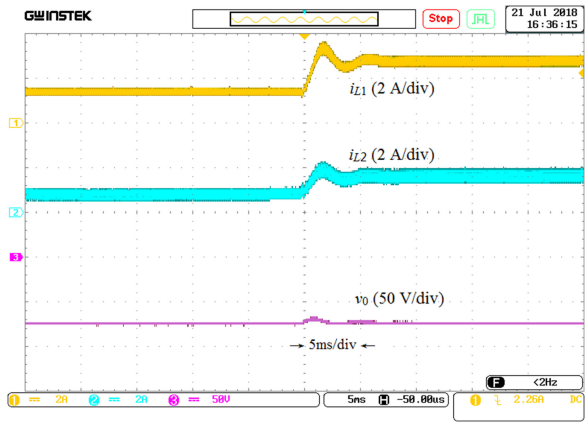

Fig. 24. Dynamic response with load current changing from 50% to 100% of the proposed converter in mode 1 (time: 5 ms/div), i_{L1} (2 A/div), i_{L2} (2 A/div), and v_o (50 V/div).

When the power switch S_1 is turned OFF, the voltages across the inductors are (77) is shown at the bottom of the next page.

According to the volt–second balance principle of inductors, the average output voltage in mode 1 considering the parasitic elements can be obtained as follows: (78) is shown at the bottom of the next page.

Similarly, the voltage gain G in mode 2 considering the parasitic resistances and forward voltage drops of diodes is shown in the following equation: (79) is shown at the bottom of the next page.

The absolute values of the voltage gain G in two modes considering the parasitic resistances and forward voltage drops of diodes are depicted in Fig. 18. From Fig. 18, it can be seen that the voltage conversion ratio is influenced by parasitic elements.

VIII. Experimental Details

The system parameters in the experiment were the same as those in the simulation. v_g and $\bar{v}_g$ are outputs of driving chip, and v_{g1} is the output of excitation tranformer, we can see that there is a little difference between v_g and v_{g1}, which is good to drive the switch.

Fig. 19 shows the experimental waveforms for the inductor currents i_{L1} and i_{L2}, output voltage v_o, capacitor voltage

$$M1-S1\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} - i_{L1}(R_{S1}+R_{L1}) \\ L_2\frac{di_{L2}}{dt} = v_{C1} - i_{L2}(R_{C1}+R_{L2}+R_{F2}) - V_{F2} - v_{\text{in}} - v_o \\ C_1\frac{dv_{C1}}{dt} = -i_{L2} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} - \frac{v_o}{R} \end{cases} \quad M2-S1\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} - i_{L1}(R_{S1}+R_{L1}) \\ L_2\frac{di_{L2}}{dt} = v_{C1} - i_{L2}(R_{C1}+R_{L2}+R_{S2}) \\ C_1\frac{dv_{C1}}{dt} = -i_{L2} \\ C_2\frac{dv_{C2}}{dt} = -\frac{v_o}{R} \end{cases} \tag{76}$$

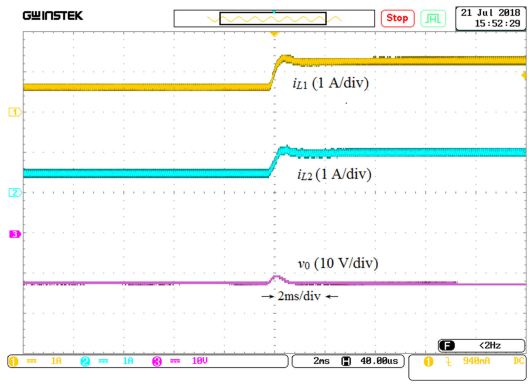

Fig. 25. Dynamic response with load current from 50% to 100% of the proposed converter in mode 2 (time: 2 ms/div). (a) Step-down state, i_{L1} (1 A/div), i_{L2} (1 A/div), and v_o (10 V/div). (b) Step-up state, i_{L1} (2 A/div), i_{L2} (2 A/div), and v_o (20 V/div).

v_{C1}, driving signal, and voltages and currents of the two power switches for the proposed converter in step-up state in mode 1, while Figs. 20 and 21 show them in step-down state and in step-up state in mode 2, respectively.

It can be observed that the circuit experiments are in good agreement with the PSpice simulations. Figs. 19–21 of comparisons between waveforms of i_{L1}, i_{L2}, v_o, and v_{C1} in simulation and experiment demonstrate that the proposed converter is usable from an engineering standpoint.

From Fig. 22, it is obvious that the efficiencies of the proposed converter in step-up state in modes 1 and 2 are higher than that of the converter in step-down state in mode 2. The highest efficiency can be reached 93.0% in experimental measurement.

When considering the transient response, the whole circuit should be in closed-loop control. The control block diagram is shown in Fig. 23.

The dynamic response of the proposed converter with voltage mode control under the output load current changing from 50% to 100% of the rated value in two modes is presented in Figs. 24 and 25. From these figures, it is clear that the proposed converter has a good dynamic response.

IX. Conclusion

An N-O high quadratic conversion ratio dc–dc converter with dual working modes is proposed in this paper.

Through analysis, comparisons, simulation, and experimental results, the following is proved.

1) The proposed converter is flexible and capable of working in step-up mode or step-up/step-down mode depending on the external requirements.
2) The proposed converter has a higher N-O voltage gain in mode 1 compared with the boost converter and the other two N-O boost converters.
3) The voltage gain of the proposed converter in mode 2 is greater than or equal to the other three buck–boost converters. Moreover, under the same voltage gain, the proposed converter in mode 2 has the lowest SDP.
4) The efficiency of the proposed converter in step-up state in mode 2 is highest among those comparative converters'

$$
\begin{aligned}
M1-S2 &\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} - v_{C1} - i_{L1}(R_{F1}+R_{L1}) - (i_{L1}-i_{L2})R_{C1} - V_{F1} \\ L_2\frac{di_{L2}}{dt} = v_{C1} - i_{L2}(R_{L2}+R_{S2}) + (i_{L1}-i_{L2})R_{C1} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} - i_{L2} \\ C_2\frac{dv_{C2}}{dt} = -\frac{v_o}{R} \end{cases} \\
M2-S2 &\begin{cases} L_1\frac{di_{L1}}{dt} = v_{\text{in}} - v_{C1} - i_{L1}(R_{F1}+R_{L1}) - (i_{L1}-i_{L2})R_{C1} - V_{F1} \\ L_2\frac{di_{L2}}{dt} = v_{C1} - i_{L2}(R_{L2}+R_{F2}) - V_{F2} - v_{\text{in}} - v_o + (i_{L1}-i_{L2})R_{C1} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} - i_{L2} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} - \frac{v_o}{R} \end{cases}
\end{aligned} \tag{77}
$$

$$
V_o = \frac{(1-D)D[V_{\text{in}} - (1-D)V_{F1}] - (1-D)^2D^2(V_{\text{in}} + V_{F2})}{(1-D)^2D^2 + \frac{R_{L1}}{R} + (1-D)^2\frac{R_{L2}}{R} + D\frac{R_{S1}}{R} + (1-D)^3\frac{R_{S2}}{R} + (1-D)\frac{R_{F1}}{R} + (1-D)^2D\frac{R_{F2}}{R} + D(1-D)\frac{R_{C1}}{R}} \tag{78}
$$

$$
V_o = \frac{(1-D)^2V_{\text{in}} - (1-D)^4V_{\text{in}} - (1-D)^3V_{F1} - (1-D)^4V_{F2}}{(1-D)^4 + \frac{R_{L1}}{R} + (1-D)^2\frac{R_{L2}}{R} + D\frac{R_{S1}}{R} + (1-D)^2D\frac{R_{S2}}{R} + (1-D)\frac{R_{F1}}{R} + (1-D)^3\frac{R_{F2}}{R} + (1-D)D\frac{R_{C1}}{R}} \tag{79}
$$

in PSpice simulation, and the highest efficiency can be reached 93.0% in experimental measurement.

5) The peak-to-peak value of input current of the proposed converter in mode 2 is lowest, and the switching frequency components of input current of the proposed converter in mode 2 are lowest among those comparative converters' in PSpice FFT analysis, which means a small volume input filter is needed.
6) The proposed converter has good dynamic response with load current changing from 50% to 100% of rated value based on the same set of hardware settings in two modes.
7) The simulation results based on PSpice and the circuit experiments verify that the proposed converter is usable in engineering applications.

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