Virtual Positive-Damping Reshaped Impedance Stability Control Method for the Offshore MVDC System

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***Abstract*—For the offshore medium-voltage direct-current (MVdc) system, the dc-side medium voltage can easily cause high-frequency oscillation and even instability owing to the complex impedance interactions. The virtual-resistance stability control method aiming at rectifier station is first introduced from low-voltage dc micro-grid application for mitigating its dc-side oscillation without affecting the load performance of the inverter station. Viewed from the dc input terminal, the small-signal dc impedance modeling of the overall system is established by considering the influences of dc cable, ac grid inductance, and input-parallel output-series structure of rectifier station. Then, the oscillation mechanism is analyzed by the impedance-based Nyquist stability criterion. It is found that only the virtual resistance deteriorates the stability of the MVdc system under the low switching-frequency condition, because the high-frequency oscillation peak may easily exceed the narrow control bandwidth of the rectifier station and fall into the negative-damping region, resulting in a poor robustness against the dc cable variation. To address this issue, the virtual positive-damping reshaped impedance stability control method is further proposed to maintain a larger positive damper in the actual oscillation frequency range regardless of the variation of dc cable length. Thus, the dc-side oscillation of the offshore MVdc system is effectively mitigated at the low switching frequency. Finally, simulation and experimental results validate the proposed control method.**

***Index Terms*—Nyquist stability criterion, offshore MVdc system, positive-damping reshaped impedance, robustness, small-signal dc impedance.**

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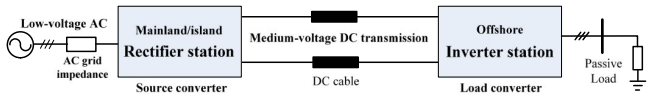


Fig. 1. Offshore MVdc system.

incremental resistor characteristic of the load converter's input impedance, but this would sacrifice the load converter's dynamic performance because the load converter's input impedance is preferred to be regulated to a negative resistor when achieving a good dynamic performance [17], [18]. To overcome this shortage, a tradeoff between the load dynamic performance and the interconnected system stability is needed [17]–[19]. In [17], the virtual adaptive parallel impedance is proposed to modify the input impedance of the load converter within a very small frequency range for maintaining the original dynamic performance of the load converter, but the control system robustness may be weak because it extremely relies on the accuracy of the filter parameters. Moreover, in the dc micro-grid interconnected system, a virtual-resistance stability control method is introduced with modifying the source output impedance to add the system damping [18]. That is to say, the source converter maintains the system stability, and the load converter guarantees the load dynamic performance, then the interconnected system stability and load dynamic performance can be both ensured. However, this method might hardly solve the high-frequency oscillation problems due to the limitation of control bandwidth. Thus, an expected active strategy with reshaping the source output impedance need to be further sought.

Meanwhile, the aforementioned stability analysis and control methods are all employed for the low-voltage applications, e.g., dc distributed power systems or dc micro grids, which are not directly applicable for the high/medium-voltage system that possesses traits such as high-voltage transmission level, complicated converter structure, long dc cable, and narrow control bandwidth of the converter [20]. Additionally, the instability phenomena cannot be identified from the dc-impedance-based approach that is only assumed to be decoupled by the dc-link capacitance, but ignores the ac-side impedance and dc cable effects [21], [22]. In [23] and [24], viewed from the dc terminal, a small-signal dc impedance model of two-terminal VSC-HVdc system is built, and the impacts of the converter control bandwidth, ac grid parameters, and the dc capacitance on system stability are analyzed. In [25], a distributed parameter dc cable modeling strategy is employed to improve the accuracy of the transmission line model, particularly for lines that are long or have a high-impedance density. Moreover, the MVdc electrical distributions for the large ship on-board power systems with the CPLs (propulsion drives) are investigated in [26]. Additionally, the effects of variations in the filtering effort and the distribution lengths, on the system stability, are also analyzed via the small-signal impedance-based stability assessment. However, the aforementioned high/medium-voltage system basically adopts the MMC or two-level structure [20]–[26], and no previous literatures have reported the small-signal impedance model and stability analysis based on a series-parallel structure for the MVdc system viewed from the dc terminal.

Moreover, in [27], several control methods are presented to enhance ac-bus voltage stability of the high/medium-voltage dc system, but they do not consider the dc-side oscillation suppression and stability control. In [28], the control parameters of source and load converters are appropriately designed to improve the system dc-side small-signal stability, but this method depends on the accuracy of the system parameters. Actually, for the high/medium-voltage interconnected system, the literature [24] indicates that the oscillation frequency is relatively high and not constant, owing to the quite small dc side storage capacitances and the long distance transmission dc cable. Additionally, the control bandwidth of the converter is not wide because of the limitation of the switching frequency. Consequently, the stability and robustness control turns to be more difficult [29]. There are extremely few reports of stability control methods that have a high reliability and consider the factors of dc cable and narrow control bandwidth. Thus, a proper way needs be further sought to mitigate the dc-side small-signal instability in the high/medium-voltage dc system, especially for the offshore MVdc considered in this paper.

In this paper, a virtual positive-damping reshaped impedance stability control method for the offshore MVdc system is proposed to effectively mitigate the dc-side oscillation with eliminating the narrow control bandwidth and dc cable effect. Because this strategy targets at the rectifier station, the load performance of the inverter station is not affected. This paper is organized as follows. First, the offshore MVdc system and its impedance stability control method are presented in Section II. Second, the dc-side output impedance of the rectifier station coupled by the input-parallel output-series (IPOS) structure and ac grid inductance is deduced in Section III, and then the small-signal dc impedance modeling of the overall system is established considering the dc cable effect. In Section IV, the system stability is analyzed in detail and the reason for the failure of the rectifier station to mitigate the dc-side oscillation using virtual-resistance stability control against the dc cable variation at a low switching frequency is found. This is because the output impedance of the rectifier station exhibits a negative damping characteristic in the dc-side oscillation range, and might be completely counteracted by the positive resistance of the dc cable. Then, a virtual positive-damping reshaped impedance stability control method is proposed to correct negative output resistance characteristic of the rectifier station to be positive. Simulation and experimental results are illustrated in Section V. Conclusions are drawn in Section VI.

II. Offshore MVDC System and Its Impedance Stability Control Method

As shown in Fig. 2, the two-terminal offshore MVdc system is mainly composed of a rectifier station in the mainland/island, a dc cable, an inverter station, and a passive network load in the offshore platform. The rectifier station is used as a power source to support the dc-side voltage, and the inverter station is used as the receiving end to supply power to the passive network. The rectifier station is an IPOS system that converts ac to dc, and the IPOS contains n submodules where the structure of each

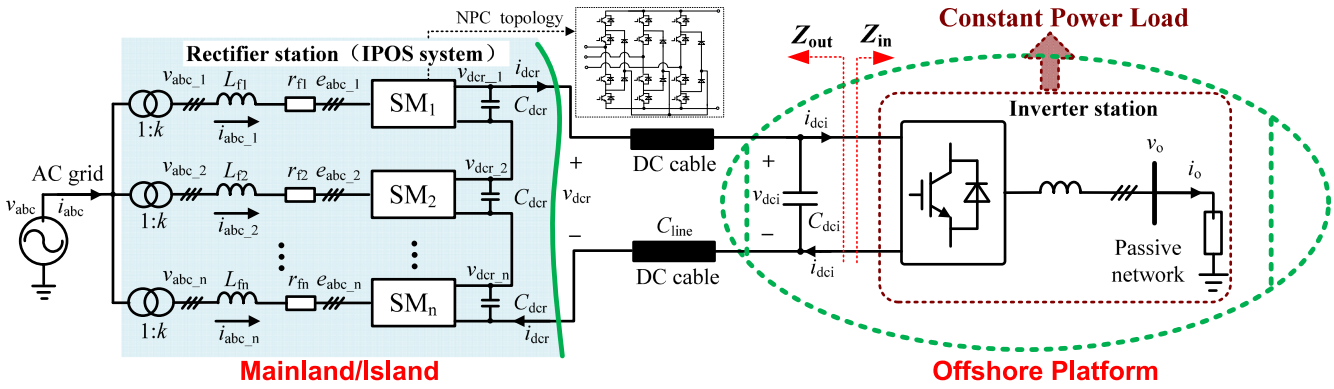


Fig. 2. Typical two-terminal offshore MVdc system.

submodule adopts a neutral-point clamped (NPC) topology. The inputs of each submodule SM_i $(i = 1, 2, \ldots)$ are isolated by transformers, and the outputs are connected in series to increase the dc side voltage and reduce the transmission loss.

In Fig. 2, v_{abc} and i_{abc} are the ac gird voltage and current of the rectifier station, respectively; $v_{\mathrm{abc\_i}}$ and $i_{\mathrm{abc\_i}}$ are the input ac voltage and current of the *i*th submodule, respectively; L_{fi} and r_{fi} are the filter inductance and its parasitic resistance of the *i*th submodule, respectively; $e_{\mathrm{abc\_i}}$ is the converter-side ac voltage of the *i*th submodule of the rectifier station; C_{dci} is the dc storage capacitance of each submodule of the rectifier station; v_{dcr} and i_{dcr} are the dc output voltage and current of the rectifier station; $v_{\mathrm{dcr\_i}}$ is the dc output voltage of the *i*th submodule of the rectifier station; v_{dci} and i_{dci} are the dc input voltage and current of the inverter station; C_{dci} is the dc storage capacitance of the inverter station; v_{o} and i_{o} are the output voltage and current of the inverter station; C_{line} is the transmission-line length of dc cable; and Z_{out} and Z_{in} are the total dc output impedance of the rectifier station and the dc input impedance of the inverter station, respectively.

Viewed from the dc input terminal, the inverter station is considered as a CPL since a small change in the dc voltage does not lead to a change in the output power of the inverter station, generating a negative incremental input resistance [10], which might easily cause dc-side oscillation and deteriorate the offshore MVdc stability. For this issue, the traditional virtual-resistance stability control method targeting the rectifier station is first introduced from low-voltage dc micro-grid application for mitigating its dc-side oscillation without affecting the load performance of the inverter station, expressed as follows:

$$v^*_{\mathrm{dcr\_}i} = \frac{1}{n} v_{\mathrm{dcr}} - R_v i_{\mathrm{dcr}} \tag{1}$$

where $v^*_{\mathrm{dcr\_}i}$ is the dc voltage reference of the *i*th submodule and R_{v} is the virtual resistance.

However, as indicated by the analyses in Section IV, under low switching-frequency and long-transmission-line conditions, it is difficult to guarantee the offshore MVdc stability on the dc-side merely using traditional virtual-resistance stability control.

1) First, the damping introduced by only the virtual-resistance stability control turns into a negative characteristic outside the control bandwidth of each submodule of the rectifier converter. Owing to the high voltage level and high power level, the switching frequency f_{sw} of the rectifier station cannot be selected as a high value considering the problem of heat dissipation. But with a decreasing switching frequency, the negative damping characteristic region becomes wider and moves towards to low frequencies.
2) Second, the dc storage capacitance C_{dci} of the inverter station, which is equal to the 1/*n* of the capacitance C_{dcr} of the rectifier station, is quite small. Combined with the impedance of the dc cable, a large oscillation peak will appear at a high oscillation frequency in the total dc output impedance Z_{out}. Once f_{sw} is not high, the oscillation frequency would exceed the control bandwidth and be located in the negative damping region.
3) In this case, the negative resistance of the rectifier converter can easily coincide with a positive resistance of dc cable at a certain length. Then, $Z_{\mathrm{out}}(s)$ will exhibit a large amplitude spike, and the interactions between $Z_{\mathrm{out}}(s)$ and $Z_{\mathrm{in}}(s)$ through the dc cable can easily lead to impedance mismatching. This causes dc-side voltage oscillation and system instability.

Therefore, considering the control bandwidth and dc cable effect, a virtual positive-damping reshaped impedance stability control method for each submodule of the rectifier station is further proposed to maintain the damping positive during the high-frequency oscillation region, as shown in Fig. 3. Its control equation is given as follows:

$$v^*_{\mathrm{dcr\_}i} = \frac{1}{n} v_{\mathrm{dcr}} - R_v G_{pd}(s) i_{\mathrm{dcr}}. \tag{2}$$

As indicated by (2), the proposed stability control method is composed of two parts: R_{v} is the traditional virtual-resistance stability control; and $G_{\mathrm{pd}}(s)$ is the transfer function of positive-damping reshaped with phase advance.

$$G_{\mathrm{pd}}(s) = \left(1 + \tau_{\mathrm{pd}} s \frac{\omega_{\mathrm{c}}}{s + \omega_{\mathrm{c}}}\right)^2 \tag{3}$$

where τ_{pd} is the time constant of the phase advance and ω_{c} is the cutoff frequency of the low-pass filter, which is designed to avoid the derivative term causing the switching harmonics and white noise amplification.

In addition, the IPOS system adopts the rectifier station dc-side voltage loop, submodule voltage-sharing loop, inner

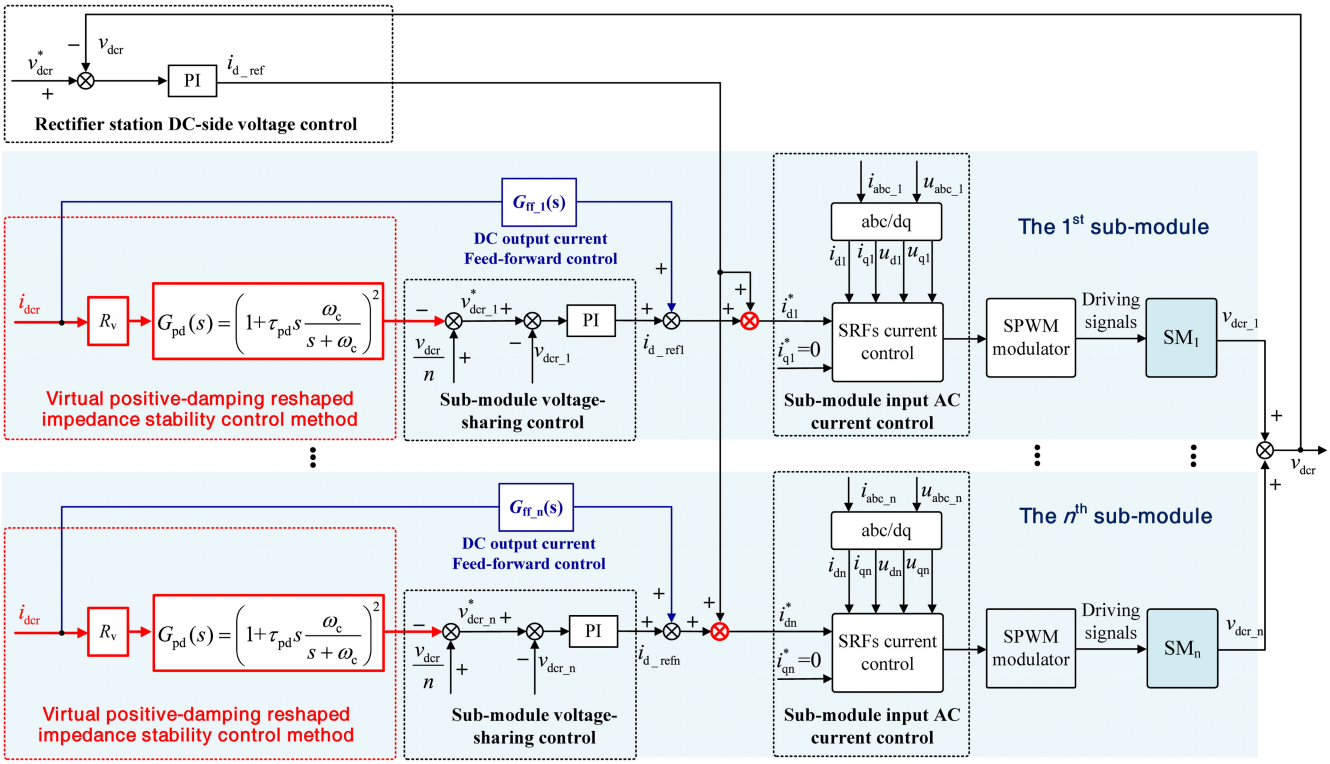


Fig. 3. Proposed virtual positive-damping reshaped impedance stability control method for the rectifier station.

current loop, and dc output current feed-forward loop control. The rectifier station dc-side voltage loop is used to accurately track the dc-side voltage reference and ensure the stable output voltage, where its output regulator value is set as the inner current reference. The submodule voltage-sharing loop is employed to adjust the inner current loop references and make the output voltage of each submodule be the same; the inner current loop control based on synchronous reference frames (SRFs) is used to guarantee the waveform quality of its input ac current; the dc output current feed-forward control is used to strengthen the ability of the rectifier converter to restrain load disturbances. $v^*_{\rm dcr}$ is the voltage reference of the rectifier station dc-side voltage loop, and the voltage reference of each submodule voltage-sharing loop is equal to v dcr/ n. $i_{\rm di}$ and $i_{\rm qi}$ are d-axis and q-axis components of the input ac current $i_{\rm abc\_i}$ of ith submodule; $v_{\rm di}$ and $v_{\rm qi}$ are d-axis and q-axis components of the input ac voltage $u_{\rm abc\_i}$ of ith submodule. $i_{\rm d\_ref}$ is the output value of the rectifier station dc-side voltage loop; $i_{\rm d\_refi}$ is the d-axis output value of the submodule voltage-sharing loop. $i^*_{\rm di}$ and $i^*_{\rm qi}$ are d-axis and q-axis reference values of the input ac current $i_{\rm abc\_i}$ of ith submodule, and the value of $i^*_{\rm di}$ is the sum of $i_{\rm d\_ref}$ and $i_{\rm d\_refi}$.

III. Small-Signal DC Impedance Modeling of Offshore MVDC System

As the impedance-based stability analysis is a very intuitive and effective way to analyze the interconnected system stability, the dc-side output impedance mode of rectifier station decoupled by the IPOS structure and ac grid inductance is first deduced, and then the small-signal dc impedance model of the overall system is established considering the dc cable effect. Here, we define Δ as the small-signal perturbation of each variable.

A. DC Output Impedance Model of Rectifier Station

As shown in Fig. 3, each submodule of the IPOS system in the SRFs can be mathematically expressed as follows:

$$\begin{cases} v_{\rm di} = (L_{\rm fi}p + r)i_{\rm di} - \omega_o L_{\rm fi} i_{\rm qi} + e_{\rm di} \\ v_{\rm qi} = (L_{\rm fi}p + r)i_{\rm qi} + \omega_o L_{\rm fi} i_{\rm di} + e_{\rm qi} \end{cases} \tag{4}$$

where $\omega_{\rm o}$ is the angular frequency of the input ac voltage; p is a differential operator; and $e_{\rm di}$ and $e_{\rm qi}$ are the d-axis and q-axis components of the $e_{\rm abc\_i}$, respectively.

The SRFs current control [30] is adopted to decouple the d-axis and q-axis components. The control equations of $e_{\rm di}$ and $e_{\rm qi}$ are as follows:

$$\begin{cases} e_{\rm di} = -(i^*_{\rm di} - i_{\rm di})G_i(s) + \omega_o L_{\rm fi} i_{\rm qi} + v_{\rm di} \\ e_{\rm qi} = -(i^*_{\rm qi} - i_{\rm qi})G_i(s) - \omega_o L_{\rm fi} i_{\rm di} + v_{\rm qi}. \end{cases} \tag{5}$$

In (5), $G_{\rm i}(s) = k_{\rm pi} + k_{\rm ii}/s$ represents the PI controller.

By substituting (5) into (4) and simplifying, the following expression is obtained for the ith submodule of IPOS system.

$$\begin{cases} (L_{\rm fi}p + r_{\rm fi})i_{\rm di} = (i^*_{\rm di} - i_{\rm di})G_i(s) \\ (L_{\rm fi}p + r_{\rm fi})i_{\rm qi} = (i^*_{\rm qi} - i_{\rm qi})G_i(s). \end{cases} \tag{6}$$

The state variables in (6) can be rewritten as the sums of steady-state values and their small perturbations, such as $i_d = I_d + \Delta i_d$ and $i_q = I_q + \Delta i_q$. Substituting these into (6) and

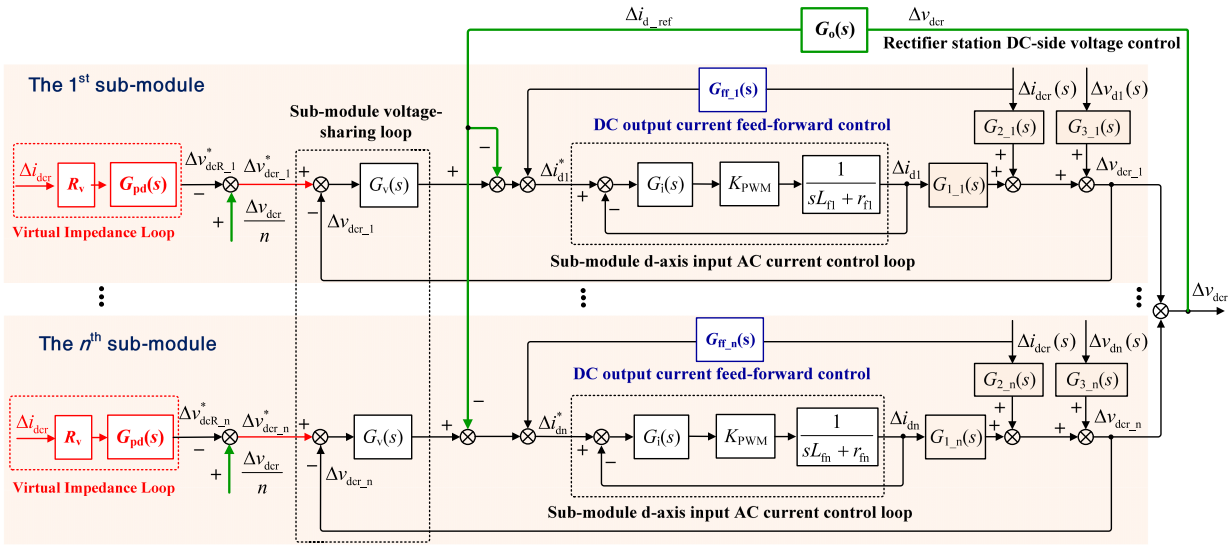


Fig. 4. Small-signal model of the control method for the IPOS system of rectifier station.

neglecting the second-order perturbations, the following small-signal equations are deduced as follows:

$$\begin{cases}(L_{\rm fi}p+r_{\rm fi})\Delta i_{\rm di}=(\Delta i^*_{\rm di}-\Delta i_{\rm di})G_i(s)\\(L_{\rm fi}p+r_{\rm fi})\Delta i_{\rm qi}=(\Delta i^*_{\rm qi}-\Delta i_{\rm qi})G_i(s).\end{cases}\tag{7}$$

Applying the Laplace transformation to (7) yields

$$\begin{cases}\Delta i_{\rm di}(s)=\Delta i^*_{\rm di}(s)=[\Delta i_{\rm di}(s)-\Delta i_{\rm di}(s)]\,G_i(s)/(L_{\rm fi}s+r_{\rm fi})\\\Delta i_{\rm qi}(s)=\Delta i^*_{\rm qi}(s)=[\Delta i_{\rm qi}(s)-\Delta i_{\rm qi}(s)]\,G_i(s)/(L_{\rm fi}s+r_{\rm fi}).\end{cases}\tag{8}$$

To facilitate the analysis, the d-axis loop is taken as an example for further study considering the symmetry between the d-axis and q-axis inner current loops. Using (8), the small-signal model of the d-axis input ac current loop is obtained, as shown in the dotted frame in Fig. 4, where $K_{\rm pwm}$ is the equivalent gain of the pulse width modulator.

Moreover, $v_{\rm dcri}$, $i_{\rm di}$, and $v_{\rm di}$ can be also rewritten as the sums of steady-state values and their small perturbations: $v_{\rm dcr\_i}=V_{\rm dcr\_i}+\Delta v_{\rm dcr\_i}$, $i_{\rm di}=I_{\rm di}+\Delta i_{\rm di}$, and $v_{\rm di}=V_{\rm di}+\Delta v_{\rm di}$. Then, according to the power balance between the two sides of each submodule of the IPOS system without considering the power losses, the relationships between the small perturbations $\Delta v_{\rm dcr\_i}(s)$ and $\Delta i_{\rm di}(s)$, $\Delta i_{\rm dcr}(s)$, $\Delta v_{\rm di}(s)$ are easily derived as $G_{\rm 1\_i}(s)$, $G_{2\_i}(s)$, and $G_{3\_i}(s)$, respectively

$$\begin{cases}\dfrac{\Delta v_{{\rm dcr}\_i}(s)}{\Delta i_{\rm di}(s)}=\dfrac{3V_{\rm di}}{2(C_{\rm dcr}V_{{\rm dcr}\_i}s+I_{\rm dcr})}=G_{1\_i}(s)\\[2ex]\dfrac{\Delta v_{{\rm dcr}\_i}(s)}{\Delta i_{\rm dcri}(s)}=-\dfrac{V_{\rm dcri}}{C_{\rm dcr}V_{{\rm dcr}\_i}s+I_{\rm dcr}}=G_{2\_i}(s)\\[2ex]\dfrac{\Delta v_{{\rm dcr}\_i}(s)}{\Delta v_{\rm di}(s)}=\dfrac{3I_q}{2(C_{\rm dcr}V_{{\rm dcr}\_i}s+I_{\rm dcr})}=G_{3\_i}(s).\end{cases}\tag{9}$$

The dc output current feed-forward control is employed to improve the anti-load-disturbance ability of the rectifier station. It is desired that the feed-forward transfer function $G_{\rm ff\_i}(s)$ in Fig. 4 can offset the impact of $\Delta i_{\rm dcr}(s)$ on $\Delta v_{\rm dcr\_i}(s)$ via $G_{2i}(s)$. Thus, by combining Fig. 4 and (9), $G_{\rm ff\_i}(s)$ can be obtained

$$G_{{\rm ff}\_i}(s)=-\frac{[sL_{\rm fi}+r_{\rm fi}+K_{\rm PWM}G_i(s)]}{K_{\rm PWM}G_i(s)}\cdot\frac{G_{2\_i}(s)}{G_{1\_i}(s)}.\tag{10}$$

Since the magnitude of $K_{\rm pww}G_{\rm i}(s)$ is much larger than that of $sL_{\rm fi}+R_{\rm fi}$, the term $sL_{\rm fi}+R_{\rm fi}$ can be neglected to facilitate the implementation of the algorithm. Then, (10) is simplified as follows:

$$G_{{\rm ff}\_i}(s)\approx-\frac{G_{2\_i}(s)}{G_{1\_i}(s)}=\frac{2V_{{\rm dcr}i}}{3V_{\rm di}}.\tag{11}$$

Then, the small-signal models of submodule voltage-sharing loop and rectifier station dc-side voltage loop control structure are built, where $G_{\rm v}(s)=k_{\rm pv}+k_{\rm iv}/s$ and $G_{\rm o}(s)=k_{\rm po}+k_{\rm io}/s$ represent the submodule voltage-sharing loop and rectifier-station dc-side voltage loop regulators, respectively.

Moreover, by applying small-signal decomposition to the virtual positive-damping reshaped impedance stability control equation for each submodule, its small-signal voltage perturbation $\Delta v^*_{{\rm dcr}\_i}$ is obtained as follows:

$$\Delta v^*_{{\rm dcr}\_i}=-R_vG_{pd}(s)\Delta i_{\rm dcr}.\tag{12}$$

Thus, by combining (8)–(12) and the small-signal model of the current/voltage loops, the small-signal dc output impedance model of the IPOS system of the rectifier station is derived as shown in Fig. 4.

While shifting the feedback vertex of $G_{\rm o}$(s) forward to the output of $v^*_{{\rm dcr}\_i}(s)$ and combining the small-signal voltage perturbation $\Delta v_{\rm dcr}/n$ of each submodule voltage-sharing loop, it is easily found that the signals of the input side are composed of n small perturbations of dc output current $\Delta i_{\rm dc}(s)$. Then, the virtual impedance loop of each submodules can be depicted together in the left-side shadow part of Fig. 5 via the superposition theorem, and the total small-signal voltage perturbation of dc output voltage $\Delta v^*_{\rm dcr}(s)$ introduced by the virtual impedance is

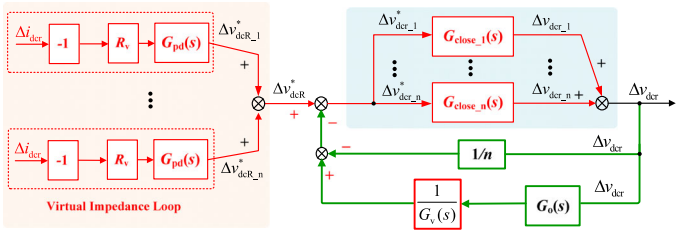


Fig. 5 Simplified small-signal dc output impedance model.

expressed as follows:

$$\Delta v^*_{\mathrm{dcR}} = \sum_{i=1}^{n} \Delta v^*_{\mathrm{dcR\_i}} = -nR_{\mathrm{v}}G_{\mathrm{pd}}(s)\Delta i_{\mathrm{dcr}}. \tag{13}$$

By calculating and merging the equivalent transfer functions $G_{\mathrm{close\_i}}(s)$ of each submodule voltage sharing loops and d-axis input ac current loops, and ignoring the impact of the input ac voltage perturbations, the simplified small-signal dc output impedance model is obtained, as shown in Fig. 5. The expression of $G_{\mathrm{close\_i}}(s)$ from its small-signal perturbation voltage reference $\Delta v^*_{\mathrm{dcr\_}i}$ to its output voltage $v_{\mathrm{dcr\_i}}$ is expressed as follows:

$$G_{\mathrm{close\_i}} = \frac{\Delta v_{\mathrm{dcr\_i}}}{\Delta v^*_{\mathrm{dcr\_i}}} = \frac{K_{\mathrm{PWM}}G_i(s)G_{1\_\mathrm{i}}(s)G_v(s)}{sL_{\mathrm{fi}} + r_{\mathrm{fi}} + K_{\mathrm{PWM}}G_i(s) + K_{\mathrm{PWM}}G_i(s)G_{1\_\mathrm{i}}(s)G_v(s)}. \tag{14}$$

Bringing $G_{1\_i}(s)$ into (14), (14) is changed as follows:

$$G_{\mathrm{close\_i}} = \frac{3K_{\mathrm{PWM}}G_iV_{\mathrm{di}}G_v(s)}{\begin{bmatrix}2L_{\mathrm{fi}}C_{\mathrm{dcr}}V_{\mathrm{dcr\_}i}s^2 + 3K_{\mathrm{PWM}}G_i(s)V_{\mathrm{di}}G_v(s) \\ +(L_{\mathrm{fi}}I_{\mathrm{dcr}} + K_{\mathrm{PWM}}G_i + 2r_{\mathrm{fi}}C_{\mathrm{dcr}}V_{\mathrm{dcr\_}i})s\end{bmatrix}}. \tag{15}$$

In (15), it is noted that the ac-side filter inductance L_{fi} has been transferred to the dc side and coupled with the dc-side energy storage capacitor C_{dcr}, resulting in the phase of $G_{\mathrm{close\_i}}(s)$ falling to $-90°\sim-180°$ at high frequencies.

Meanwhile, according to (14), the equivalent transfer function from $\Delta v_{\mathrm{dcr}}(s)$ to $v^*_{\mathrm{dcr}}(s)$ for the rectifier station dc-side voltage loop is derived as follows:

$$\frac{\Delta v_{\mathrm{dcr}}}{\Delta v^*_{\mathrm{dcR}}} = \frac{\sum_{i=1}^{n} G_{\mathrm{closei}}}{1 + \left[\frac{G_{\mathrm{o}}(s)}{G_{\mathrm{v}}(s)} - \frac{1}{n}\right]\sum_{i=1}^{n} G_{\mathrm{closei}}}. \tag{16}$$

Thus, by combining (13)–(16) and the simplified small-signal dc output impedance model, the small-signal dc output impedance model of the rectifier station $Z_{\mathrm{dcr}}(s)$ is obtained

$$Z_{\mathrm{dcr}}(s) = -\frac{\Delta v_{\mathrm{dcr}}}{\Delta i_{\mathrm{dcr}}} = -\frac{\Delta v_{\mathrm{dcr}}}{\Delta v^*_{\mathrm{dcR}}} \cdot \frac{\Delta v^*_{\mathrm{dcR}}}{\Delta i_{\mathrm{dcr}}} = nR_{\mathrm{v}}G_{\mathrm{pd}}(s)\frac{\sum_{i=1}^{n} G_{\mathrm{closei}}}{1 + \left[\frac{G_{\mathrm{o}}(s)}{G_{\mathrm{v}}(s)} - \frac{1}{n}\right]\sum_{i=1}^{n} G_{\mathrm{closei}}}. \tag{17}$$

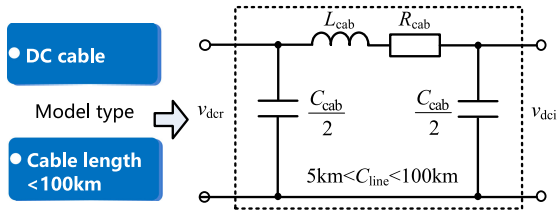


Fig. 6. π-type model of dc cable.

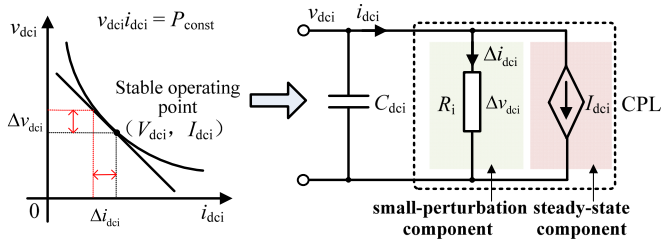


Fig. 7. Negative incremental impedance model of the CPL.

B. Models of DC Cable and DC Input Impedance of Inverter Station

Because the ground capacitance of the dc cable is large and the cable length C_{line} is generally less than 100 km, the π-type model is adopted for the dc cable, as shown in Fig. 6, where L_{cab}, R_{cab}, and C_{cab} represent the lumped parameters of inductance, resistance, and capacitance, respectively. Their values are proportional to the length C_{line} of the dc cable. The dc cable is used while $C_{\mathrm{line}} > 5$ km. Otherwise, the overhead line is used for the short-distance transmission.

Normally, a small change in the dc voltage does not lead to a change in the output power of the inverter station, and the dynamic response of the inverter station is faster than that of the rectifier station in this paper, so the inverter station is simplified to a CPL [10]. Fig. 7 shows the negative incremental impedance model of the CPL. Its power characteristic is

$$p_{\mathrm{const}} = v_{\mathrm{dci}}i_{\mathrm{dci}} \tag{18}$$

where p_{const}, v_{dci}, and i_{dci} represent the dc input power, input voltage, and input current of the inverter station (CPL), respectively.

Expanding (18) using the first-order Taylor series, it yields

$$i_{\mathrm{dci}} = 2\frac{P_{\mathrm{const}}}{V_{\mathrm{dci}}} - \frac{P_{\mathrm{const}}}{V^2_{\mathrm{dci}}}v_{\mathrm{dci}} \tag{19}$$

where P_{const}, and V_{dci} represent the steady-state power and steady-state voltage, respectively.

Considering that v_{dcii} and i_{dci} are expressed by the sums of steady-state values and their small perturbations ($v_{\mathrm{dci}} = V_{\mathrm{dci}} + \Delta v_{\mathrm{dci}}$ and $i_{\mathrm{dci}} = I_{\mathrm{dci}} + \Delta i_{\mathrm{dci}}$), (19) is rewritten as

$$I_{\mathrm{dci}} + \Delta i_{\mathrm{dci}} = 2\frac{P_{\mathrm{const}}}{V_{\mathrm{dci}}} - \frac{P_{\mathrm{const}}}{V^2_{\mathrm{dci}}}(V_{\mathrm{dci}} + \Delta v_{\mathrm{dci}}) = \frac{P_{\mathrm{const}}}{V_{\mathrm{dci}}} - \frac{P_{\mathrm{const}}}{V^2_{\mathrm{dci}}}\Delta v_{\mathrm{dci}}. \tag{20}$$

TABLE I
ELECTRICAL PARAMETERS OF OFFSHORE MVDC SYSTEMS

Parameters	Values	Parameters	Values
Input AC voltage	760 V	Rated DC voltage	10 kV
AC system frequency	50 Hz	Rated power	200 kW
Filter reactor inductance of sub-module	15 mH	DC cable resistance	0.016 Ω/km
Filter reactor resistance of sub-module	0.02 Ω	DC cable capacitance	1.128 μF/km
DC capacitor of sub-module	176. 25 μF	DC cable inductance	0.485 mH/km
DC capacitor of inverter station	40 μF	K_{pwm}	2000

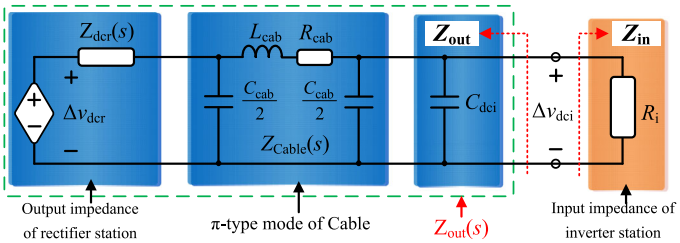


Fig. 8. Small-signal dc impedance model of the offshore MVdc system.

From (20), the small-signal impedance Z_{in} and equivalent current source I_{i} of constant power are derived as follows:

$$I_{\text{dci}} = \frac{P_{\text{const}}}{V_{\text{dci}}}, \quad R_{\text{i}} = \frac{\Delta v_{\text{dci}}}{\Delta i_{\text{dci}}} = -\frac{V_{\text{dci}}^2}{P_{\text{const}}}. \tag{21}$$

On the basis of Figs. 5–7, the small-signal dc impedance model of the offshore MVdc system can be depicted in Fig. 8. The total equivalent output impedance $Z_{\text{out}}(s)$ is composed of the output impedance $Z_{\text{dcr}}(s)$ of the rectifier station, the dc-cable impedance $Z_{\text{Cable}}(s)$, and the dc-side capacitance of the inverter station C_{dci}. Thus, $Z_{\text{out}}(s)$ is described as follows:

$$Z_{\text{out}}(s) = \left[Z_{\text{dcr}}(s) \| \frac{2}{sC_{cab}} + sL_{cab} + R_{cab}\right] \| \frac{2}{sC_{cab}} \| \frac{1}{sC_{dci}}. \tag{22}$$

According to Fig. 8, the dc input impedance $Z_{\text{in}}(s)$ of the inverter station is

$$Z_{\text{in}}(s) = R_i. \tag{23}$$

Moreover, according to Fig. 8, the relationship between Δv_{dcr} and Δv_{dci} is derived as follows:

$$\Delta v_{\text{dci}}(s) = \Delta v_{\text{dcr}}(s) \cdot \frac{Z_{\text{in}}(s)}{Z_{\text{in}}(s)+Z_{\text{out}}(s)} = \frac{\Delta v_{\text{dcr}}(s)}{1+Z_{\text{out}}(s)/Z_{\text{in}}(s)}$$
$$= \Delta v_{\text{dcr}}(s) \cdot \frac{1}{1+T_{\text{o}}(s)}. \tag{24}$$

In (24), $T_{\text{o}}(s) = Z_{\text{out}}(s)/Z_{\text{in}}(s)$, which is not only the ratio of the output impedance of the rectifier station to the input impedance of the inverter station, but also the equivalent loop gain of the two-terminal offshore MVdc system. Obviously, $T_{\text{o}}(s)$ is the one responsible for stability. Therefore, a necessary and sufficient condition for stability of the system can be obtained by applying the Nyquist Criterion to $T_{\text{o}}(s)$, i.e., the interconnected system is stable if and only if the Nyquist contour of $T_{\text{o}}(s)$ does not encircle the $(-1, 0)$ point.

IV. DC-SIDE OSCILLATION AND ITS VIRTUAL POSITIVE-DAMPING RESHAPED ANALYSIS

According to the small-signal impedance models of the offshore MVdc system built in Section III, the dc-side oscillation mechanism of the offshore MVdc system is investigated using the Nyquist stability criterion. Also, the reason why the traditional virtual-resistance stability control fails to suppress the system high-frequency oscillation under the low switching-frequency condition is analyzed in detail.

Table I shows the system electrical parameters according to the system topology, capacity, and practical engineering experience. To exclude the impact of improper parameter selection on the system stability analysis, the parameters of the voltage-current three-loop control of the rectifier station are designed based on the control bandwidth and stability margin. Considering the control system dynamic performance, the bandwidth of the inner current loop is selected as 1/5 of the switching frequency; the bandwidth of the submodule voltage-sharing loop is selected as 1/5 of that of the inner current loop; and the bandwidth of the dc-side voltage loop is selected as 1/5 of that of the submodule voltage-sharing loop. Considering the control system stability margin, the phase margin of the submodule voltage-sharing loop is above 60°, and the phase margin of the dc-side voltage loop is above 80°. Meanwhile, in order to further facilitate the effect of the switching frequency on the system stability, four different switching frequencies are presented, where the high switching frequency mode is selected as 20 kHz, and the low switching frequency mode is selected as 12, 8, and 4 kHz, respectively. The corresponding control parameters are shown in Table II.

A. DC-Side Oscillation and its Virtual-Resistance Stability Mechanisms

From Fig. 9(a), the total dc output impedance Z_{out} only considering π-type dc cable can be derived as (25). In this case,

TABLE II
CONTROL PARAMETERS OF THE OFFSHORE MVDC SYSTEMS

f_{sw}=20kHz		f_{sw}=12kHz		f_{sw}=8kHz		f_{sw}=4kHz	
Parameters	Values	Parameters	Values	Parameters	Values	Parameters	Values
k_{pn}	0.068	k_{pn}	0.039	k_{pn}	0.020	k_{pn}	0.014
k_{in}	0.5	k_{in}	0.5	k_{in}	0.5	k_{in}	0.5
k_{pv}	1.643	k_{pv}	0.985	k_{pv}	0.649	k_{pv}	0.327
k_{iv}	5	k_{iv}	5	k_{iv}	5	k_{iv}	5
k_{pi}	0.188	k_{pi}	0.113	k_{pi}	0.079	k_{pi}	0.038
k_{ii}	10	k_{ii}	10	k_{ii}	10	k_{ii}	10

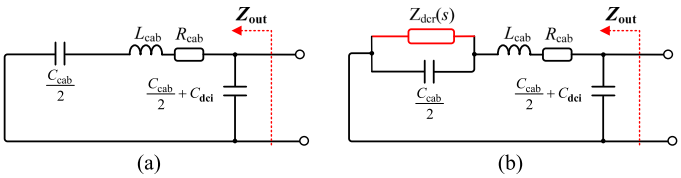


Fig. 9. Contrastive equivalent model of Z_{out}. (a) Only considering π-type dc submarine cable. (b) Considering the reshaping Z_{dcr}.

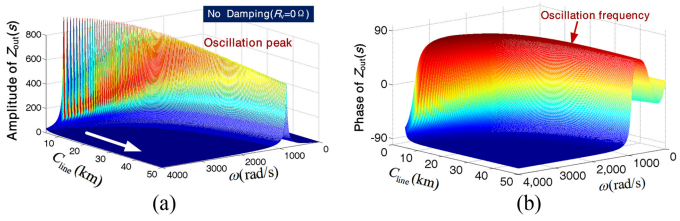


Fig. 10. Bode diagram of $Z_{\text{out}}(s)$ with different values of C_{line}, $R_{\text{v}} = 0$. (a) Amplitude of $Z_{\text{out}}(s)$. (b) Phase of $Z_{\text{out}}(s)$.

the characteristic equation of $Z_{\text{out}}(s)$ can be expressed as the multiplication of a first-order system by a second-order weakly damped system. Obviously, the second-order system has an oscillation frequency ω_{res}, and its expression is derived as (26) follows:

$$Z_{\text{out}}(s) = \frac{2s^2 + 2s\frac{R_{\text{cab}}}{L_{\text{cab}}} + \frac{4}{L_{\text{cab}}C_{\text{cab}}}}{(C_{\text{cab}} + 2C_{\text{dci}})\left\{s(s^2 + s\frac{R_{\text{cab}}}{L_{\text{cab}}} + \omega_{\text{res}}^2)\right\}} \tag{25}$$

$$\omega_{\text{res}} = \sqrt{\frac{4(C_{\text{cab}} + C_{\text{dci}})}{L_{\text{cab}}C_{\text{cab}}(C_{\text{cab}} + 2C_{\text{dci}})}}. \tag{26}$$

Moreover, Fig. 10 shows the amplitude and phase of $Z_{\text{out}}(s)$ with different dc-cable length C_{line} under no damping control ($R_{\text{v}} = 0$). Obviously, an oscillation peak exists in the amplitude of Z_{out} (s), which is caused by the coupling between the inverter station dc-side capacitance C_{dci} and the π-type cable mode, indicated by (26). Simultaneously, with the increase of C_{line}, the oscillation frequency moves towards a low-frequency bandwidth, and its peak gradually decreases owing to the

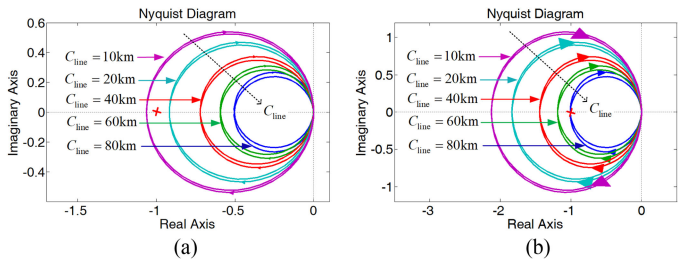


Fig. 11. Nyquist diagram of $T_{\text{o}}(s)$ with different values of C_{line} under the half and full load conditions, $R_{\text{v}} = 0$. (a) Half load, P = 100 kW. (b) Full load, P = 200 kW.

increasing dc-cable resistance. Moreover, the phase of $Z_{\text{out}}(s)$ is inverted to 90° at the oscillating frequency. In accordance with the negative resistance of $Z_{\text{in}}(s)$, the phase of $T_{\text{o}}(s)$ at the oscillation frequency would exceed 180°. In this case, according to the Nyquist stability criterion, the system will lose stability as long as $T_{\text{o}}(s)$ has a large magnitude.

Fig. 11 shows the Nyquist diagrams of $T_{\text{o}}(s)$ with different values of C_{line} under the half and full load conditions, $R_{\text{v}} = 0$. As shown in Fig. 11(a), with the decrease of C_{line}, the Nyquist curve of $T_{\text{o}}(s)$ expands to the left half-plane, possibly enclosing (−1,0), and might make the system unstable. That is because the oscillation peak of $Z_{\text{out}}(s)$ becomes larger that causes the amplitude of $T_{\text{o}}(s)$ to further increase. Simultaneously, as indicated by a comparison of Fig. 11(a) and (b), the system is more likely to become unstable under the same line length with a larger output power P. That is also because the dc input impedance $Z_{\text{in}}(s)$ turns to be small with a larger P, and then the amplitude of $T_{\text{o}}(s)$ further increases. In this case, the worst operation condition is located in the full load.

According to the aforementioned analyses, the root cause of system instability is the oscillation peak existing in $Z_{\text{out}}(s)$, with $R_{\text{v}} = 0$. For this issue, the virtual-resistance stability control by reshaping Z_{dcr} is introduced from the low-voltage micro-grid applications for enhancing the dc-side damping and suppressing the oscillation peak, as shown in Fig. 9(b). The analysis presented in Appendix shows that adjusting Z_{dcr} to an appropriately resistance can suppress the dc-side oscillation

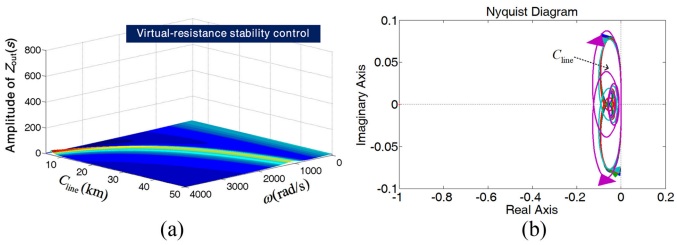


Fig. 12. Diagrams of the impedance-based stability information under the traditional virtual-resistance stability control, $f_{sw} = 20$ kHz. (a) Bode diagram of $Z_{out}(s)$. (b) Nyquist diagram of $T_o(s)$.

peak and that the suppression ability is proportional to the resistance.

Moreover, Fig. 12 shows diagrams of the impedance-based stability information under the virtual-resistance stability control, where $f_{sw} = 20$ kHz, $P = 200$ kW (full load), and $R_v = 1$. In this case, the amplitude of $Z_{out}(s)$ obviously decreases from 800 or more to less than 20 at the oscillation frequency, and the effect of cable length on the oscillation peak is also essentially eliminated. Moreover, the Nyquist curve of $T_o(s)$ is almost unchanged regardless of the cable length variation. Thus, while the control system maintains a good oscillation-peak suppression ability, $Z_{out}(s)$ and $T_o(s)$ would keep a small magnitude, and the control system would be still stable against loads and cable length variations.

B. Drawbacks of Traditional Virtual-Resistance Stability Control Under the Low Switching-Frequency Condition

However, the traditional virtual-resistance stability control mentioned in Section III only analyzes the condition of rectifier-station submodule at high switching frequency ($f_{sw} = 20$ kHz) condition, but not considers the practical device switching loss that causes the submodule be in a low switching-frequency condition. Thus, in this section, the impact of the virtual-resistance control on the system stability in the low-switching frequency mode is analyzed in detail.

Fig. 13 shows Nyquist diagrams of $T_o(s)$ under the traditional virtual-resistance stability control in the low switching-frequency condition, where f_{sw} is set as 12, 8, and 4 kHz, respectively. The control parameters with different values of f_{sw} are presented in Table II. For the above three values of f_{sw}, with changes in the dc cable length, their Nyquist curves all appear to enclose $(-1, 0)$ and the system will lose stability especially when the dc cable length is around 8, 14, and 25 km, respectively. Obviously, under the low switching-frequency condition, the traditional virtual-resistance stability control may result in an unstable region, and its robustness against the variations in the dc-cable length is poor. Moreover, with f_{sw} further decreasing, the likelihood of the dc-cable length region resulting in the system being unstable increases. In this case, a low f_{sw} is not conducive to a long-distance power transmission. Then, it is desirable to reveal the reason why the traditional virtual-resistance stability control fails to suppress the system oscillation and deteriorates its stability.

Fig. 14 shows the bode diagram of $Z_{dcr}(s)$ with different values of f_{sw}. It is obvious that when only the traditional virtual-resistance stability control is used, the phase of $Z_{dcr}(s)$ is below $-90°$ at a high-frequency bandwidth. This means that the virtual impedance $Z_{dcr}(s)$ turns into a negative damping characteristic. Actually, according to the Fig. 14 and earlier (15), the essential cause of the negative damping is that the ac-side filter inductance L_{fi} is transferred to the dc side and coupled with the dc-side energy storage capacitor C_{dcr}, resulting in the phase of $Z_{dcr}(s)$ falling to the range of $-90°\sim180°$ outside the control bandwidth of the submodule voltage-sharing loop. With the decrease of the switching frequency, the crossover frequency where the phase curve of $Z_{dcr}(s)$ crosses $-90°$ shifts towards a lower frequency bandwidth, and its positive damping region becomes narrower.

Fig. 15 shows the contrastive bode diagrams of $Z_{out}(s)$ with different switching frequencies under traditional virtual-resistance stability control. In the high switching frequency condition, as shown in Fig. 15(a), with increasing dc cable length, the oscillation peak of $Z_{out}(s)$ will move towards the low frequency direction, but its magnitude remains almost unchanged and its oscillation peak even turns to be smaller, because the damping characteristic around the oscillation frequency is positive. However, in the low switching-frequency condition, the control bandwidth becomes narrow with the decrease of f_{sw}, and the dc-side oscillation frequency is located in the high frequency area because C_{dci}, which is equal to the $1/n$ of C_{dcr}, is quite small. Then, the oscillation frequency may easily exceed the control bandwidth, and its damping characteristic becomes negative in this case. Simultaneously, as shown in Fig. 15(b), with the increase of C_{line}, the positive resistance of dc cable increases, and the negative resistance of Z_{dcr} decreases. The worst case is that the positive resistance of dc cable is counteracted by the negative resistance of Z_{dcr}, where the damping of the total equivalent output impedance Z_{out} (s) turns to be 0. In this case, a larger oscillation peak appears in the amplitude of Z_{out} (s) and leads to the deterioration of the system stability.

Fig. 16 further shows the amplitude of $Z_{out}(s)$ with the variation of C_{line} under traditional virtual-resistance stability control, $f_{sw} = 4$ kHz. Obviously, the virtual-resistance stability control fails to suppress the oscillation peak with the wide variation of C_{line} in the low switching-frequency condition. Especially, in the interval of 20–30 km, its maximum oscillation peak is far greater than that in the case with no damping, as indicated by Fig. 12(a) and Fig. 16. Then, the virtual-resistance stability control will seriously deteriorate the system stability. Meanwhile, according to the previous analysis, the essential reason for the poor robustness against the C_{line} variation is that the positive resistance of dc cable is counteracted by the negative resistance of Z_{dcr}. Therefore, in order to remove the adverse effects of C_{line}, the negative resistance characteristic of Z_{dcr} must be removed.

C. Virtual Positive-Damping Reshaped Impedance Stability Control

To solve this problem, a virtual positive-damping reshaped impedance stability control method is further proposed to

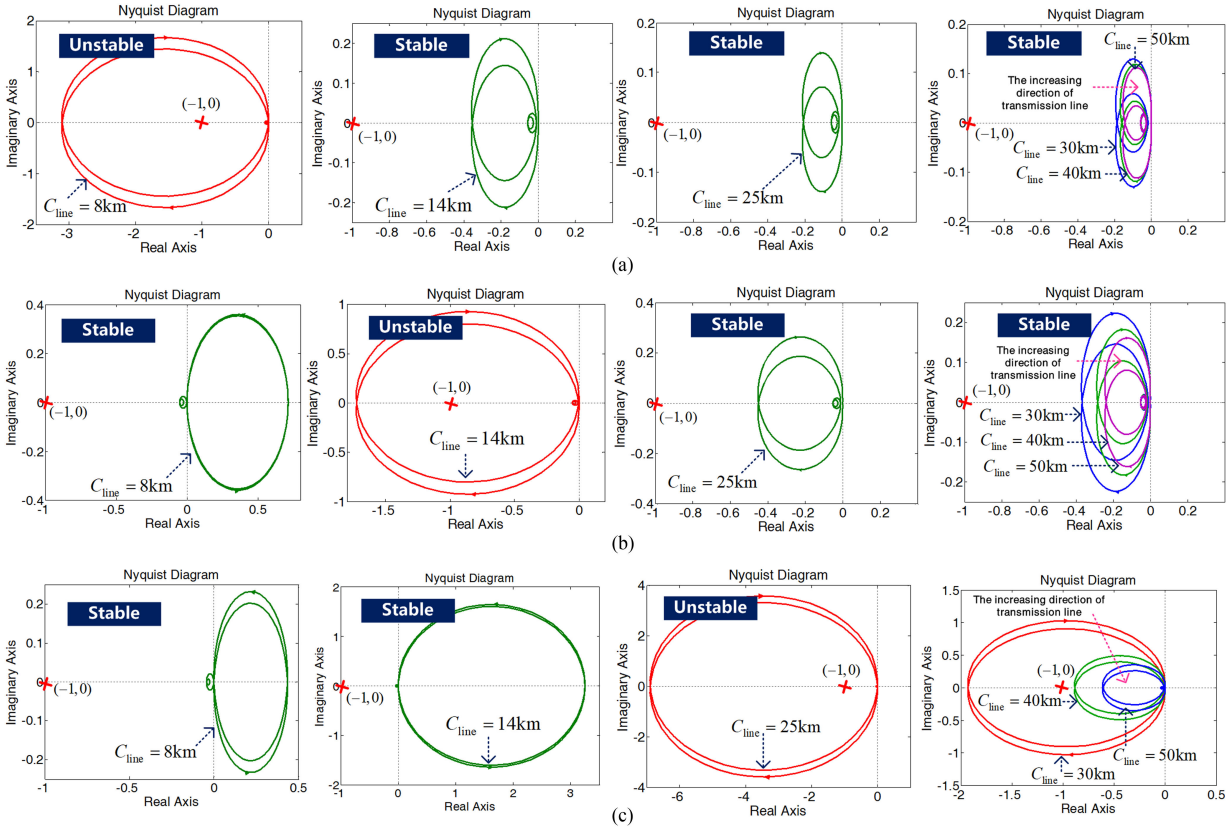


Fig. 13. Nyquist diagram of $T_o(s)$ under the traditional virtual-resistance stability control under the low switching-frequency condition. (a) $f_{sw} = 12$ kHz. (b) $f_{sw} = 8$ kHz. (c) $f_{sw} = 4$ kHz.

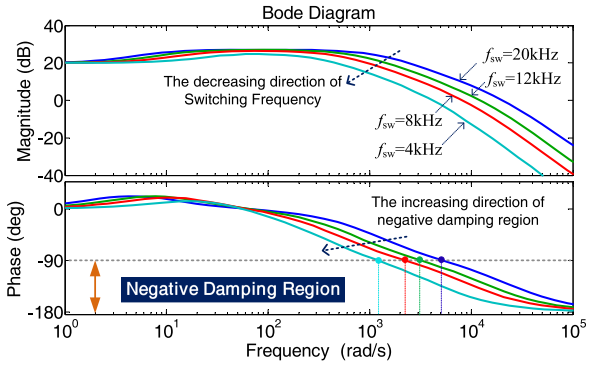
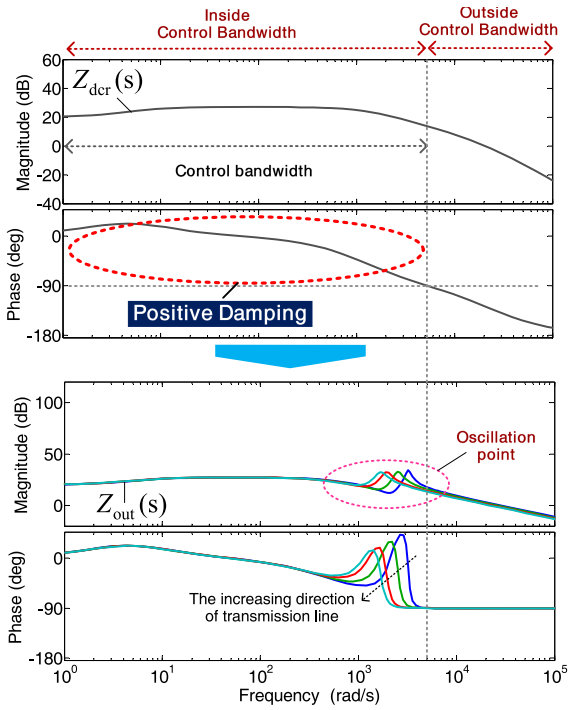


Fig. 14. Bode diagram of $Z_{dcr}(s)$ with using traditional virtual-resistance control.

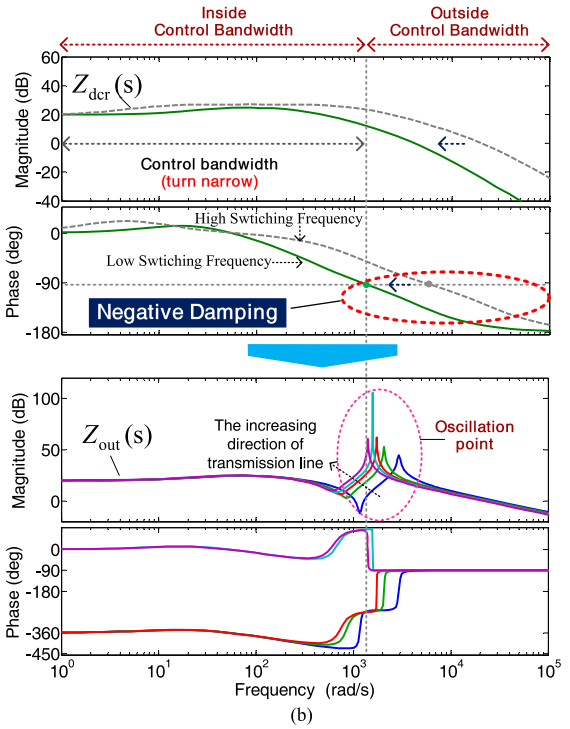
correct the negative damping characteristic at the dc oscillation frequency in the low switching-frequency condition, as shown in Fig. 3. The transfer function $G_{pd}(s)$ is presented to advance the phase of Z_{dcr} outside the control bandwidth, and it is realized in the form of integral and negative feedback according to (27), which can effectively avoid the harmonic amplification caused by the differential terms of $G_{pd}(s)$. The implementation diagram of $G_{pd}(s)$ is depicted in Fig. 17

$$G_{pd}(s)=1+\frac{2\tau_{pd}\omega_c}{1+\omega_c/s}+\left(\frac{\tau_{pd}\omega_c}{1+\omega_c/s}\right)\cdot\left(\frac{\tau_{pd}\omega_c}{1+\omega_c/s}\right). \quad (27)$$

Fig. 18(a) shows the bode diagram of $G_{pd}(s)$, where $f_{sw} = 4$ kHz, $\omega_c = 1.2 \times 10^4$ rad/ s, $\tau_{pd} = 1$, and $R_v = 1\,\Omega$. Actually, considering the shortest dc cable length is set to 5 km, the maximum oscillation frequency is approximately equal to 3.53×10^3 rad/ s according to (26). Obviously, the magnitude of $G_{pd}(s)$ is approximately 1 inside the control bandwidth, and the rate of the amplitude outside the bandwidth presents 40 dB/dec. Moreover, its phase is above 0° and even close to 135° outside the control bandwidth. Fig. 18(b) shows the bode diagram of $Z_{dcr}(s)$ with the proposed method. Obviously, the magnitude of $Z_{dcr}(s)$ could remain unchanged inside the control bandwidth, and even turn to be constant outside the control bandwidth to remove the system damping attenuation. Meanwhile, the phase of $Z_{dcr}(s)$ could also remain above $-90°$, and almost close to 0°. Then, the negative resistance component of $Z_{dcr}(s)$ is completely removed during the maximum resonant frequency range, and the impedance of $Z_{dcr}(s)$ can be corrected to positive damping characteristic. Fig. 18(c) further shows the bode diagram of $Z_{out}(s)$ with the proposed method. By comparing Figs. 18(b) and 15(c), it is known that although a resonance peak band still exists in the $Z_{out}(s)$, but it is suppressed effectively. That means using virtual positive-damping reshaped impedance stability control method not only can adjust the $Z_{dcr}(s)$ to be positive during the maximum resonant frequency range, but also can remove the system damping attenuation, allowing the system damping and oscillation peak suppression to be improved.



(a)



(b)

Fig. 15. Contrastive bode diagrams of $Z_{\text{out}}(s)$ with different switching frequencies under traditional virtual-resistance stability control. (a) High switching frequency condition, $f_{\text{sw}} = 20$ kHz. (b) Low switching-frequency condition, $f_{\text{sw}} = 4$ kHz.

Moreover, Fig. 19 shows the amplitude of $Z_{\text{out}}(s)$ with the variation of C_{line} under the proposed control, $f_{\text{sw}} = 4$ kHz. Obviously, the positive damping characteristic of $Z_{\text{out}}(s)$ can be ensured, and the oscillation peak suppression effect can be guaranteed regardless of C_{line} variation. That means that the unstable area of the virtual-resistance stability control could be eliminated, and the robustness problem against C_{line} variation in the low switching-frequency condition could be well solved.

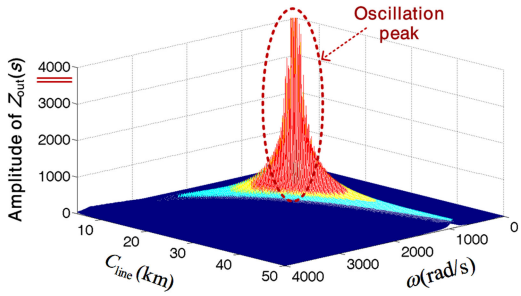


Fig. 16. Amplitude of $Z_{\text{out}}(s)$ with the variation of C_{line} under traditional virtual-resistance stability control, $f_{\text{sw}} = 4$ kHz.

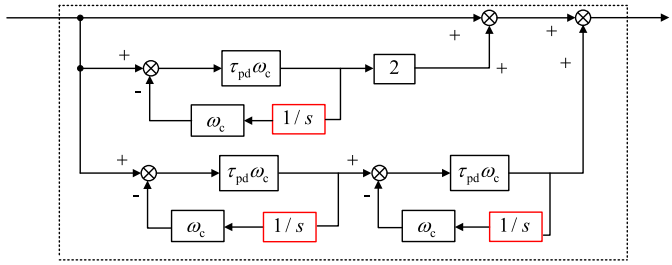


Fig. 17. Implementation diagram of $G_{\text{pd}}(s)$.

V. Experimental Results

To verify the validity of the proposed control method, the control hardware-in-the-loop experiments are carried out based on the DSP+FPGA control boards and the real-time digital simulation RT-LAB platform from OPAL-RT Technologies. The experimental parameters are shown in Table I and II. Its rectifier part is an IPOS system that contains five submodules with adopting NPC topology. The input of each submodule is isolated by a transformer, and its output voltage is set as 2 kV. The dc side voltage of the IPOS system can reach 10 kV since the outputs of submodules are connected in series. Among the dc-side capacitors of the submodule, eight are connected in series and three are in parallel, with a total capacitance of 176.25 μF. The proposed control method for each submodule is entirely implemented in the TI DSP TMS320F2812 and EP2C8Q208C-8N.FPGA control boards. The main power circuits are simulated by the RT-LAB OP5600 simulator and the simulation step is 20 μs. Because of the high-voltage and high-power level, f_{sw} is selected as 8 kHz. For advancing the phase of $G_{\text{pd}}(s)$ outside the control bandwidth, τ_{pd} is designed to be lower than the reciprocal of the bandwidth control and is set as 1. For avoiding the switching harmonics and white-noise amplification, the cutoff frequency ω_c is set as 2.52×10^4 rad/ s (πf_{sw}).

Figs. 20 and 21 show the contrastive dynamic experimental results under no damping and the proposed stability control method to verify its stability and dynamic performances, where C_{line} is 30 km. Fig. 20 shows that P increases from 50 to 100 kW, and Fig. 21 shows that P increases from 100 to 200 kW (full load), respectively.

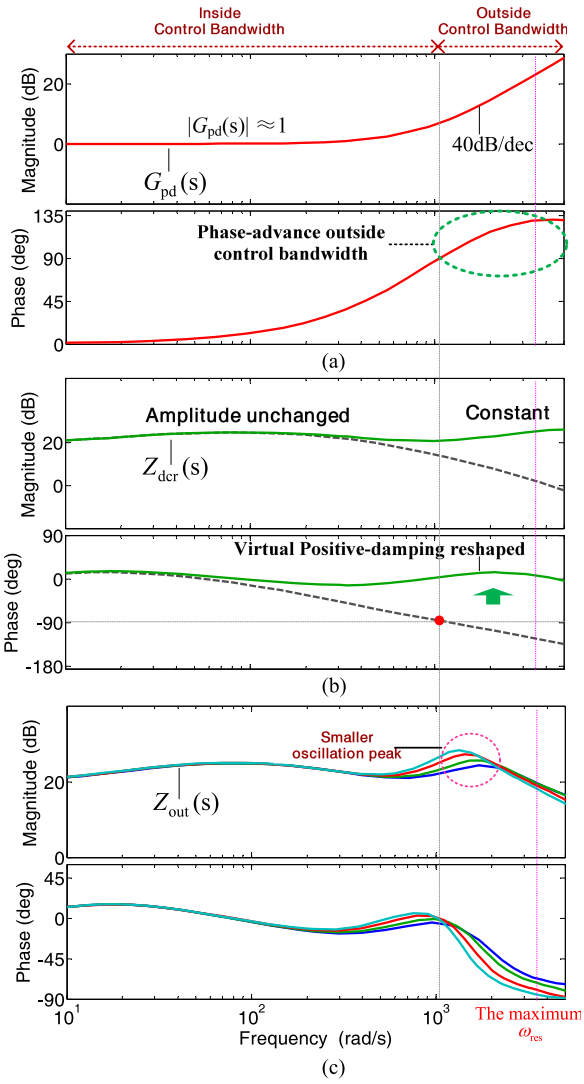


Fig. 18. Control performance of virtual positive-damping reshaped impedance stability control. (a) Bode diagram of G_{pd}. (b) Bode diagram of Z_{dcr}. (c) Bode diagram of Z_{out}.

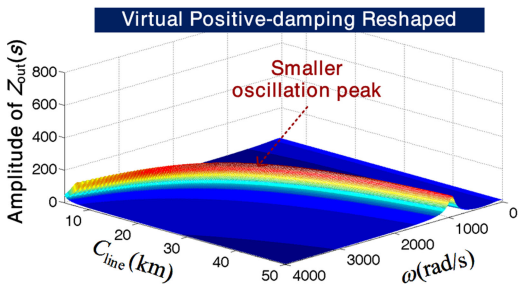


Fig. 19. Amplitude of $Z_{out}(s)$ with the variation of C_{line} under the proposed control, $f_{sw} = 4$ kHz.

Comparing Fig. 20(a) and (b), it reveals that the system dynamic performance under the proposed control method is consistent with that under no damping control, as the inverter-station output currents can achieve a smooth and fast transition after only one cycle in both cases. Hence, according to the contrastive dynamic experimental results, it is noted that the proposed

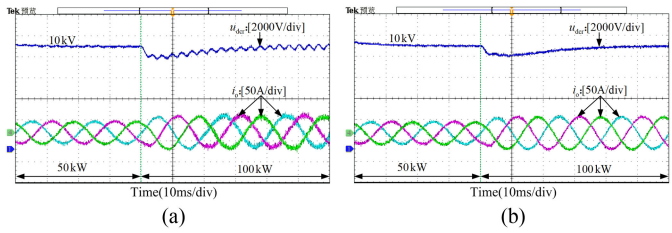


Fig. 20. Dynamic experimental results while P changes from 50 kW to 100 kW. (a) No damping control. (b) Proposed stability control method.

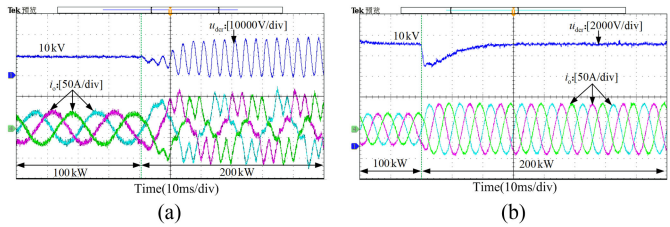


Fig. 21. Dynamic experimental results while P changes from 100 kW to 200 kW. (a) No damping control. (b) Proposed stability control method.

control method targeting the rectifier station cannot affect the load performance of the inverter station.

Moreover, as shown in Fig. 20(a), with no damping control, the system can remain stable with a small transmission power P, e.g., 50 kW, but a slight oscillation occurs in the dc-side output voltage during the transient process such as P increases from 50 to 100 kW, and then the output current of inverter station is also slightly deteriorated. Moreover, the offshore MVdc system could lose stability with a large transmission power P. As shown in Fig. 21(a), while the transmission power P is increased from the half-load 100 kW to full-load 200 kW, the dc-side output voltage of the rectifier station appears to oscillate immediately, leading to serious distortion in the output current of the inverter station and making stable system operation difficult. These experimental results prove that a larger transmission power yields a more unstable system.

As shown in Figs. 20(b) and 21(b), when the virtual positive-damping reshaped impedance stability control is implemented, the oscillation of the dc-side output voltage can be well suppressed, and then the quality of the inverter station output current is significantly improved. Hence, the system can maintain stable operation regardless of the changes in P.

Figs. 22 and 23 show the contrastive experimental results under only traditional virtual-resistance stability control and proposed stability control with different C_{line}, where P is 200 kW.

As shown in Fig. 22, with the implementation of the traditional virtual-resistance stability control, the system stability is significantly affected by C_{line}. As shown in Fig. 22(a), the waveform qualities of the rectifier-station dc-side output voltage and the inverter-station output current are both smooth when $C_{line} = 40$ km, because the dc-side oscillation frequency falls within the system control bandwidth due to the large C_{line}, indicating a large positive damping characteristic. However, when the dc-cable length is 15 km, as shown in Fig. 22(b), the dc-side voltage exhibits an obvious oscillation, and its

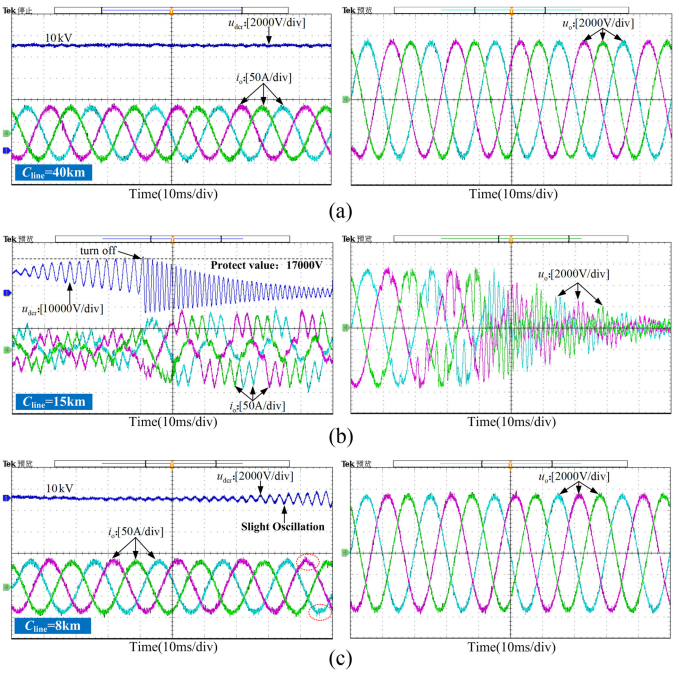


Fig. 22. Experimental results under the traditional stability control with different values of C_{line}, $f_{\text{sw}} = 8$ kHz. (a) $C_{\text{line}} = 40$ km. (b) $C_{\text{line}} = 15$ km. (c) $C_{\text{line}} = 8$ km.

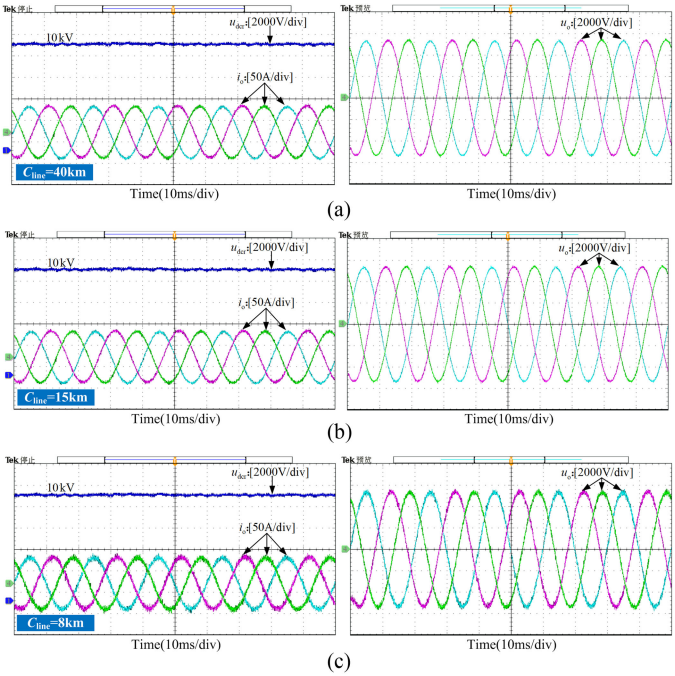


Fig. 23. Experimental results under the proposed stability method with different values of C_{line}, $f_{\text{sw}} = 8$ kHz. (a) $C_{\text{line}} = 40$ km. (b) $C_{\text{line}} = 15$ km. (c) $C_{\text{line}} = 8$ km.

oscillation amplitude increases continuously. Then, the overvoltage protection will be triggered, and the offshore MVdc would lose stability. Obviously, the experimental results are consistent with the previous analyses, and the reason is that the increasing oscillation frequency, resulting from the shorter dc cable length, has exceeded the narrow control bandwidth of rectifier station, and be located in the negative damping region. While the negative damping of the rectifier station is counteracted by the positive resistance of dc cable, the damper of total output impedance $Z_{\text{out}}(s)$ is approximately 0, and a larger oscillation peak appears and leads to the deterioration of system stability. Meanwhile, with the further reduction of the cable length, as shown in Fig. 22(c), while C_{line} is 8 km, the dc-side voltage oscillation can be suppressed to a certain degree compared with the case of $C_{\text{line}} = 15$ km. However, the oscillation suppression effect is not good, and the output current waveform has some deterioration since the damper is relatively small. Moreover, the dc-side voltage oscillations are clearly growing which indicates that the system will also remain unstable. Obviously, it is found that only traditional virtual-resistance stability control might fail to mitigate the dc-side oscillation and result in an unstable region, and its robustness against variations in the dc-side cable length is poor.

Fig. 23 shows the experimental results under the proposed virtual positive-damping reshaped impedance stability control method with different values of C_{line}. Although an oscillation frequency still exists in the dc-side voltage, but it is suppressed effectively regardless of the C_{line} variation. As shown in Fig. 23, the dc-side output voltage and inverter station output current can have good power quality regardless of the changes in the cable length, and the robustness problem against C_{line} variation in the low switching-frequency condition is well solved. That is because that using virtual positive-damping reshaped impedance stability control method not only can completely remove the negative resistance component of Z_{dcr} outside control bandwidth, but also can eliminate the system damper attenuation. Then, the system damper can maintain a large positive value regardless of the inside or outside control bandwidth, and the robustness problem against C_{line} variation can be well solved. Obviously, the proposed strategy enhances the oscillation suppression ability and also improves the robustness against the C_{line} variation.

VI. Conclusion

The offshore MVdc system supplying power to its special equipment can easily undergo high-frequency oscillation and even instability owing to the impedance mismatching. In this paper, a virtual positive-damping reshaped impedance stability control method is proposed to increase the offshore MVdc system stability. The small-signal dc impedance modeling of overall system is established with considering the IPOS structure, ac grid inductance, and dc cable effects. The oscillation mechanism is also analyzed via impedance-based Nyquist stability criterion. Some interesting conclusions are listed below.

1) The virtual-resistance stability control method introduced from low-voltage dc micro-grid application can mitigate its dc-side oscillation at a high switching frequency. But it fails to mitigate the dc-side oscillation and deteriorates the system stability at the low switching-frequency condition, because the large oscillation frequency, resulting from the high dc voltage and dc-cable length, can easily exceed the narrow control bandwidth of the rectifier station and fall

$$Z_{\rm out}(s)=\frac{2s^2+2s(\frac{R_{\rm cab}}{L_{\rm cab}}+\frac{2}{C_{\rm cab}R_{\rm v}})+\frac{4}{L_{\rm cab}C_{\rm cab}}+\frac{4R_{\rm cab}}{L_{\rm cab}C_{\rm cab}R_{\rm v}}}{(C_{\rm cab}+2C_{\rm dci})\left\{\underbrace{s^3+s^2(\frac{R_{\rm cab}}{L_{\rm cab}}+\frac{2}{C_{\rm cab}R_{\rm v}})+s[\omega_{\rm res}^2+\frac{2R_{\rm cab}}{L_{\rm cab}C_{\rm cab}R_{\rm v}}]+\frac{4}{L_{\rm cab}C_{\rm cab}R_{\rm v}(C_{\rm cab}+2C_{\rm dci})}}_{\Delta}\right\}} \tag{A2}$$

into its negative damping region. The robustness against the variations in the dc-cable length is poor.

2) The essential cause of the negative damping is that the ac-side filter inductance is transferred to the dc side and coupled with the dc-side energy storage capacitor, resulting in its phase falling to the range of $-90°\sim180°$ outside the control bandwidth.
3) The proposed strategy with phase advance is further presented to maintain a larger positive damper during the actual dc-side oscillation frequency range regardless of the variations in the dc-cable length, enhancing the system stability in the low switching frequency.

APPENDIX

To confirm that shaping $Z_{\rm dcr}$ can effectively enhance the dc-side damping and suppress the oscillation peak, the detailed mathematical relationship between the damping degree and $Z_{\rm dcr}$ is derived and analyzed in this part.

If the impedance $Z_{\rm dcr}$ is designed to be purely resistive $R_{\rm v}$

$$Z_{\rm dcr}=R_{\rm v}. \tag{A1}$$

Considering the effect of $Z_{\rm dcr}$ on $Z_{\rm out}$, the expression of $Z_{\rm out}$ is changed into (A2) shown at the top of this page according to Fig. 9

The above characteristic equation of $Z_{\rm out}(s)$ in (A2) can also be written as a zero-pole mode

$$\Delta=(C_{\rm cab}+2C_{\rm dci})(s+K_1\omega_{\rm n})(s^2+2\xi\omega_{\rm n}s+\omega_{\rm n}^2) \tag{A3}$$

where ξ is the damping factor of the conjugate poles; ω_n is the resonant angular frequency of the conjugate poles; K_1 is the ratio of the distance between the introduced poles and the imaginary axis to the distance between the complex conjugate poles and the imaginary axis.

We set

$$k=\omega_{\rm n}/\omega_{\rm res}. \tag{A4}$$

Then, the damping factor ξ is derived as

$$\xi=R_{\rm v}\cdot\left[2(1-k^2)(C_{\rm cab}+C_{\rm dci})\omega_{\rm res}+0.25R_{\rm cab}(C_{\rm cab}+2C_{\rm dci})k^2\omega_{\rm res}\right]. \tag{A5}$$

According to (A5), it is obviously noted that the damping factor ξ is clearly proportional to $Z_{\rm dcr}\,(R_{\rm v})$. Meanwhile, as shown in Fig. 24, the oscillation peak of $Z_{\rm out}$ decreases with the increase of $Z_{\rm dcr}\,(R_{\rm v})$, and its suppression ability is proportional to $Z_{\rm dcr}\,(R_{\rm v})$. If $Z_{\rm dcr}\,(R_{\rm v})$ is large, the amplitudes of $Z_{\rm out}$ and $Z_{\rm in}$ do not interact, and the system does not lose stability owing to the Nyquist stability criterion. In this case, the system can be returned to the stable point by adjusting $Z_{\rm dcr}$ to an appropriate resistance.

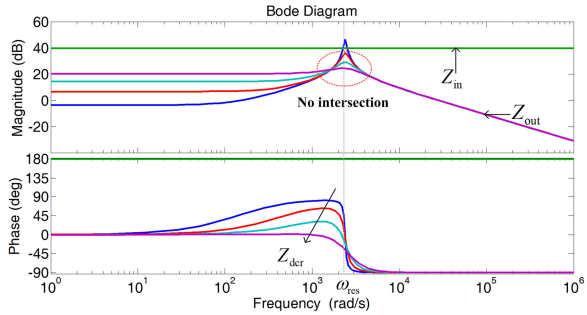


Fig. 24. Bode diagrams of $Z_{\rm out}$ and $Z_{\rm in}$ with the shaping $Z_{\rm dcr}$.

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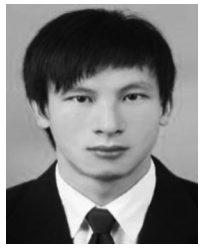

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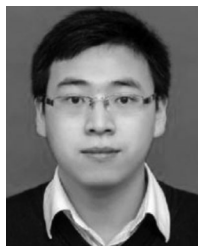

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