Principle and Robust Impedance-Based Design of Grid-tied Inverter with LLCL-Filter under Wide Variation of Grid-Reactance

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***Abstract*—Currently, how the inductive grid impedance variation affects the stability of digitally controlled grid-tied inverters with a high-order (*LCL* or *LLCL*) filter has been numerously studied. Note that a distributed power system may contain the capacitive load, the power factor correction (PFC) capacitor, and the long cable. During the design of grid-tied inverters, we should address the effects of the equivalent grid reactance, including both the inductive and the capacitive impedances, on the stability of system. Nevertheless, up to now, to the best knowledge of authors, the detailed parameter design method of the *LCL*- or *LLCL*-filter-based grid-tied inverter has not yet been introduced, when the capacitive grid impedance is addressed. In this paper, by using the passivity-based analysis, the detailed stability study on the *LLCL*-filter-based grid-tied inverter is carried out, when the grid reactance varies in a wide range. Based on the analysis, an exact and robust parameter design of system is proposed. Simulations and experimental results on a 220 V/2 kW prototype confirm that by using the proposed parameter design method, a high-performance grid-tied inverter system can be achieved under the rigid grid condition.**

***Index Terms*—Distributed power system, grid reactance variation, impedance-based, passivity, stability, time delay.**

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the capacitive grid impedance appears. Yoon *et al.* [27] assessed the system stability by using the impedance-based stability criterion, when a power factor correction (PFC) capacitor C_{PFC} is considered. However, how the variation of a PFC capacitor C_{PFC} influences the stability of system need be further explored. Song *et al.* [28] had analyzed the high-frequency resonance phenomenon of a doubly fed induction generator (DFIG) system, under the network impedance of series *RL* and shunt capacitors. However, the detailed stability solution was not proposed. In [29], Bai *et al.* had considered the existence of a PFC capacitor and proposed a method to cancel the nonpassive regions by using voltage-source inverters with different power filters, sampling frequencies, and control strategies. Nevertheless, this method may also turn invalid in a distributed power system only with identical grid-tied inverters.

Further on, it should be pointed out that the passivity-based analysis was only considered within the Nyquist frequency in [26]–[29]. However, according to [31], the instability of the grid-tied inverter maybe appears in the frequency range between the Nyquist frequency and the switching frequency. Meanwhile, to the best knowledge of authors, the parameter design of *LCL* or *LLCL* filter has not yet been introduced so far, when the capacitive grid impedance is addressed.

In this paper, the passivity-based analysis is extended up to the switching frequency, where two nonpassive regions will be figured out. Once the inverter output admittance intersects with the grid admittance within the two nonpassive regions, the whole system may become unstable. Based on the analysis, an exact and robust parameter design for the *LLCL* filter together with the electromagnetic interference (EMI) capacitor is proposed to ensure the stability of whole system, considering the wide variation of grid reactance. Note that the design can be also applied to the *LCL*-filter-based grid-tied inverter, where the trap inductor of the *LLCL* filter is just set zero.

The rest of this paper is organized as follows. Section II presents the modeling of the *LLCL*-filter-based grid-tied inverter. Section III is devoted to the stability analysis of the *LLCL*-filter-based grid-tied inverter, under a wide-range variation of grid reactance. Section IV introduces the proposed measures and a step-by-step design procedure. A design example is illustrated in Section V. Simulations and measured results are presented to verify the proposed design method in Sections VI and VII. Conclusions are finally drawn in Section VIII.

II. MODELING OF *LLCL*-TYPE GRID-TIED INVERTER

A. System Description

Fig. 1 shows a single *LLCL*-filter-based grid-tied inverter connected to the ideal grid via the equivalent reactances of C_g and L_g. (L_1, L_2, C_f, L_f) and (L_g, C_g) are the parameters of the filter and the grid reactance, respectively.

The plant-equivalent block diagram is shown in Fig. 2, together with impedances of Z_1, Z_{LC}, and Z_2 for L_1, L_f C_f trap, and L_2, respectively. Meanwhile, $G_c(s)$ is a current controller, $G_d(s)$ is the total delay time, and $G_{\text{inv}} = U_{\text{dc}}/U_{\text{tri}}$ is the gain of inverter, where U_{dc} is the dc voltage and U_{tri} is the amplitude value of the triangle carrier.

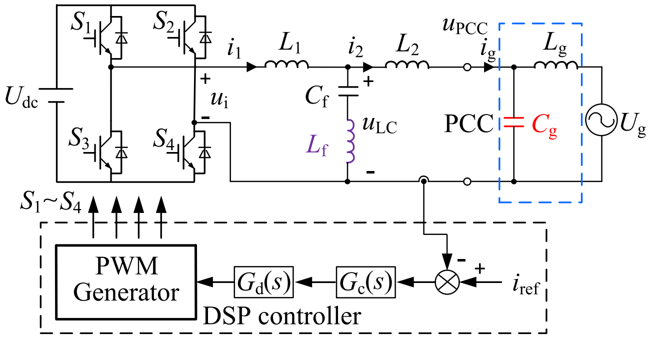

Fig. 1. Single *LLCL*-filter-based grid-tied inverter connected to the ideal grid via the equivalent reactances of C_g and L_g.

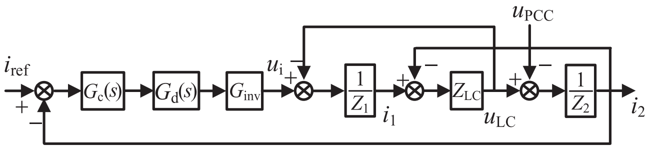

Fig. 2. Block diagram of the grid-tied inverter with a single-loop grid-injected current control.

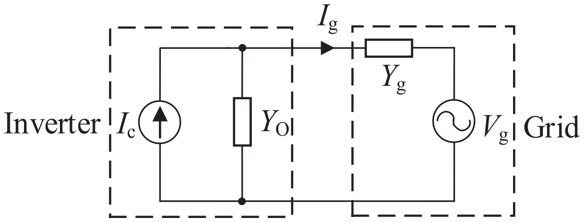

Fig. 3. Norton equivalent model of the *LLCL*-filter-based grid-tied inverter with the grid-injected current feedback control.

The proportional resonant (PR) and harmonic compensator (HC) controller is adopted as the current controller in this paper, while the transfer function of $G_c(s)$ is

$$G_c(s) = K_p + \sum_{h=1,3,5,7,9,\ldots} \frac{K_{ih}s}{s^2 + (\omega_0 h)^2} \tag{1}$$

where $\omega_o\,(= 2\pi f_o)$ is the fundamental angular frequency and K_p and K_{ih} are the proportional and resonant gains, respectively.

The total delay time $G_d(s)$, including the computational delay and the modulation delay, is commonly expressed as

$$G_d(s) = \frac{\sin\frac{\omega T_s}{2}}{\frac{\omega T_s}{2}} e^{-\lambda T_s s} \tag{2}$$

where $T_s = 1/f_s$ is the sampling period and λ is the delay time normalized with T_s. The normal value of λ is selected as 1 or 1.5 in a real operation [32].

B. Norton Equivalent Model

Fig. 3 shows the Norton equivalent model of the *LLCL*-filter-based grid-tied inverter with the grid-injected current feedback control, where the inverter output admittance can be obtained as (3) shown at the bottom of the next page.

Besides, the grid admittance and its resonance frequency can be respectively expressed as

$$Y_g(s) = \frac{s^2 L_g C_g + 1}{s L_g} \tag{4}$$

$$f_g = \frac{1}{2\pi\sqrt{C_g L_g}}. \tag{5}$$

III. STABILITY ANALYSIS CONSIDERING THE GRID-REACTANCE VARIATION

A. Nonpassive Regions of the Inverter Output Admittance

To be passive, a linear continuous system $G(s)$ must satisfy the following two requirements at frequency ω [31]:

1) $G(s)$ has no right-half-plane (RHP) poles.
2) $\mathrm{Re}\,[G\,(j\omega)] \geq 0 \leftrightarrow \arg\,[G\,(j\omega)] \in [-90°, 90°]\ \forall\ \omega > 0$.

Then, the passivity violation can be identified by inspecting the negative real part of inverter output admittance. The real part of (3) is calculated as (6) shown at the bottom of this page, where A and B are defined as follows:

$$A = K_p G_{\text{inv}} (1 - C_f L_f \omega^2) \frac{\sin \frac{\omega T_s}{2}}{\frac{\omega T_s}{2}} \cos\,(\lambda T_s \omega)$$

$$B = (L_1 + L_2)\omega - C_f(L_1 L_2 + L_1 L_f + L_2 L_f)\omega^3$$
$$- K_p G_{\text{inv}} (1 - C_f L_f \omega^2) \frac{\sin \frac{\omega T_s}{2}}{\frac{\omega T_s}{2}} \sin\,(\lambda T_s \omega).$$

Within the switching frequency of ω_s, the term of $(1 - C_f L_f \omega^2)$ will be always positive. Meanwhile, the denominator of (6) is also always positive. Note that K_p, G_{inv} and $\sin(\omega T_s/2)/(\omega T_s/2)$ are also always positive; therefore, the polarity of $\mathrm{Re}\,[Y_{\mathrm{o}}(j\omega)]$ depends on the term of $[1 - C_f(L_1 + L_f)]\omega^2$ and the cosine term.

When $[1 - C_f(L_1 + L_f)]\omega^2 = 0$, the resonant frequency f_p can be calculated as

$$f_p = \frac{1}{2\pi\sqrt{C_f(L_1 + L_f)}}. \tag{7}$$

For the cosine term, f_{d1} and f_{d2} are both critical frequencies, which are defined in (8), respectively

$$\begin{cases} f_{\mathrm{d}1} = \frac{f_s}{4\lambda} \\ f_{\mathrm{d}2} = \frac{3f_s}{4\lambda}. \end{cases} \tag{8}$$

The plots of $\cos\,(\lambda T_s \omega)$ and $[1 - C_f(L_1 + L_f)]\omega^2$, together with their combined polarities, are shown in Fig. 4, where the term of $[1 - C_f(L_1 + L_f)]\omega^2$ is drawn for three frequency cases of f_p. It can be seen that the region $[f_{d2},\ f_s]$ is always nonpassive. When f_p is smaller than f_{d1}, the nonpassive region $[f_p,\ f_{d1}]$ appears. And the nonpassive region $[f_{d1},\ f_p]$ also appears when f_p is larger than f_{d1}. Note that, within f_{d2}, as long as f_{d1} is equal to f_p, the first nonpassive region disappears.

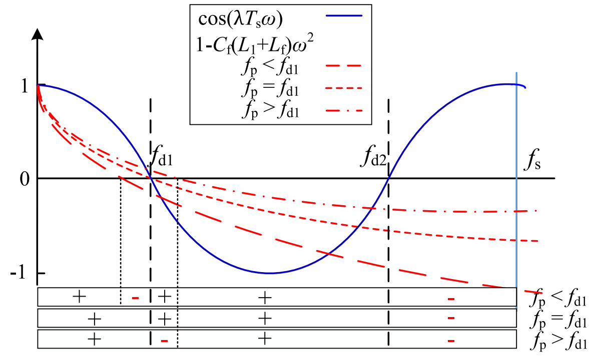

Fig. 4. Nonpassive regions of the inverter output admittance.

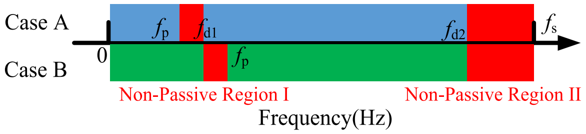

Fig. 5. Summarized nonpassive regions.

According to the aforementioned analysis, the nonpassive regions with two different cases (Case A: $f_p < f_{d1}$, Case B: $f_p > f_{d1}$) are summarized in Fig. 5. The nonpassive region of $[f_p,\ f_{d1}]$ in Case A or $[f_{d1},\ f_p]$ in Case B is defined as the Nonpassive Region I (NPR_I), while $[f_{d2}, f_s]$ is defined as the Nonpassive Region II (NPR_II).

B. Possible Instability Under the Wide Variation of Grid Reactance

In fact, the real distributed grid inductance and capacitance are unknown and may vary in a wide range, which causes the wide variation of f_g. Therefore, the intersection of the grid admittance and the inverter output admittance, which may also vary in a wide range and locate in NPR_I or NPR_II. Once the absolute value of the phase difference at the intersection is beyond 180°, the system will become unstable according to the impedance-based stability criterion [33]–[35]. Take Case A as an example; Fig. 6 shows the Bode plots of the inverter output admittance and the grid admittance with two different f_g values, where the system appears unstable.

Based on the earlier analysis, it can be deduced that in order to stabilize the grid-tied inverter under the wide variation of grid reactance, the following are the two basic strategies:

$$Y_O(s) = \frac{s^2 C_f L_f + 1}{s^3 C_f(L_1 L_2 + L_1 L_f + L_2 L_f) + s^2 K_p G_{\text{inv}} C_f L_f \frac{\sin \frac{\omega T_s}{2}}{\frac{\omega T_s}{2}} e^{-\lambda T_s S} + s(L_1 + L_2) + K_p G_{\text{inv}} \frac{\sin \frac{\omega T_s}{2}}{\frac{\omega T_s}{2}} e^{-\lambda T_s S}} \tag{3}$$

$$\mathrm{Re}[Y_O(j\omega)] = \frac{K_P G_{\text{inv}} [1 - C_f(L_1 + L_f)\omega^2](1 - C_f L_f \omega^2) \frac{\sin \frac{\omega T_s}{2}}{\frac{\omega T_s}{2}} \cos\,(\lambda T_s \omega)}{A^2 + B^2} \tag{6}$$

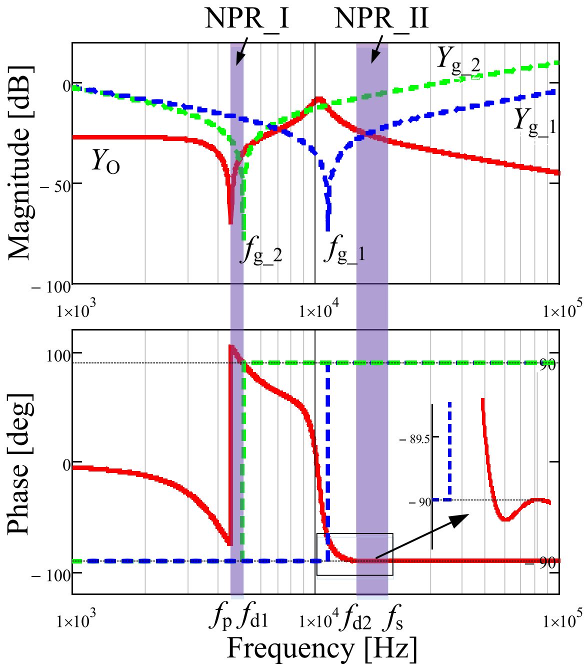

Fig. 6. Bode plots of the inverter output admittance and the grid admittance with two different f_g values.

1) Minimize the nonpassive regions as much as possible, which is preferentially recommended.
2) Avoid the intersection of the inverter output admittance and grid admittance falling in the nonpassive regions of the grid-tied inverter.

IV. PROPOSED MEASURES AND DESIGN PROCEDURE UNDER GRID-REACTANCE VARIATION

A. *Proposed Measures Against Grid-Reactance Variation*

As shown in Fig. 5, if $f_p = f_{d1}$, NPR_I can be eliminated. However, it cannot be always guaranteed, because f_p is dependent on the parameters (L_1, C_f, L_f) of the filter, which may shift in the actual application.

Also, as shown in Fig. 6, when f_g is high enough, the intersection of the grid admittance and the inverter output admittance will possible fall in NPR_II. In order to avoid the intersection falling into NPR_II, the minimum value of L_gC_g should be set. In fact, to improve the EMI noise suppressing performance of the high-order-filter-based grid-tied inverter, a parallel capacitance C_{EMI} is generally needed [36]–[38], which can guarantee the lower limit value of grid capacitance C_g.

Therefore, the measures to enhance the stability of the presented grid-tied inverter system against grid-reactance variation are proposed as follows:

1) According to regulating the resonant parameters based on (7), set $f_p = f_{d1}$ to eliminate NPR_I.
2) Select the minimum capacitance $C_{g\text{-}\min}$ to limit the intersection of grid reactance and the inverter output admittance under the stiffest grid condition, so that the intersection will never fall in NPR_II.

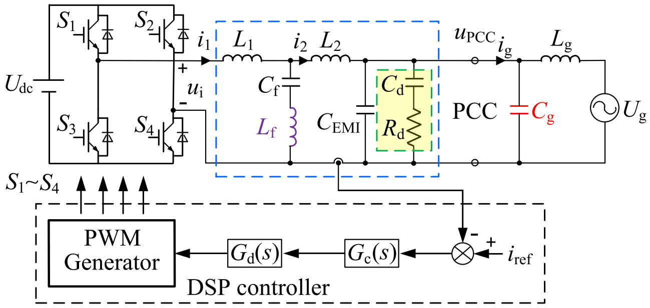

Fig. 7. Proposed filter structure for the grid-tied inverter.

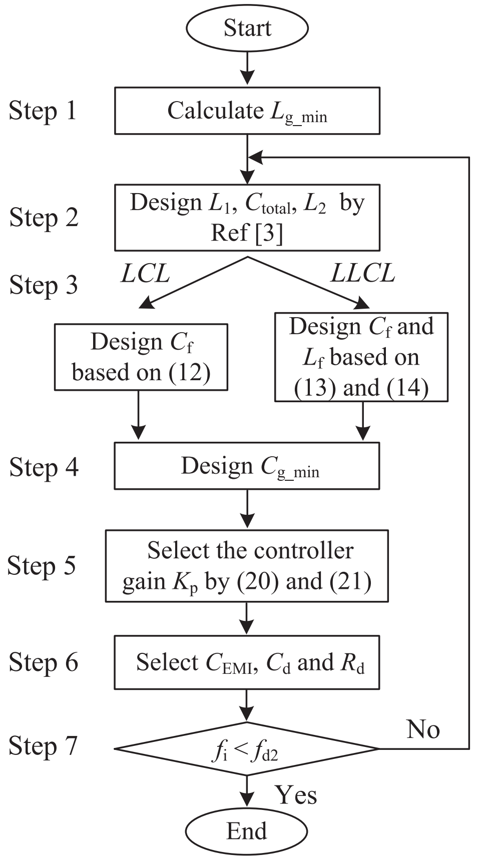

Fig. 8. Proposed design flowchart.

3) Add an *RC* damper to reshape grid admittance and ensure the system stability, when the original intersection locates in NPR_I due to the parameter drifting of the filter.

According to the aforementioned measures, Fig. 7 shows the proposed filter structure for the grid-tied inverter, where C_{EMI}, R_d, and C_d are the EMI capacitor of C_{EMI}, the damping resistor, and the capacitor, respectively.

B. *Design Procedure*

The single-loop current control design contains the following seven steps, where the design flowchart is shown in Fig. 8.

Step 1: Calculate the Minimum Grid Inductance $L_{g\text{-}\min}$.

In actual, the real grid inductance consists of the transformer leakage inductance L_{leak} and the power line inductance L_{line}.

Considering *x* as the short-circuit inductance, L_{leak} can be calculated as

$$L_{\text{leak}} = x\frac{U_g^2}{\omega_0 P} \tag{9}$$

where *x* is generally between 4% and 7%, U_g is the grid fundamental root-mean-square voltage, ω_0 is the fundamental frequency in radians per second, and *P* is the rated capacity of transformer.

Considering the minimum grid inductance, L_{line} is neglected and $L_{g\_\min} = L_{\text{leak}}$.

Step 2: Design L_1, C_{total}, and L_2.

The *LCL* or *LLCL* filter designs have been introduced in [3], and the design principle for the inductors L_1 and L_2 is not changed.

1) Select the tolerable current ripple on the converter side → design of the converter-side inductor L_1

$$15\% \leq \frac{\Delta I_1}{I_{\text{ref}}} = \frac{1}{8}\frac{2U_{\text{dc}}}{L_1 f_s I_{\text{ref}}} \leq 40\% \tag{10}$$

where ΔI_1 is the converter-side current ripple and I_{ref} is the rated reference peak current.

2) Select the reactive power absorbed in the rated condition → total capacitance C_{total}. Considering *y* as the percentage of the reactive power absorbed in rated condition

$$C_{\text{total}} = C_f + C_{g\_\min} \leq \frac{5\% P_{\text{rated}}}{U_g^2 \omega_0} \tag{11}$$

where P_{rated} is the rated generated power.

3) Note that if L_f of *LLCL* filter is just set to zero, then the traditional *LCL* filter will be obtained. For an *LCL* filter, L_2 mainly depends on the objective to attenuate each harmonic around the switching frequency down to 0.3%, which is in accordance to the IEEE Standard 519-2014.

For an *LLCL* filter, owing to the $L_f - C_f$ trap, the current harmonics around the switching frequency satisfy the requirements of IEEE Standard 519-2014 with far more ease. Therefore, L_2 is designed to attenuate harmonics around the second integer multiple of the switching frequency to be lesser than 0.3%.

Step 3: Design the Bypass Filtering Branch.

For an *LCL* filter, the capacitor C_{f_LCL} can be calculated in (12) according to $f_p = f_{d1}$ $(L_f = 0)$

$$C_{f\_LCL} = \frac{16\lambda^2}{L_1 (2\pi f_s)^2}. \tag{12}$$

For an *LLCL* filter, the resonant capacitor C_{f_LLCL} can be calculated in (13) according to $f_p = f_{d1}$. As a result, the resonant inductor L_f can be selected at the converter switching frequency of f_s, according to (14). But the series trap is also influenced by its quality factor *Q* expressed in (15), where R_f represents the gapped equivalent resistance of the inductor L_f. The value of *Q* should be considered between the usual range of $10 \leq Q \leq 50$ [3]

$$C_{f\_LLCL} = \frac{16\lambda^2 - 1}{L_1 (2\pi f_s)^2} \tag{13}$$

$$L_f = \frac{1}{C_{f\_LLCL} (2\pi f_s)^2} \tag{14}$$

$$Q = \frac{1}{R_f}\sqrt{\frac{L_f}{C_f}}. \tag{15}$$

Step 4: Design the Minimum Grid Capacitance $C_{\text{g\_min}}$.

There may be very small value of C_g in the actual power grid, resulting in that the mentioned intersection falls in NPR_II, as shown in Fig. 5. Therefore, the minimum grid capacitance $C_{g\_\min}$ should be chosen to guarantee the lower limit value of grid capacitance so that the variation range of the grid reactance is reduced. Then, $C_{g\_\min}$ can be selected as follows:

$$C_{g\_\min} = C_{\text{total}} - C_f. \tag{16}$$

Step 5: Design the Proportional Gain K_P of the PR + HC Regulator.

From Fig. 1, the open-loop transfer function of the proposed system can be written as

$$\begin{aligned} G_{ol}(s) &= G_c(s) G_d(s) G_{\text{inv}} G_{\text{filter}}(s) \\ &= \frac{1}{C_g L_g C_f L_f}\frac{(s^2+\omega_g^2)(s^2+\omega_f^2)}{s(as^4+bs^2+c)} G_c(s) G_d(s) G_{\text{inv}} \end{aligned} \tag{17}$$

where $G_{\text{filter}}(s)$ is the transfer function of the grid-injected current i_2 versus the output voltage u_i of the inverter, and *a*, *b*, c are defined as follows:

$$a = C_g L_g (C_f L_1 L_2 + C_f L_f L_1 + C_g L_f L_2)$$

$$b = C_f L_1 (L_2 + L_f + L_g) + C_f L_f (L_2 + L_g) + C_g L_g (L_1 + L_2)$$

$$c = L_1 + L_2 + L_g.$$

The current controller G_c(s) is usually simplified as K_P, since the resonance terms have a negligible influence on system stability, if the maximum control bandwidth is well set. Then, the gain margin and the phase margin of the system can be calculated as

$$\text{GM} = -20\log\left|K_P G_{\text{inv}} G_{\text{filter}}(j\omega)\right|\Big|_{\omega = 2\pi f_{d1}} \tag{18}$$

$$\text{PM} = 180^\circ + \left(\angle G_{\text{filter}}(j\omega) - \frac{360}{2\pi}\lambda T_s \omega\right)\Bigg|_{\omega = 2\pi f_c} \tag{19}$$

where f_c is the crossover frequency of the system.

The minimum crossover frequency of the system is generally set higher than the highest harmonic compensator frequency under the weakest grid condition of maximum equivalent grid inductance and maximum real grid capacitance. Then, the minimum control gain can be calculated as

$$K_{P\_min} = \frac{1}{G_{\text{inv}} G_{\text{filter}}(j\omega)}\Bigg|_{\omega = 2\pi f_{\text{cweak}}} \tag{20}$$

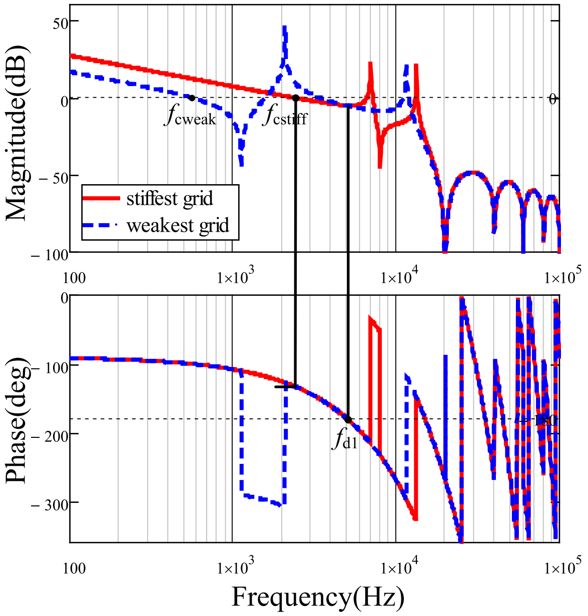

Fig. 9. Bode plots of the system under the stiffest grid condition with $C_{g\_\min}$ and the weakest grid condition with the maximum grid capacitance.

where $f_{\rm cweak}$ is the minimum crossover frequency.

At the same time, in order to ensure a sufficient stability margin for the entire system, the maximum control gain should be chosen using the following equation:

$$K_{P\_\max} = \min(K_{P\_{\rm stiff}1}, K_{P\_{\rm stiff}2}) \tag{21}$$

where $K_{P\_{\rm stiff}1}$, $K_{P\_{\rm stiff}2}$ are the controller gains, which are determined by GM = 3 dB and PM = 30° according to (18) and (19), respectively, under the stiffest grid condition of real grid inductance and minimum real capacitance $C_{g\_\min}$, as shown in Fig. 9. If $K_{P\_\max}$ is smaller than $K_{P\_\min}$, it is necessary to cut down the desired control bandwidth until there is a proper value range.

Step 6: Select $C_{\rm EMI}$, $C_{\rm d}$, and $R_{\rm d}$.

Although f_p has been equal to f_{d1}, NPR_I still appears when the filter parameters drift. Once the intersection locates in NPR_I and the absolute value of the phase difference is beyond 180°, the whole system will become unstable. In order to guarantee the stability of the whole system, a novel *RC* damper designed to reshape grid admittance is first proposed, which is shown in Fig. 7, aiming at that the phase difference of the inverter output admittance Y_o and the damped grid admittance Y_{grc} is limited between (−180°, 180°).

The damping capacitor C_d can be split from $C_{g\_\min}$, and the rest of $C_{g\_\min}$ is used as $C_{\rm EMI}$. To balance the damping effect and the damping losses, an equal value of $C_{\rm EMI}$ and C_d may be a proper selection [11]. Then, $C_{\rm EMI}$ and C_d can be selected as follows:

$$C_{\rm EMI} = C_d = \frac{C_{g\_\min}}{2}. \tag{22}$$

No matter [f_p, f_{d1}] or [f_{d1}, f_p], the phase difference of the inverter output admittance and the grid admittance is largest, when f_g is close to f_p. The *RC* damper can enlarge the intersection frequency and reduce the phase difference well. Therefore, the damping resistor value is selected by the equivalent *Q*-factor method [12], which can be represented as

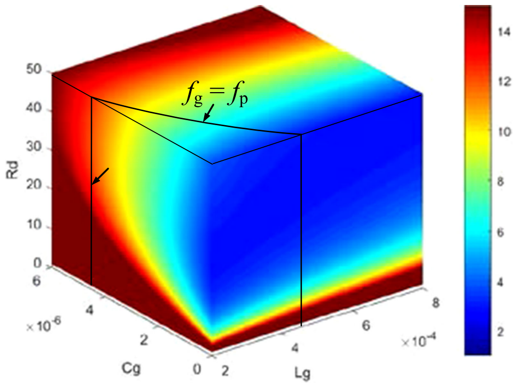

Fig. 10. Relationship between the *Q*-factor, the damper resistor, the grid inductance, and the grid capacitance for the damped grid admittance.

$$Q_E = \frac{1}{R_E}\sqrt{\frac{L_E}{C_E}} \tag{23}$$

where Q_E is the equivalent *Q*-factor, and R_E, L_E, and C_E are the equivalent resistance, inductance, and capacitance of the equivalent series *LCR* circuit, respectively.

As shown in Fig. 7, the equivalent resistance R_E and capacitance C_E of the grid capacitance, $C_{\rm EMI}$, and the *RC* parallel damper can be calculated as

$$\begin{aligned}&\left.\frac{1}{s(C_{\rm EMI}+C_g)}//\left(\frac{1}{sC_d}+R_d\right)\right|_{s=j\omega}\\ &= \left.\frac{R_{\rm d}C_{\rm d}s+1}{R_dC_d(C_{\rm EMI}+C_g)s^2+(C_d+C_{\rm EMI}+C_g)s}\right|_{s=j\omega}\\ &= R_E+\frac{1}{sC_E}.\end{aligned} \tag{24}$$

Then, at the dominant resonance frequency, the equivalent resistance R_E, the inductance L_E, and capacitance C_E of the equivalent *LCR* circuit can be calculated as

$$\begin{aligned}R_E &= \left.\frac{R_dC_d^2}{(C_d+C_{\rm EMI}+C_g)^2-(R_dC_d(C_{\rm EMI}+C_g)s)^2}\right|_{s=j2\pi f_{\rm res}}\\ L_E &= L_g\\ C_E &= \left.\frac{(R_dC_d(C_{\rm EMI}+C_g)s)^2-(C_d+C_{\rm EMI}+C_g)^2}{R_d^2C_d^2(C_{\rm EMI}+C_g)s^2-(C_d+C_{\rm EMI}+C_g)}\right|_{s=j2\pi f_{\rm res}}.\end{aligned} \tag{25}$$

Substituting (25) into (23), the *Q*-factor at the dominant resonance frequency can be calculated. Therefore, *Q*-factor as a function of the damping resistor and the grid inductance and capacitance can be plotted in Fig. 10.

As shown in Fig. 10, the *Q*-factor will become large while R_d decreases and C_g and L_g increase. Therefore, R_d is selected to aim at the optimal *Q*-factor under the condition of $f_g = f_p$. Note that in the reasonable range, the larger value of R_d, the more damping power loss.

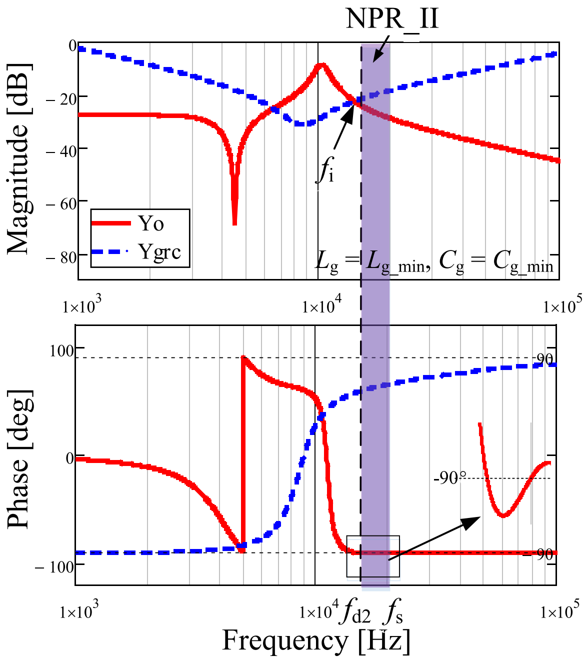

Fig. 11. Bode plots of the inverter output admittance and the damped grid admittance under the stiffest grid condition with $C_{g\_\min}$.

The damped grid admittance is expressed as

$$Y_{grc}(s) = \frac{s^3 L_g C_g R_d C_d + s^2 L_g (C_g + C_d) + s R_d C_d + 1}{s^2 L_g R_d C_d + s L_g}. \tag{26}$$

Finally, the Bode plots of the inverter output admittance and the damped grid admittance are plotted to verify the phase difference whether to satisfy below 180° when $f_g = f_p$.

Step 7: Check $f_i < f_{d2}$.

After the aforementioned six steps, it is necessary to verify whether the maximum frequency f_i of the intersection locates in NPR_II under the stiffest grid condition with $C_{g\_\min}$, as shown in Fig. 11. It is not easy to directly solve the exact value of f_i. Therefore, a simple engineering method is developed here. Under the condition of $L_g = L_{g\_\min}$ and $C_g = C_{g\_\min}$, if the magnitude of the inverter output admittance is smaller than that of the damped grid admittance at f_{d2}, then f_i is smaller than f_{d2}, and the system will be stable. The magnitude difference of the inverter output admittance and the damped grid admittance is defined as

$$\left.\Delta Y(f, L_g, C_g)\right|_{\substack{L_g = L_{g\_\min},\\ C_g = C_{g\_\min},\\ f = f_{d2}}} = Y_{Oa}(f) - Y_{grca}(f, L_g, C_g) \tag{27}$$

where $Y_{Oa}(f)$ and $Y_{grca}(f, L_g, C_g)$ are the magnitudes of $Y_O(s)$ and $Y_{grc}(s)$, respectively.

If

$$\left.\Delta Y(f, L_g, C_g)\right|_{\substack{L_g = L_{g\_\min},\\ C_g = C_{g\_\min},\\ f = f_{d2}}}$$

is smaller than zero, f_i is not in NPR_II. Then, the design procedure ends. Otherwise, it needs to return *Step 2* to reselect parameters.

V. DESIGN EXAMPLE

Assume that there is a 40-kW system, which consists of 20 sets of 2-kW, 220-V/50-Hz inverters. In order to illustrate the proposed parameter design for the grid-tied inverter under the wide variation of grid reactance, an example of a 2-kW, 220-V/50-Hz *LLCL*-filter-based system is designed step by step according to the procedure introduced in Section IV, where the parameters are shown as $f_s = 20$ kHz, $U_{\mathrm{dc}} = 350$ V, $U_{\mathrm{tri}} = 0.25$ V, and an 11th harmonic compensator is desired.

The systematic design procedure is shown as follows:

1) $P = 40$ kW, $x = 5.2\%$, L_{leak} is calculated as 0.2 mH according to (9). Then, $L_{g\_\min}$ is equal to 0.2 mH.
2) Adopting the 30% current ripple for the converter-side inductor L_1, and L_1 is selected to be 1.2 mH. The total capacitor value C_{total} is designed as 2.8 μF to limit the reactive power to 2.36%. If some of the constraints cannot be met, it should be increased until the limit of 5%. L_2 is designed as 0.22 mH to attenuate harmonics around the second integer multiple of the switching frequency to be less than 0.3%.
3) For $\lambda = 1$, the resonant capacitor C_f can be calculated as 0.8 μF by using (13). The resonant inductor L_f is selected as 80 μH by using (14). Series resistor $R_{\mathrm{f}} = 0.2\ \Omega$ and quality factor Q is calculated to 50 by (15).
4) $C_{g\_\min}$ is selected as 2 μF according to (16).
5) Considering the maximum real grid capacitance $C_{\mathrm{g}} = 60\ \mu$F, the real grid inductance is 0.2 mH under the stiffest grid condition, while the equivalent grid capacitance and inductance, respectively, become 3 μF and 4 mH under the weakest grid condition, if there are 20 inverters in parallel. If the minimum crossover frequency of the system f_{cweak} is set to 550 Hz, $K_{P\_\min}$ can be calculated as 0.016 using (20). Under the stiffest grid condition with $C_{g\_\min}$, if GM = 3 dB, K_{P_stiff1} can be calculated as 0.019 using (19), and if PM = 30°, K_{P_stiff2} can be calculated as 0.022 using (18). Finally, the controller gain of K_P is selected as 0.017, whereas K_{ih} is then set to 18.2.
6) The C_{EMI} and C_d are both chosen as 1 μF according to (22). When C_f drifts +5%, L_1 and L_f drift +25%, the value of f_p becomes 4.34 kHz. In order to ensure the Q-factor less than 12 when $L_{\mathrm{g}} = 0.2$ mH and $C_{\mathrm{g}} = 4.5\ \mu$F, R_d selected as 25 Ω according to Fig. 10. Then, in order to verify the phase difference whether to satisfy below 180° nearby f_p, the Bode plots of the inverter output admittance and the damped grid admittance are shown in Fig. 12. It can be seen that the damped grid admittance does not interact with the inverter output admittance in NPR_I.
7) The value of

$$\left.\Delta Y(f, L_g, C_g)\right|_{\substack{L_g = L_{g\_\min},\\ C_g = C_{g\_\min},\\ f = f_{d2}}}$$

And the magnitude difference of the inverter output admittance and the damped grid admittance is negative. Therefore, the design procedure ends.

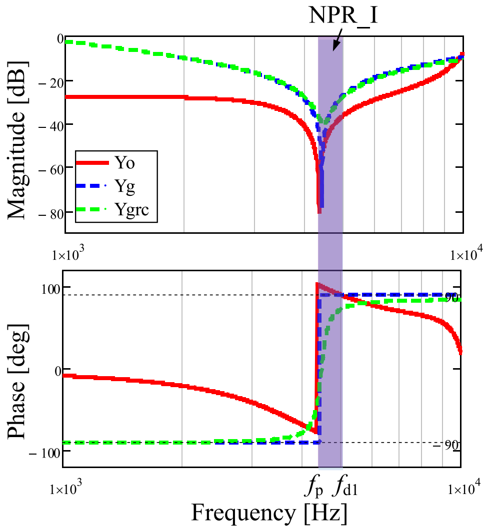

Fig. 12. Bode plots of the inverter output admittance and the damped grid admittance when $L_g = 0.2$ mH and $C_g = 4.5\ \mu$F.

TABLE I
DESIGNED PARAMETERS OF CONVERTER

Parameter	Symbol	Value
Inverter-side inductor	L_1	1.2 mH
Parasitic resistance	R_{L1}	0.1 Ω
Resonant inductor	L_f	80 μH
Series resistance	R_f	0.2 Ω
Resonant capacitor	C_f	0.8 μF
Grid-side inductor	L_2	0.22 mH
Parasitic resistance	R_{L2}	0.01 Ω
Gain of inverter	G_{inv}	1400
Proportional gain	K_P	0.017
Resonant gain	K_{ih}	18.2
Delay time coefficient	λ	1
Switching frequency	f_s	20 kHz
Resonance frequency	f_p	5 kHz
Minimum Grid capacitor	C_{g_min}	2 μF
Critical frequency	f_{d1}	5 kHz
	f_{d2}	15 kHz
Minimum Crossover Frequency	f_{cweak}	550 Hz
Capacitor for suppressing the EMI noise	C_{EMI}	1 μF
Grid impedance shaping resistor	R_d	25 Ω
Grid impedance shaping Capacitor	C_d	1 μF

Finally, the designed parameters of the converter are listed in Table I.

VI. SIMULATION

In order to confirm the effectiveness of proposed measures, simulations are carried out with the PSIM software. The designed converter parameters have been shown in Table I, then the calculated nonpassive region NPR_II is [15, 20] kHz. The four contradistinctive cases of grid parameters used for simulation are also shown in Table II. Among them, Case 1 and Case 2 are designed under the normal operation, while Case 3 and Case 4 are designed when filter parameters drift.

TABLE II
GRID PARAMETERS

Condition	Normal operation		Parameter drifting	
Parameter	Case 1	Case 2	Case 3	Case 4
L_g	0.3 mH	0.3 mH	0.51 mH	0.51 mH
R_g	0.06Ω	0.06Ω	0.1Ω	0.1Ω
C_g	1 μF	1 μF	1 μF	1 μF
C_{EMI}		1 μF	1 μF	1 μF
R_d				25 Ω
C_d				1 μF

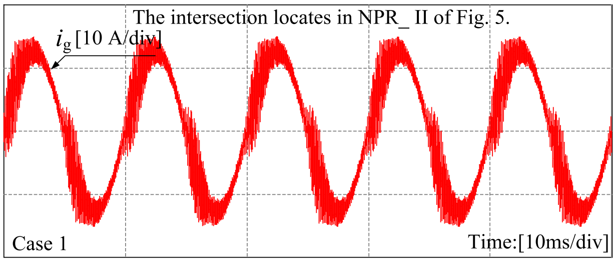

Fig. 13. Simulated grid-injected current of the *LLCL*-filter-based system with parameters of Case 1, when the intersection locates in NPR_II of Fig. 5.

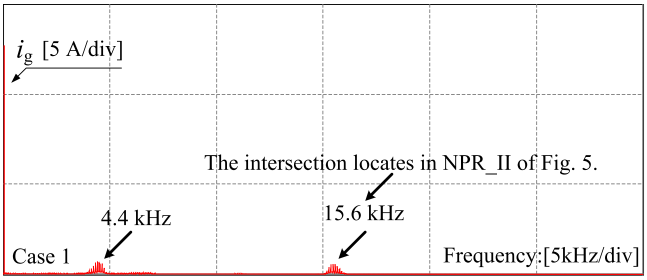

Fig. 14. Simulated FFT waveform of the grid-injected current with parameters of Case 1, when the intersection locates in NPR_II of Fig. 5.

For Case 1, the intersection frequency is calculated as 15.6 kHz, which locates in NPR_II. The simulated waveform and the FFT waveform of the grid-injected current are shown in Figs. 13 and 14, where the excessive grid-injected current harmonics respectively appear around the frequencies of 15.6 and 4.4 kHz.

Based on Case 1, Case 2 uses an extra capacitor C_{EMI} to avoid the intersection falling into NPR_II. The simulated grid-injected current in Fig. 15 shows the system operates stably again.

However, $f_p = f_{d1}$ cannot always be guaranteed, because the filter parameters may drift in the actual application. In our case, C_f and L_f drift +25% and −20% respectively, and they become 1 μF and 64 μH, then NPR_I appears. In this case, f_p is calculated as 4.477 kHz and NPR_I as [4.477, 5] kHz.

For Case 3, the intersection frequency becomes 4.7 kHz, which locates in NPR_I. The simulated waveform and the FFT waveform of the grid-injected current have been, respectively,

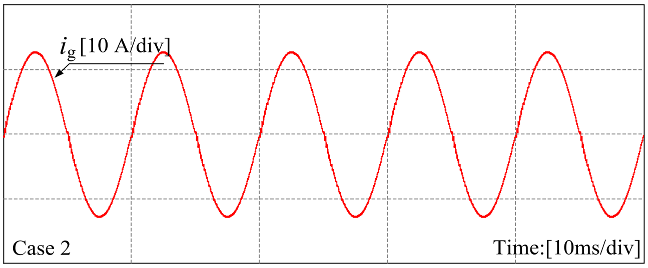

Fig. 15. Simulated grid-injected current of the *LLCL*-filter-based system with the C_{EMI}, where the parameters of Case 2 are adopted.

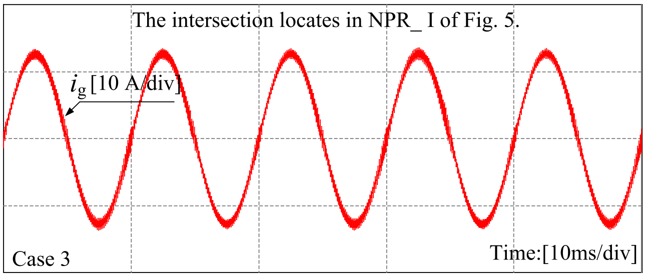

Fig. 16. Simulated grid-injected current of the *LLCL*-filter-based system with parameters of Case 3, when the intersection locates in NPR_I of Fig. 5.

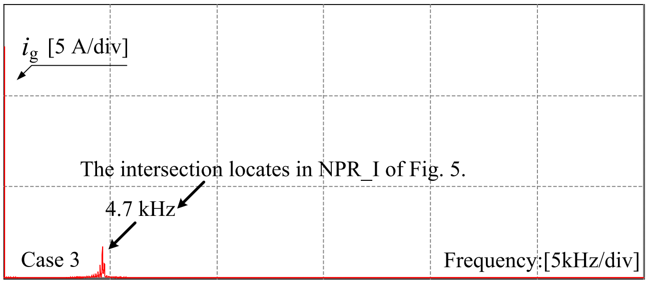

Fig. 17. Simulated FFT waveform of the grid-injected current with parameters of Case 3, when the intersection locates in NPR_I of Fig. 5.

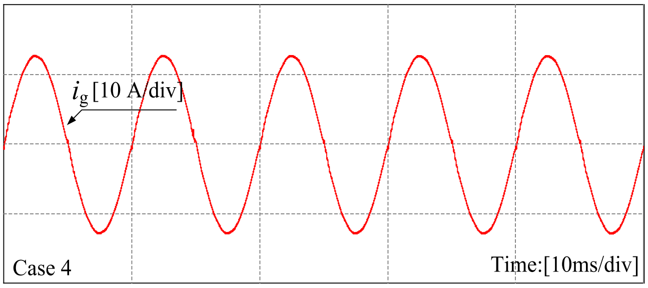

Fig. 18. Simulated grid-injected current with parameters of Case 4, when the intersection locates in NPR_I of Fig. 5 and the *RC* damper is adopted.

shown in Figs. 16 and 17, where the excessive grid-injected current harmonics appear around the frequency of 4.7 kHz.

Based on Case 3, Case 4 adopts the *RC* damper to eliminate the excessive grid-injected current harmonics, where the simulated grid-injected current in Fig. 18 shows that the system becomes stable again.

These simulation results in Figs. 13–18 are in good agreement with the previous theoretical analysis and the feasibility of the proposed design methods is confirmed.

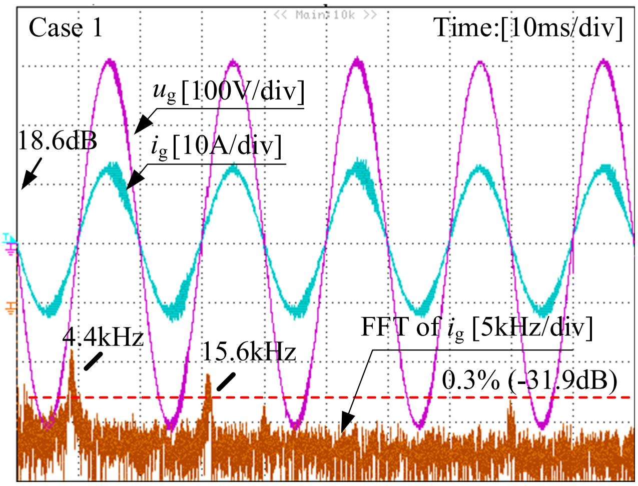

Fig. 19. Measured grid voltage waveform, grid-injected current waveform, and FFT waveform of grid-inject current with parameters of Case 1, when the intersection locates in NPR_II of Fig. 5.

VII. EXPERIMENTS

In order to further verify the theoretical analysis, a 2-kW/220-V prototype based on a DSP (TMS320LF2812) controller is constructed, and the circuit parameters are basically the same as those used in simulations. An inductor of L_g and a capacitor of C_g are used to emulate the equivalent grid inductance and capacitance, respectively. All the experimental waveforms are captured from a Yokogawa DL 1640 digital oscilloscope.

A. *Experimental Results*

Also, as shown in Table II, Case 1 and Case 2 are designed under the normal operation, while Case 3 and Case 4 are designed when filter parameters drift.

For Case 1, the measured grid-injected current waveform, grid voltage waveform, and the FFT waveform of grid-injected current have been shown in Fig. 19, which match well those of the simulations in Figs. 13 and 14. As expected, the excessive grid-injected current harmonics appear around 15.6 kHz, which locates in NPR_II.

To avoid the intersection point of the inverter output admittance and the damped grid admittance falling intro NPR_II, an extra capacitor C_{EMI} is used in Case 2. The measured grid-injected current waveform, grid voltage waveform, and the FFT waveform of grid-injected current have been shown in Fig. 20, indicating that the system operates stably again.

However, the filter parameters may drift in the actual application. If C_f and L_f, respectively, drift $+25\%$ and -20%, NPR_I appears, which is [4.477, 5] kHz.

For Case 3, the measured grid-injected current waveform, grid voltage waveform, and the FFT waveform of the grid-injected current have been shown in Fig. 21, which match well those of the simulations in Figs. 15 and 16. It can be seen that the excessive grid-injected current harmonics appear around 4.7 kHz, which locates in NPR_I.

To eliminate the excessive grid-injected current harmonics, the *RC* damper is adopted as Case 4. The measured grid-

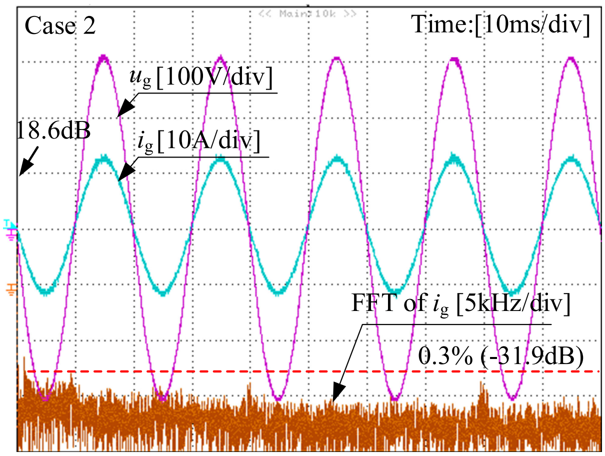

Fig. 20. Measured grid voltage, grid-injected current, and FFT waveform of grid-inject current with parameters of Case 2, when the intersection locates in NPR_II of Fig. 5, and the $C_{\mathrm{EMI}} = 1\ \mu$F is added.

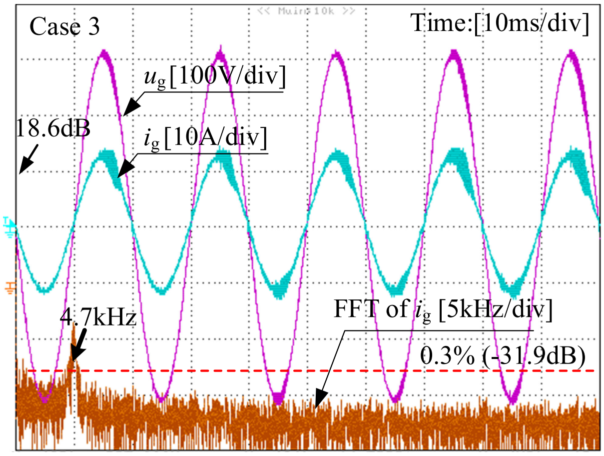

Fig. 21. Measured grid voltage waveform, grid-injected current waveform, and FFT waveform of grid-injected current with parameters of Case 3, when the intersection locates in NPR_I of Fig. 5.

injected current waveform, grid voltage waveform, and the FFT waveform of grid-injected current have been shown in Fig. 22, where the system becomes stable again.

Fig. 23 shows the dynamic waveform of the grid-injected current of Case 4 when it changes from 12.6 to 6.3 A under the condition that $C_g = 3\ \mu$F and $L_g = 4$ mH. The grid-injected current rapidly follows the grid-injected current reference, which verifies that the system has enough control bandwidth under the weakest grid condition.

Fig. 24 shows the measured current I_d of the R_d–C_d branch of the *LLCL*-filter-based system under the condition that $C_g = 3\ \mu$F and $L_g = 4$ mH. The power loss rate of the *RC* parallel damper can be calculated according to $(I_d^2 R_d/P_o)\%$, where P_o is the power injected into the grid. The power loss rate can be limited to 0.01% according to the measured current value.

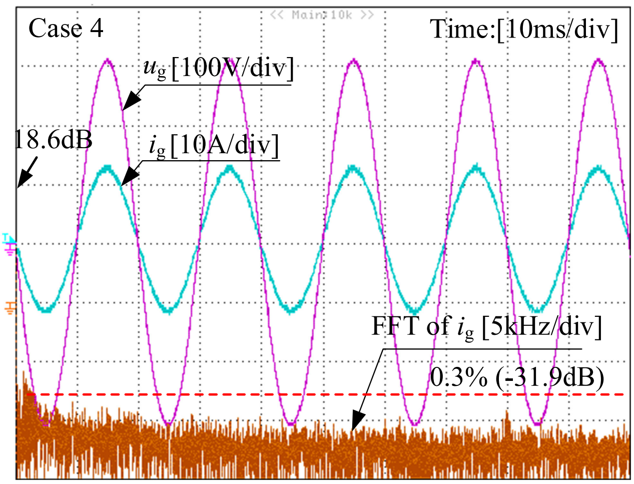

Fig. 22. Measured grid voltage waveform, grid-injected current waveform, and FFT waveform of grid-injected current with parameters of Case 4, when the intersection locates in NPR_I of Fig. 5, and the *RC* damper is adopted.

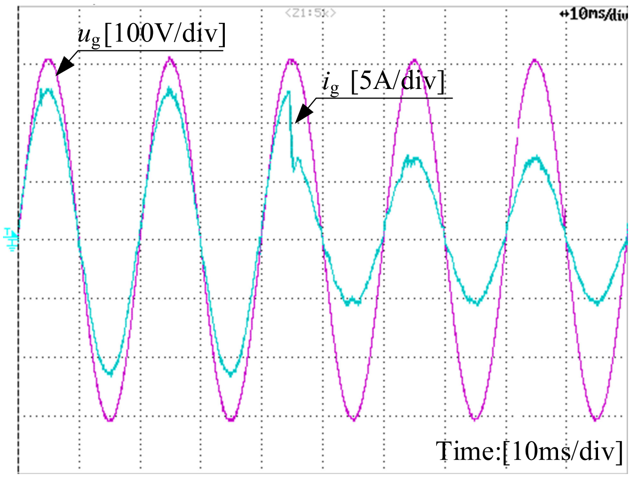

Fig. 23. Measured grid voltage grid-injected current of Case 4, when the grid-injected current reference regulates under the condition that $C_g = 3\ \mu$F and $L_g = 4$ mH.

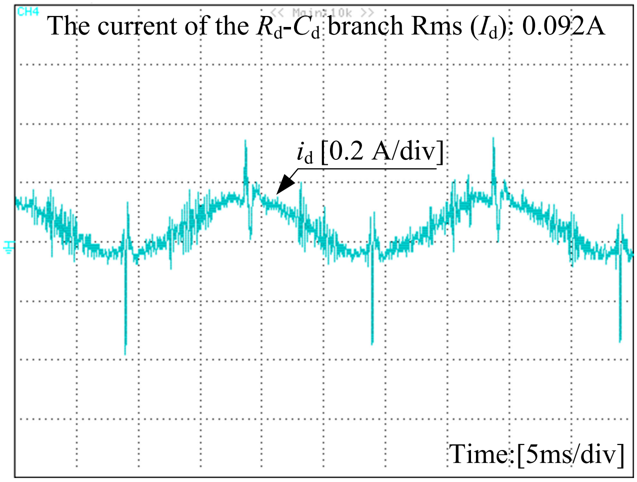

Fig. 24. Measured current waveform of the $C_d - R_d$ branch of the *LLCL*-filter-based system under the condition that $C_g = 3\ \mu$F and $L_g = 4$ mH.

B. Analysis and Discussion

From the experimental results, it can be seen that these are identical to the previous theoretical analysis and the simulation results. Moreover, the followings still need to be claimed.

1) Due to the small values of the damping resistor and capacitor, the extra damping power losses can almost be ignored.
2) Under the tolerance of the industrial power filter, C_f can drift ±5%, L_1 and L_f can drift within ±25%. Substituting these tolerances to (7), the value of f_p varies between 87.5% and 115.6% of its nominal value f_{p_nom}. The system can still work well with the *RC* damper, showing the characteristic of high robustness.
3) In fact, there is a tradeoff between the control bandwidth and the maximum tolerated values of the equivalent C_g and L_g. The bigger multiplication value of $C_g\, L_g$, the narrower control bandwidth of the system, where the highest harmonic compensator frequency has to be suppressed correspondingly.

VIII. CONCLUSION

This paper has first fully analyzed the characteristic of the *LLCL*-filter-based grid-tied inverter output admittance under the wide variation of grid reactance, where some conclusions can be drawn as follows:

1) Within the switching frequency, one or two nonpassive regions can be identified, depending on the delay time and the resonance frequency f_p.
2) When the grid reactance varies in a wide range, the intersection of the inverter output admittance and the grid admittance may fall in the nonpassive region.
3) In order to prevent the possible harmonic instability, there are two basic solutions recommended, which are narrowing the nonpassive region as much as possible and avoiding the intersection locating in the nonpassive region.
4) When L_f of *LLCL* filter is set to zero, the aforementioned three points can be also applied on the traditional *LCL*-filter-based system.

Second, based on the analysis, the exact and robust parameter design of the *LLCL* filter, the EMI capacitor, and the *RC* passive damper has been introduced in detail. The whole system can operate stably under a wide variation of grid reactance.

Finally, the simulations and experiments are developed on a 2-kW/220-V *LLCL*-filter-based single-phase grid-tied inverter prototype, where results have well confirmed the theoretical analysis and the feasibility of the proposed measures.

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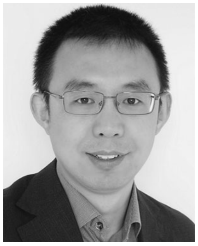

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