# Letters

## Optimality in the Sense of Arm Current Distribution of MMC VSC-HVDC

Pablo Briff, *Senior Member, IEEE*

***Abstract*—This letter investigates the optimality of the modular multilevel converter (MMC) voltage source converters high-voltage direct current (VSC-HVDC), which constitutes a linear time-invariant (LTI) system for sufficiently large number of submodules per valve. The contribution of this letter is the mathematical proof that MMC VSC-HVDC is the optimal LTI topology in the sense of arm current distribution. Namely, the findings of this work show that MMC VSC-HVDC attains an optimal limit in the way the ac and dc components of the converter arm currents are distributed in the field of linear converter topologies, and may only be outperformed by nonlinear or time-varying VSC-HVDC topologies.**

***Index Terms*—High-voltage direct current (HVDC), linear time-invariant (LTI), modular multilevel converter (MMC), voltage source converters (VSC).**

### I. Introduction

In THE recent years, a significant amount of effort has been invested in the research and development of high-voltage direct current (HVDC) voltage source converters (VSCs) in the power delivery industry and academia. The modular multilevel converter (MMC) [1] has gained an indisputable position in the HVDC industry as a preferred topology for point-to-point and multiterminal schemes, due to its efficient solution to the ac–dc power conversion problem. Although much literature has been written in the field of MMC, most of the research work has focused its attention in the system design [2], [3], control [4], [5], and protection of the circuit [6], [7]. Yet, to the best of the author's knowledge, the optimality of MMC VSC-HVDC in the sense of arm current distribution has not been proven before.

The contribution of this letter is the proof that MMC VSC-HVDC is the optimal linear time-invariant (LTI) topology in the sense of arm current distribution. This sets an upper limit on the attainable arm current distribution performance when operating the converter topology with a control law linearly dependent on the inputs and outputs, as well as with time-invariant circuital connections. More fundamentally, the outcome of this work suggests that, in order for a converter topology to outperform MMC VSC-HVDC in terms of arm current distribution,

Manuscript received June 26, 2018; revised August 8, 2018 and September 9, 2018; accepted October 10, 2018. Date of publication October 14, 2018; date of current version March 29, 2019.

The author is with the GE's Grid Solutions—HVDC Research and Technology, Stafford ST16 1WS, U.K. (e-mail:

let $i_{k+3} \triangleq (\tilde{i}_{k+3} + I_{k+3})$. Let $\mathbf{V}_{\rm dc} \triangleq V_{\rm dc}\,\mathbf{1}$ and $\mathbf{I}_{\rm dc} \triangleq I_{\rm dc}\,\mathbf{1}$, where $\mathbf{1} = [1\,1\,1]^T$.

*3) Sign Convention:* In this letter, inverter sign convention has been adopted, i.e., a current is deemed as positive (negative) when it circulates from the output $y^{(i)}$ to the input $x_k^{(i)}$ through the upper (lower) arm currents.

*4) Voltage Identity Operator:* The identity operator for the voltage waveform is defined by the parallel connection, denoted by "//", i.e.,

$$y^{(v)} = y^{(v)} // y^{(v)}. \tag{1}$$

*5) LTI System:* A system is considered as LTI if for a transformation $T(\cdot)$ of the inputs $x_k$, the following three conditions are fulfilled [9]:

*a) Linearity:*

$$T\left(\sum_k a_k x_k\right) = \sum_k a_k T(x_k) \tag{2}$$

where $a_k$ are constants and $k = \{1, 2, 3\}$. Equation (2) is also known as the *superposition property* of linear systems.

*b) Time-Invariance:*

$$y(t) = T(x_k(t)) \xrightarrow{\text{delay } \tau} y(t-\tau) \equiv T(x_k(t-\tau)) \tag{3}$$

for constant delay time $\tau$.

*c) Response to Sinusoidal Inputs:* For a given input waveform $x_k = A_k\, e^{j(\omega_k t + \phi_k)}$, the output of the LTI system is $y = A\, e^{j(\omega_k t + \phi)}$, with $A, A_k, \omega_k, \phi_k, \phi, t \in \mathbb{R}$ and $j = \sqrt{-1}$.

*6) Incrementally LTI System:* A system is considered as *incrementally* LTI or affine [9] if for the input waveforms $x_k$, the output $y$ can be written as

$$y = \sum_k \left(T(x_k) + v_k\right) \tag{4}$$

where $T(\cdot)$ is an LTI system on the inputs $x_k$, and $v_k$ is a nonzero continuous-time quantity. From (4), it follows that $\Delta y \triangleq (y - \sum_k v_k)$ is LTI.

Rewriting (4) to include the discretization in the valves voltages, the discretized output $y'$ is given by

$$y' = \sum_k \left(T(x_k) + v_k\right) + e_d \tag{5}$$

where $e_d \triangleq (y' - y)$ represents the discretization error at any switching instant of duration $1/f_{\rm sw}$ introduced by the discrete voltage levels in the VSC valves. In order to consider $\Delta y' \triangleq (y' - \sum_k v_k)$ as LTI, it must hold

$$|e_d| \ll \min(y, \hat{x}_k) \quad \forall k \iff y' \approx y \tag{6}$$

i.e., the discretization error $e_d$ shall be negligible with respect to the peak values of $y, x_k$, in which case the outputs $y, y'$ can be considered equivalent. In order to fulfil (6), each valve shall be fitted with a sufficiently large number of SMs, typically in the range of 200–400 SMs/valve [10].

*7) Non-LTI System:* A system that does not conform to the definitions in Sections II-A5 and II-A6 due to time-varying behavior in $T(x_k)$ arising from the converter's circuital operation, nonlinear characteristics in $v_k$, or considerable discretization error $e_d$. Examples of non-LTI topologies are the alternate arm converter [11] and the series bridge converter [12] due to their time-variance in $T(x_k)$ and nonlinearity in $v_k$, as well as two-level and three-level VSCs where $e_d$ is comparable with $y$ and $\hat{x}_k$ (i.e., (6) does not hold).

### B. Assumptions

In steady state, the input waveforms $x_k$:

1) form a balanced three-phase system with peak value $\hat{x}$ and angular frequency $\omega_0$;
2) add to zero, i.e., $\sum_k x_k = 0$;
3) have no dc component, i.e., their mean value is $\bar{x}_k = 0$.

Furthermore, it is assumed that $N$, the number of SMs per valve, is such that (6) holds.

### C. HVDC-Specific Design Criteria

An optimally designed VSC-HVDC topology shall:

1) provide symmetrical dc pole-to-ground voltage;
2) utilize all the input waveforms $x_k$ to conform the output waveforms $y$;
3) minimize the converter energy storage requirement;
4) optimize the current loading within the converter arms.

Criterion II-C.1 relates to the minimization of the voltage insulation requirement of the HVDC converter [13], [14], making symmetrical monopole the most common HVDC topology [15].

Criterion II-C.2 relates to the efficient utilization of the input waveforms to establish the output waveforms in a three-phase converter [16] as well as to ensure steady-state ac power balance and system stability under unbalanced conditions [17].

Criterion II-C.3 relates to the minimization of the converter valves' voltage requirement, at a given SM capacitance value, due to its impact on cost, weight, and power losses [8], [18].

Criterion II-C.4 relates to the way the arm currents are distributed within the VSC, namely the distribution of the ac and dc components of the arm currents, which dominate the converter's power losses [19], [20] and thermal rating [21] of the VSC. Since the latter quantities exhibit a quadratic dependence with the ac and dc components of the arm currents, an optimization problem involving $\tilde{i}_k^2, \tilde{i}_{k+3}^2, I_k^2, I_{k+3}^2$ can be stated to derive how the optimal VSC arm currents are distributed. To this end, the concept of optimality in the sense of arm current distribution is defined below.

## III. Optimality in the Sense of Arm Current Distribution for LTI Converter Topologies

### A. Definition

A VSC-HVDC topology is optimal in the sense of arm current distribution (OACD) if it minimizes the sum of the square of the arm currents for each input (ac) and output (dc) current references.

### B. Necessary and Sufficient Conditions

A VSC-HVDC topology is LTI OACD if all of the following are met.

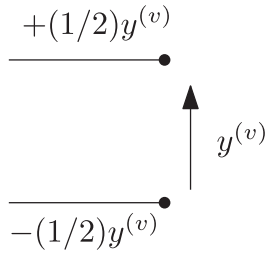


Fig. 1. Symmetrical output voltage $y^{(v)}$.

1) It complies with the HVDC-specific design criteria, as specified in Section II-C.
2) It can be described by an LTI system, as specified in Sections II-A5 and II-A6.
3) It attains OACD, as specified in Section III-A.

### C. Existence and Uniqueness of the LTI OACD VSC-HVDC Topology

*Proposition 1:* MMC is the LTI OACD VSC-HVDC topology.

*Proof:* Provided below.

*1) Existence of the LTI OACD VSC-HVDC Topology:* In order to prove its existence, the optimal topology is derived by obtaining its output voltages and current as shown below.

*a) Derivation of the Output Voltage $y^{(v)}$:* Using Criterion II-C.1, the upper-to-lower output voltage shall be written as

$$y^{(v)} = +(1/2)y^{(v)} - (-(1/2)y^{(v)}) \tag{7}$$

i.e., the upper-to-lower output voltage $y^{(v)}$ is composed of the difference of the upper output voltage $+(1/2)y^{(v)}$ and the lower output voltage $-(1/2)y^{(v)}$, as shown in Fig. 1.

The LTI necessary condition outlined in Section III-B2 limits the possible transformations $T(\cdot)$ on the inputs $x_k^{(v)}$ to those that constitute an LTI system. Namely, the contribution of input $x_k^{(v)}$ to the upper output voltage $+(1/2)y^{(v)}$ shall be expressed as

$$+(1/2)y^{(v)} = a_k x_k^{(v)} + v_k \tag{8}$$

where $a_k$ is a voltage amplification factor and $v_k$ is a scalar quantity representing the $k$th arm valve voltage. The factor $a_k$ can be varied, for example, by means of onload tap-changers [22]. Without loss of generality, let $a_k = 1$. From (8), it follows that

$$v_k = -x_k^{(v)} + (1/2)y^{(v)}. \tag{9}$$

Since $x_k^{(v)}, y^{(v)}$ are continuous-time quantities, the linearity of $v_k$ in (9) relies on the fact that $v_k$ is fitted with sufficient number of SMs (see Section II-A6). Moreover, (9) implies that $v_k$ shall provide the output dc voltage $+(1/2)y^{(v)}$ as well as cancel out the input sinusoidal content $x_k^{(v)}$ (see Section II-A5c). This indicates that an LTI converter valve must be fitted with sufficient voltage so as to provide the difference between input and output voltages. The minimum valve voltage rating is given by $\max|v_k| \approx (1/2)y^{(v)} + \hat{x}_k^{(v)}$. Namely, when operating as a linear system, the converter energy storage requirement is dominated by the quantities $y^{(v)}$ and $\hat{x}_k^{(v)}$. From (9), $0 \le v_k \le v_{\max}$, where $v_{\max}$ is the maximum valve's voltage rating. Hence, if $v_k = 0$, then $x_k^{(v)} = +(1/2)y^{(v)}$; similarly, if $v_k = v_{\max}$ then $x_k^{(v)} = -v_{\max} + (1/2)y^{(v)}$. Therefore, using Criterion II-C.3 leads to the minimum valve's voltage rating $v_{\max} = y^{(v)}$ for maximum symmetrical swing[1] in $x_k^{(v)}$.

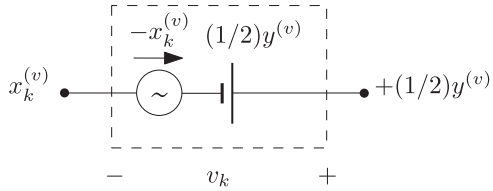


Fig. 2. Linear construction of $+(1/2)y^{(v)}$ from $x_k^{(v)}$.

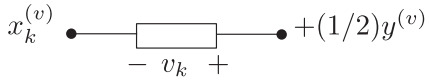


Fig. 3. Upper arm valve model.

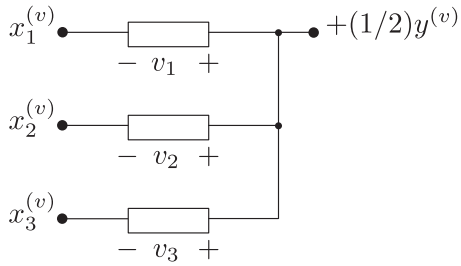


Fig. 4. Parallel connection at the output $+(1/2)y^{(v)}$.

Fig. 2 represents $v_k$ as a linear block connecting $x_k^{(v)}$ to $+(1/2)y^{(v)}$. The construct $v_k$, shown in Fig. 3, is commonly referred to as *valve*.

Using Criterion II-C.2 and (1), the output $+(1/2)y^{(v)}$ is built as

$$+(1/2)y^{(v)} = (x_1^{(v)} + v_1)//(x_2^{(v)} + v_2)//(x_3^{(v)} + v_3). \tag{10}$$

Fig. 4 summarizes the parallel connection stated by (10).

Extending (9) to the lower output voltage $-(1/2)y^{(v)}$ by means of three additional valves $v_{k+3} = \{v_4, v_5, v_6\}$ leads to

$$-v_{k+3} = -x_k^{(v)} - (1/2)y^{(v)}. \tag{11}$$

Note that $-v_{k+3}$ has been defined in (11) since the output voltage of HB valves cannot be negative. Naturally

$$v_{k+3} = x_k^{(v)} + (1/2)y^{(v)} \tag{12}$$

as shown in Figs. 5 and 6.

Simultaneously building the outputs $+(1/2)y^{(v)}$ and $-(1/2)y^{(v)}$ from inputs $x_k$ leads to the parallel connections shown in Fig. 7.

[1]Third harmonic injection or energy balancing techniques have not been considered in this expression.

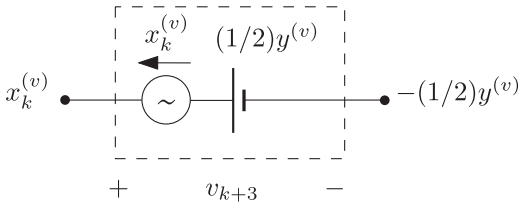


Fig. 5. Linear construction of $-(1/2)y^{(v)}$ from $x_k^{(v)}$.

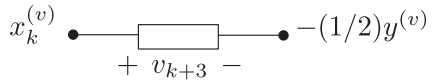


Fig. 6. Lower arm valve model.

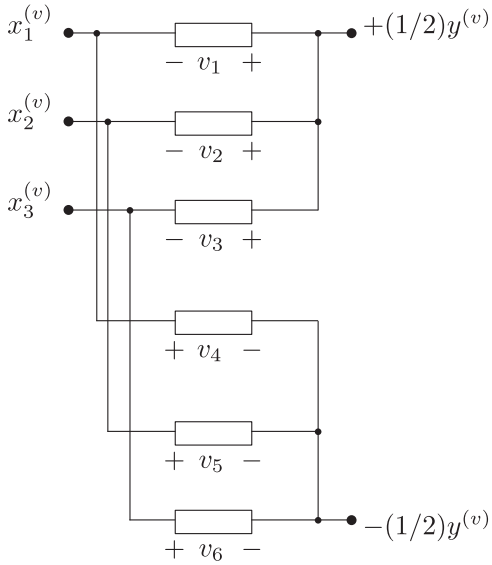


Fig. 7. Parallel connections at the inputs $x_k^{(v)}$.

*b) Derivation of the Output Current $y^{(i)}$:* The parallel connection at the input shown in Fig. 7 splits the input currents into two paths. Using Criterion C.4, the distribution of the converter arm currents shall be optimized. Since the input and output currents $x_k^{(i)}, y^{(i)}$ are orthogonal functions [9] over one fundamental period $T_0 = 2\pi/\omega_0$, i.e., $\int_0^{T_0} x_k^{(i)} y^{(i)} dt = 0$, the optimization of the arm current distribution can be performed separately for inputs and output waveforms.

The optimal distribution of the upper and lower arm currents $\tilde{i}_k, \tilde{i}_{k+3}$ due to the input current $x_k^{(i)}$ is found by stating the following optimization problem

$$\min \tilde{J} = \left(\tilde{i}_k^2 + \tilde{i}_{k+3}^2\right) \quad \text{s.t.} \quad \tilde{i}_k - \tilde{i}_{k+3} = x_k^{(i)}. \tag{13}$$

The solution of (13), shown in (14), is depicted in Fig. 8

$$\tilde{i}_k = -\tilde{i}_{k+3} = (1/2)x_k^{(i)}. \tag{14}$$

Similarly, the parallel connection made at the output arising from Fig. 7 splits the output current into paths. The optimal distribution of the upper arm currents $I_k$ due to the output current

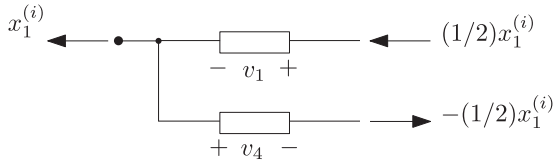


Fig. 8. Input current $x_k^{(i)}$ is equally distributed into two paths.

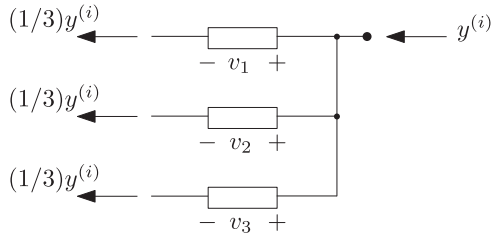


Fig. 9. Output current $y^{(i)}$ is equally distributed into three paths.

$y^{(i)}$ is found as

$$\min J = \sum_{k=1}^{3} I_k^2 \quad \text{s.t.} \quad \sum_{k=1}^{3} I_k = y^{(i)}. \tag{15}$$

The solution of (15), shown in (16), is depicted in Fig. 9

$$I_k = (1/3)y^{(i)}. \tag{16}$$

Stating a similar problem to that shown in (15), the solution of the lower arm currents $I_{k+3}$ due to $y^{(i)}$ is $I_{k+3} = I_k = (1/3)y^{(i)}$. Combining (14), (16), and using the superposition property, the converter arms currents are given by

$$\begin{aligned} i_k &= \tilde{i}_k + I_k = (1/2)x_k^{(i)} + (1/3)y^{(i)} \\ i_{k+3} &= \tilde{i}_{k+3} + I_{k+3} = -(1/2)x_k^{(i)} + (1/3)y^{(i)} \end{aligned} \tag{17}$$

where $\{i_k\}$ represent the upper arm currents and $\{i_{k+3}\}$ represent the lower arm currents, with $k = \{1, 2, 3\}$. Since the arm currents have been obtained from the optimization problems (13) and (15), the arm currents shown in (17) comply with the OACD necessary condition described in Section III-B3.

Using the HVDC nomenclature $[x_1^{(v)}\ x_2^{(v)}\ x_3^{(v)}]^T = \mathbf{v_{abc}}$, $[x_1^{(i)}\ x_2^{(i)}\ x_3^{(i)}]^T = \mathbf{i_{abc}}$, $y^{(v)} = V_{\rm dc}$, $y^{(i)} = I_{\rm dc}$, and rewriting (9), (12), (17) leads to the following converter equations in vector form:

$$\begin{aligned} \mathbf{v_k} &= [v_1\ v_2\ v_3]^T = -\mathbf{v_{abc}} + (1/2)\mathbf{V}_{\rm dc} \\ \mathbf{v_{k+3}} &= [v_4\ v_5\ v_6]^T = \mathbf{v_{abc}} + (1/2)\mathbf{V}_{\rm dc} \\ \mathbf{i_k} &= [i_1\ i_2\ i_3]^T = (1/2)\mathbf{i_{abc}} + (1/3)\mathbf{I}_{\rm dc} \\ \mathbf{i_{k+3}} &= [i_4\ i_5\ i_6]^T = -(1/2)\mathbf{i_{abc}} + (1/3)\mathbf{I}_{\rm dc}. \end{aligned} \tag{18}$$

The converter topology depicted in Fig. 7, together with the converter equations described in (18), corresponds to the MMC proposed in [1]. The resulting circuit topology, which satisfies the design criteria necessary conditions outlined in Section III-B1, is depicted in Fig. 10 together with its current and voltage quantities.

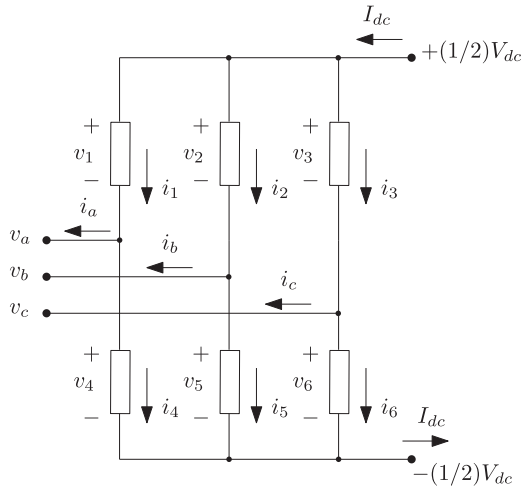


Fig. 10. MMC topology, OACD.

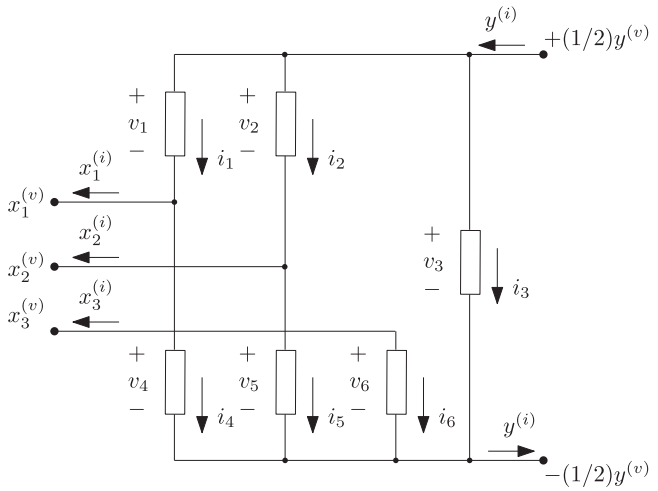


Fig. 11. Generic LTI topology with HB valves.

Since the converter topology shown in Fig. 10 has been derived in compliance with the necessary and sufficient conditions described in Section III-B, it is concluded that the MMC is LTI OACD.

*2) Uniqueness of the LTI OACD Topology:* Section III-C1 has proven the existence of an LTI OACD topology, but not its uniqueness. To complete the proof of Proposition 1, it remains to show that no other LTI topology outperforms MMC in the sense of arm current distribution.

The optimality of a topology shall be assessed by its arm current distribution cost function. For notational simplicity, let (13) be rewritten in matrix form for the upper and lower arm currents, i.e.,

$$\min \tilde{J} = \tilde{\mathbf{x}}^T \tilde{\mathbf{x}} \quad \text{s.t.} \quad \tilde{\mathbf{A}}\tilde{\mathbf{x}} = \tilde{\mathbf{b}} \tag{19}$$

where $\tilde{\mathbf{x}} = [\tilde{i}_1 \tilde{i}_2 \dots \tilde{i}_6]^T$, $\tilde{\mathbf{A}} = [\tilde{\mathbf{w}}_\mathbf{1}^T \tilde{\mathbf{w}}_\mathbf{2}^T \tilde{\mathbf{w}}_\mathbf{3}^T]^T$, $\tilde{\mathbf{b}} = [x_1^{(i)}\, x_2^{(i)}\, x_3^{(i)}]^T$, and $\tilde{\mathbf{w}}_\mathbf{k}^T$ represents the electrical connections of each of the converter arms to the ac current inputs $x_k^{(i)}$ arising from Kirchhoff's current law (KCL). The solution to the convex optimization problem (19) is given by [23]

$$\tilde{\mathbf{x}}_{\text{opt}} = \tilde{\mathbf{A}}^T \left(\tilde{\mathbf{A}}\tilde{\mathbf{A}}^T\right)^{-1} \tilde{\mathbf{b}}. \tag{20}$$

Each element of $\tilde{\mathbf{x}}_{\text{opt}}$ is expressed as $\tilde{i}_k = \tilde{\mathbf{p}}_\mathbf{k}^T\, \tilde{\mathbf{b}}$, where $\tilde{\mathbf{p}}_\mathbf{k} = [p_{k1}\, p_{k2}\, p_{k3}]^T$ is a vector of proportions of $x_k^{(i)}$ in each converter arm. Likewise, rewriting (15) in matrix form for the upper and lower arm currents gives

$$\min J = \mathbf{x}^T \mathbf{x} \quad \text{s.t.} \quad \mathbf{A}\mathbf{x} = \mathbf{b} \tag{21}$$

where $\mathbf{x} = [I_1 I_2 \dots I_6]^T$, $\mathbf{A} = [\mathbf{w_1}^T \mathbf{w_2}^T]^T$, $\mathbf{b} = y^{(i)}\mathbf{1}$. The vectors $\mathbf{w_1}, \mathbf{w_2}$ represent the electrical connections of the converter arms to the dc current output $y^{(i)}$ using KCL. Equation (21) yields

$$\mathbf{x}_{\text{opt}} = \mathbf{A}^T \left(\mathbf{A}\mathbf{A}^T\right)^{-1} \mathbf{b}. \tag{22}$$

Each element of $\mathbf{x}_{\text{opt}}$ is expressed as $I_k = p_k\, y^{(i)}$, where $p_k$ is the proportion of $y^{(i)}$ in each converter arm.

The total minimum cost $J_{\min}$ is given by the sum of the optimal values of $J$ and $\tilde{J}$, i.e.,

$$J_{\min} = \tilde{\mathbf{x}}_{\text{opt}}^T\, \tilde{\mathbf{x}}_{\text{opt}} + \mathbf{x}_{\text{opt}}^T\, \mathbf{x}_{\text{opt}}. \tag{23}$$

For the MMC circuit (see Fig. 10), the matrices $\tilde{\mathbf{A}}_\mathbf{0}, \mathbf{A_0}$ are formed of the respective vectors $\tilde{\mathbf{w}}_\mathbf{1} = [1\,0\,0\,(-1)\,0\,0]^T$, $\tilde{\mathbf{w}}_\mathbf{2} = [0\,1\,0\,0\,(-1)\,0]^T$, $\tilde{\mathbf{w}}_\mathbf{3} = [0\,0\,1\,0\,0\,(-1)]^T$, $\mathbf{w_1} = [1\,1\,1\,0\,0\,0]^T$, and $\mathbf{w_2} = [0\,0\,0\,1\,1\,1]^T$. As expected, plugging $\tilde{\mathbf{A}} = \tilde{\mathbf{A}}_\mathbf{0}, \mathbf{A} = \mathbf{A_0}$ into (20) and (22) leads to the solutions shown in (14) and (16). From (23), the minimum per-unitized cost attained by MMC is

$$J_0 \triangleq \frac{J_{\min}}{\left(y^{(i)}\right)^2} = \frac{2}{3} + \frac{3}{2}\alpha^2 \tag{24}$$

where $\left(y^{(i)}\right)^2$ is the per-unit base for $J_{\min}$, and $\alpha = \hat{x}_k^{(i)}/y^{(i)}$.

A more optimal LTI converter topology than MMC, if it exists, shall satisfy the necessary and sufficient conditions outlined in Section III-B with less or equal energy storage requirement in the converter valves, i.e., up to $6y^{(v)}$. For the sake of simplicity in the analysis, and without loss of generality, let us assume that six HB valves, denoted as $v_1, v_2, \dots, v_6$, are used. Each HB valve's voltage shall be composed of a dc voltage and optionally an ac voltage, provided that the total instantaneous valve's voltage is non-negative and limited to a maximum value. This implies that HB valves cannot be directly connected between two ac inputs since they are unable to synthesize a negative voltage. Also, there must be at least three valves, e.g., $v_1, v_2, v_6$, connecting an ac voltage input $x_k^{(v)}$ to a dc voltage output $\pm(1/2)y^{(v)}$, to provide the difference between ac and dc voltages [see (9)]. Furthermore, in a topological arrangement where the ac components $\tilde{i}_k$ of the arm currents do not automatically cancel at the output, a shunt circuit composed of at least one valve, e.g., $v_3$, shall be utilized to circulate the difference between ac and dc currents. The remaining two valves, e.g., $v_5, v_6$, may be used to conveniently, for example, configure the converter arms current distribution.

Fig. 11 shows a generic LTI topology consisting of HB valves, which will be used as a baseline to obtain LTI candidate

topologies in order to evaluate the uniqueness of the LTI OACD topology derived in Section III-B. For example, disconnecting in Fig. 11, the negative terminal of $v_3$ from $-(1/2)y^{(v)}$ and connecting it to $x_3^{(v)}$ leads to the MMC topology shown in Fig. 10. Other than MMC, the possible LTI topologies using HB valves that may attain LTI OACD, denoted as T1, T2, . . ., T8, are listed below:

T1) defined as shown in Fig. 11, and vectors $\tilde{\mathbf{w}}_\mathbf{1} = [1\,0\,0\,(-1)\,0\,0]^T$, $\tilde{\mathbf{w}}_\mathbf{2} = [0\,1\,0\,0\,(-1)\,0]^T$, $\tilde{\mathbf{w}}_\mathbf{3} = [0\,0\,0\,0\,0\,(-1)]^T$, $\mathbf{w}_\mathbf{1} = [1\,1\,1\,0\,0\,0]^T$, and $\mathbf{w}_\mathbf{2} = [0\,0\,1\,1\,1\,0]^T$. Using (23), the minimum per-unitized cost for this topology is $J_1 = (1/2) + 2\alpha^2$.

T2) defined by $v_1, v_2, v_3, v_5, v_6$ as shown in Fig. 11, and $v_4 // v_1$, yields $J_2 = (2/3) + 2\alpha^2$.

T3) defined by $v_1, v_2, v_3, v_5, v_6$ as shown in Fig. 11, and $v_4 // v_2$, yields $J_3 = (3/5) + (7/3)\alpha^2$.

T4) defined by $v_1, v_2, v_3, v_5, v_6$ as shown in Fig. 11, and $v_4 // v_3$, yields $J_4 = (1/3) + (5/2)\alpha^2$.

T5) defined by $v_1, v_2, v_3, v_6$ as shown in Fig. 11, and $v_4 // v_1$, $v_5 // v_6$, yields $J_5 = 1 + 2\alpha^2$.

T6) defined by $v_1, v_2, v_3, v_6$ as shown in Fig. 11, and $v_4 // v_5 // v_6$, yields $J_6 = 1 + (7/3)\alpha^2$.

T7) defined by $v_1, v_2, v_3, v_6$ as shown in Fig. 11, and $v_1 // v_5$, $v_3 // v_4$, yields $J_7 = (1/2) + (5/2)\alpha^2$.

T8) defined by $v_1, v_2, v_3, v_6$ as shown in Fig. 11, and $v_3 // v_4 // v_5$, yields $J_8 = (1/3) + 3\alpha^2$.

Variants of topologies T1–T8 produce the same cost functions detailed above. Next, the per-unitized costs $J_q$ are compared with MMC's cost $J_0$, with $q = 1, 2, \ldots, 8$. Notice that $J_0 < J_q$ for $\alpha > (1/\sqrt{3})$. Topologies T1 and T4 are the first of the set T1–T8 to yield a smaller cost than $J_0$ for $\alpha < (1/\sqrt{3})$, and hence they shall be considered as candidate topologies to outperform MMC in the sense of arm current distribution. It remains to show that topologies T1, T4 satisfy the necessary conditions of LTI OACD (see Section III-B).

Recalling the ac–dc power balance equation for balanced systems at unity power factor, i.e., $(3/2)\hat{x}_k^{(v)}\hat{x}_k^{(i)} = y^{(v)}y^{(i)}$, the ratio of the input voltage peak value and the output voltage is

$$\beta = \frac{\hat{x}_k^{(v)}}{y^{(v)}} = \frac{2}{3\alpha}. \tag{25}$$

Using (25) at $\alpha = (1/\sqrt{3})$, the value at which topologies T1, T4 outperform MMC's cost, yields $\beta = (2/\sqrt{3})$, or $\hat{x}_k^{(v)} = (2/\sqrt{3})y^{(v)}$. However, this violates the maximum ac voltage attainable by an HB valve, namely $\hat{x}_k^{(v)} = (1/2)y^{(v)}$ [see (9) and (12)]. Hence, the candidate topologies T1 and T4 fail to satisfy the linearity necessary condition (see Section III-B2) and cannot be considered LTI OACD topologies. This conclusion is extended to all topologies T1–T8. It can then be concluded that MMC's LTI OACD property is unique when using HB valves.

Finally, let us consider the inclusion of full-bridge (FB) valves. Due to space constraints, only the best candidate linear topology using FB valves in terms of total cost, denoted as T9, is detailed below.

T9) defined by $v_1, v_2, v_3, v_6$ as shown in Fig. 11, $v_4$ connected to $x_1^{(v)}, x_2^{(v)}$, and $v_5$ connected to $x_2^{(v)}, x_3^{(v)}$, yields $J_9 = 1 + (9/8)\alpha^2$.

Topology T9 produces a cost $J_9 < J_0$ for $\alpha < (2\sqrt{2}/3)$, which gives $\beta > (1/\sqrt{2})$ and a minimum total converter voltage requirement of $6.62y^{(v)}$, which exceeds that of MMC. In other words, when the total converter voltage rating is limited to that of MMC, topology T9 fails to satisfy the linearity necessary condition and hence cannot be considered LTI OACD. Therefore, the uniqueness of MMC's LTI OACD property is also extended to linear converters using FB valves. This completes the proof of Proposition 1. ■

## IV. Conclusion

The proof of Proposition 1 indicates that MMC VSC-HVDC, which constitutes an LTI system for sufficiently large number of SMs per valve, attains optimal arm current distribution. This is achieved, however, at the expense of the converter energy storage requirement. In other words, prioritizing arm current distribution optimality over energy storage requirement using an LTI HVDC converter leads to the well-known MMC VSC-HVDC topology. In summary, this work concludes that MMC VSC-HVDC attains an optimal limit in the way the ac and dc components of the converter arm currents are distributed in the field of linear converter topologies, and may only be outperformed by nonlinear or time-varying VSC-HVDC topologies.

## References


[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. Power Tech. Conf.*, 2003, vol. 3, 6 pp.

[2] R. Alvarez, M. Wahle, H. Gambach, and J. Dorn, "Optimum semiconductor voltage level for MMC submodules in HVDC applications," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Sep. 2016, pp. 1–9.

[3] D. Zhang, R. Datta, A. Rockhill, Q. Lei, and L. Garces, "The modular embedded multilevel converter: A voltage source converter with IGBTs and thyristors," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2016, pp. 1–8.

[4] S. Kubera, R. Alvarez, and J. Dorn, "Control of switching frequency for modular multilevel converters by a variable hysteresis band modulation," in *Proc. 18th Eur. Conf. Power Electron. Appl.*, Sep. 2016, pp. 1–7.

[5] C. D. Barker, R. S. Whitehouse, A. G. Adamczyk, and G. G. Soto, "Low frequency active power oscillation damping using a MMC-VSC HVDC link," in *Proc. 13th IET Int. Conf. AC DC Power Transmiss.*, Feb. 2017, pp. 1–6.

[6] S. Cui and S. K. Sul, "A comprehensive dc short-circuit fault ride through strategy of hybrid modular multilevel converters (mmcs) for overhead line transmission," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7780–7796, Nov. 2016.

[7] M. Stumpe, P. Ruffing, P. Wagner, and A. Schnettler, "Adaptive single-pole autoreclosing concept with advanced dc fault current control for full-bridge mmc vsc systems," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 321–329, Feb. 2018.

[8] C. Oates, "Modular multilevel converter design for vsc hvdc applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 2, pp. 505–515, Jun. 2015.

[9] A. V. Oppenheim, A. Willsky, and I. Young, *Signals and Systems*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1983.

[10] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1631–1656, Dec. 2017.

[11] M. M. C. Merlin *et al.*, "The extended overlap alternate arm converter: A voltage-source converter with dc fault ride-through capability and a compact design," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3898–3910, May 2018.

[12] E. Amankwah *et al.*, "The series bridge converter (SBC): Design of a compact modular multilevel converter for grid applications," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2016, pp. 2588–2593.

[13] Cigre working group b4.61, "General guidelines for HVDC electrode design," CIGRE Working Group B4.61. General Guidelines HVDC Electrode Design, 2017.

[14] A. Junyent-Ferré, P. Clemow, M. M. C. Merlin, and T. C. Green, "Operation of hvdc modular multilevel converters under dc pole imbalances," in *Proc. 16th Eur. Conf. Power Electronics Appl.*, Aug. 2014, pp. 1–10.

[15] S. Mukherjee, M. Saltzer, Y.-J. Hafner, and S. Nyberg, "Cable overvoltage for MMC based VSC HVDC system: Interaction with converters," in *Proc. CIGRE Study Committee B1 Meeting Int. Colloquium*, 2017.

[16] E. W. Kimbark, *Direct Current Transmission*, vol. 1. New York, NY, USA: Wiley, 1971.

[17] P. Kundur, N. J. Balu, and M. G. Lauby, *Power System Stability and Control*, vol. 7. New York, NY, USA: McGraw-Hill, 1994.

[18] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electron.*, vol. 8, no. 3, pp. 350–360, 2015.

[19] P. S. Jones and C. C. Davidson, "Calculation of power losses for MMC-based VSC HVDC stations," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

[20] A. Hassanpoor, S. Norrga, and A. Nami, "Loss evaluation for modular multilevel converters with different switching strategies," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, Jun. 2015, pp. 1558–1563.

[21] P. D. Judge and T. C. Green, "Dynamic thermal rating of a modular multilevel converter HVDC link with overload capacity," in *Proc. IEEE Eindhoven PowerTech*, Jun. 2015, pp. 1–6.

[22] H. Feng, K. Viereck, S. Breker, and J. Rudolph, "Approach for on-load tap-changer control based on intelligent voltage stability margin estimation by using local measurements," *CIRED - Open Access Proc. J.*, vol. 2017, no. 1, pp. 952–955, 2017.

[23] S. Boyd and L. Vandenberghe, *Convex Optimization*. Cambridge, U.K.: Cambridge Univ. Press, 2004.