Isolated Bidirectional DC–DC Converter With Quasi-Resonant Zero-Voltage Switching for Battery Charge Equalization

Junlong Lu, *Student Member, IEEE*, Yi Wang, *Member, IEEE*, and Xin Li

***Abstract*—Charge equalization for a series-connected battery string is necessary to enhance usage life and performance of cells. In this paper, an isolated bidirectional dc–dc converter with quasi-resonant zero-voltage switching (ZVS) is proposed for centralized charge equalization system. Through the quasi-resonant operation, the proposed converter can achieve ZVS operations in both boost and buck modes, which decreases switching losses and improves the efficiency. The energy in leakage inductance is released to output side in the boost mode and recycled to the input side in the buck mode, which eliminates the voltage spike. Moreover, the proposed converter has fewer components than existing converters used in the centralized charge equalization system. The operating principle and theoretical derivation of the proposed converter are presented. The ZVS implementations and conditions are analyzed and illustrated in detail. Finally, the experiments using a 7.2 Ah battery string of 13 cells are conducted. The results verify the validity of the proposed converter and show that the equalizer achieves good performance in terms of equalizing speed and efficiency.**

***Index Terms*—Bidirectional dc–dc, charge equalization, quasi-resonant, zero-voltage switching (ZVS).**

I. Introduction

THE RAPID development of electric vehicles and other devices (such as drones) that require a mobile power supply has increased the usage of battery packs. Generally, a battery pack is composed of a large number of cells connected in series and in parallel to achieve high voltage and large capacity. In this case, charge equalization of the battery pack is a crucial issue because unbalance in the battery pack may result in failure or even explosion [1], [2]. Therefore, charge equalization technology should be adopted to improve the performance and useful life of battery packs.

The charge equalization technologies are mainly divided into dissipative type and nondissipative type. Because of the high energy consumption and low efficiency of the dissipative

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The authors are with the Power Electronics and Electrical Drives Research Center, Harbin Institute of Technology Shenzhen Graduate School, Shenzhen 518055, China (e-mail:

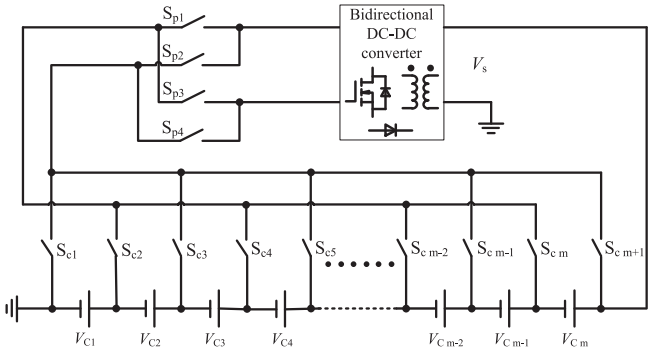


Fig. 1. Centralized structure charge equalization system with *m* cells.

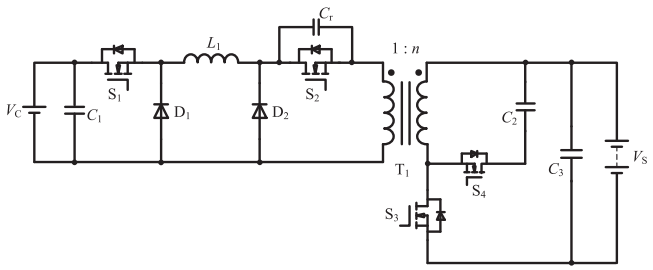


Fig. 2. Proposed quasi-resonant bidirectional dc–dc topology.

as that of the cells. The circuit proposed in [16] shares an inductor between two adjacent cells, which reduces the number of inductors; however, it increases the number of switches and diodes. A parallel multilevel charge equalizer that adopts multiple independent equalization circuits to achieve simultaneous equalization of different cells is proposed in [17]. The charge equalization technique proposed in [18] simplifies the control system, whereas in [19] a modularized integrated charge equalization method is proposed. However, these equalizers are not suitable for a system with a large number of cells because it suffers the disadvantages of complex structure, low reliability, and high cost.

The centralized charge equalization technology has been rapidly developed owing to the small number of converters and high reliability of the circuit. Fig. 1 shows an *m*-cell charge equalization system based on a centralized structure. The energy is transferred between the unbalanced cell and battery string through a bidirectional dc–dc converter. In this case, the bidirectional dc–dc converter is a critical part in the centralized structure charge equalization system. A bidirectional dc–dc converter based on a forward circuit is presented in [21]. Charge balance is realized by switching the switch array. However, in the discharge mode, the voltage spike caused by transformer leakage cannot be avoided, which may damage the devices. A centralized charge-balancing technique based on a bidirectional full-bridge structure is adopted in [22] and [23], whereas a bidirectional flyback dc–dc converter is used in [24] and [25]. However, these topologies suffer from the problem of many components and low efficiency. Harada and Sakamoto proposed a switched capacitor snubber circuit for high-frequency pulsewidth modulation (PWM) converters in [26], from which, both the main switch and the snubber-switch can achieve zero-voltage switching (ZVS)

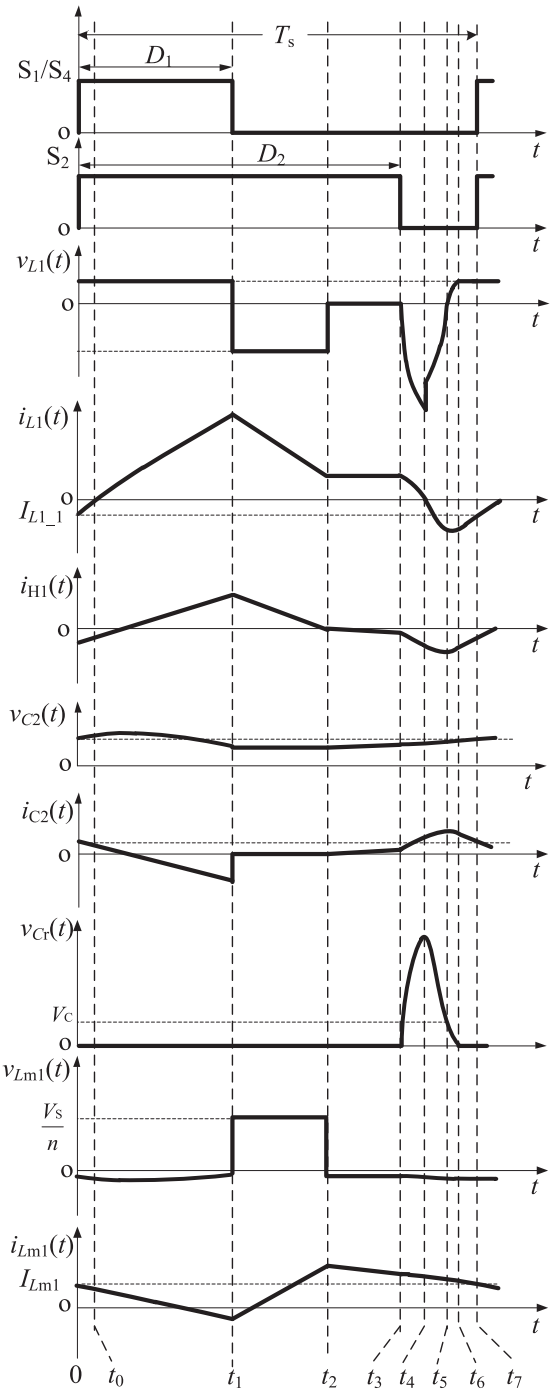


Fig. 3. Operating waveforms in the boost mode.

operation. This switched snubber technique is applicable to the switch and diode of any PWM converters and has been widely used in many applications. This paper is also inspired by the switched snubber presented in [26]. However, the snubber circuit in this paper does not contain the snubber-switch and has a simpler structure.

In this paper, an isolated bidirectional dc–dc converter for battery charge equalization is proposed. The proposed converter can achieve ZVS in both boost and buck modes through a quasi-resonance operation, which reduces the switching loss

and improves efficiency. Section II presents the operating principle and theoretical derivation of the proposed quasi-resonant bidirectional dc–dc converter. The ZVS analysis and parameter designs are discussed in Section III. The experimental results are provided in Section IV. Finally, conclusion is drawn in Section V.

II. Operating Principle and Theoretical Derivation of the Proposed Quasi-Resonant Bidirectional DC–DC Converter

Fig. 2 shows the quasi-resonant bidirectional dc–dc converter proposed in this paper, Fig. 2 shows that low-voltage side V_C is connected to a single lithium-ion cell, whereas high-voltage side V_S is connected to the battery string. The turn ratio of the transformer T_1 is 1:n. T_s denotes the switching cycle; thus, the switching frequency is expressed as $f_s = \frac{1}{T_s}$. During the charge equalization process, energy is transferred between the single cell and battery string.

A. Boost Mode

According to the control principle of charge equalization, when a single lithium-ion cell is overcharged, equalization is activated. In this case, the extra energy is transferred from the overcharged cell to the battery string, and the converter operates in the boost mode. Fig. 3 shows the main waveforms in one switching cycle in the boost mode, where D_1 is the duty cycle of switches S_1 and S_4 and D_2 is the duty cycle of switch S_2. We assume that the voltage across C_2 is constant and V_{C2_1} represents the voltage across C_2 in the boost mode; L_{m1} and L_{s1} represent the magnetizing and leakage inductances of transformer T_1 in the boost mode, respectively; and $i_{H1}(t)$ represents the current that flows through the high-voltage side of T_1 in the boost mode.

According to the operating waveforms shown in Fig. 3, the converter has eight stages in one switching cycle in the boost mode. Fig. 4 shows the specific working process.

Stage 1 [0–t$_0$]: At time zero, S_1, S_2, and S_4 are turned ON. At the end of the last switching cycle, the magnetizing current does not return to zero and flows through the body diodes of S_1 and S_2. The energy in magnetizing inductance L_{m1} is recycled to V_C. Thus, ZVS of S_1 and S_2 is achieved at time zero. During this stage, L_1 and L_{s1} are connected in series, and both of them freewheel through S_1, V_C, T_1, and S_2. We assume that I_{L1_1} represents the current value of inductor L_1 at the end of the last switching cycle and $I_{L1\_1} < 0$. Then, inductor current $i_{L1}(t)$ and leakage inductance current $i_{Ls1}(t)$ are expressed as follows:

$$i_{L1}(t) = i_{L_{s1}}(t) = I_{L1\_1} + \frac{nV_C + V_{C2\_1}}{n(L_1 + L_{s1})}t. \tag{1}$$

Because S_4 is turned ON, the voltage across L_{m1} is clamped to $\frac{V_{C2\_1}}{n}$. Thus, magnetizing current $i_{Lm1}(t)$ gradually decreases. By assuming that I_{Lm1} represents the current value of L_{m1} at the end of the last switching cycle, magnetizing current $i_{Lm1}(t)$ can then be expressed as follows:

$$i_{Lm1}(t) = I_{Lm1} - \frac{V_{C2\_1}}{nL_{m1}}t. \tag{2}$$

From (1) and (2), $i_{H1}(t)$ can be obtained by the following:

$$i_{H1}(t) = \frac{i_{L1}(t) - i_{Lm1}(t)}{n} = \frac{I_{L1\_1} - I_{Lm1}}{n} + \left[\frac{nV_C + V_{C2\_1}}{n^2(L_1 + L_{s1})} + \frac{V_{C2\_1}}{n^2 L_{m1}}\right]t. \tag{3}$$

When $i_{L1}(t)$ is reduced to zero, this stage ends, and the duration time of this stage can be calculated by the following:

$$t_0 = \frac{-nI_{L1\_1}(L_1 + L_{s1})}{nV_C + V_{C2\_1}}. \tag{4}$$

Stage 2 [t_0–t_1]: At t_0, L_1 and L_{s1} are still connected in series but are reversely charged by $(V_C + \frac{V_{C2\_1}}{n})$ through S_1, S_2, and S_4. $i_{L1}(t)$, $i_{Lm1}(t)$, and $i_{H1}(t)$ are still expressed as (1), (2), and (3), respectively.

Stage 3 [t_1–t_2]: At t_1, S_1 and S_4 are turned OFF and S_2 remains ON. L_1 and L_{s1} freewheel through S_2, V_S, the body diode of S_3, and diode D_1. Inductor current $i_{L1}(t)$ is expressed as follows:

$$i_{L1}(t) = i_{L_{s1}}(t) = i_{L1}(t_1) - \frac{V_S}{n(L_1 + L_{s1})}(t - t_1). \tag{5}$$

Because L_{m1} is charged by equivalent voltage $\frac{V_S}{n}$ in the low-voltage side of T_1, $i_{Lm1}(t)$ is expressed as follows:

$$i_{Lm1}(t) = i_{Lm1}(t_1) + \frac{V_S}{nL_{m1}}(t - t_1). \tag{6}$$

From (5) and (6), $i_{H1}(t)$can be obtained by the following:

$$i_{H1}(t) = \frac{i_{L1}(t) - i_{Lm1}(t)}{n} = \frac{i_{L1}(t_1) - i_{Lm1}(t_1)}{n} - \left[\frac{V_S}{n^2(L_1 + L_{s1})} + \frac{V_S}{n^2 L_{m1}}\right](t - t_1). \tag{7}$$

When $i_{H1}(t)$ is reduced to zero, this stage ends, and the duration time of this stage can be calculated by the following: eq. (8) shown at the bottom of this page.

Stage 4 [t_2–t_3]: At t_2, $v_{Lm1}(t)$ is clamped to $\frac{V_{C2\_1}}{n}$; thus, $i_{Lm1}(t)$ gradually decreases. Because the voltages across series-connected inductors L_1 and L_{s1} are relatively small, $i_{L1}(t)$ and i_{Ls1}(t) can be regarded as approximately constant. Therefore,

$$\begin{aligned} t_2 - t_1 &= \frac{nL_{m1}[i_{L1}(t_1) - i_{Lm1}(t_1)](L_1 + L_{s1})}{V_S L_{m1} + V_S L_1 + V_S L_{s1}} \\ &= \frac{nL_{m1}(I_{L1\_1} - I_{Lm1})(L_1 + L_{s1}) + [(nV_C + V_{C2\_1})L_{m1} + V_{C2\_1}(L_1 + L_{s1})]D_1 T_s}{V_S L_{m1} + V_S L_1 + V_S L_{s1}} \end{aligned} \tag{8}$$

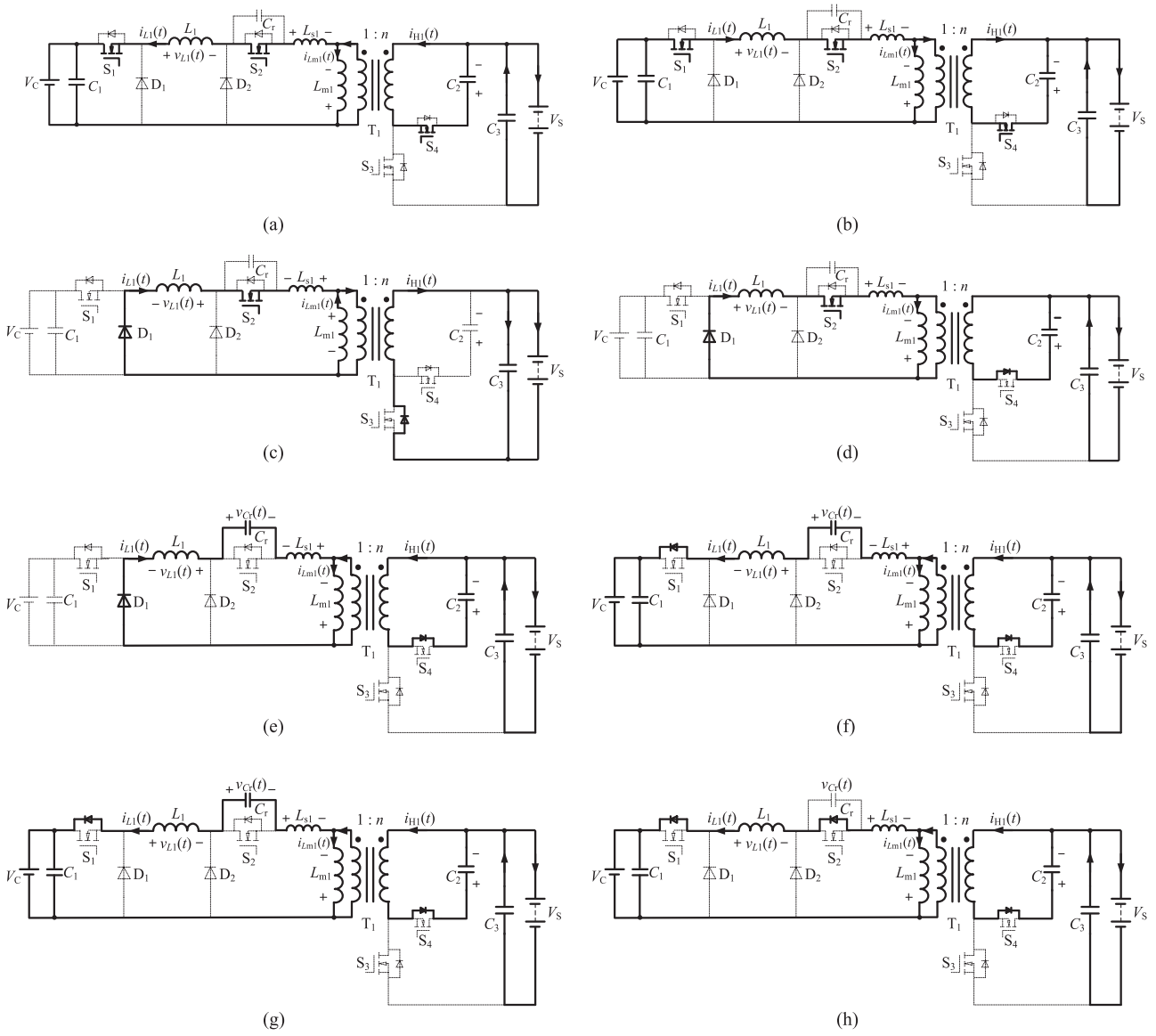


Fig. 4. Current-flow paths in the boost mode. (a) Stage 1 [0– t_0]. (b) Stage 2 [t_0–t_1]. (c) Stage 3 [t_1–t_2]. (d) Stage 4 [t_2–t_3]. (e) Stage 5 [t_3–t_4]; (f) Stage 6 [t_4–t_5]. (g) Stage 7 [t_5–t_6]. (h) Stage 8 [t_6–t_7].

$i_{L1}(t_3)$ can be obtained by the following:

$$i_{L1}(t_3) = i_{L1}(t_2) = I_{L1\_1} + \frac{nV_C + V_{C2\_1}}{n(L_1 + L_{s1})} \cdot D_1 T_s - \frac{V_S}{n(L_1 + L_{s1})}(t_2 - t_1). \tag{9}$$

Stage 5 [t_3–t_4]: At t_3, S_2 is turned OFF; then, C_2 is charged and $v_{Lm1}(t)$ is still clamped to $\frac{V_{C2\_1}}{n}$. In this case, the equivalent resonant inductor ($L_1 + L_{s1}$) and the equivalent resonant capacitor C_r resonate. The energy in L_1 and L_{s1} is transferred to C_r. Resonant current $i_{L1}(t)$ and resonant voltage $v_{\mathrm{Cr}}(t)$ can be expressed as follows:

$$\begin{cases} (L_1 + L_{s1})\frac{di_{L1}(t)}{dt} + v_{\mathrm{Cr}}(t) = \frac{v_{C2\_1}}{n} \\ C_r \frac{dv_{\mathrm{Cr}}(t)}{dt} = i_{L1}(t). \end{cases} \tag{10}$$

From (10), resonant current $i_{L1}(t)$ and resonant voltage $v_{\mathrm{Cr}}(t)$ are respectively calculated using

$$i_{L1}(t) = i_{L_{s1}}(t) = i_{L1}(t_3)\cos[\omega_o(t - t_3)] + \frac{V_{C2\_1}}{nz_o}\sin[\omega_o(t - t_3)] \tag{11}$$

$$v_{\mathrm{Cr}}(t) = \frac{V_{C2\_1}}{n} - \frac{V_{C2\_1}}{n}\cos[\omega_o(t - t_3)] + z_o i_{L1}(t_3)\sin[\omega_o(t - t_3)] \tag{12}$$

where z_o is the characteristic impedance and w_o is the resonant angular frequency; they are expressed as follows:

$$z_o = \sqrt{\frac{L_1 + L_{s1}}{C_r}} \tag{13}$$

$$w_o = 2\pi f_r \tag{14}$$

$$f_r = \frac{1}{2\pi\sqrt{(L_1 + L_{s1})C_r}}. \tag{15}$$

When $i_{L1}(t)$ drops to zero, this stage ends, and the duration time of this stage can be calculated by

$$t_4 - t_3 = \frac{1}{2f_r} - \frac{1}{w_o} \cdot \arctan\frac{nz_o i_{L1}(t_3)}{V_{C2\_1}}. \tag{16}$$

Stage 6 [t_4–t_5]: At t_4, $i_{L1}(t)$ drops to zero and $v_{\mathrm{Cr}}(t)$ reaches its maximum. Then, C_r begins to discharge through L_1, L_{s1}, the body diode of S_1, V_C, and T_1. L_1 is reversely charged, and $i_{L1}(t)$ increases. The resonant tank also includes $(L_1 + L_{s1})$ and C_r. Resonant current $i_{L1}(t)$ and resonant voltage $v_{\mathrm{Cr}}(t)$ are respectively expressed as follows:

$$i_{L1}(t) = i_{L_{s1}}(t) = \frac{nV_C + V_{C2\_1} - nV_{\mathrm{Cr}}(t_4)}{nz_o}\sin[\omega_o(t - t_4)] \tag{17}$$

$$v_{\mathrm{Cr}}(t) = V_C + \frac{V_{C2\_1}}{n} - \left[V_C + \frac{V_{C2\_1}}{n} - V_{Cr}(t_4)\right] \times \cos[\omega_o(t - t_4)]. \tag{18}$$

When $v_{\mathrm{Cr}}(t)$ drops to $(V_C + \frac{V_{C2\_1}}{n})$, this stage ends. The duration time of this stage is calculated by the following:

$$t_5 - t_4 = \frac{1}{4f_r}. \tag{19}$$

Stage 7 [t_5–t_6]: At t_5, C_r is still discharged, and $i_{L1}(t)$ decreases. The expressions of $i_{L1}(t)$ and $v_{\mathrm{Cr}}(t)$ are the same as those in Stage 6. When $v_{\mathrm{Cr}}(t)$ drops to zero, this stage ends, and the duration time of this stage is calculated by the following:

$$t_6 - t_5 = \frac{1}{w_o} \cdot \arcsin\frac{nV_C + V_{C2\_1}}{nV_{\mathrm{Cr}}(t_4) - (nV_C + V_{C2\_1})}. \tag{20}$$

Then, the inductor current value $i_{L1}(t_6)$ is calculated by the following:

$$i_{L1}(t_6) = i_{L_{s1}}(t_6) = -\frac{\sqrt{n^2V_{\mathrm{Cr}}^2(t_4) - 2n(nV_C + V_{C2\_1})V_{Cr}(t_4)}}{nz_o}. \tag{21}$$

Stage 8 [t_6–t_7]: Because $i_{L1}(t)$ has not decreased to zero at t_6, L_1 will freewheel through the body diodes of S_1 and S_2. In this stage, $i_{L1}(t)$ is expressed as follows:

$$i_{L1}(t) = i_{L_{s1}}(t) = i_{L1}(t_6) + \frac{nV_C + V_{C2\_1}}{n(L_1 + L_{s1})}(t - t_6). \tag{22}$$

From (16), (19), and (20), the duration time of this stage is calculated by the following:

$$t_7 - t_6 = T_s - D_2T_s - (t_6 - t_3) = T_s - D_2T_s - \left[\frac{1}{2f_r} - \frac{1}{w_o} \cdot \arctan\frac{nz_o i_{L1}(t_3)}{V_{C2\_1}}\right] - \frac{1}{4f_r} - \left[\frac{1}{w_o} \cdot \arcsin\frac{nV_C + V_{C2\_1}}{nV_{Cr}(t_4) - (nV_C + V_{C2\_1})}\right]. \tag{23}$$

When one switching cycle ends, the inductor current value $i_{L1}(t_7)$ and magnetizing current value $i_{L1}(t_7)$ can be respectively calculated by the following:

$$I_{L1\_1} = i_{L1}(t_7) = i_{L_{s1}}(t_7) = i_{L1}(t_6) + \frac{nV_C + V_{C2\_1}}{n(L_1 + L_{s1})}(t_7 - t_6) \tag{24}$$

$$I_{Lm1} = i_{Lm1}(t_7) = i_{Lm1}(t_2) - \frac{V_{C2\_1}}{nL_{m1}}(t_7 - t_2). \tag{25}$$

Applying the volt–second balance law to L_{m1} during a switching cycle yields the following:

$$\frac{V_S}{nL_{m1}}(t_2 - t_1) = \frac{V_{C2\_1}}{nL_{m1}}[T_s - (t_2 - t_1)]. \tag{26}$$

From (26), (t_2–t_1) is calculated by the following:

$$t_2 - t_1 = \frac{V_{C2\_1}}{(V_{C2\_1} + V_S)f_s}. \tag{27}$$

We assume that

$$z_o i_{L1}(t_3) = k\left(V_C + \frac{V_{C2\_1}}{n}\right). \tag{28}$$

By substituting (27) and (28) into (9), substituting (21), (23), and (28) into (24), and combining (9) and (24), k can be obtained by (30) shown at the bottom of this page.

$$k = f^{-1}(D_1). \tag{29}$$

By substituting (27) and (28) into (9) and substituting (27) and (28) into (25), I_{L1_1} and I_{Lm1} can be respectively expressed

$$D_1 = f(k) = \frac{kf_s}{2\pi f_r} + \frac{f_s\sqrt{k^2 - 2k}}{2\pi f_r} + \frac{V_{C2\_1}V_S}{(V_{C2\_1} + V_S)(nV_C + V_{C2\_1})} - \left[1 - D_2 - \frac{3f_s}{4f_r} - \frac{f_s}{2\pi f_r}\arcsin\left(\frac{1}{k-1}\right) + \frac{f_s}{2\pi f_r}\arctan\left(\frac{nkV_C + kV_{C2\_1}}{V_{C2\_1}}\right)\right] \tag{30}$$

by the following:

$$I_{L1\_1} = \frac{k(nV_C + V_{C2\_1})}{nz_o} - \frac{nV_C + V_{C2\_1}}{n(L_1 + L_{s1})} \cdot \frac{D_1}{f_s} + \frac{V_S V_{C2\_1}}{n(L_1 + L_{s1})(V_{C2\_1} + V_S) f_s} \quad (31)$$

$$I_{Lm1} = \frac{k(nV_C + V_{C2\_1})}{nz_o} - \frac{V_{C2\_1}}{nL_{m1}} \times \left[\frac{1}{f_s} - \frac{V_{C2\_1}}{(V_{C2\_1} + V_S) f_s} - \frac{D_1}{f_s}\right]. \quad (32)$$

Applying the volt–second balance law to L_1 during a switching cycle yields the following:

$$\frac{D_1}{f_s}\left(V_C + \frac{V_{C2\_1}}{n}\right) - \frac{V_S}{n}(t_2 - t_1) + \int_{t_3}^{t_6} v_{L1}(t)dt + \left(V_C + \frac{V_{C2\_1}}{n}\right)(t_7 - t_6) = 0. \quad (33)$$

By substituting (23) and (27) into (33), V_{C2_1} can be expressed as (34) shown at the bottom of this page, where $\delta = \frac{D_1 + 1 - D_2}{f_s} - \frac{2+k}{4f_r}$.

In the above discussion, leakage inductance L_{s1} is always connected in series to L_1, and the energy in L_{s1} is released to the output side, which reduces the voltage spike. When the proposed converter operates in the boost mode, quasi-resonance occurs among L_1, L_{s1}, and C_r. In this case, the magnetizing current can return to zero in each switching cycle, which avoids saturation of the transformer core. Moreover, the quasi-resonance operation makes S_1, S_2, and S_4 realize ZVS and greatly reduces the switching loss.

B. Buck Mode

When a single cell is detected to be in an undercharged state, energy needs to be transferred from the battery string to the unbalanced cell. In this case, the proposed converter operates in the buck mode. Fig. 5 shows the main waveforms in the buck mode, where D_3 is the duty cycle of switches S_1, S_2, and S_3, whereas D_4 is the duty cycle of clamping switch S_4. τ is the delay time between the gate drive signal of S_4 and that of S_3. L_{m2} represents the magnetizing inductance in the buck mode, and $L_{m2} = n^2 L_{m1}$. L_{s2} represents the leakage inductance in the buck mode, and $L_{s2} = n^2 L_{s1}$. C_{DS3} represents the drain–source capacitance of S_3. We assume that the clamping capacitor C_2 is sufficiently large and the voltage across C_2 is a constant value, namely, V_{C2_2}. $i_{S\_2}(t)$ represents the input current in the buck mode.

According to the operating waveforms shown in Fig. 5, each switching cycle is divided into ten stages when the converter operates in the buck mode. The current-flow paths in the buck mode are shown in Fig. 6.

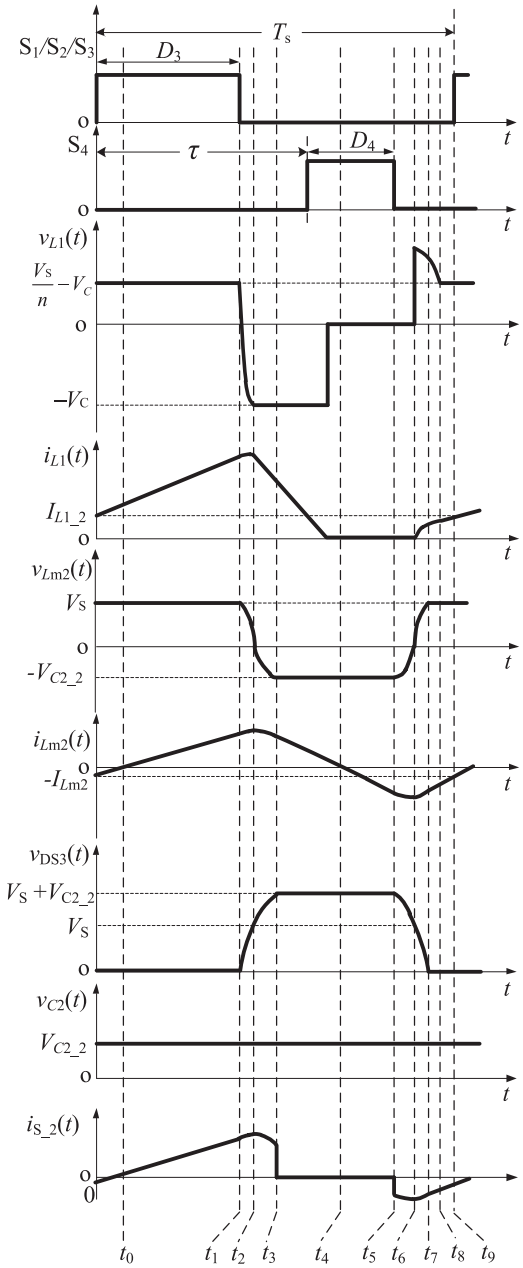


Fig. 5. Operating waveforms in the buck mode.

Stage 1 [0–t_0]: At time zero, S_1, S_2, and S_3 are turned ON. However, the current flows through the body diodes of S_1, S_2, and S_3 because the magnetizing current $i_{Lm2}(t)$ has not dropped to zero at the end of the last switching cycle. In this case, S_1, S_2, and S_3 can achieve ZVS. The energy in magnetizing inductance L_{m2} is recycled to V_S. In this stage, L_1 is charged because the voltage in the low-voltage side of T_1 is clamped to $\frac{V_S}{n}$. We assume that I_{L1_2} and $-I_{Lm2}$ represent the current values of L_1 and L_{m2} at the end of the last switching cycle, respectively.

$$V_{C2\_1} = \frac{V_S T_s - \delta n V_C - \delta V_S - \sqrt{(\delta n V_C + \delta V_S - V_S T_s)^2 - 4\delta^2 n V_C V_S}}{2\delta} \quad (34)$$

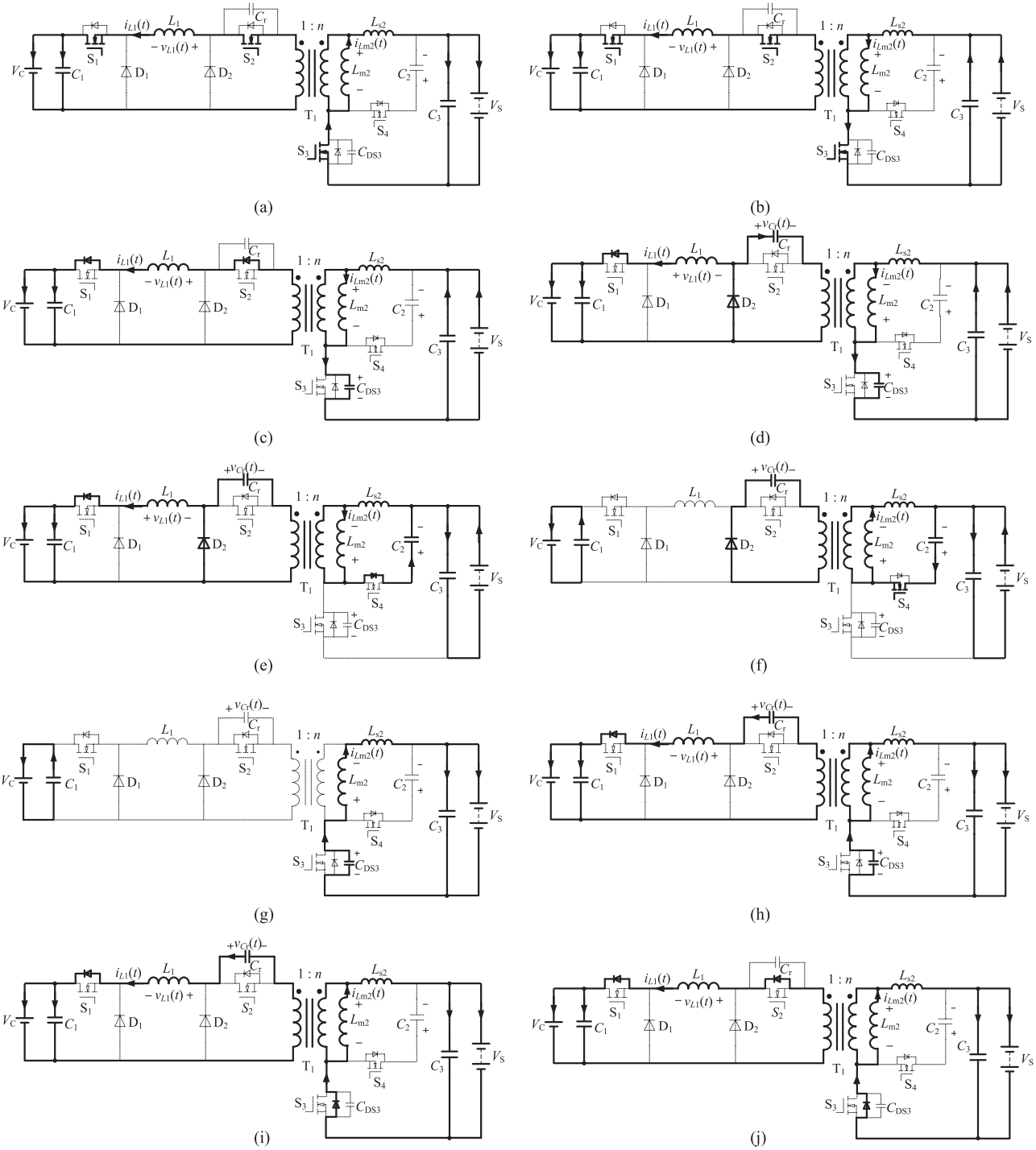


Fig. 6. Current-flow paths in the buck mode. (a) Stage 1 [0–t_0]. (b) Stage 2 [t_0–t_1]. (c) Stage 3 [t_1–t_2]. (d) Stage 4 [t_2–t_3]. (e) Stage 5 [t_3–t_4]. (f) Stage 6 [t_4–t_5]. (g) Stage 7 [t_5–t_6]. (h) Stage 8 [t_6–t_7]. (i) Stage 9 [t_7–t_8]. (j) Stage 10 [t_8–t_9].

Because L_{s2} is much smaller than L_{m2}, then $i_{L1}(t)$, $i_{Lm2}(t)$, and $i_{Ls2}(t)$ are approximately expressed respectively as follows:

$$i_{L1}(t) = I_{L1\_2} + \left(\frac{V_S}{nL_1} - \frac{V_C}{L_1}\right)t \tag{35}$$

$$i_{Lm2}(t) = -I_{Lm2} + \frac{V_S}{L_{m2}}t \tag{36}$$

$$i_{Ls2}(t) = \frac{i_{L1}(t)}{n} + i_{Lm2}(t) = \frac{I_{L1\_2}}{n} - I_{Lm2} + \left(\frac{V_S}{n^2L_1} - \frac{V_C}{nL_1} + \frac{V_S}{L_{m2}}\right)t. \tag{37}$$

Stage 2 [t_0–t_1]: At t_0, L_1 continues to be charged and $i_{Lm2}(t)$ starts to increase in the positive direction. At t_1, the magnetizing

current value $i_{Lm2}(t_1)$ is obtained by

$$i_{Lm2}(t_1) = \frac{V_S t_1}{L_{m2}} - I_{Lm2}. \tag{38}$$

Stage 3 [t_1–t_2]: At t_1, S_3 is turned OFF, C_{DS3} is charged, and $v_{DS3}(t)$ gradually increases. In this stage, $v_{Lm2}(t)$ is still greater than zero; thus, $i_{Lm2}(t)$ continues to increase, but the slope decreases. In this case, diode D_2 is reversed biased, and the body diode of S_2 is still forward biased. During this stage, the resonant tank consists of L_{m2}, L_{s2}, and resonant capacitor C_{DS3}. Resonant current $i_{Ls2}(t)$ and resonant voltage $v_{\mathrm{CDS3}}(t)$ are respectively expressed as follows:

$$i_{L_{s2}}(t) = i_{L_{s2}}(t_1)\cos[\omega_{o1}(t-t_1)] + \frac{V_S}{z_{o1}}\sin[\omega_{o1}(t-t_1)] \tag{39}$$

$$v_{\mathrm{DS3}}(t) = V_S - V_S\cos[\omega_{o1}(t-t_1)] + i_{L_{s2}}(t_1) z_{o1}\sin[\omega_{o1}(t-t_1)] \tag{40}$$

where z_{o1} is the characteristic impedance and w_{o1} is the resonant angular frequency. They are expressed as follows:

$$z_{o1} = \sqrt{\frac{L_{m2}+L_{s2}}{C_{\mathrm{DS3}}}} \tag{41}$$

$$w_{o1} = 2\pi f_{r1} \tag{42}$$

$$f_{r1} = \frac{1}{2\pi\sqrt{(L_{m2}+L_{s2})C_{\mathrm{DS3}}}}. \tag{43}$$

Then, $v_{Lm2}(t)$, $v_{L1}(t)$, $i_{L1}(t)$, and $i_{Lm2}(t)$ can be respectively expressed as follows:

$$v_{Lm2}(t) = V_S - v_{\mathrm{DS3}}(t) \tag{44}$$

$$v_{L1}(t) = \frac{v_{Lm2}(t)}{n} - V_C \tag{45}$$

$$i_{L1}(t) = i_{L1}(t_1) + \int_{t_1}^{t}\left(\frac{v_{Lm2}(t)}{nL_1} - \frac{V_C}{L_1}\right)dt \tag{46}$$

$$i_{Lm2}(t) = i_{Ls2}(t) - \frac{i_{L1}(t)}{n}. \tag{47}$$

Stage 4 [t_2–t_3]: At t_2, $v_{DS3}(t)$ increases to V_S. After t_2, $v_{DS3}(t)$ continues to increase, and $i_{Lm2}(t)$ begins to decrease. Because $v_{Lm2}(t)$ is less than zero, the body diode of S_2 is reversed biased, and C_r is charged with a small current. In this stage, resonant current $i_{Ls2}(t)$ and resonant voltage $v_{\mathrm{CDS3}}(t)$ can be respectively expressed as follows:

$$i_{Ls2}(t) = i_{Ls2}(t_2)\cos[\omega_{o1}(t-t_2)] \tag{48}$$

$$v_{\mathrm{DS3}}(t) = V_S + i_{Lm2}(t_2) z_{o1}\sin[\omega_{o1}(t-t_2)]. \tag{49}$$

Meanwhile, L_1 freewheels through V_C, diode D_2, and the body diode of S_1; then, $i_{L1}(t)$ is expressed as follows:

$$i_{L1}(t) = i_{L1}(t_2) - \frac{V_C}{L_1}\cdot(t-t_2). \tag{50}$$

Stage 5 [t_3–t_4]: At t_3, $v_{DS3}(t)$ increases to $(V_S + V_{C2\_2})$. At this point, the body diode of S_4 begins to conduct. Then, L_{m2} and L_{s2} resonate with C_2. Because the resonant cycle is much longer than the switching cycle, $v_{C2}(t)$ only slightly fluctuates. Resonant current $i_{Lm2}(t)$ and resonant voltage $v_{C2}(t)$ can be respectively expressed as follows:

$$i_{Lm2}(t) = i_{L_{s2}}(t) = i_{Lm2}(t_3)\cos[\omega_{o2}(t-t_3)] - \frac{V_S + V_{C2\_2}}{z_{o2}}\sin[\omega_{o2}(t-t_3)] \tag{51}$$

$$v_{C2}(t) = (V_S + V_{C2\_2})\cos[\omega_{o2}(t-t_3)] + z_o i_{Lm2}(t_3)\sin[\omega_{o2}(t-t_3)] \tag{52}$$

where z_{o2} is the characteristic impedance and w_{o2} is the resonant angular frequency. They are expressed as follows:

$$z_{o2} = \sqrt{\frac{L_{m2}+L_{s2}}{C_2}} \tag{53}$$

$$w_{o2} = 2\pi f_{r2} \tag{54}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_{m2}+L_{s2})C_2}}. \tag{55}$$

Because the body diode of S_4 is always in a conducting state, S_4 can achieve ZVS when S_4 is turned ON at any time in this stage.

Stage 6 [t_4–t_5]: At t_4, $i_{Lm2}(t)$ drops to zero. Thereafter, L_{m2} is reversely charged, and $i_{Lm2}(t)$ increases. $V_{\mathrm{Cr}}(t)$ is clamped to $\frac{v_{C2}(t)}{n}$. Resonant current $i_{Lm2}(t)$ and resonant voltage $v_{C2}(t)$ can also be expressed as (51) and (52), respectively.

Stage 7 [t_5–t_6]: At t_5, clamping switch S_4 is turned OFF. L_{m2} freewheels through V_S and C_{DS3}; then, $i_{Lm2}(t)$ begins to decrease. Simultaneously, C_{DS3} begins to discharge, and $v_{DS3}(t)$ decreases. $v_{Lm2}(t)$ gradually decreases from V_{C2_2}; thus, diode D_2 is reversed biased. Because L_1 operates in the discontinuous conduction mode, $i_{L1}(t)$ drops to zero at t_5. In this stage, the resonant tank is composed of L_{m2}, L_{s2}, and resonant capacitor C_{DS3}. Then, resonant current $i_{Lm2}(t)$ and resonant voltage $v_{CDS3}(t)$ are respectively expressed as follows:

$$i_{Lm2}(t) = i_{L_{s2}}(t) = i_{Lm2}(t_5)\cos[\omega_{o1}(t-t_5)] - \frac{V_{C2\_2}}{z_{o1}}\sin[\omega_{o1}(t-t_5)] \tag{56}$$

$$v_{\mathrm{DS3}}(t) = V_S + V_{C2\_2}\cos[\omega_{o1}(t-t_5)] + z_{o1} i_{Lm2}(t_5)\sin[\omega_{o1}(t-t_5)]. \tag{57}$$

Then, $v_{Lm2}(t)$ can be expressed as follows:

$$v_{Lm2}(t) = V_S - v_{\mathrm{DS3}}(t). \tag{58}$$

Stage 8 [t_6–t_7]: At t_6, $V_{DS3}(t)$ drops to V_S, and the voltage at the high-voltage side of T_1 is positive. Then, C_r starts to discharge and L_1 is charged. During this stage, resonant current $i_{Lm2}(t)$, resonant voltage $v_{C\mathrm{DS3}}(t)$, and $v_{Lm2}(t)$ are still expressed as (56), (57), and (58), respectively. Because the voltage at the low-voltage side of T_1 is clamped, L_1 is charged and C_r discharges.

Stage 9 [t_7–t_8]: At t_7, C_{DS3} finishes discharging, and $v_{DS3}(t)$ drops to zero. The voltage in the low-voltage side of T_1 is clamped to $\frac{V_S}{n}$; thus, the body diode of S_3 is forward biased. However, C_r has not finished discharging, which makes

the body diode of S_2 have a reversed bias. Then, $i_{Lm2}(t)$ is expressed as follows:

$$i_{Lm2}(t) = i_{Lm2}(t_7) + \frac{V_S}{L_{m2}}(t - t_7). \tag{59}$$

In this stage, L_1 resonates with C_r, and resonant current $i_{L1}(t)$ and resonant voltage $v_{\rm Cr}(t)$ can be respectively expressed as follows:

$$i_{L1}(t) = i_{L1}(t_7)\cos[\omega_{o3}(t - t_7)] + \frac{V_S - nV_C - nv_{\rm cr}(t_7)}{nz_{o3}}\sin[\omega_{o3}(t - t_7)] \tag{60}$$

$$v_{\rm cr}(t) = \frac{V_S}{n} - V_C - \left[\frac{V_S}{n} - V_C - v_{cr}(t_7)\right]\cos[\omega_{o3}(t - t_7)] + z_{o3}i_{L1}(t_7)\sin[\omega_{o3}(t - t_7)] \tag{61}$$

where z_{o3} is the characteristic impedance and w_{o3} is the resonant angular frequency. They are expressed as follows:

$$z_{o3} = \sqrt{\frac{L_1}{C_r}} \tag{62}$$

$$w_{o3} = 2\pi f_{r3} \tag{63}$$

$$f_{r3} = \frac{1}{2\pi\sqrt{L_1 C_r}}. \tag{64}$$

Stage 10 [t_8–t_9]: At t_8, C_r finishes discharging, and the body diode of S_2 is forward biased. At t_9, S_3 is turned ON, and the next switching cycle begins. In this case, $i_{Lm2}(t)$ has not dropped to zero, which makes the body diode of S_3 always remain forward biased. Therefore, S_1, S_2, and S_3 can achieve ZVS. $i_{Lm2}(t)$ can be expressed as (59), whereas $i_{L1}(t)$ is expressed as follows:

$$i_{L1}(t) = i_{L1}(t_8) + \left[\frac{V_S - nV_C}{nL_1}\right](t - t_8). \tag{65}$$

By applying the volt–second balance law to L_{m2} during one switching cycle, V_{C2_2} can be expressed as follows:

$$V_{C2\_2} = \frac{D_3 V_S}{1 - D_3}. \tag{66}$$

According to the operating principle of the proposed converter in the buck mode, in each switching cycle, ZVS of switches S_1, S_2, S_3, and S_4 can be realized through the quasi-resonance operation that occurs among L_{m2}, C_{DS3}, and C_2. In this case, a full range of ZVS can be achieved. Simultaneously, the magnetizing current can return to zero, and the magnetic remanence is eliminated. Moreover, the voltage spike caused by the leakage inductance can be suppressed because of the quasi-resonant operation through the active clamping network.

III. ZVS Analysis and Parameter Design

A. ZVS Conditions in the Boost Mode

According to the operating principle in the boost mode, S_1, S_2, and S_4 can achieve ZVS, whereas S_3 is always turned OFF. To achieve ZVS in S_4, we need to ensure that the current in the high-voltage side of T_1 is less than zero, that is, $i_{H1}(0) = \frac{i_{L1}(0) - i_{Lm1}(0)}{n} < 0$. Fig. 3 shows that at time zero, $i_{Lm1}(0)$ is always greater than zero; thus, only by ensuring $i_{L1}(0) = I_{L1\_1} < 0$ can we guarantee that C_2 is always charging through the body diode of S_4 at the beginning of each switching cycle when S_4 can achieve ZVS in the boost mode.

The ZVS operations of S_1 and S_2 occur when a current flows through the body diodes of S_1 and S_2 before they are turned ON, namely, $i_{L1}(0) = I_{L1\_1} < 0$. Assuming that the average discharging current of a single lithium-ion battery is $I_{\rm discharge}$, then $I_{\rm discharge}$ can be calculated by

$$\begin{aligned} I_{\rm discharge} &= \frac{1}{T_s}\left[\int_0^{t_1} i_{L1}(t)dt + \int_{t_4}^{t_7} i_{L1}(t)dt\right] \\ &= I_{L1\_1}D_1 + \frac{{D_1}^2(nV_C + V_{C2\_1})}{2n(L_1 + L_{s1})f_s} \\ &\quad - \frac{(k-1)(nV_C + V_{C2\_1})f_s C_r}{n\pi}. \end{aligned} \tag{67}$$

From (67), I_{L1_1} can be expressed as follows:

$$I_{L1\_1} = \frac{I_{\rm discharge}}{D_1} - \frac{D_1(nV_C + V_{C2\_1})}{2nf_s(L_1 + L_{s1})} + \frac{f_s C_r(k-1)(nV_C + V_{C2\_1})}{n\pi D_1}. \tag{68}$$

Let $I_{L1\_1} < 0$. Then, the ZVS conditions of switches S_1, S_2, and S_4 in the boost mode are expressed as follows:

$$(L_1 + L_{s1}) < \frac{{D_1}^2(nV_C + V_{C2\_1})\pi}{2\pi n I_{\rm discharge} f_s + 2f_s^2(k-1)(nV_C + V_{C2\_1})C_r}. \tag{69}$$

By substituting the parameters listed in Table I into (69), the ZVS boundary curve can be obtained as shown in Fig. 7, which shows the ZVS region and the maximum discharge current with respect to L_1 and L_{s1}. Fig. 7 shows that the smaller the value of $(L_1 + L_{s1})$ is, the larger are the maximum discharge current and the ZVS region. Because the discharge current is 2 A in the experiments in this study, the ZVS of all switches can be guaranteed from no load to full load only by satisfying $(L_1 + L_{s1}) < 25$ μH in the boost mode.

B. ZVS Conditions in the Buck Mode

According to the operating principle and the waveforms shown in Fig. 5 in the buck mode, L_1 is always charging at the end of each switching cycle. Then, $i_{L1}(0) > 0$ is satisfied at the starting time of the next cycle, that is, current flows through the body diodes of S_1 and S_2 before they are turned ON. Therefore, ZVS of S_1 and S_2 can always be achieved in the entire operating range.

The ZVS condition of switch S_4 is $i_{Lm2}(\tau) > 0$, as shown in Fig. 5. Thus, we only need to adjust the turning-OFF to turning-ON interval time between S_3 and S_4 to be greater than the charging time of the drain–source capacitance of S_4, namely, $(\tau - D_3T_s) > (t_3 - t_1)$. From (40) and (49), the range of τ can be expressed as follows:

$$\tau > D_3T_s + \frac{1}{2f_{r1}}. \tag{70}$$

TABLE I
PARAMETERS OF THE PROPOSED BIDIRECTIONAL DC–DC CONVERTER

Parameters		Values/Ratings
Rated voltage in low voltage side (V_C)		3.7 V
Rated voltage in high voltage side (V_S)		48.1 V
Switching frequency (f_s)		20 kHz
Inductors	L_1	5 μH; Fe-Si-Al magnetic core, CS172125; Turns = 8
	L_f	25 μH; Fe-Si-Al magnetic core, CS172125; Turns = 17
Transformer T_1		Ferroxcube PC44/PQ3230 ferrite core; Turns ratio (1 : n) = 1 : 6; Primary turns N_1 = 5; Secondary turns N_2 = 30; Air gap δ = 3.1 mm; Magnetizing inductance L_{m2} = 65 μH; Leakage inductance L_{s2} = 7 μH
Capacitors	C_1	1 mF/16 V, solid-state capacitor
	C_2	4.7 μF/100 V, polypropylene film capacitor
	C_3	100 μF/100 V, aluminum electrolytic capacitor
	C_r	470 nF/100 V, polypropylene film capacitor
	C_f	1 mF/16 V, aluminum electrolytic capacitor
MOSFETs	S_1, S_2	IRF1010ZSPbF V_{DSS} = 55 V, I_D = 75 A, $R_{DS(on)}$ = 7.5 mΩ
	S_3, S_4	IRF540ZSPbF V_{DSS} = 100 V, I_D = 36 A, $R_{DS(on)}$ = 26.5mΩ
	S_{p1}–S_{p4}, S_{c1}–S_{c14}	IRF7862PbF V_{DSS} = 30 V, I_D = 21 A, $R_{DS(on)}$ = 3.3 mΩ
Diodes	D_1, D_2	STPS40L45CG V_{RRM} = 45 V, $I_{F(AV)}$ = 40 A, V_F = 0.49 V

Therefore, by controlling τ to satisfy (70), S_4 can achieve ZVS. In this paper, τ is selected as $0.5\,T_s$.

In order to ensure that the magnetizing current returns to zero within one switching cycle and achieves ZVS of S_3, S_4 must be in conducted state until the current flowing through the magnetizing inductance L_{m2} becomes in the reverse direction. It means $i_{Lm2}(t) < 0$ at $t = \tau + D_4T_s$. As shown in Fig. 5, it can be expressed as follows:

$$D_4T_s > t_4 - t_3. \tag{71}$$

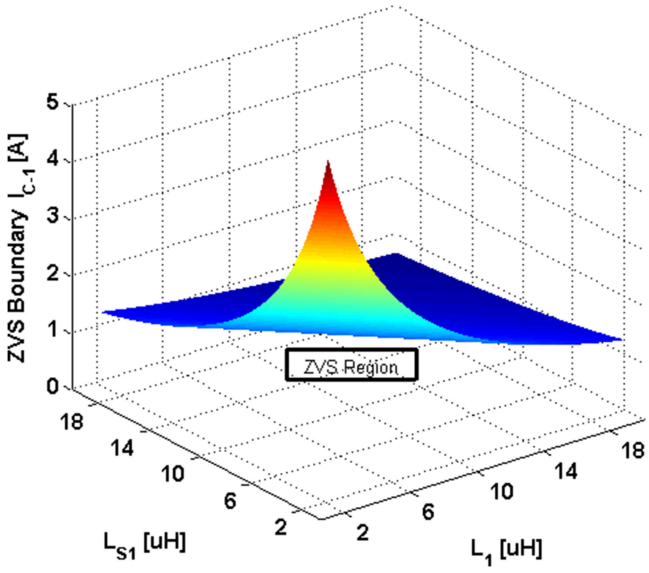


Fig. 7. ZVS boundary according to L_1 and L_{s1} in the boost mode.

From (51) and (36), the duration time of stage 5 and $i_{Lm2}(t_3)$ can be calculated as follows:

$$\begin{cases} t_4 - t_3 = \frac{1}{\omega_{o2}} \arctan \frac{i_{Lm2}(t_3) z_{o2}}{V_S + V_{C2\_2}} \\ i_{Lm2}(t_3) = -I_{Lm2} + \frac{V_S}{L_{m2}} D_3 T_s. \end{cases} \tag{72}$$

By substituting (72) into (71), the range of D_4 can be expressed as follows:

$$D_4 > \frac{f_s}{\omega_{o2}} \arctan \frac{(V_S - L_{m2} I_{Lm2}) D_3 T_s z_{o2}}{L_{m2}(V_S + V_{C2\_2})}. \tag{73}$$

By substituting the experimental parameters into (73), D_4 is set as 0.4 in this study.

To achieve ZVS of S_3 in the buck mode, we only need to satisfy $i_{S\_2}(0) < 0$. Assuming that the average charging current of a single lithium-ion battery is I_{charge} and the average input current in the buck mode is I_{S_2}, then $I_{S\_2} = \frac{V_C I_{\text{charge}}}{V_S}$. From Fig. 6, I_{S_2} can be calculated by

$$\begin{aligned} I_{S\_2} &= \frac{1}{T_s}\left[\int_0^{t_3} i_{S\_2}(t)dt + \int_{t_5}^{t_9} i_{S\_2}(t)dt\right] \\ &\approx \frac{1}{T_s}\left[\int_0^{T_s - \tau - D_4T_s + D_3T_s} \left[i_{S\_2}(t_5) + \frac{V_S - nV_C}{n^2 L_1} t + \frac{V_S}{L_{m2}} t\right] dt. \end{aligned} \tag{74}$$

Then, $i_{S\_2}(0)$ can be expressed as follows:

$$\begin{aligned} i_{S\_2}(0) &= i_{S\_2}(t_5) + (T_s - \tau - D_4T_s)\left(\frac{V_S - nV_C}{n^2 L_1} + \frac{V_S}{L_{m2}}\right) \\ &= \frac{V_C I_{\text{charge}} T_s}{V_S(T_s - \tau - D_4T_s + D_3T_s)} \\ &\quad + (T_s - \tau - D_4T_s - D_3T_s)\left(\frac{V_S - nV_C}{2n^2 L_1} + \frac{V_S}{2L_{m2}}\right). \end{aligned} \tag{75}$$

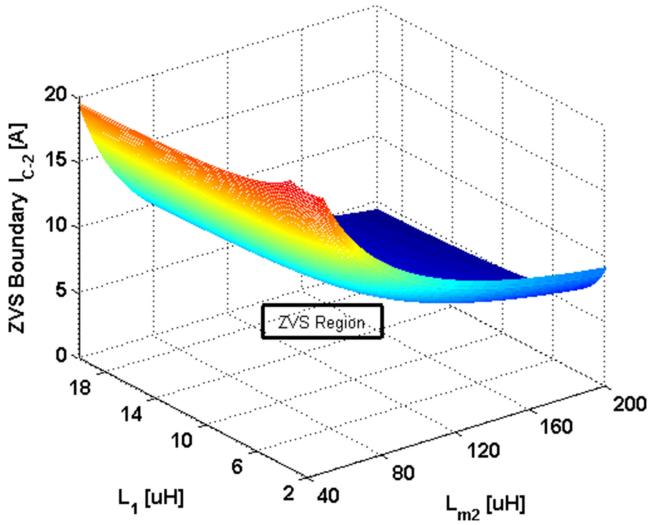


Fig. 8. ZVS boundary according to L_1 and L_{m2} in the buck mode.

The ZVS condition of switch S_3 in the buck mode is $i_{S\_2}(0) < 0$, then, from (75), the condition is given by the following:

$$I_{\text{charge}} < \left(\frac{V_S - nV_C}{n^2 L_1} + \frac{V_S}{L_{m2}}\right)\frac{V_S f_s}{2V_C} \times (T_s - \tau - D_4 T_s + D_3 T_s) \times (\tau + D_4 T_s + D_3 T_s - T_s). \quad (76)$$

By substituting the parameters listed in Table I into (76), the ZVS boundary curve and ZVS region can be obtained and shown in Fig. 8. Fig. 8 shows that the maximum equalizing charge current can reach a larger value by adjusting the values of L_1 and L_{m2} to achieve a wide ZVS region. Because the equalizing charge current is 3 A in the experiments in this study, by substituting the parameters listed in Table I, $D_3 = 0.25$, $D_4 = 0.4$, $\tau = 0.5T_s$, and $I_{\text{charge}} = 3$ A into (76), the ZVS of S_3 can be guaranteed by satisfying $(\frac{1}{L_1} + \frac{72}{L_{m2}}) > 2.86 \times 10^5$ H^{-1} in the buck mode.

C. Parameter Design

In the boost mode, according to the above analysis, to achieve ZVS of S_1, S_2, and S_4, it should be guaranteed that the resonant voltage $v_{\text{cr}}(t)$ has been reduced to zero at the end of each switching cycle, that is, the resonant time (t_6–t_3) should be less than $(1 - D_2)T_s$. From (23), it can be expressed as follows:

$$t_6 - t_3 = \frac{1}{2f_r} - \frac{1}{w_o} \cdot \arctan\frac{k(nV_C + V_{C2\_1})}{V_{C2\_1}} + \frac{1}{4f_r} + \frac{1}{w_o} \cdot \arcsin\frac{1}{k-1} < (1 - D_2)\frac{1}{f_s}. \quad (77)$$

The steady-state value of D_2 is regulated to approximately 0.85 in the control system. To satisfy (77), the resonant frequency is selected as $f_r = 5f_s$, that is

$$f_r = \frac{1}{2\pi\sqrt{(L_1 + L_{s1})C_r}} = 5f_s. \quad (78)$$

At the end of each switching cycle, we need to ensure that the resonant current $i_{L1}(t)$ is not reduced to zero, that is, $i_{L1}(t_7) = I_{L1\_1} < 0$. By substituting (78) into (24) and (31), the range of k can be calculated by the following:

$$2.4 < k < 10\pi D_1 - \frac{10\pi D_1 V_C V_S}{(V_{C2\_1} + V_S)(nV_C + V_{C2\_1})}. \quad (79)$$

To avoid saturation of the transformer magnetic core, we need to ensure that the magnetizing current alternates between the positive and negative directions during one switching cycle, which can be expressed as follows:

$$i_{Lm2}(t_1) = i_{L1}(t_3) - \frac{V_S}{nL_{m2}}(t_2 - t_1) = \frac{k(nV_C + V_{C2\_1})}{nz_o} - \frac{V_S}{nL_{m1}} \cdot \frac{V_{C2\_1}}{(V_{C2\_1} + V_S)f_s} < 0. \quad (80)$$

Because the average discharging current is $I_{\text{discharge}} = 2$ A, the average output current in the boost mode is then $I_{S\_1} = \frac{V_C I_{\text{discharge}}}{V_S}$. Subsequently, from Fig. 3, I_{S_1} can be calculated by the following:

$$I_{S\_1} = \frac{V_C I_{\text{discharge}}}{V_S} = \frac{1}{T_s}\int_{t_1}^{t_2} i_{H1}(t)dt = \frac{1}{T_s} \cdot \frac{1}{2} \cdot \left[\frac{V_S}{n^2(L_1 + L_{s1})} + \frac{V_S}{n^2 L_{m1}}\right] \cdot (t_2 - t_1)^2 = \frac{1}{T_s} \cdot \frac{1}{2} \cdot \left[\frac{V_S}{n^2(L_1 + L_{s1})} + \frac{V_S}{n^2 L_{m1}}\right]\left[\frac{V_{C2\_1}}{(V_{C2\_1} + V_S)f_s}\right]^2. \quad (81)$$

Substituting (78) and (81) into (80) allows calculation of the range of $(L_1 + L_{s1})$ by

$$\frac{10\pi V_S^2 V_{C2\_1}^2 + k(nV_C + V_{C2\_1})(V_S + V_{C2\_1})V_S V_{C2\_1}}{20\pi V_C I_{\text{discharge}} n^2 (V_S + V_{C2\_1})^2 f_s} < (L_1 + L_{s1}). \quad (82)$$

According to the range of k in (79), the value of k is selected as five. Substituting the parameters listed in Table I into (82) yields $(L_1 + L_{s1}) > 3.5\ \mu$H. According to the ZVS condition analysis previously described, $(L_1 + L_{s1}) < 25\ \mu$H can be obtained from (69). Therefore, on the basis of the above conditions, we set $(L_1 + L_{s1}) = 5.19\ \mu$H, $L_{s1} = 0.19\ \mu$H, $L_{s2} = n^2 L_{s1} = 7.0\ \mu$H, and $L_1 = 5\ \mu$H in this study.

From (78), C_r can be calculated by the following:

$$C_r = \frac{1}{100\pi^2 {f_s}^2 (L_1 + L_{s1})}. \quad (83)$$

From (81), L_{m1} can be calculated by the following:

$$L_{m1} = \frac{{V_S}^2 V_{C2\_1}^2 (L_1 + L_{s1})}{2n^2 V_C I_{\text{discharge}} (V_{C2\_1} + V_S)^2 (L_1 + L_{s1}) f_s - {V_S}^2 V_{C2\_1}^2}. \quad (84)$$

According to (83) and (84), $C_r = 470$ nF, $L_{m1} = 1.8\ \mu$H, and $L_{m2} = n^2 L_{m1} = 65\ \mu$H can be obtained.

In this paper, the ferroxcube PC44/PQ3230 is selected as the transformer core. In order to decrease the value of magnetizing inductance, the air gap is required in the transformer core.

We assume that the turns of primary and secondary windings of transformer T_1 are N_1 and N_2, respectively. Moreover, the equivalent inductance coefficient and cross-sectional area of the transformer core are A_L and A_e, respectively. Then, the air gap δ can be calculated as follows:

$$\begin{cases} V_S = \frac{N_2 f_s A_e \Delta B}{D_3} \\ L_{m2} = N_2^2 A_L \\ \delta = \frac{\mu_0 A_e}{A_L} \end{cases} \tag{85}$$

where μ_0 is the permeability of vacuum and $\mu_0 = 4\pi \times 10^{-7}$ H/m. By substituting the parameters in this experiment into (85), the air gap is calculated as $\delta = 3.1$ mm.

In the buck mode, the clamping capacitor C_2 should be sufficiently large to ensure that the voltage is approximately constant and reduces the voltage stresses of the switches. However, this condition will affect the transient response speed of the circuit. Simultaneously, according to the operating principle in the buck mode, to achieve ZVS of S_3, the resonant cycle between L_{m2}, L_{s2}, and C_2 should be much greater than the turn-OFF time of S_3. To retain a certain margin, the resonance cycle is considered as five times the turn-OFF time of S_3; thus, the resonance cycle should be satisfied by the following:

$$2\pi\sqrt{(L_{m2} + L_{s2})C_2} > 5(1 - D_3)T_s. \tag{86}$$

Therefore, C_2 can be calculated by the following:

$$C_2 > \frac{12(1 - D_3)^2}{(L_{m2} + L_{s2})\pi^2 {f_s}^2}. \tag{87}$$

By substituting the experimental parameters into (87), C_2 is set as 4.7 μF in this study.

IV. Experimental Results

A. Prototype of Charge Equalization System for a Series-Connected Battery String of 13 Cells

A battery string that contains 13 series-connected 7.2 Ah lithium-ion cells is used in the experiment. The rated and maximum voltages of the single lithium-ion cell are 3.7 and 4.2 V, respectively. Therefore, the rated and maximum voltages of the battery string are 48.1 and 54.6 V, respectively. Fig. 9 shows the photograph of the prototype.

To obtain the model characteristics of the lithium-ion battery, charging and discharging experiments on the lithium-ion battery are conducted in this study. Fig. 10 shows the measured experimental data of the voltage and state-of-charge (SOC) values of the 7.2 Ah lithium-ion cell in the charging and discharging states, respectively. The *V*–SOC characteristic curve is then obtained through curve fitting using MATLAB. Fig. 10 shows that in a certain range, the SOC value displays a large difference between the charging and discharging states at the same cell voltage, which means that the SOC value, instead of the voltage value, is more accurate in reflecting the working state of the cell.

Fig. 11 shows the control strategy of the charge equalization system. The CPU reads the current sampling values to determine whether the single cell is in the charging or discharging

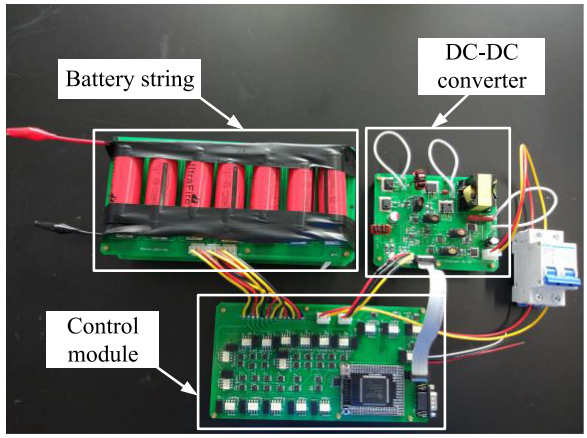


Fig. 9. Photograph of the prototype.

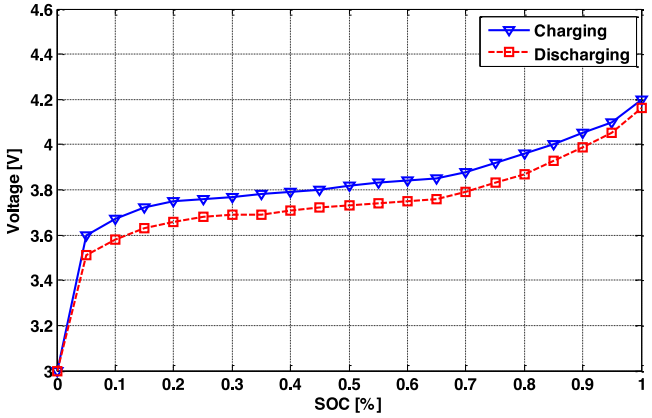


Fig. 10. Charging/discharging *V*–SOC curves of the 7.2 Ah lithium-ion battery.

state at this moment. Then, the SOC_i of the each corresponding cell can be estimated according to the V-SOC characteristic curve. Therefore, both average value $\overline{\mathrm{SOC}}$ and difference value $\Delta\mathrm{SOC}_i (= \mathrm{SOC}_i - \overline{\mathrm{SOC}})$ can be calculated. If more than one cell requires equalization, the difference values $\Delta\mathrm{SOC}_i s$ of these cells will be sorted in descending order. Then, by judgment from the program, the cell with the maximum value of $\Delta\mathrm{SOC}_i$ will be equalized first. After the equalization of one cell is complete, another cell with the maximum value of $\Delta\mathrm{SOC}_i$ in the rest unbalanced cells will be equalized. Furthermore, the equalization priority of the overcharged cells is higher than that of the undercharged cells, because the overcharged cells may be more likely to be damaged without equalization.

When $\Delta\mathrm{SOC}_i\_\mathrm{max} > 2\%$, the bidirectional dc–dc converter operates in the boost mode, and the maximum equalizing discharging current is regulated to 2 A through the control system. When $\Delta\mathrm{SOC}_i\_\mathrm{max} < -2\%$, the bidirectional dc–dc converter operates in the buck mode, and the maximum equalizing charging current is regulated to 3 A. In this case, the difference in the SOC values among the different cells is controlled within 2%. In order to improve equalization efficiency, charge equalization is usually activated in the later charging stage of battery pack. In addition, equalization in the initial charging stage of battery

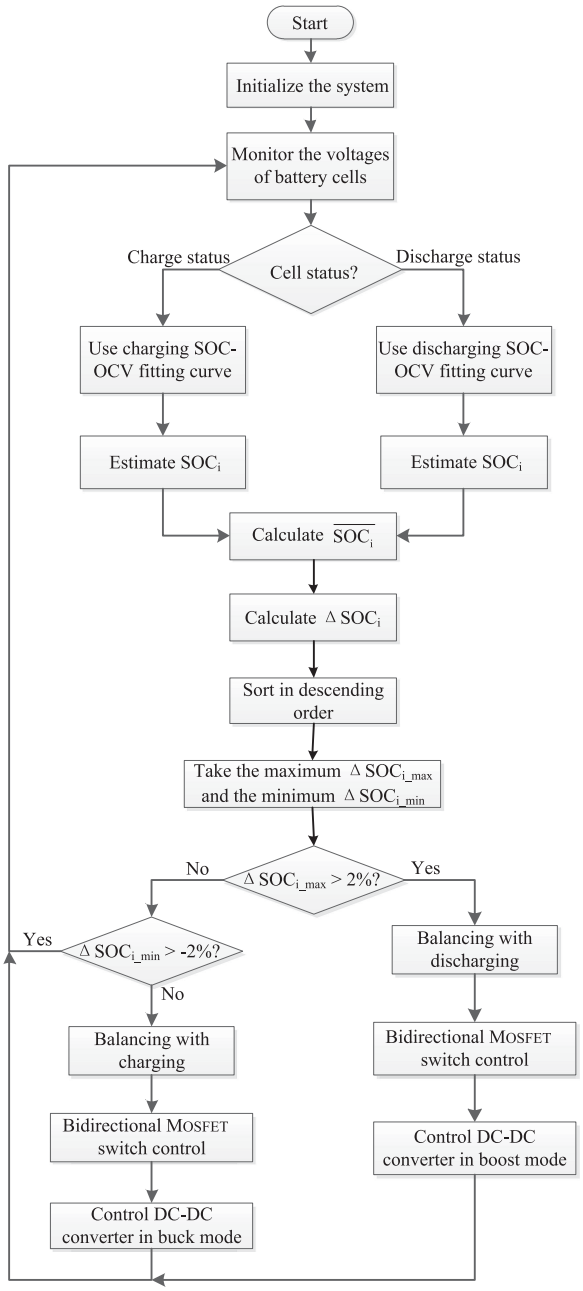


Fig. 11. Control strategy of the charge equalization.

pack may not make much sense because it is usually improbable that overcharge or undercharge of battery cells occurs in the initial stage. Hence, the equalization experiment in this paper is conducted under the condition that the battery pack is operated at the later charging stage when the charging current of the battery pack is relatively small. An external dc power source is acted as the charger in this experiment.

Fig. 12 shows the schematic diagram of the charge equalization system. Each cell voltage is detected in real time via monitoring by IC LTC6803. Then, the sampling data of the cell voltage are transmitted to the CPU through the communication interface. Meanwhile, the charging current of the battery string and the current in the low-voltage side of the bidirectional

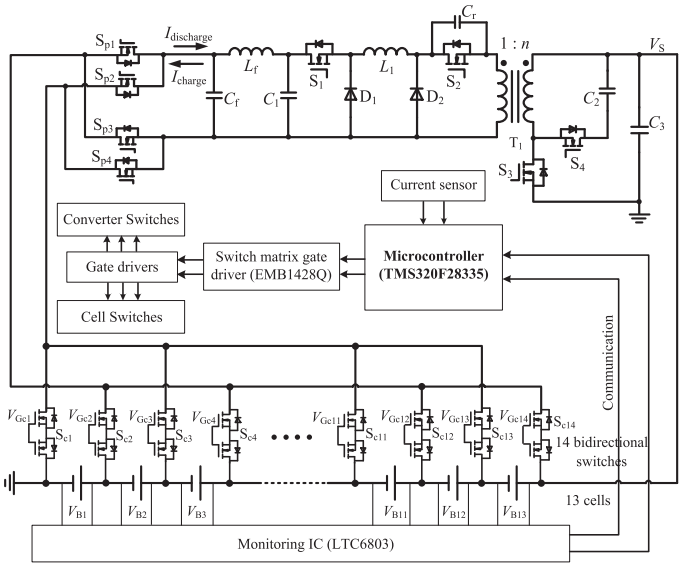


Fig. 12. Schematic diagram of the charge equalization.

dc–dc converter (equalizing charge or discharge currents) are detected by the current sensors. Switches S_{c1}–S_{c14} represent the bidirectional switches for selecting a certain cell that requires equalization, whereas S_{p1}–S_{p4} represent the polarity switches for connecting the unbalanced cell to the bidirectional dc–dc converter. MOSFET IRF7862PbF is selected in this study as the unit for the bidirectional switch. Despite the use of many MOSFETS, the volume and cost do not increase because the power rating and package of the MOSFETS are small. S_{p1} and S_{p4} are turned ON when an odd-numbered cell needs to be equalized, whereas S_{p2} and S_{p3} are turned ON when an even-numbered cell needs to be equalized. To obtain low-ripple equalizing charge and discharge currents, filter inductor L_f and filter capacitor C_f are connected to the low-voltage side. TMS320F28335 is used as the microcontroller in this paper. Switch matrix gate driver EMB1428Q is used to extend the PWM ports because one TMS320F28335 chip has only 12 PWM ports and cannot meet the requirements in this experiment. An optocoupler needs to be connected between each PWM signal output from EMB1428Q and the gate of the corresponding MOSFET for electric isolation and to increase the driving force of the PWM signals.

B. Experimental Results of the Proposed Bidirectional DC–DC Converter and Charge Equalization

During the equalization process, a single lithium-ion cell is connected to the low-voltage side of the bidirectional dc–dc converter, and the high-voltage side is connected to the battery string, which consists of 13 cells. The parameters used in the experiment are listed in Table I.

In the case when one cell is detected as being overcharged, the extra energy should be transferred to the battery string. Then, the proposed converter operates in the boost mode. In this case, the input side is connected to the unbalanced cell, whereas the output side is connected to the battery string. Fig. 13 shows the experimental waveforms in the boost mode. The conversion efficiency of the boost mode is approximately 83.4%. In Fig. 13(a),

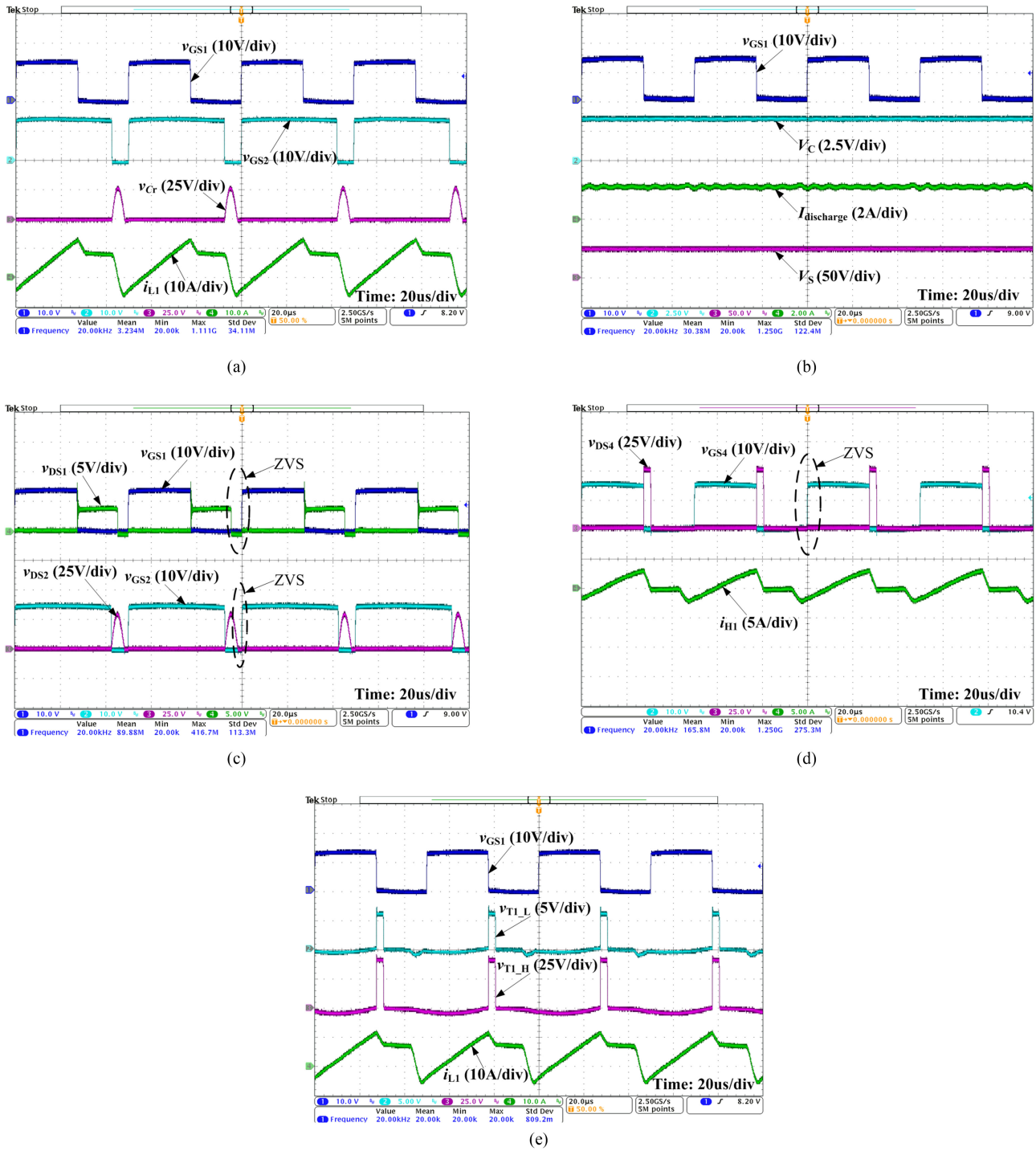


Fig. 13. Experimental waveforms of the proposed converter in the boost mode. (a) v_{GS1}, v_{GS2}, $v_{\rm Cr}$, i_{L1}. (b) v_{GS1}, V_C, $I_{\rm discharge}$, V_S. (c) ZVS waveforms of S_1 and S_2. (d) ZVS waveforms of S_4. (e) Transformer voltage waveforms.

the oscilloscope channels represent S_1 gate drive signal v_{GS1}, S_2 gate drive signal v_{GS2}, resonant voltage $v_{\rm Cr}$, and resonant current i_{L1}. Fig. 13(a) shows that quasi-resonant operation occurs after S_2 is turned OFF during each switching cycle. The equalizing discharge current is regulated to 2 A, as shown in Fig. 13(b).

The output voltage is approximately 50 V, which is the voltage of the battery string. Fig. 13(c) and (d) show the ZVS waveforms of S_1, S_2, and S_4. Fig. 13(c) shows that the drain–source voltage v_{DS2} is equal to $v_{\rm Cr}$. According to the principle of quasi-resonance discussed in Section II, resonant voltage $v_{\rm Cr}$ decreases to zero before S_2 is turned ON during each switching cycle. Then, ZVS of S_2 is achieved. Similarly, ZVS of S_1 is also achieved. Fig. 13(d) shows that current i_{H1} always flows through the body diode of S_4 before S_4 is turned ON. Then, ZVS of S_4 is achieved. Furthermore, as shown in Figs. 3 and 4,

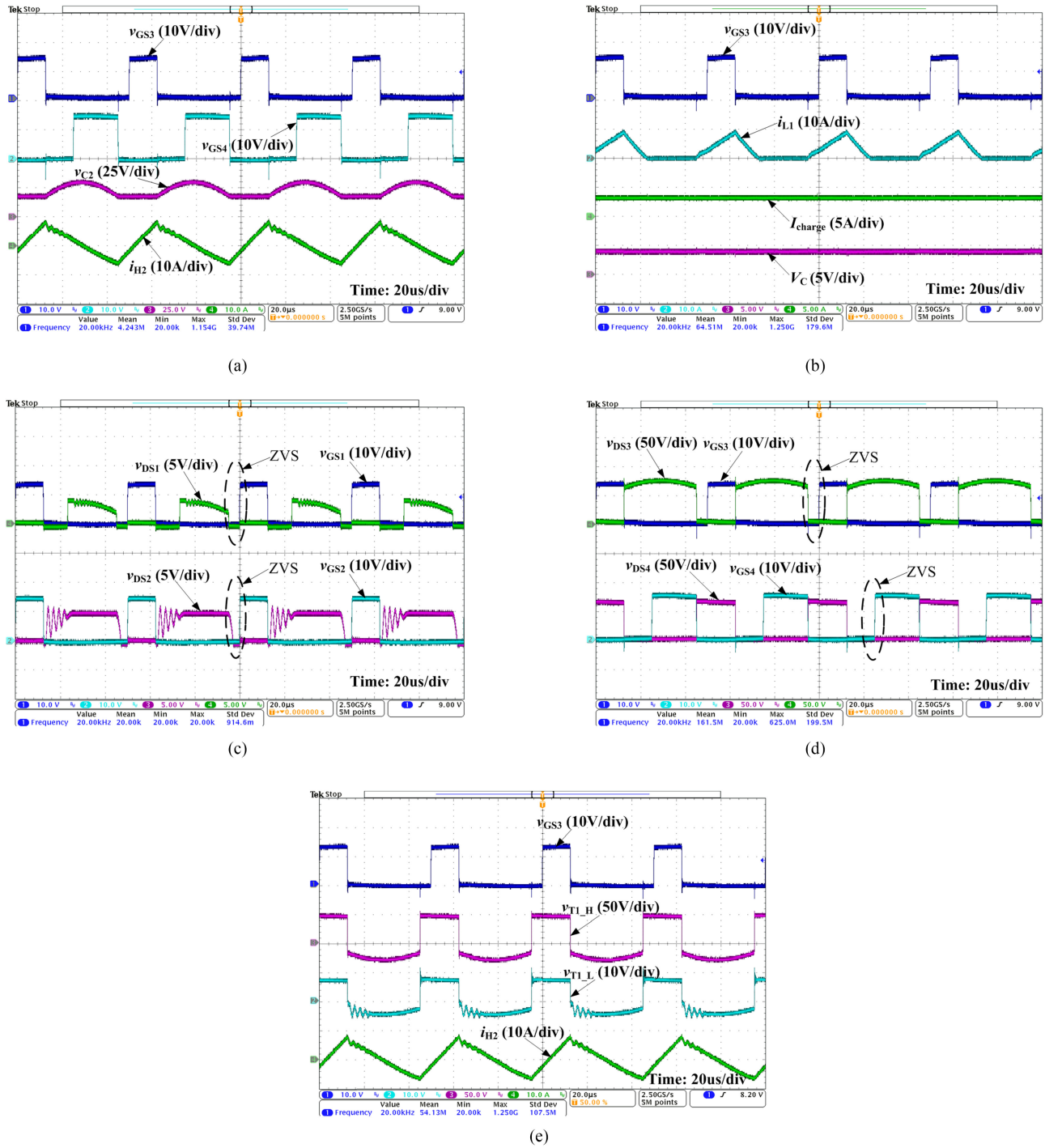
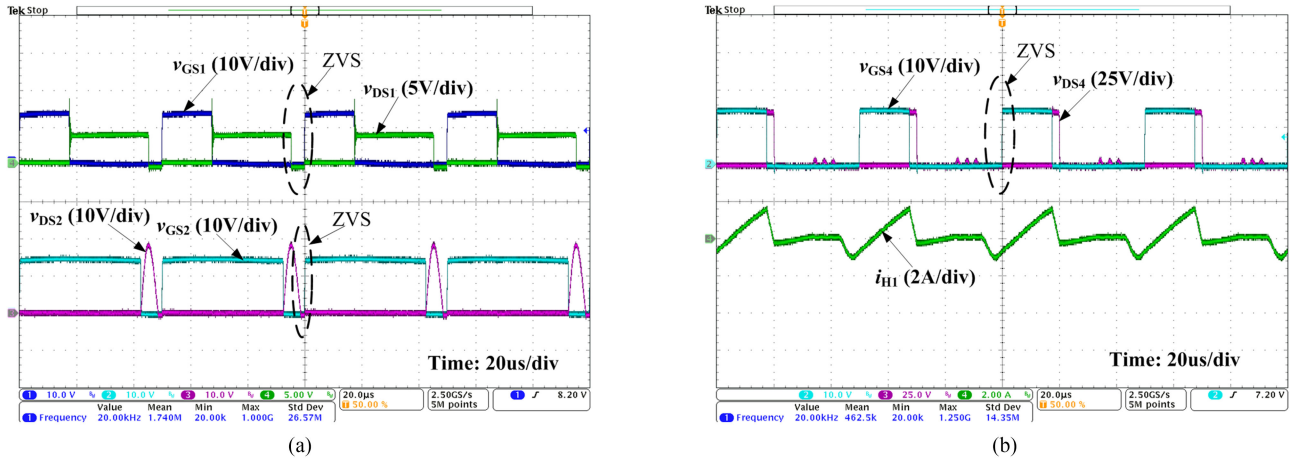


Fig. 14. Experimental waveforms of the proposed converter in the buck mode. (a) v_{GS3}, v_{GS4}, v_{C2}, i_{H2}. (b) v_{GS3}, i_{L1}, I_{charge}, V_C. (c) ZVS waveforms of S_1 and S_2. (d) ZVS waveforms of S_3 and S_4. (e) Transformer voltage waveforms.

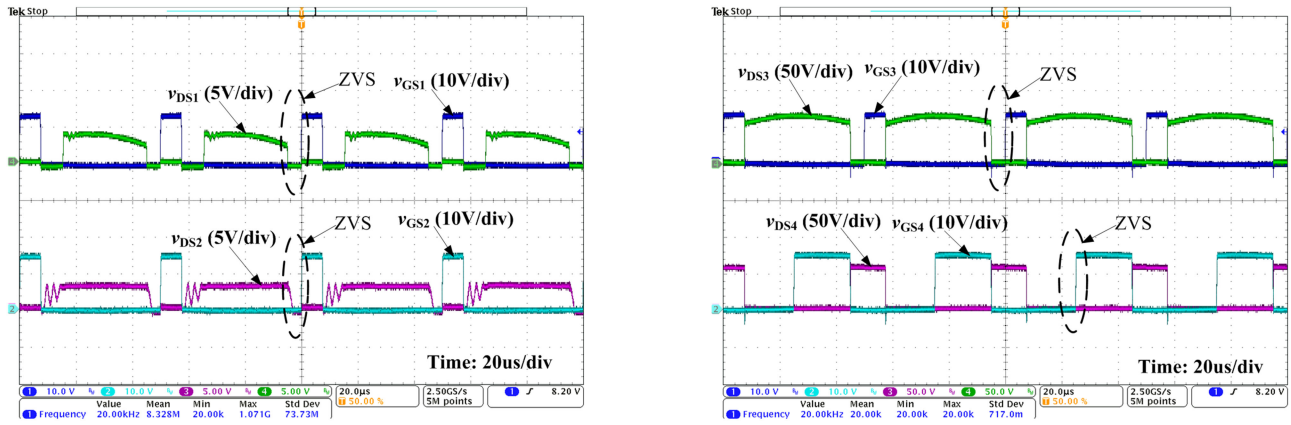
according to the operating principle of the proposed converter in the boost mode, during each switching cycle, when $i_{H1}(t)$ is reduced to zero at t_2, the body diode of S_4 conducts and $v_{Lm1}(t)$ is clamped to $\frac{V_{C2\_1}}{n}$. Then, the drain–source voltage of S_4 becomes zero. This state lasts until the next switching cycle begins, which means that the drain–source voltage of S_4 maintains zero during $[t_2, t_7]$ in Fig. 3. Therefore, when S_4 is turned ON at the beginning of the next switching cycle, its ZVS is achieved, as shown in Fig. 13(d). From the above discussion, we can learn that all the switches of the proposed converter except S_3 can realize ZVS operations in the boost mode.

Fig. 13(e) shows the transformer voltage waveforms in the boost mode, where v_{T1_H} and v_{T1_L} represent high-side and low-side voltages of transformer T_1, respectively. As shown in the experimental waveforms, the positive values of v_{T1_H} and v_{T1_L} occur after S_1 is turned OFF, during which time the



(a) (b)

Fig. 15. ZVS waveforms with equalizing discharge current of 1 A in the boost mode. (a) ZVS waveforms of S_1 and S_2. (b) ZVS waveforms of S_4.



(a) (b)

Fig. 16. ZVS waveforms with equalizing charge current of 1.5 A in the buck mode. (a) ZVS waveforms of S_1 and S_2. (b) ZVS waveforms of S_3 and S_4.

energy in L_1 is released to the battery string V_S. This process corresponds to the stage 3 in Fig. 4.

When one cell is detected to be undercharged, equalization is activated, and this cell will be charged. In this case, the proposed converter operates in the buck mode. Fig. 14 shows the experimental waveforms in the buck mode. The conversion efficiency of the buck mode is approximately 84.2%. In Fig. 14(a), the four channels represent S_3 gate drive signal v_{GS3}, S_4 gate drive signal v_{GS4}, capacitor voltage v_{C2}, and current i_{H2} flowing through L_{s2}. We can see that a time delay exists between the turn OFF of S_3 and turn ON of S_4, where the ZVS operation of S_4 can be realized. Fig. 14(b) shows that the equalizing charge current of the unbalanced cell is regulated to 3 A with a small current ripple.

Fig. 14(c) and (d) show the ZVS waveforms of S_1 to S_4. According to the operating principle in the buck mode, before S_1 and S_2 are turned ON, resonant voltage v_{Cr} is reduced to zero. Then, the body diodes of S_1 and S_2 are forward biased. Therefore, ZVS of S_1 and S_2 can be achieved when they are turned ON in the next switching cycle. Moreover, in the buck mode, when S_2 is turned OFF at t_1, as shown in Fig. 5, C_{DS3} is charged, and $v_{DS3}(t)$ gradually increases. At t_2, $v_{DS3}(t)$ increases to V_S. After that, $v_{Lm2}(t)$ becomes less than zero and is clamped to $\frac{v_{C2}(t)}{n}$. Therefore, C_r is charged by the voltage $\frac{v_{Lm2}(t)}{n}$. In this case, the resonance occurs between C_r and leakage inductance L_{s1} and the resonance frequency is calculated as $f_r = \frac{1}{2\pi\sqrt{L_{s1}C_r}} \approx 500$ kHz. This process is a damped oscillation due to the damping in the resonant tank, such as the on-resistance of diode D_2. The oscillation process occurs in stages 4 and 5 of Fig. 6. The process lasts until the resonance ends and the capacitor voltage $V_{\mathrm{Cr}}(t)$ is clamped to $\frac{v_{C2}(t)}{n}$, as shown in Fig. 14(c). Meanwhile, ZVS of S_3 and S_4 are also achieved through quasi-resonant operation. According to Figs. 5 and 6 of buck mode, during each switching cycle, when S_3 is turned OFF at t_1, the drain–source capacitance C_{DS3} is charged, and $v_{DS3}(t)$ gradually increases. When $v_{DS3}(t)$ increases to $(V_S + V_{C2\_2})$ at t_3, the body diode of S_4 begins to conduct and the drain–source voltage of S_4 becomes zero. According to the analysis in Section III, the switching condition of S_4 can be determined by (70) and (73). Hence, S_4 can achieve ZVS when S_4 is turned ON at any time during $[t_3, t_4]$, as

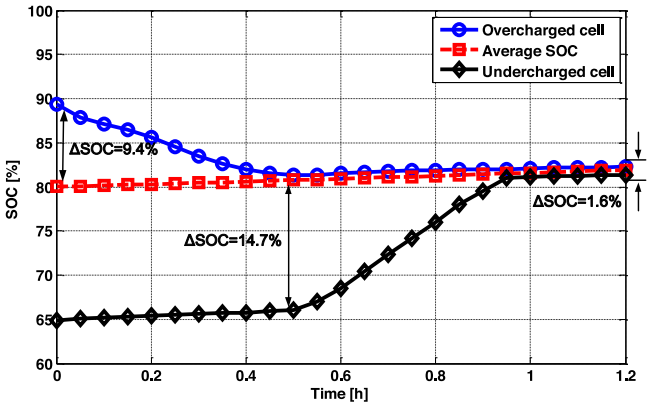


Fig. 17. Equalization result of the lithium-ion battery cells.

shown in Fig. 14(d). In this case, all the switches of the proposed converter can realize ZVS operations in the buck mode.

Fig. 14(e) shows the transformer voltage waveforms in the buck mode. As shown in the waveforms, the positive values of v_{T1_H} and v_{T1_L} occur as long as switch S_3 or its body diode conducts, which corresponds to the stages 1, 2, 9, and 10 in Fig. 6. In addition, voltage oscillations occur in the negative values of v_{T1_L}, this is due to the resonance occurs between C_r and leakage inductance L_{s1}.

In the actual system, as the charging time changes, the equalizing current may be decreased to prevent overcharge or undercharge in the late of the equalization process. In this case, the ZVS can also be achieved in the proposed converter. Figs. 15 and 16 show the ZVS experimental waveforms of the proposed converter with equalizing discharge current of 1 A and equalizing charge current of 1.5 A.

According to the waveforms in Fig. 15, both the maximum voltages across switches and the maximum currents are reduced under the equalizing discharge current of 1 A in the boost mode. At the same time, the ZVS of switches S_1, S_2, and S_4 can also be achieved under this condition.

Fig. 16 shows the ZVS experimental waveforms for the buck mode with the equalizing charge current of 1.5 A. When the equalization process is nearly complete, a smaller equalizing current may be required to prevent overcharge. According to the ZVS analysis in Section III, the ZVS of S_1 to S_4 can be realized by satisfying parameter matching. As shown in the waveforms, the ZVS of S_1 to S_4 can be achieved under the small equalizing charge current of 1.5 A.

The SOC data of the cells are read by the upper computer through the serial communication interface RS232 in the experiment. Then, the SOC equalization curve can be drawn in MATLAB. Fig. 17 depicts the result of the charge equalization. Fig. 17 shows that the SOC of the overcharged cell is 89.4% (4.067 V), which is 9.4% higher than the average SOC. The SOC of the undercharged cell is 64.9% (3.861 V), which is 15.1% lower than the average SOC. According to the control-strategy principle, the overcharged cell will be equalized first. In this case, the overcharged cell is discharged at a maximum current of 2 A through the proposed bidirectional dc–dc converter. During the equalization, the real-time voltage of the cell is detected, and the corresponding SOC is estimated. After 31 min, equalization of the first cell is completed. Then, balancing of the undercharged cell starts, and a 3 A charging current is provided. Equalization of the undercharged cell is completed after 24 min.

C. Comparison

To demonstrate the advantages of the proposed converter, comparison between the proposed and other converters in centralized charge-equalization systems is listed in Table II.

As listed in Table II, the bidirectional flyback dc–dc converter with two transformers in [24] and [25] was well designed to transfer energy between the cell and battery string. The control scheme of this equalizer is simple and easy to implement. However, the voltage stresses on the switches will be very high without an auxiliary snubber network. Generally, the lossy snubber network (such as RCD snubber) is adopted in flyback converter to reduce the voltage spike, however, this increases the losses. In addition, ZVS operations cannot be achieved in either boost or buck mode in the converter in [24] and [25]. Moreover, this equalizer contains many bidirectional switches, which increase the complexity of the system. The bidirectional full-bridge circuit in [23] can realize bidirectional flow of energy, but it suffers from the disadvantage of using more switches and complex driving circuits, which reduces the stability and reliability of the converter. Compared with the converter in [21], although the proposed converter in this study has two more diodes, ZVS operations of all switches can be realized in both boost and buck modes through quasi-resonant operations, which greatly decrease the switching losses and improve the efficiency. However, the converter in [21] can only achieve ZVS operations of two switches in the high-voltage side in the buck mode. Moreover, a voltage spike caused by the leakage inductance in the boost mode cannot be avoided in the converter in [21], but this problem is solved in the converter proposed in this paper through quasi-resonant operation, which decreases the voltage stresses on the power devices.

In terms of control circuits, the equalizer in [24] has a lot of bidirectional switches because each battery cell corresponds to two separate bidirectional switches, which results in many driving circuits and increases the complexity. Likewise, the driving circuits in [23] are complex due to its large number of switches in the bidirectional dc–dc converter. Although the equalizer in [21] shows a simpler control system, the drive capability of both ICs EMB1428 and EMB1499 is very small. In this case, the extra driving circuits are essential when the ratings of power switches are relatively large. As shown in Fig. 12, in this paper, switch matrix gate driver EMB1428Q is used to extend the PWM ports. Then, an optocoupler is connected between each PWM signal output from EMB1428Q and the gate of the corresponding MOSFET for electric isolation and to increase the driving force of the PWM signals. The sampling data of the cell voltage are transmitted to the CPU through the communication interface. Compared with similar equalizers, the proposed charge equalizer has a relatively good control.

TABLE II
COMPARISON BETWEEN THE PROPOSED AND OTHER CONVERTERS IN THE CENTRALIZED CHARGE-EQUALIZATION SYSTEMS OF THE 13 BATTERY CELLS

		Proposed equalizer	Bidirectional flyback in [24][25]	Bidirectional full-bridge in [23]	Bidirectional forward in [21]
DC-DC converter	Number of inductors	1	0	1	1
	Number of transformers	1	2	1	1
	Number of capacitors	4	2	2	3
	Number of switches	4	2	8	4
	Number of diodes	2	2	0	0
	ZVS operation in boost mode	Yes	No	Yes	No
	ZVS operation in buck mode	Yes	No	No	Yes
	Voltage spike caused by leakage inductance	No	Yes	Yes	Yes
Bidirectional switches and polarity switches		32	52	32	32
Equalization speed		Good	Satisfactory	Satisfactory	Satisfactory
Efficiency		High	Medium	Low	Medium
Control complexity		G	S	S	E

E: Excellent, G: Good, S: Satisfactory.

V. CONCLUSION

An isolated bidirectional dc–dc converter with quasi-resonant ZVS for battery charge equalization is proposed in this paper. ZVS operations are achieved in both boost and buck modes through quasi-resonant technique, which reduces the switching loss. Compared with the existing converters, the proposed converter has fewer components, lower voltage stress, and higher efficiency. Furthermore, the voltage spike caused by the leakage inductance can be avoided because energy is transferred into the resonant capacitor. Moreover, the magnetizing current can return to zero in each switching cycle, and the remanence is eliminated, which avoids saturation of the transformer core. Experimental results of the charge equalization using 13 battery cells verified that the proposed equalizer has a good performance in terms of efficiency and balancing speed compared with existing similar equalizers.

However, it must be acknowledged that the proposed converter has several limitations. The first issue is that the current ratings of switches S_1–S_4 used in the experiment are very high for reducing the conduction losses, as the peak value of the resonant current is relatively large. This may result in higher cost. The second issue is that the conduction losses of the polarity switches were not considered, which causes the deviation on the efficiency measurements in practice. In future studies, we propose to address these issues to further improve the performance of the converter and increase the conversion efficiency.

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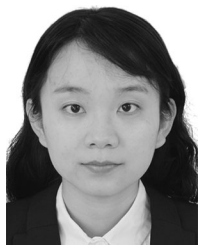
Junlong Lu (S'14) was born in Jiangxi, China, in 1987. He received the B.S. degree from the Harbin University of Science and Technology, Harbin, China, in 2011, and the M.S. degree from the Harbin Institute of Technology Shenzhen Graduate School, Shenzhen, China, where he is currently working toward the Ph.D. degree in power electronics and power drives, in 2013.

His current research interests include power electronics, charge equalization converters, soft-switching techniques, and renewable energy systems.

Yi Wang (M'09) was born in Heilongjiang, China, in 1966. He received the B.S. degree from Xi'an Technological University, Xi'an, China, in 1988, and the M.S. and Ph.D. degrees from the Harbin Institute of Technology, Harbin, China, in 1996 and 2002, respectively.

Since 2009, he has been a Professor with the Harbin Institute of Technology Shenzhen Graduate School, Shenzhen, China. His research interests include renewable energy systems, electric motor drive design, electric vehicle control techniques, and power electronics converters.

Dr. Wang is the Reviewer of the Proceedings of the CSEE.



Xin Li was born in Hebei, China, in 1993. She received the B.S. degree from Yanshan University, Qinhuangdao, China, in 2015. She is currently working toward the M.S. degree in power electronics and power drives at the Harbin Institute of Technology Shenzhen Graduate School, Shenzhen, China.

Her current research interests include power electronics, electromagnetic compatibility, and modeling and control of power converters.