Investigating the EMI Mitigation in Power Inverters Using Delay Compensation

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***Abstract*—Electromagnetic emissions (EMEs) of electric and electronic units should comply with national and international standards. Software approaches to reduce the conducted EME are preferable, since they do not require additional on-board hardware. Many techniques have been developed with different levels of efficiency. This paper aims to analyze a new software approach to mitigate the conducted emissions of three-phase power inverters, focusing on those used to drive brushless DC motors. This has been done reducing the conducted electromagnetic interferences common mode (CM) component through software compensation of parasitic delays. The technique is verified both analytically and experimentally, and its performances have been compared to the spread spectrum modulation (SSM) ones. The proposed approach shows better performances with respect to SSM below 24 MHz. The results confirm the effectiveness of the delay compensation technique in terms of CM conducted emissions reduction. Moreover, the proposed approach has no drawbacks on safety and it does not present reductions in the inverter efficiency.**

***Index Terms*—Bipolar pulsewidth modulation (bPWM), brushless DC (BLDC), common mode (CM) emissions, electromagnetic interferences (EMIs), motor drives, signal aligning.**

I. Introduction

IN RECENT years, the research on power electronic systems has become of crucial importance for modern applications. This is mainly due to the most recent achievements in electric motor design and control. These motors are supplied in most cases by a DC voltage source. In order to control a brushless electric motor, this DC voltage is converted into sinusoidal or trapezoidal voltage waveforms by means of switching inverters. The strong evolution of the devices used in power switching modules of the last decade has strongly reduced their commutation time. This has led to an improvement in the system efficiency, since the shorter the switching times, the lower the energy loss.

Although the system efficiency increases, an essential element to be considered is the electromagnetic compatibility (EMC) of the module with the surrounding environment. If the switching time decreases and if the voltage swing is large, which means higher *dv/dt*, the electromagnetic emissions (EMEs) level

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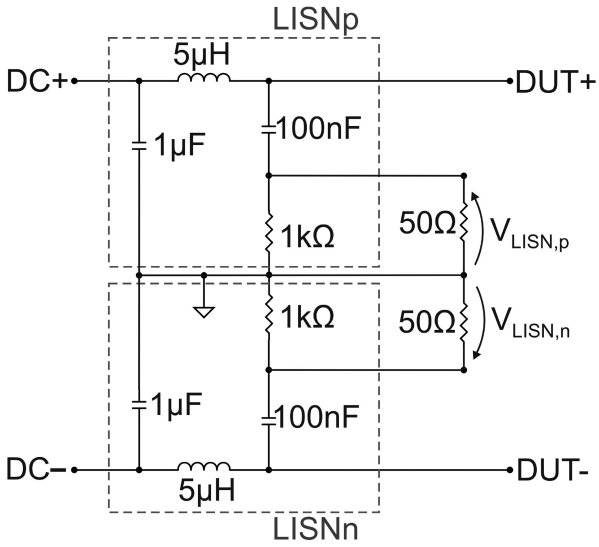

Fig. 1. LISNs connection according to CISPR 25.

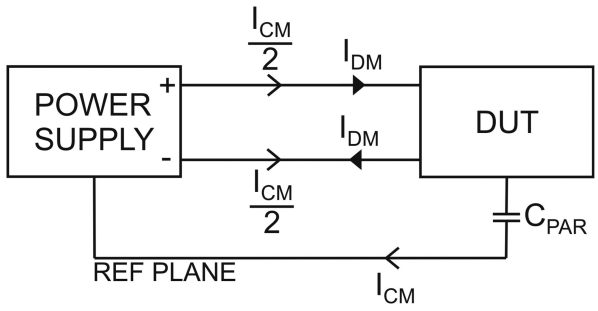

Fig. 2. Conducted EMI currents.

techniques and the spread spectrum modulation (SSM) techniques, which are based on spreading the disturbance energy over a wider frequency range [9]. The voltage waveform shaping techniques, such as slew rate and S-shape control, act on redefining the shape of the high *dv/dt* waveforms in order to reduce their spectral components. The main drawback of that is the increased power dissipation, and only a tradeoff between efficiency and emissions is feasible, as shown in [10]. With this solution, both the gate current and the drain-to-source voltage of each switch have to be measured, and that makes the control circuit more complex and expensive. The EMI reduction of that approach is effective only from 150 kHz to 1 MHz. The SSM technique [9], [11], instead, is able to reduce the EMI over a wider frequency range, but it could have several other drawbacks, as analyzed in [12]. The SSM techniques are able to reduce the EMI level by around 5–10 dB [8].

Other techniques, such as the one shown in [13] and [14], have a more specific application and they are based on the alignment of the voltage waveforms at the circuit outputs. In these works, the EMI reduction method has only been applied to single-phase inverters driving an *RLC* load. The results gained from that approach were obtained using a measurement technique that did not include the two line impedance stabilization networks (LISNs); therefore, it was not compliant with the standard EMC measurement procedures [2]–[4]. Moreover, some external parasitic capacitors were connected to the network in order to emphasize the EMI reduction effect. The results, however, were not completely satisfactory: looking at the CM current spectra, the EMI reduction was effective only over a narrow frequency range. In particular, in [14] the CM current is measured, comparing two cases: the first with a delay between the output voltage waveforms of 200 ns and the second with the delay almost nulled. In the second case, the CM emissions are lowered by only 10 dB. This reduction refers to the best case in the frequency range from 500 kHz to 5 MHz. The results obtained in that work were also limited by the hardware PWM resolution available at that time. Furthermore, the application was restricted to a single-phase inverter, with no analysis on the generation of the conducted EMI in complementary PWM-driven inverters.

This paper analyzes and proposes a software-based EMI reduction technique that can be applied to both single-phase and three-phase inverters, driven by complementary PWM. A preliminary discussion on the effectiveness of this approach was presented in [15]. This paper performs a deeper analysis on the CM EMI generation and on its reduction, and further proposes an analytical model of the emissions. The CM EMI generation mechanisms are illustrated in Section II. Section III presents the case of study of this paper, i.e., a brushless DC (BLDC) motor driver. On the basis of the analytical analysis of the CM EMI presented in Section IV, which focuses on the output voltages misalignment effect on the generated emissions, the results of some SPICE simulations are presented in Section V. In this section, the effectiveness of the proposed method is compared to that of the widely used SSM. The considerations and the analysis made in this study are proven in Section VI. In this section, the EMI reduction method is applied both to a single-phase inverter and to a three-phase inverter driving a BLDC motor. Finally, conclusions are drawn in Section VII.

II. Electromagnetic Conducted Emission in Switching Circuits

The EMEs are divided into two categories, considering their propagation along the power supply cables (conducted emissions) or in the free space as electromagnetic field (radiated emissions). In this paper, only the former are analyzed and studied.

The measurement of the conducted emissions is regulated by international standards, such as ISO and CISPR. These regulations prescribe limits on the emissions, which electronic systems have to comply with. In this paper, the CISPR 25 [2] regulation has been considered as the reference standard; in particular, its procedures for the EMC characterization of alternators and generators have been employed. Such procedures impose the use of two LISNs to measure the conducted EMI. Such networks are shown in Fig. 1. They are used to fix the impedance seen by the equipment under test toward the power supply lines. The LISNs

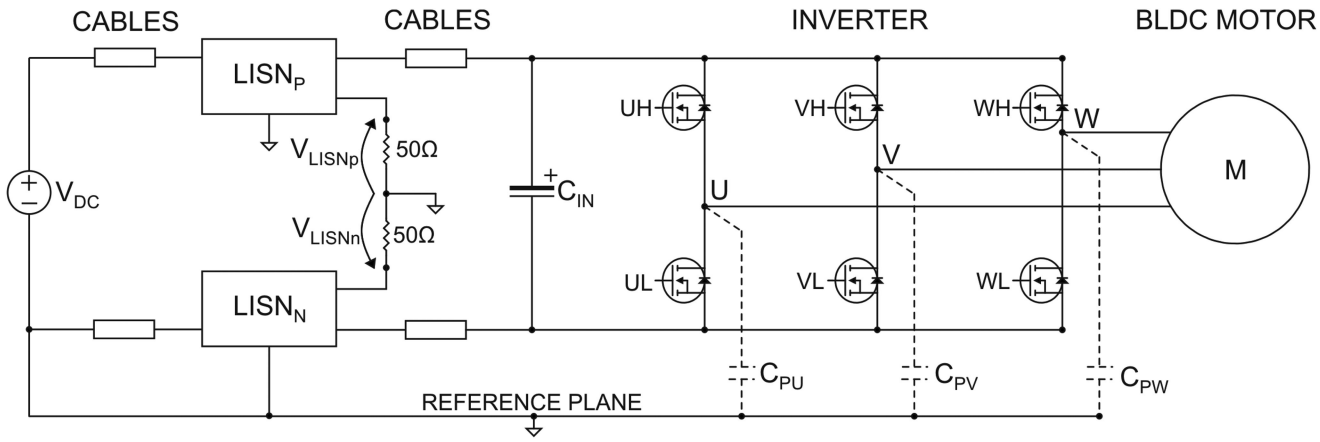

Fig. 3. Three-phase inverter schematic.

component values according to CISPR 25 are $L_{\mathrm{LISN}} = 5\,\mu$H and $C_{\mathrm{LISN}} = 1\,\mu$F.

From their output port, the conducted emissions can be measured with the use of an EMI receiver or a spectrum analyzer. The signal spectrum at the output port of both LISNs has to be lower than the prescribed limits.

The conducted interferences, for diagnosis purposes, can be divided into differential mode (DM) and CM emissions. In order to understand the difference between the two emission modes, consider the schematic shown in Fig. 2, in which the power supply block comprises both the DC source and the LISNs.

Some disturbance current could be injected into the parasitic capacitances, which are present between the device under test's (DUT) switching nodes and the reference plane C_{PAR}. These currents will flow in the 50 Ω LISN resistors, generating a voltage signal measured by the EMI receiver, i.e., the CM disturbance. On the other hand, the DM mode disturbances are those RF currents that enter in the positive power supply input of the DUT and exit from the negative one. These disturbances will propagate to the LISN 50 Ω resistors and are therefore measured [1], [16]. The CISPR 25 [2] rules state that the conducted emissions should be measured from 150 kHz to 30 MHz.

In the following section, the conducted emission generation mechanism in BLDC motor drivers is presented.

III. Generation of the EMI in BLDC Drivers

This section shows the generation mechanism of the conducted EMI produced by an inverter driving a BLDC motor. To this purpose, let us consider the circuit shown in Fig. 3. It shows the three-phase inverter, which is supplied by a DC voltage source. Its legs are made of two *n*-channel power MOSFETs, driven by a dual output gate driver, which provides the MOS gate signals, i.e., UH, UL, etc. The output nodes of the inverter U, V, and W are connected to a BLDC motor.

The BLDC motor is driven by three trapezoidal waveforms, as shown in Fig. 4, displaced in phase of 120° and modulated by bipolar PWM (bPWM) in order to vary the average voltage at the driving nodes, i.e., $\bar{V}_{\mathrm{U}}$, $\bar{V}_{\mathrm{V}}$, and $\bar{V}_{\mathrm{W}}$. The control scheme is divided into six possible configurations of the outputs (steps),

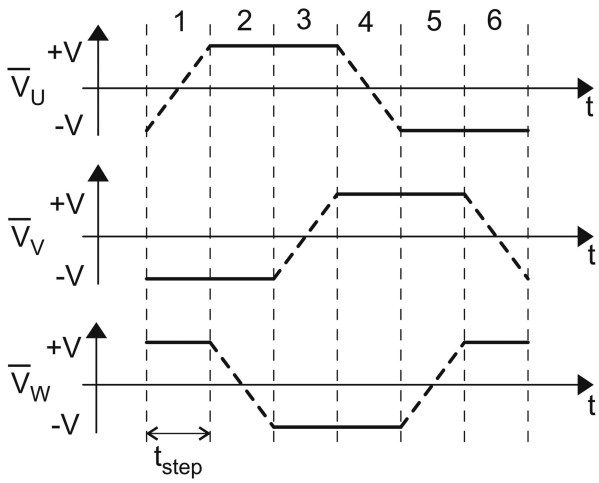

Fig. 4. BLDC motor driving waveforms.

as can be seen in the figure. In each of these configurations, one output is driven by a bPWM with duty cycle greater than 0.5 (+V), another by a bPWM with complementary duty cycle (−V), whereas the remaining is left floating (dashed line), i.e., the two nMOS of this leg are kept OFF. Therefore, for each step, only two legs are active [17].

The voltage level V is proportional to the speed of the BLDC motor. The motor manufacturer provides the $k_{\mathrm{rpm}}[\frac{\mathrm{r/min}}{\mathrm{V}}]$ constant, which relates the voltage V to the speed, $\omega_{\mathrm{mech}}[\mathrm{r/min}] = k_{\mathrm{rpm}}V$. The rotor speed is related to the electric one through the number of pole pairs p, with the relationship $\omega_{\mathrm{el}}[\mathrm{rad/s}] = \frac{2\pi}{60}p\omega_{\mathrm{mech}}$. Therefore, the duration of each time step is given by

$$t_{\mathrm{step}} = \frac{T_{\mathrm{el}}}{6} = \frac{2\pi}{p\omega_{\mathrm{mech}}\frac{2\pi}{60}} \cdot \frac{1}{6} \tag{1}$$

where T_{el} is the electric period.

The inverter is connected to the power supply line through two LISNs, as explained in the previous section. These circuits are used to measure the conducted EMI, connecting an EMI receiver, e.g., a spectrum analyzer, to their RF outputs. In order to perform conducted emission measurements, the system has to be placed above a copper plane, i.e., the reference plane, at

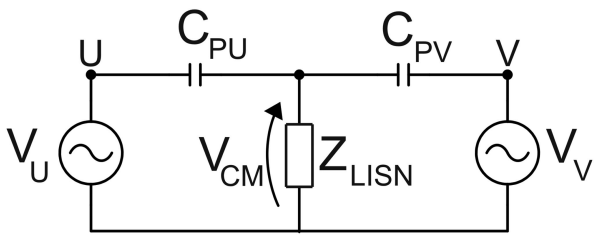

Fig. 5. CM equivalent circuit.

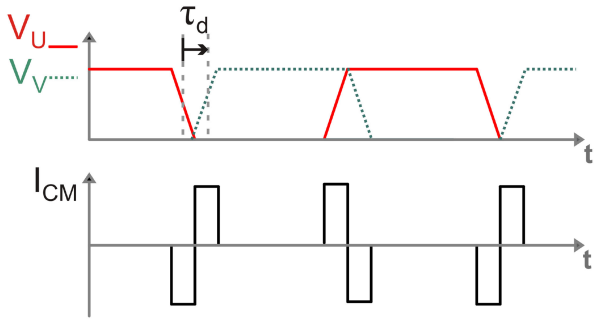

Fig. 6. Output waveforms with phase shift.

which the LISNs protective earth terminal has to be connected [2]. The differential mode emissions are therefore given by the ripple current generated by the DUT and not filtered by the input capacitor C_{IN}, whereas the CM conducted emissions are produced by the output switching nodes, whose voltage transients generate high-frequency currents flowing through the parasitic capacitances C_{PU}, C_{PV}, and C_{PW} to the LISNs. The disturbances injected into the parasitic capacitance present between the windings of the motor and the reference plane can be neglected, since the motor chassis is assumed to be not connected to the plane. The filter design to reduce the conducted emissions is different accordingly to the mode that is dominant in a specific frequency range. Generally, the DM emissions are dominant at low frequencies, whereas the CM emissions prevail over the DM ones in the higher frequency range [18]. In this study, the focus is on the reduction of CM EMI. As starting point, in what follows a mathematical model of the CM signals is derived.

IV. CM Interferences Generation

This section aims to analyze the CM signals generated by the switching circuit, and to derive the spectra that are measured at the LISN output in an approximated analytical form. The purpose of this analysis is to demonstrate that the CM emission can be reduced when a bPWM is used and the inverter output signals are perfectly complementary.

As illustrated in Section III, for each driving step, only two legs are driven by bPWM, whereas the third output is left floating. Therefore, the circuit can be reduced, for modeling purposes, to a two-legs full bridge considering, for example, only the U and V legs. It is possible to neglect the W leg in this case since the signal present at the W node has no large voltage swing. The voltage at the W node is that of the neutral node of the load, which is almost completely filtered by the parasitic capacitance C_{PW}.

Aiming to model the CM equivalent circuit, the voltages at nodes U and V can be modeled with two voltage signal sources V_{U} and V_{V}, which drive the parasitic capacitances C_{PU} and C_{PV}, respectively. The reference plane is connected to the two LISNs, which can be modeled as a 25 Ω impedance (Z_{LISN}). This equivalent circuit, for the CM analysis, is shown in Fig. 5. The voltages generated by V_{U} and V_{V} are trapezoidal pulses, with some superimposed ringing. For the sake of simplification, the duty cycle has been fixed to 0.5 in this analysis. This particular duty cycle choice has no influence on the analysis carried out.

The Fourier series of the outputs trapezoidal signal is expressed as

$$v(t) = \sum_{n=-\infty}^{\infty} V_{\mathrm{U}}(jn\omega_0)e^{jn\omega_0 t}, \tag{2}$$

$$V(jn\omega_0) = \frac{V_0}{2}\frac{\sin(\frac{1}{4}n\omega_0 T)}{\frac{1}{4}n\omega_0 T}\frac{\sin(\frac{1}{2}n\omega_0\tau_r)}{\frac{1}{4}n\omega_0\tau_r} \cdot e^{-j0.5n\omega_0(\frac{T}{2}+\tau_r)}\frac{\psi^2+(2\alpha+\frac{k}{V_0}\omega_r)\psi+\alpha^2+\omega_r^2}{\psi^2+2\alpha\psi+\alpha^2+\omega_r^2}, \tag{3}$$

where V_0 is the signal amplitude at nodes U and V, $\psi = jn\omega_0$, w_0 is the trapezoidal wave angular frequency, i.e., the PWM switching frequency, τ_r is the rising/falling time, ω_r is the ringing angular frequency, and α is the ringing damping coefficient [1]. Since the two voltages V_{U} and V_{V} are complementary, they can be represented as

$$V_{\mathrm{U}}(jn\omega_0) = V(jn\omega_0), \tag{4}$$

$$V_{\mathrm{V}}(jn\omega_0) = V(jn\omega_0)\cdot e^{-jn\omega_0(\frac{T}{2}+\tau_{\mathrm{d}})}, \tag{5}$$

where T is the waveform period and τ_d is an additional delay, as shown in Fig. 6. This delay is due to unsymmetrical trace routing or to active devices mismatch (nMOS, drivers, microcontroller outputs). Among these contributions to τ_d, the most important one is that due to the gate drivers. Usually silicon makers provide a typical and a maximum value for this parameter, which can take values within tens of nanoseconds.

The voltage at the LISNs CM output $V_{\mathrm{CM}}(jn\omega_0)$ can be calculated using the superposition of the two voltage generators, giving the following result:

$$V_{\mathrm{CM}}(jn\omega_0) = V(jn\omega_0)\cdot D(jn\omega_0)\cdot H(jn\omega_0) = V(jn\omega_0)\cdot(1+e^{-jn\omega_0(\frac{T}{2}+\tau_d)})\cdot\frac{jn\omega_0 RC}{1+2jn\omega_0 RC}, \tag{6}$$

where $C_{\mathrm{PU}} = C_{\mathrm{PV}} = C$ and $R = Z_{\mathrm{LISN}}$. It is possible to derive the contribution of τ_{d} on the emissions, computing the magnitude of $D(jn\omega_0) = (1+e^{-jn\omega_0(\frac{T}{2}+\tau_d)})$

$$|D(jn\omega_0)| = |(1+e^{-jn\omega_0(\frac{T}{2}+\tau_d)})| = \sqrt{2-2\cos(n\omega_0\tau_d)}. \tag{7}$$

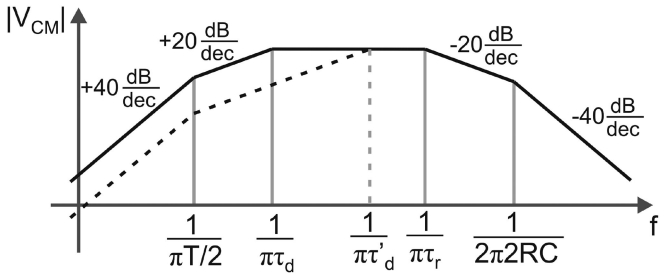

Fig. 7. CM voltage spectrum. The continuous line is the reference spectrum, where a time delay τ_d is present between the output waveforms. When the delay is reduced from τ_d to τ_d', the low frequency part of the spectrum is modified as the dashed line indicates.

TABLE I
MODEL PARAMETERS

Parameter	Value
V_0	12 V
T	20 μs
D	0.5
t_r	10 ns
C	6 pF

The peak magnitude of this term is 2. When τ_d is equal to 0, $D(jn\omega_0) = 0$ and the CM voltage measured on the LISN is ideally nulled. Actually, this does not occur, because of the ringing mismatch between the output nodes and other CM contributions not discussed before. The cosine contribution under the square root can be approximated for low frequencies with its Taylor expansion. In this range, the envelope of $|D(jn\omega_0)|$ has a slope of +20 dB/dec, whereas for higher frequencies it gives a constant contribution of 6 dB.

The $|V_{\rm CM}(jn\omega_0)|$ Bode diagram is illustrated in Fig. 7. The order of poles and zeros may change according to the parameters values, i.e., rise–falling time, duty cycle, τ_d, etc.

It is worth underlining that if the time delay τ_d tends to zero, the pole $f_{\rm P2} = 1/(\pi\tau_d)$ moves at higher frequencies. The delay contribution envelope at frequencies higher than $f_{\rm P2}$ is fixed to 6 dB. This means that if $f_{\rm P2}$ moves up, the magnitude of $V_{\rm CM}$ decreases up to the new $f_{\rm P2}$. Another effect deriving from the constant contribution of the delay term over $f_{\rm P2}$ is that there are no more advantages on the emission reduction from this frequency up.

A MATLAB simulation varying τ_d has been performed. The parameters employed in this model are reported in Table I.

In Fig. 8, the CM emission spectrum is shown for $\tau_d = 100$ ns (continuous line), $\tau_d = 10$ ns (dashed line), and $\tau_d = 1$ ns (dashed-dotted line). The value of τ_d was not set to 0 ns, otherwise the spectra would be zero over the whole frequency range, since the term $D(j\omega_0)$ would be null. The fixed poles in this

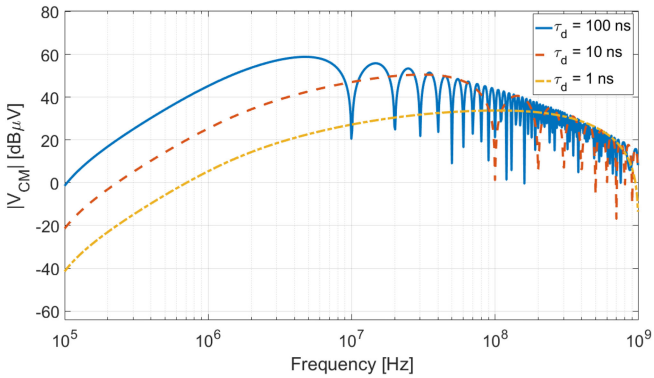

Fig. 8. Analytical CM emission model.

simulation are $f_{\rm P1} = 1/(\pi T/2) = 31.8$ kHz, $f_{\rm P3} = 1/(\pi\tau_{\rm r}) = 12.7$ MHz, and $f_{\rm P4} = 1/(2\pi 2RC) = 318$ MHz. The pole $f_{\rm P2}$ instead changes when the time delay $\tau_{\rm d}$ changes. Respectively, the pole frequencies for the three above-mentioned cases are 3.18, 31.8, and 318 MHz. In the frequency range 1–30 MHz, the benefit resulting from the alignment of the switching voltages is evident. Furthermore, it should be noticed that the contribution to the conducted emission due to resonances was not considered. In the following section, this analytical approximation is compared with a SPICE simulation.

V. CIRCUIT ANALYSIS

The inverter circuit has been simulated with SPICE, considering only two legs out of three. This simulation aims to compare the SSM efficiency in reducing the CM conducted emissions against the one of the proposed signal aligning technique.

The simulated schematic is shown in Fig. 9 and the simulation parameter values are reported in Table II. It is a two-legs full bridge, whose parasitics have been considered in the simulation. The circuit drives, with a $f_{\rm SW} = 50$ kHz bPWM, a 695 μH inductor. The two LISNs are connected between the power supply (12 V DC battery) and the inverter. The parasitic capacitances between the U and V nodes and the reference plane are equal to 6 pF. This value has been estimated from the geometry of the designed inverter, which is characterized in Section VI.

The output voltages and the CM current $I_{\rm CM}$, which resulted from transient SPICE simulations, have been plotted in Figs. 10 and 11, respectively. Two cases have been simulated: the first with $\tau_d = 100$ ns and the second with $\tau_d \approx 0$ ns. The current $I_{\rm CM}$ has been filtered, in order to reject disturbances above 30 MHz. From Fig. 11, it is possible to see that the peak current is highly reduced, and the current shape of the delayed condition is similar to the one shown in Fig. 6.

A. Delay Compensation Technique

In this paragraph, the analytical approximation proposed in Section III is compared with SPICE simulations. To this purpose, the schematic of Fig. 9 has been simulated in two different configurations. The CM voltage is defined as

$$V_{\rm CM} = \frac{V_{\rm LISN,p} + V_{\rm LISN,n}}{2}. \tag{8}$$

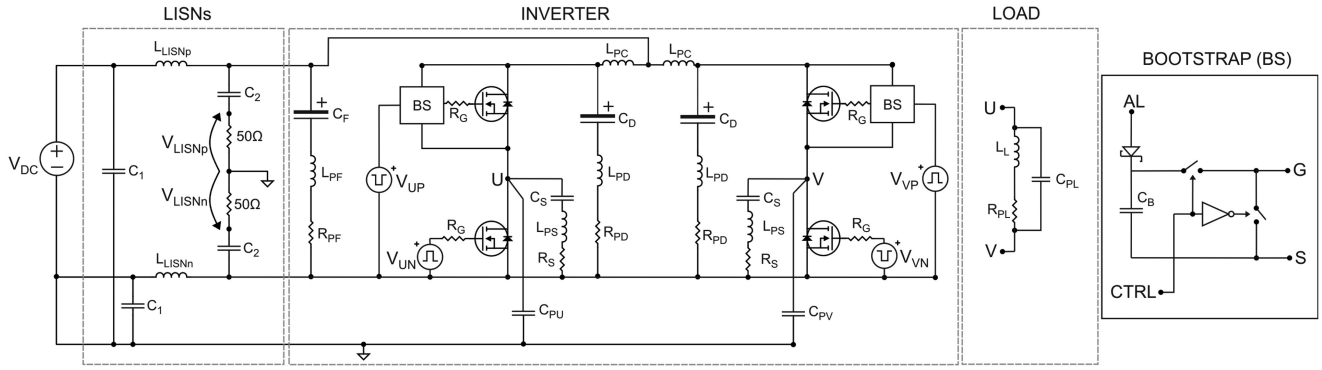

Fig. 9. Simulated schematic.

TABLE II
SIMULATION PARAMETERS

Parameter	Value	Parameter	Value
V_{DC}	12 V	C_{B}	47 nF
L_{LISN}	5 μH	C_1	1 μF
C_2	100 nF	C_{F}	4700 μF
L_{PF}	20 nH	R_{PF}	60 mΩ
R_{G}	3.3 Ω	C_{D}	10 μF
L_{PD}	10 nH	R_{PD}	60 mΩ
$C_{\mathrm{PU,PV}}$	6 pF	L_{L}	695 μH
C_{PL}	30 pF	R_{PL}	60 mΩ
R_{S}	3.9 Ω	C_{S}	4.7 nF
L_{PS}	2 nH	L_{PC}	100 nH

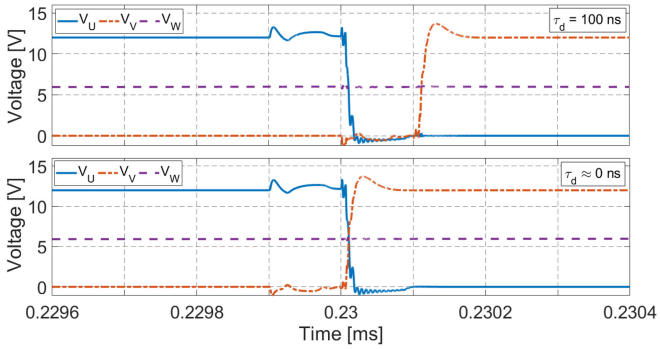

Fig. 10. Inverter output waveforms obtained from simulation for $\tau_d = 100$ ns and $\tau_d \approx 0$ ns.

In the first case, the output waveforms are shifted in time of $(\frac{T}{2} + \tau_d)$, where τ_d is greater than the rising or falling time of the output nodes, e.g., 100 ns. Therefore, there is a time interval in which both the outputs are low, and another one in which both the outputs are high. The results of both the simulation and the analytical approximation are shown in Fig. 12. The model differs from the simulation only over a small frequency range. This can be due to some parasitic effects that have not been modeled in Section III. Moreover, from the simulation, it results that the addition of the third leg W, whose transistors are kept OFF, has no impact on the magnitude of the spectra. This is due to the low-magnitude, low-frequency voltage present at the motor neutral node.

In the second case, the comparison has been made for $\tau_d = 5$ ns. The results are shown in Fig. 13. In this case, the CM emission model accurately follows the simulated behavior at low frequencies, whereas in the higher frequency range, the

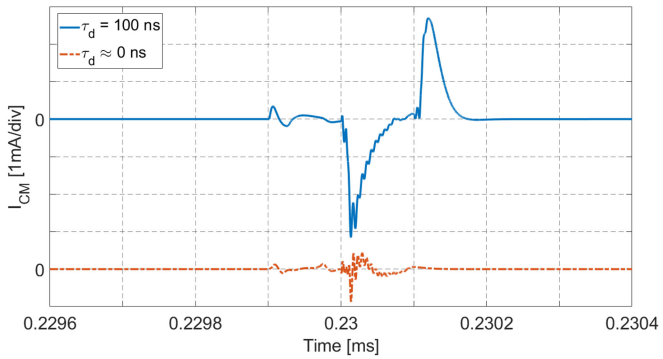

Fig. 11. CM current obtained from simulation for $\tau_d = 100$ ns and $\tau_d \approx 0$ ns.

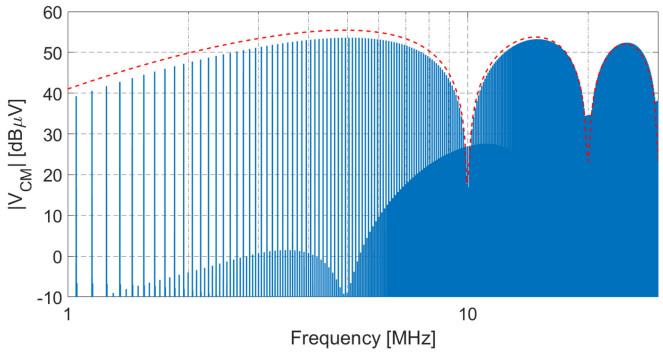

Fig. 12. CM voltage spectra: simulation results (solid line) compared with analytical model (dashed line), $\tau_d = 100$ ns.

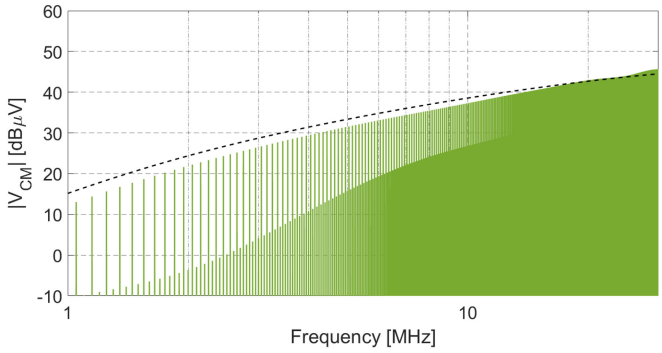

Fig. 13. CM voltage spectra: simulation results (solid line) compared with analytical model (dashed line), τ_d=5 ns.

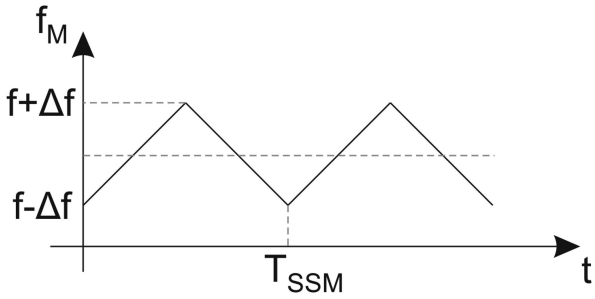

Fig. 14. SSM modulation waveform.

approximation is less accurate. This can be due, as in the previous case, to parasitics, but since the conducted emissions are evaluated from 150 kHz to 30 MHz [2], the frequency range above 30 MHz is out of this paper's scope.

The ringing contribution has been neglected in the mathematical model and from the simulation results, as shown in Figs. 12 and 13, the ringing effect is not present, although the parasitics have been included in the schematic, because it occurs at frequencies above 30 MHz. The ringing signal can be damped, as shown in the schematic in Fig. 9 with passive (or active) snubber circuits. In this way, its contribution on the CM conducted emissions, which is represented by a peak in the measured spectra at the ringing frequency, can be minimized.

B. SSM Technique

In order to test the proposed technique performances, it has been compared with the SSM EMI reduction method. The phase shift between outputs is set as in the previous simulation, to 100 ns, but the SSM technique has been applied in an attempt to reduce the CM conducted emissions. The modulation depth for this simulation is 20%, i.e., the switching frequency varies in $f_{\rm M} = f \pm \Delta f$ range, where $f = 50$ kHz and $\Delta f = 10$ kHz. The modulation waveform is triangular and its frequency is $f_{\rm SSM} = 1/T_{\rm SSM} = 625$ Hz, giving a modulation index $m = \Delta f \cdot T_{\rm SSM} = 16$ [9], [19]. The modulation waveform is shown in Fig. 14.

In Fig. 15, it is possible to see that the proposed technique, in the frequency range of interest for the conducted emissions

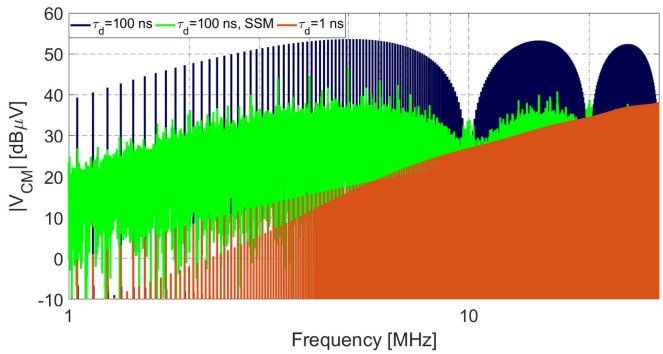

Fig. 15. Comparison of different CM EMI reduction techniques: in blue the reference spectrum, obtained with $\tau_d = 100$ ns, in green the spectrum when the SSM is applied, and in red the spectrum with the delay compensation technique ($\tau_d = 1$ ns).

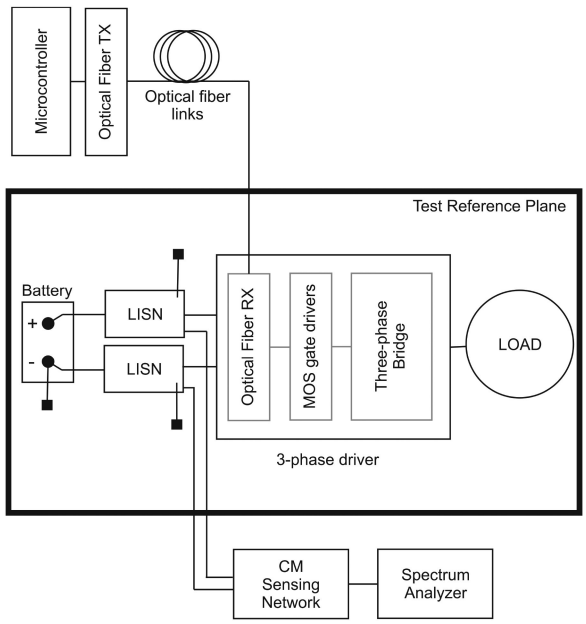

Fig. 16. Test setup block diagram.

(150 kHz–30 MHz), is more efficient compared to SSM. In fact, using a delay reduction to 1 ns, which can be reached with commercial microcontrollers, below 24 MHz the signal aligning technique reduces the CM conducted EMI better than the SSM.

In the following section, the effectiveness of the proposed technique is validated by experiments, both for an inductive load and for a BLDC motor.

VI. Experimental Results

In order to prove experimentally the above-proposed technique, a test bench has been designed and conducted EMC measurements have been carried out according to CISPR 25 rules [2]. The test bench block diagram is shown in Fig. 16. The setup is composed of the copper test reference plane, on which the 12-V battery, the two LISNs, the inverter power module, and the load have been placed. The load chassis and the inverter power module are isolated from the reference plane by means of a wooden board and a paper sheet, respectively. The inverter

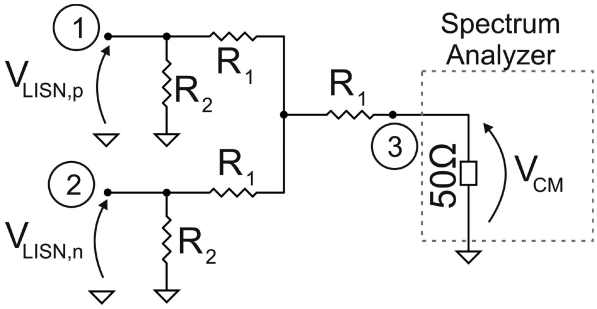

Fig. 17. CM voltage sensing network.

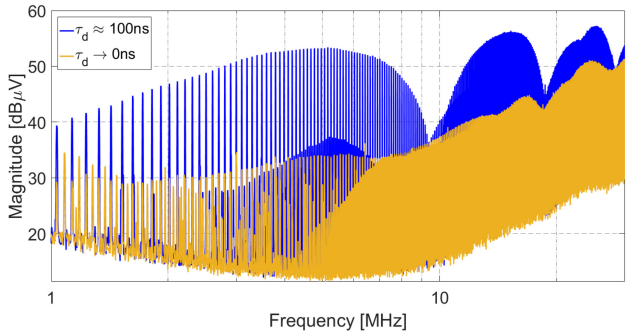

Fig. 18. Preliminary measurement with inductive load: CM voltage.

control signals are provided by optical fiber links, isolating the microcontroller from the rest of the system. Therefore, the microcontroller emissions have not been measured by the LISNs, since the control board is located far from the reference plane. The inverter power module is a full bridge made up of four power MOSFETs that can carry up to 50 A. Each bridge leg is driven by a dual 1.6-A gate driver, with independent gate control. The prototype board, considering in particular its layout, has not been designed to minimize the EMI generation. Moreover, in order to maximize the resolution of the technique effectiveness, no input filter has been placed.

Since this paper aims to analyze the CM EMI spectra, a CM sensing network (CMSN), as shown in Fig. 17, has been prototyped. The CMSN inputs ①–② and output ③ have been connected to the test connectors of the LISNs and to the spectrum analyzer input, respectively. The CMSN has been designed using $R_1 = 28.7\,\Omega$, $R_2 = 49.9\,\Omega$. With this network, the CM voltage at the output, $V_{\rm CM}$ (8) is scaled by a factor 0.536, equal to $-$ 5.4 dB.

A. Preliminary Measurements

In this preliminary measurement setup, the load is a 695 μH inductor, connected to two inverter outputs, in order to prove the EMI reduction method using initially only two legs and to compare the measurements with the illustrated simulation results. The differential mode is filtered using a 4700 μF DC link capacitor. The circuit is supplied by a 12-V battery and the inductor is driven by a 50% bPWM.

The reference schematic is shown in Fig. 3, in which only the U and V legs have been used.

Two measurement configurations have been carried out. In the first one, the phase delay between the two outputs has been set to $\tau_d \approx 100$ ns. In the second configuration, the two output voltages $V_{\rm U}$ and $V_{\rm V}$ have been set in phase manually, minimizing τ_d. To this purpose, the output waveforms were sampled with a 1-GHz oscilloscope and the PWM duty cycle and phase were adjusted for each leg in order to obtain an almost null phase shift between the active output waveforms.

The result of these measurements is shown in Fig. 18. It can be seen that the results of the performed measurements are in line with both the analytical model and the simulations illustrated in the previous sections.

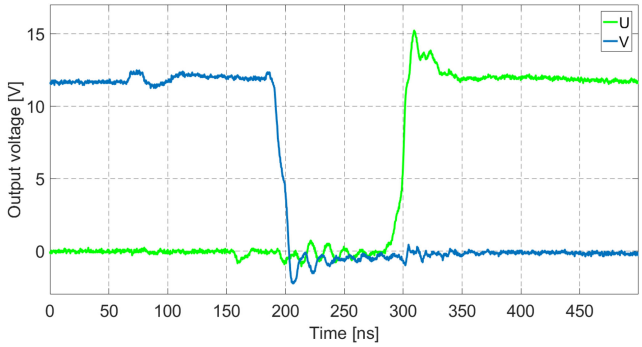

Fig. 19. U and V output voltages with phase shift $\approx$ 100 ns.

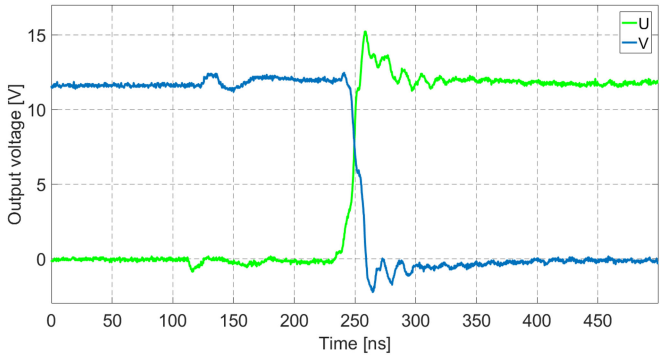

Fig. 20. U and V output voltages with phase shift $\approx$ 0 ns.

B. Three-Phase BLDC Driver Emission Reduction Measurements

Once a BLDC motor was connected to the driver board, another set of conducted emission measurements has been performed. In this case, all three legs are used to drive the BLDC motor, but only two at a time are active, as explained in Section II. The results can therefore be compared to those seen for the inductor load, with some superimposed emissions due to the commutation instants between two consequent control steps.

The CM emissions of the system have again been evaluated in two different cases: the first one, shown in Fig. 19, in which τ_d is around 100 ns and the second one, shown in Fig. 20, in which the output voltages are complementary and their edges are aligned in the best possible way.

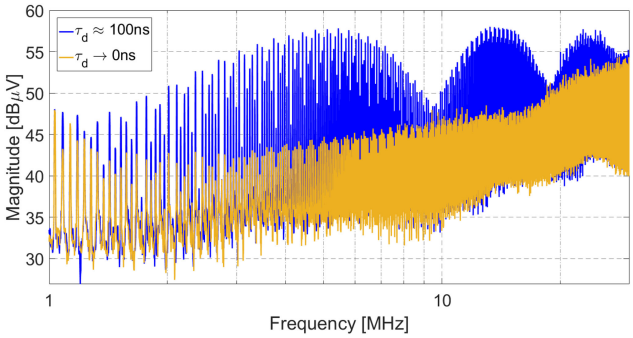

Fig. 21. Spectra of the common mode conducted emissions obtained from the measurement carried out with a BLDC motor inserted in the test setup.

According to the simulations, there should be a reduction in the CM emission of around 10–15 dB between 1 and 30 MHz. The results are shown in Fig. 21.

It can be seen that above 1 MHz the CM emissions are lowered over the whole frequency band, with reduction peaks of 15 dB. Since in the simulations, some emission contributions are not reported, such as ringing and motor chassis coupling with the reference plane, the results shown in Fig. 21 are in accordance with the simulation results.

VII. Conclusion

In this paper, the relationship between the misalignment of the output voltage waveforms of a BLDC motor driver and CM conducted emissions has been analyzed theoretically and proven by simulations and measurements. The proposed technique can be used in all bPWM-driven systems, both single phase and three phase. It has been shown that if the edges of high-voltage swing signals are properly aligned, the CM emissions are significantly lowered. This alignment does not affect the dead time needed to avoid the cross conduction in each leg. In this paper, it has been demonstrated by simulations that the signal aligning technique gives better results than the SSM, when the output waveforms are not perfectly complementary. Indeed, the proposed technique reduces the CM disturbances more than the SSM below 24 MHz; the performances over this frequency are comparable between the two techniques. To confirm the technique's efficiency, measurements were performed, whose results have demonstrated that the CM emission level is reduced by around 15 dB when the output waveforms are aligned.

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